National Semiconductor

November 1994

54F/74F191 Up/Down Binary Counter with Preset and Ripple Clock

General Description

The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

- High-Speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

Commercial	Military	Package Number	Package Description
74F191PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F191DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F191SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F191SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F191FM (Note 2)	W16A	16-Lead Cerpack
	54F191LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols Connection Diagrams Pin Assignment Pin Assignment for **DIP, SOIC and Flatpak** for LCC Ρ., Q₂Ū/DNC CE Q₀ 8 7 6 5 4 16 Ρ. V_{CC} Q₁. 15 ۰Po Q₃ 9 GND 10 NC 11 P₃ 12 P₂ 13 Q2 Q₀· 14 CP CE -13 RC TL/F/9495-1 Ū∕D∙ 12 тс IEEE/IEC \mathbf{Q}_2 1 PI Q3 CTRDIV16 GND CE 14 15 16 17 18 M2 [DOWN] 2(CT=0)Z PL TC NC RC CP Ū∕D TC TL/F/9495-2 M3 [UP] 3(CT=15)Z 1, 2-/1, 3+ 6,1 [1] [2] 0 [4] Q2 [8] Q₃ TL/F/9495-4 TRI-STATE® is a registered trademark of National Semiconductor Corporation. TL/F/9495

RRD-B30M75/Printed in U. S. A.

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E 2 P1

■ 20 V_{CC}

🛋 19 P₀

TL/F/9495-3

54F/74F191 Up/Down Binary Counter with Preset and Ripple Clock

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Unit Loading/Fan Out

		54	IF/74F
Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
CE	Count Enable Input (Active LOW)	1.0/3.0	20 μA/-1.8 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	$20 \mu \text{A} / -0.6 \text{mA}$
P ₀ -P ₃	Parallel Data Inputs	1.0/1.0	20 µA/ -0.6 mA
P ₀ -P ₃ PL	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	20 µA/ -0.6 mA
Ū/D	Up/Down Count Control Input	1.0/1.0	20 µA/ -0.6 mA
$Q_0 - Q_3$	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
RC	Ripple Clock Output (Active LOW)	50/33.3	-1 mA/20 mA
тс	Terminal Count Output (Active HIGH)	50/33.3	-1 mA/20 mA

Functional Description

The 'F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Data inputs (P_0-P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the \overline{U}/D input signal, as indicated in the Mode Select Table. \overline{CE} and \overline{U}/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until \overline{U}/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, the RC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures 1 and 2. In Figure 1, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in *Figure 2*. All clock inputs are driven in parallel and the $\overline{\rm RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{\rm RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure 3* avoids ripple delays and their associated restrictions. The \overline{CE} input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures 1* and *2* doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

Mode Select Table

	In	puts		Mode
PL	CE	Ū/D	СР	mode
н	L	L		Count Up
н	L	Н		Count Down
L	Х	Х	Х	Preset (Asyn.)
н	н	Х	Х	No Change (Hold)

50	Toursten	Table
RC	I ruth	Table

	Inputs		Output
CE	TC*	СР	RC
L	Н	U	ъ
н	Х	х	н
Х	L	х	н

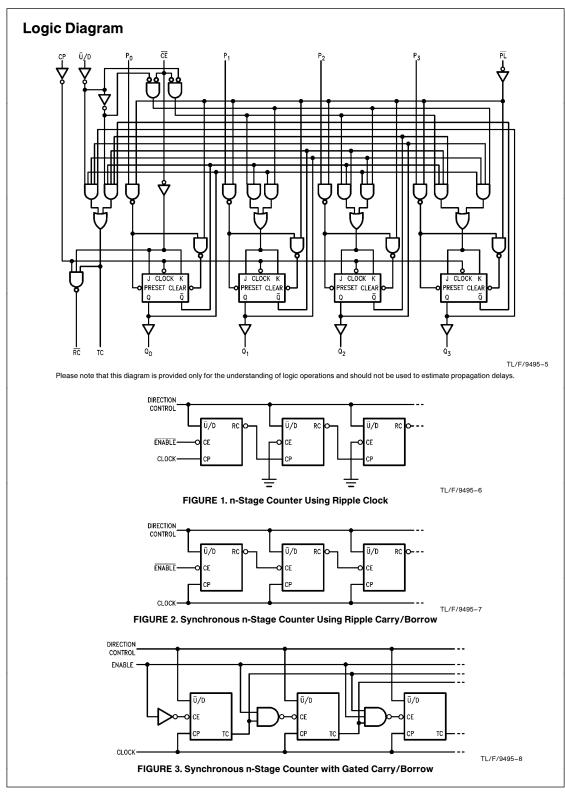
*TC is generated internally

H = HIGH Voltage Level L = LOW Voltage Level

L = LOW VoltagX = Immaterial

_____ = LOW-to-HIGH Clock Transition

ר = LOW Pulse



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to	
Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	- 0.5V to V _{CC}
TRI-STATE [®] Output	-0.5V to $+5.5V$
Current Applied to Output	

Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

in LOW State (Max) twice the rated I_{OL} (mA) Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

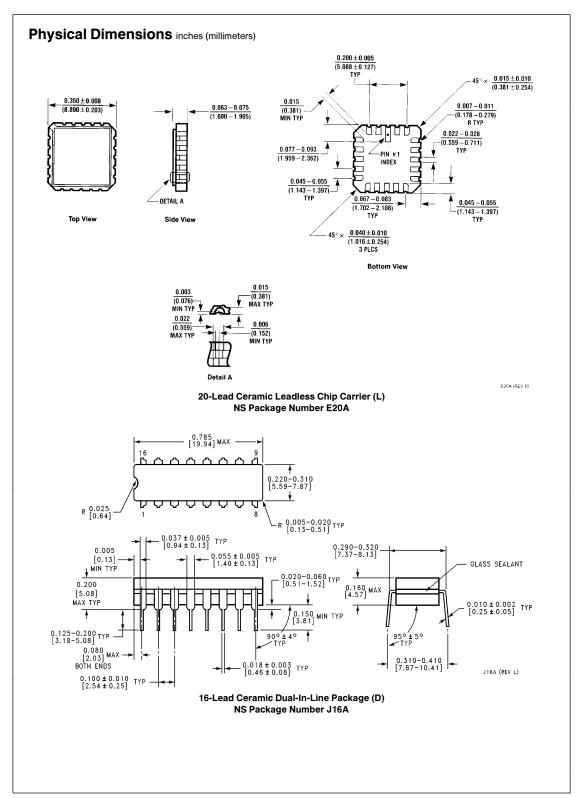
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

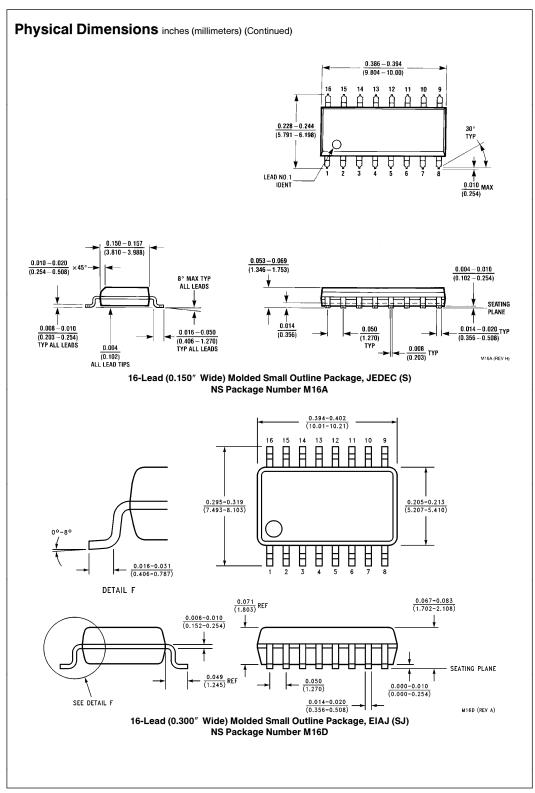
DC Electrical Characteristics

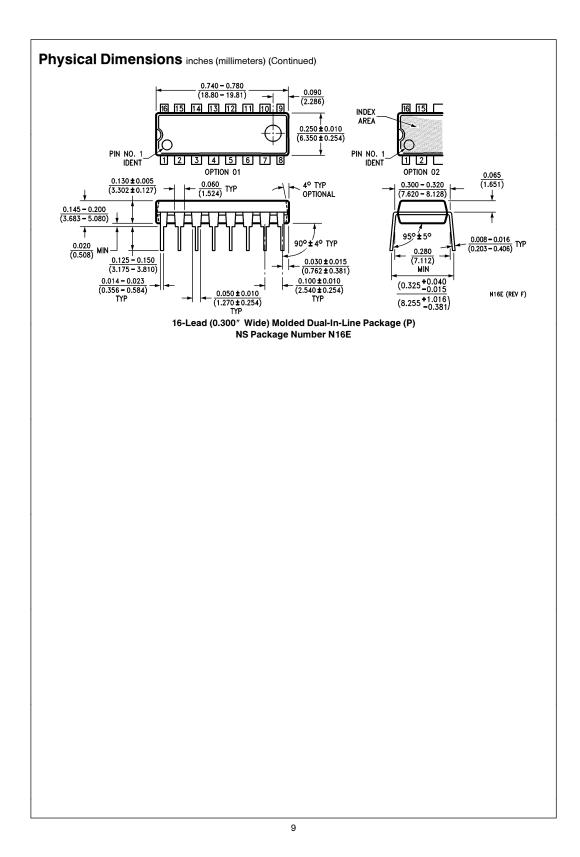
Symbol	Parame	tor		54F/74	F	Units	vcc	Conditions
Symbol	Falane		Min	Тур	Max	Units	VCC	conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Vo	oltage			-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7			V	Min	$I_{OH} = -1 \text{ mA}$ $I_{OH} = -1 \text{ mA}$ $I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}			0.5 0.5	V	Min	$I_{OL} = 20 \text{ mA}$ $I_{OL} = 20 \text{ mA}$
Ιн	Input HIGH Current	54F 74F			20.0 5.0	μΑ	Max	$V_{IN} = 2.7V$
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μΑ	Max	$V_{IN} = 7.0V$
I _{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μΑ	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9 \ \mu A$, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F			3.75	μΑ	0.0	V _{IOD} = 150 mV All Other Pins Grounded
IIL	Input LOW Current				-0.6 -1.8	mA	Max	$V_{IN} = 0.5V$ (except \overline{CE}) $V_{IN} = 0.5V$ (\overline{CE})
los	Output Short-Circuit	Current	-60		-150	mA	Max	$V_{OUT} = 0V$
ICC	Power Supply Curren	t		38	55	mA	Max	

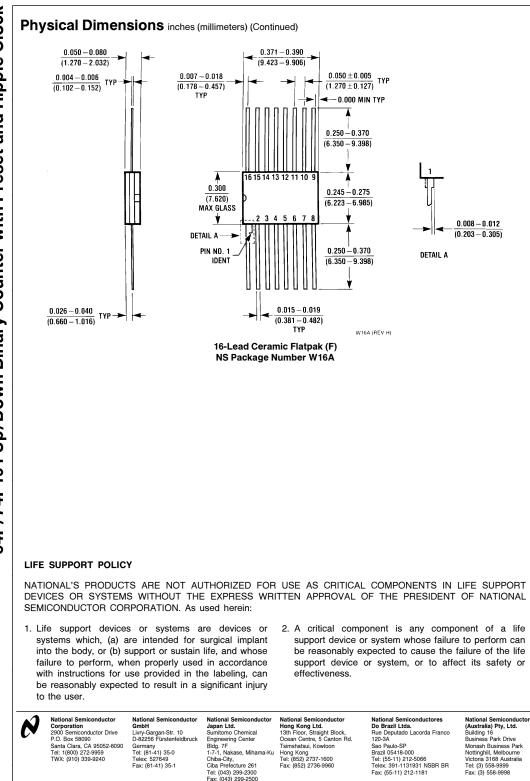
			74F		5	4F	7	4F	
Symbol	Parameter	v	$\Gamma_A = +25^{\circ}$ $\Gamma_{CC} = +5.0^{\circ}$ $C_L = 50 \text{pF}$	v		_C = Mil 50 pF		; = Com 50 pF	Units
		Min	Тур	Max	Min	Max	Min	Max	1
f _{max}	Maximum Count Frequency	100	125		75		90		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	3.0 5.0	5.5 8.5	7.5 11.0	3.0 5.0	9.5 13.5	3.0 5.0	8.5 12.0	
PLH PHL	Propagation Delay CP to TC	6.0 5.0	10.0 8.5	13.0 11.0	6.0 5.0	16.5 13.5	6.0 5.0	14.0 12.0	- ns
PLH PHL	Propagation Delay CP to \overline{RC}	3.0 3.0	5.5 5.0	7.5 7.0	3.0 3.0	9.5 9.0	3.0 3.0	8.5 8.0	ns
PLH PHL	Propagation Delay \overline{CE} to \overline{RC}	3.0 3.0	5.0 5.5	7.0 7.0	3.0 3.0	9.0 9.0	3.0 3.0	8.0 8.0	
PLH PHL	Propagation Delay \overline{U}/D to \overline{RC}	7.0 5.5	11.0 9.0	18.0 12.0	7.0 5.5	22.0 14.0	7.0 5.5	20.0 13.0	ns
PLH PHL	Propagation Delay Ū/D to TC	4.0 4.0	7.0 6.5	10.0 10.0	4.0 4.0	13.5 12.5	4.0 4.0	11.0 11.0	113
PLH PHL	Propagation Delay P _n to Q _n	3.0 6.0	4.5 10.0	7.0 13.0	3.0 6.0	9.0 16.0	3.0 6.0	8.0 14.0	ns
PLH PHL	Propagation Delay PL to Q _n	5.0 5.5	8.5 9.0	11.0 12.0	5.0 5.5	13.0 14.5	5.0 5.5	12.0 13.0	ns
PLH PHL	Propagation Delay P _n to TC	5.0 6.5		14.0 13.0			5.0 6.0	15.0 14.0	ns
PLH PHL	Propagation Delay P_n to \overline{RC}	6.5 6.0		19.0 14.0			6.5 6.0	20.0 15.0	ns
PLH PHL	Propagation Delay PL to TC	8.0 6.0		16.5 13.5			8.0 6.0	17.5 14.5	ns
PLH PHL	Propagation Delay PL to RC	10.0 9.0		20.0 15.5			10.0 9.0	21.0 16.0	ns

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