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National Semiconductor

# 54ACTQ377
# Octal D Flip-Flop with Clock Enable

## General Description

The ACTQ377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

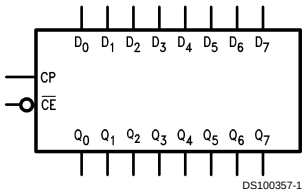
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

The ACTQ377 utilizes FACT Quiet Series® technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series features GTO® output control and undershoot corrector in addition to a split ground bus for superior performance.

## Features

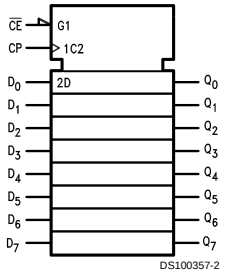
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- TTL-compatible inputs and outputs
- Standard Microcircuit Drawing (SMD) 5962-9219001

## Logic Symbols




DS100357-1

IEEE/IEC




DS100357-2

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $\overline{CE}$ | Clock Enable (Active LOW) |
| $Q_0$–$Q_7$ | Data Outputs |
| CP | Clock Pulse Input |

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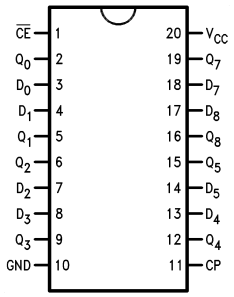
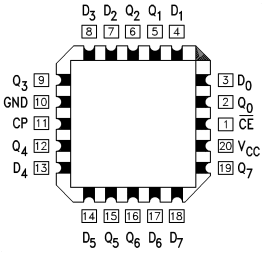
## Connection Diagrams

**Pin Assignment for DIP and Flatpak**




DS100357-3

**Pin Assignment for LCC**

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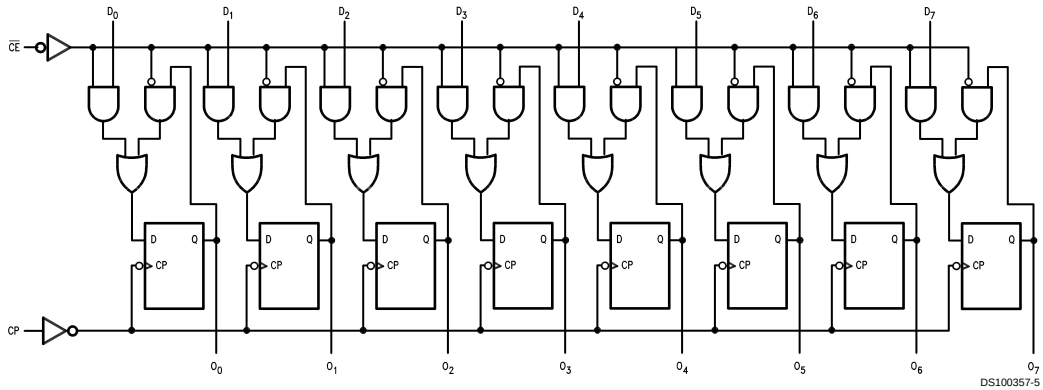
## Mode Select-Function Table

| Operating Mode | Inputs | | | Outputs |
|---|---|---|---|---|
| | CP | $\overline{CE}$ | $D_n$ | $Q_n$ |
| Load '1' | N | L | H | H |
| Load '0' | N | L | L | L |
| Hold (Do Nothing) | N | H | X | No Change |
| | X | H | X | No Change |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
N = LOW-to-HIGH Clock Transition

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current per Output Pin ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65˚C to +150˚C |
| Junction Temperature ($T_J$) | |
| CDIP | 175˚C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| 'ACTQ | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 54ACTQ | −55˚C to +125˚C |
| Minimum Input Edge Rate (ΔV/Δt) | |
| 'ACTQ Devices | |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | 125 mV/ns |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

## DC Characteristics for 'ACTQ Family Devices

| Symbol | Parameter | $V_{CC}$ (V) | 54ACTQ $T_A$ = −55˚C to +125˚C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.4<br>5.4 | V | $I_{OUT}$ = −50 μA |
| | | | | | (Note 2) $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | 3.70 | V | $I_{OH}$ = −24 mA |
| | | 5.5 | 4.70 | | $I_{OH}$ = −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | | | | (Note 2) $V_{IN}$ = $V_{IL}$ or $V_{IH}$ |
| | | 4.5 | 0.50 | V | $I_{OL}$ = 24 mA |
| | | 5.5 | 0.50 | | $I_{OL}$ = 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 1.6 | mA | $V_I$ = $V_{CC}$ − 2.1V |
| $I_{OLD}$ | (Note 3) Minimum Dynamic | 5.5 | 50 | mA | $V_{OLD}$ = 1.65V Max |
| $I_{OHD}$ | Output Current | 5.5 | −50 | mA | $V_{OHD}$ = 3.85V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | 160.0 | μA | $V_{IN}$ = $V_{CC}$ or GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 5.0 | 1.5 | V | (Note 4) |

## DC Characteristics for 'ACTQ Family Devices (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | 54ACTQ $T_A$ = −55°C to +125°C Guaranteed Limits | Units | Conditions |
|---|---|---|---|---|---|
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 5.0 | -1.2 | V | (Note 4) |

**Note 2:** *All outputs loaded; thresholds on input associated with output under test.

**Note 3:** †Maximum test duration 2.0 ms, one output loaded at a time.

**Note 4:** Max number of outputs defined as (n). Data inputs are driven 0V to 3V. one output GND.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 5) | 54ACTQ $T_A$ = −55°C to +125°C $C_L$ = 50 pF Min | 54ACTQ $T_A$ = −55°C to +125°C $C_L$ = 50 pF Max | Units | Fig. No. |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | 5.0 | 85 | | MHz | |
| $t_{PLH}$ | Propagation Delay CP to $Q_n$ | 5.0 | 1.5 | 10.0 | ns | |
| $t_{PHL}$ | Propagation Delay CP to $Q_n$ | 5.0 | 1.5 | 10.0 | ns | |

**Note 5:** Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

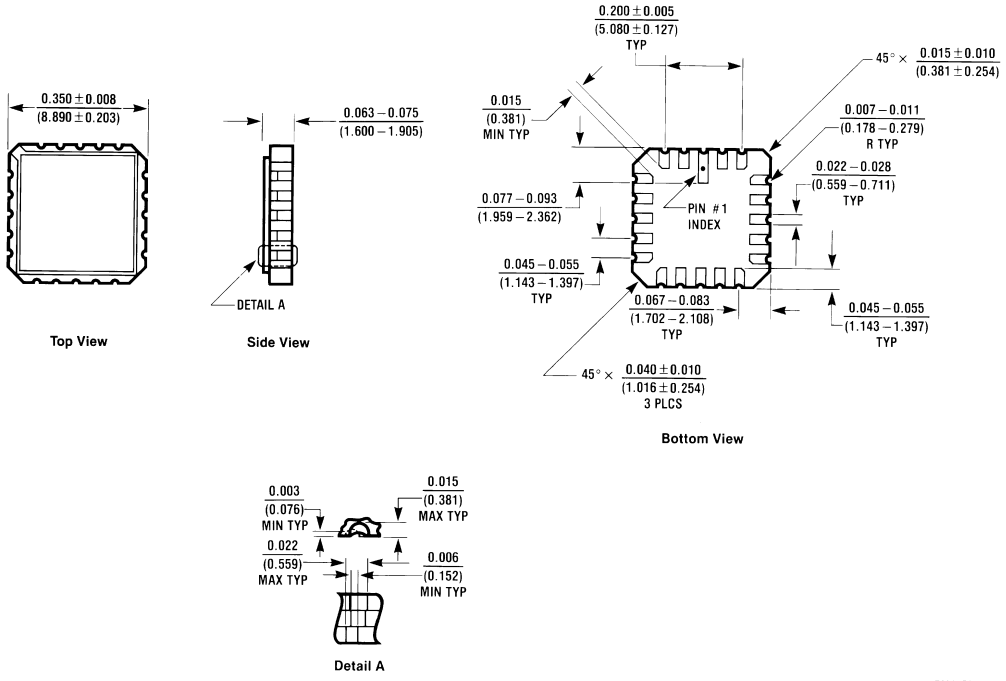
| Symbol | Parameter | $V_{CC}$ (V) (Note 6) | 54ACTQ $T_A$ = −55°C to +125°C $C_L$ = 50 pF Guaranteed Minimum | Units | Fig. No. |
|---|---|---|---|---|---|
| $t_s$ | Setup Time, HIGH or LOW $D_n$ to CP | 5.0 | 4.0 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $D_n$ to CP | 5.0 | 1.5 | ns | |
| $t_s$ | Setup Time, HIGH or LOW $\overline{CE}$ to CP | 5.0 | 5.0 | ns | |
| $t_h$ | Hold Time, HIGH or LOW $\overline{CE}$ to CP | 5.0 | 1.5 | ns | |
| $t_w$ | CP Pulse Width HIGH or LOW | 5.0 | 5.0 | ns | |

**Note 6:** Voltage Range 5.0 is 5.0V ±0.5V

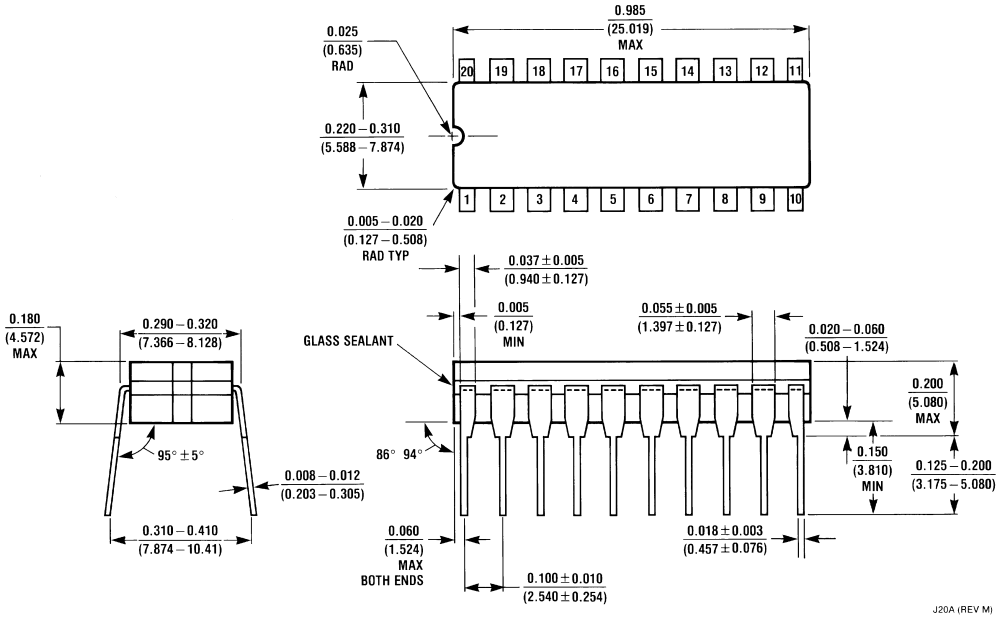
## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 10.0 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 80.0 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted

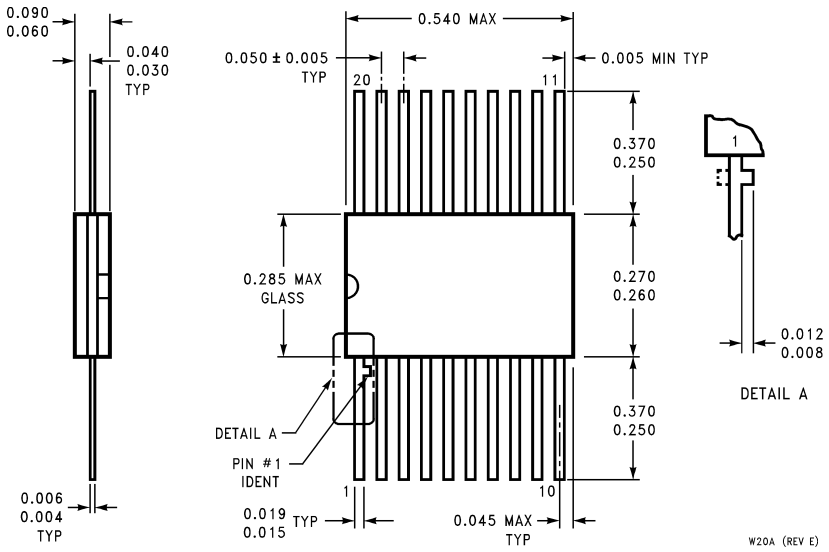



**20 Terminal Ceramic Leadless Chip Carrier (L)**
**NS Package Number E20A**




**20 Lead Ceramic Dual-In-Line Package (D)**
**NS Package Number J20A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20 Lead Ceramic Flatpak (F)**
**NS Package Number W20A**

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