National Semiconductor

July 1998

54AC191
Up/Down Counter with Preset and Ripple Clock

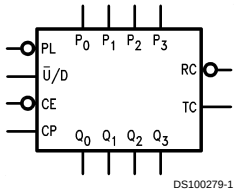
General Description

The 'AC191 is a reversible modulo 16 binary counter. It features synchronous counting and asynchronous presetting. The preset feature allows the 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

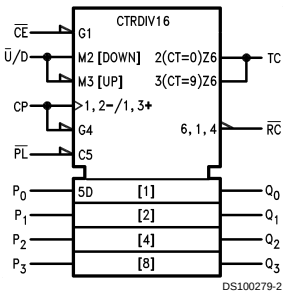
- I_{CC} reduced by 50%
- High speed — 133 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable
- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC191: 5962-89749

Logic Symbols



DS100279-1

IEEE/IEC

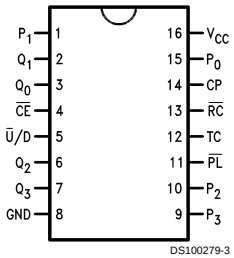


DS100279-2

Pin Names	Description
$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
$\overline{U}$/D	Up/Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output
TC	Terminal Count Output

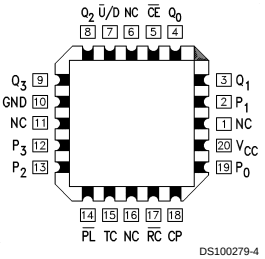
Connection Diagrams

Pin Assignment for DIP and Flatpack



DS100279-3

Pin Assignment for LCC



DS100279-4

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Functional Description

The ’AC191 is a synchronous up/down counter. The ’AC191 is organized as a 4-bit binary counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Load inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 15 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, $\overline{RC}$ output wil go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in *Figure 1* and *Figure 2*. In *Figure 1*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in *Figure 2*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure 3* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figure 1* and *Figure 2* doesn’t apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Mode Select Table

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs				Outputs
$\overline{PL}$	$\overline{CE}$	TC*	CP	$\overline{RC}$
H	L	H	⌐¬	⌐¬
H	H	X	X	H
H	X	L	X	H
L	X	X	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Functional Description (Continued)

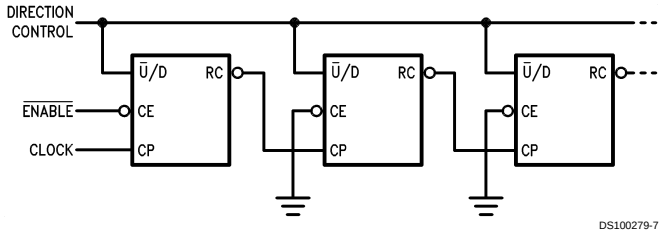


FIGURE 1. N-Stage Counter Using Ripple Clock

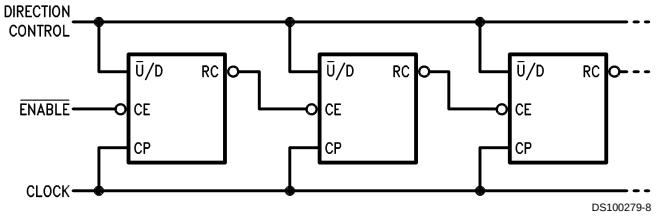


FIGURE 2. Synchronous N-Stage Counter Using Ripple Carry/Borrow

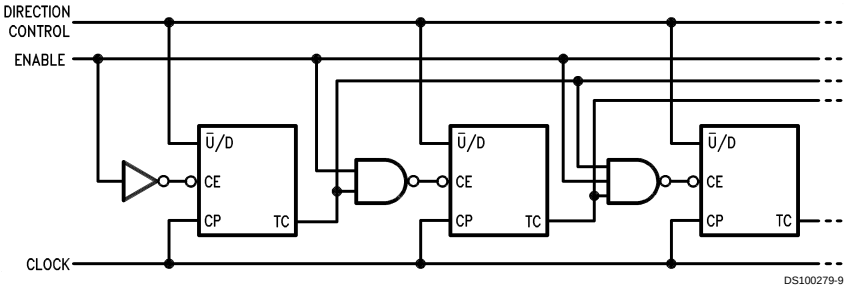
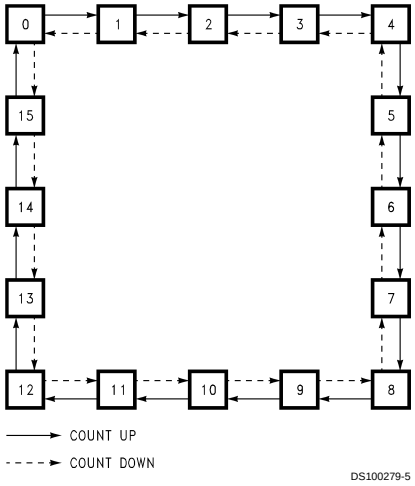
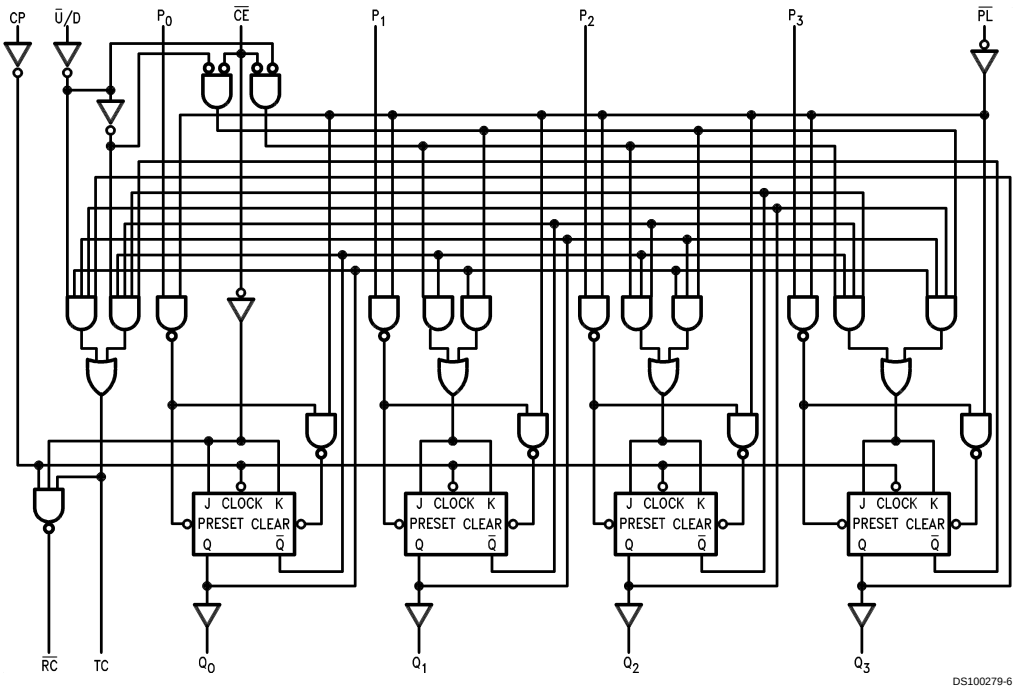


FIGURE 3. Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	3.15		
		5.5	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	1.35		
		5.5	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	I_{OUT} = −50 μA
		4.5	4.4		
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	2.4		−12 mA
		4.5	3.7	V	I_{OH} −24 mA
		5.5	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	I_{OUT} = 50 μA
		4.5	0.1		
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		3.0	0.50		12 mA
		4.5	0.50	V	I_{OL} 24 mA
		5.5	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V_{IN} = V_{CC} or GND

DC Characteristics for 'AC Family Devices (Continued)

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 5)	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Count Frequency	3.3	55		MHz	
		5.0	80			
t_{PLH}	Propagation Delay CP to Q_n	3.3	1.0	16.5	ns	
		5.0	1.0	12.0		
t_{PHL}	Propagation Delay CP to Q_n	3.3	1.0	16.0	ns	
		5.0	1.0	12.0		
t_{PLH}	Propagation Delay CP to TC	3.3	1.0	19.5	ns	
		5.0	1.0	14.0		
t_{PHL}	Propagation Delay CP to TC	3.3	1.0	19.0	ns	
		5.0	1.0	14.5		
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3	1.0	14.0	ns	
		5.0	1.0	10.5		
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3	1.0	12.5	ns	
		5.0	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3	1.0	14.0	ns	
		5.0	1.0	10.0		
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3	1.0	12.5	ns	
		5.0	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3	1.0	14.5	ns	
		5.0	1.0	11.0		
t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3	1.0	15.0	ns	
		5.0	1.0	11.0		
t_{PLH}	Propagation Delay $\overline{U}$/D to TC	3.3	1.0	14.0	ns	
		5.0	1.0	10.5		
t_{PHL}	Propagation Delay $\overline{U}$/D to TC	3.3	1.0	13.5	ns	
		5.0	1.0	10.0		
t_{PLH}	Propagation Delay P_n to Q_n	3.3	1.0	16.5	ns	
		5.0	1.0	11.5		
t_{PHL}	Propagation Delay P_n to Q_n	3.3	1.0	15.5	ns	
		5.0	1.0	10.5		
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3	1.0	18.0	ns	
		5.0	1.0	12.5		
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3	1.0	15.5	ns	
		5.0	1.0	11.5		

Note 5: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

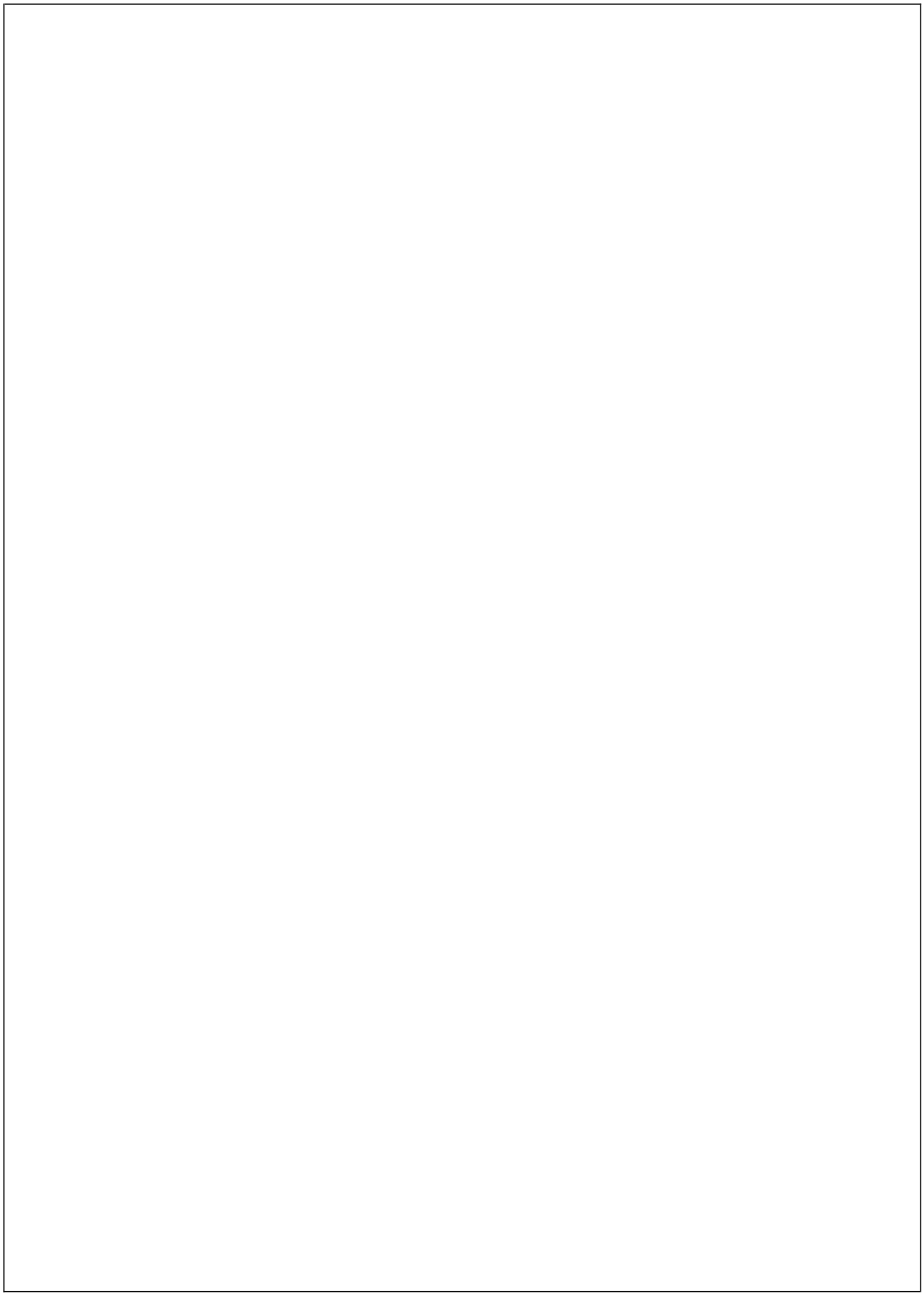
AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 6)	54AC $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW	3.3	4.0	ns	
	P_n to $\overline{PL}$	5.0	3.0		
t_h	Hold Time, HIGH or LOW	3.3	1.5	ns	
	P_n to $\overline{PL}$	5.0	2.0		
t_s	Setup Time, LOW	3.3	9.0	ns	
	$\overline{CE}$ to CP	5.0	6.0		
t_h	Hold Time, LOW	3.3	0	ns	
	$\overline{CE}$ to CP	5.0	0.5		
t_s	Setup Time, HIGH or LOW	3.3	10.5	ns	
	$\overline{U}$/D to CP	5.0	7.5		
t_h	Hold Time, HIGH or LOW	3.3	0	ns	
	$\overline{U}$/D to CP	5.0	1.0		
t_w	$\overline{PL}$ Pulse Width, LOW	3.3	5.0	ns	
		5.0	5.0		
t_w	CP Pulse Width, LOW	3.3	6.0	ns	
		5.0	6.0		
t_{rec}	Recovery Time	3.3	1.5	ns	
	$\overline{PL}$ to CP	5.0	1.0		

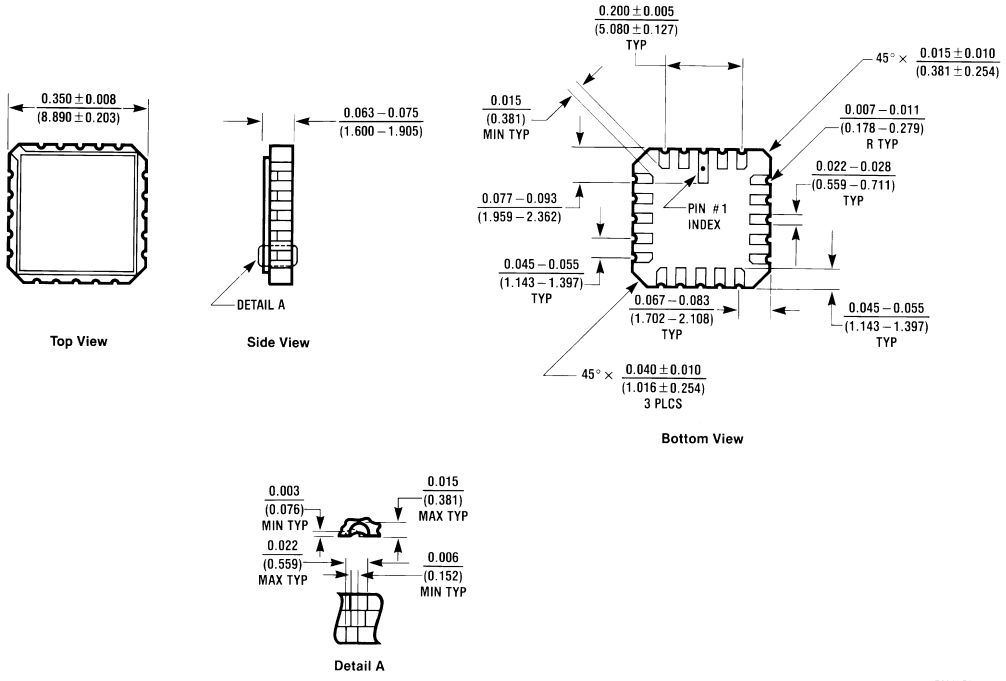
Note 6: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

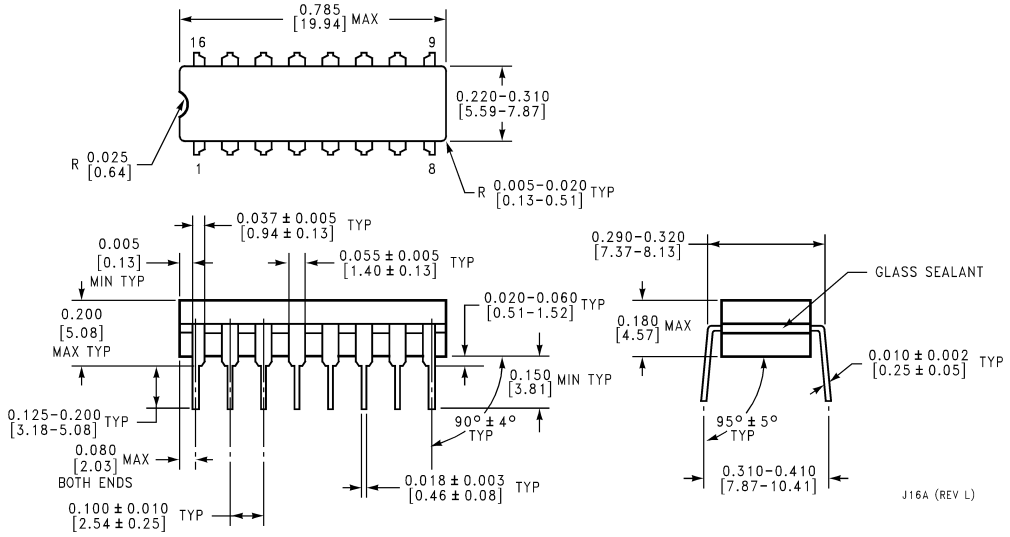
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	75.0	pF	V_{CC} = 5.0V



Physical Dimensions inches (millimeters) unless otherwise noted

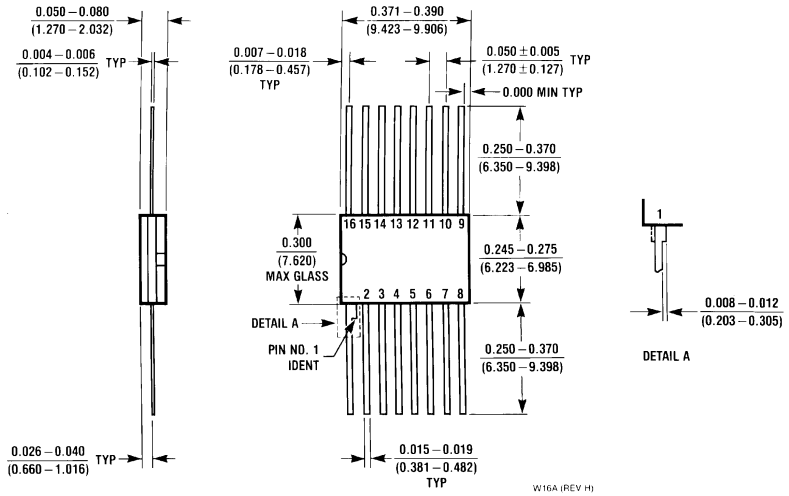


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A



16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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