

## 54ABT646

# Octal Transceivers and Registers with TRI-STATE® Outputs

### General Description

The 54ABT646 consists of bus transceiver circuits with TRI-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control  $\overline{OE}$  and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control  $\overline{OE}$  is Active LOW. In the isolation mode (control  $\overline{OE}$  HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

### Features

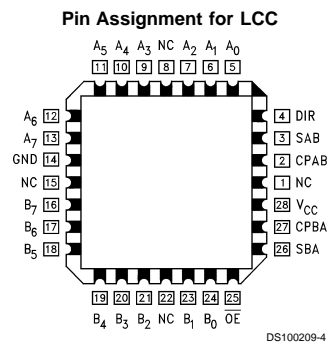
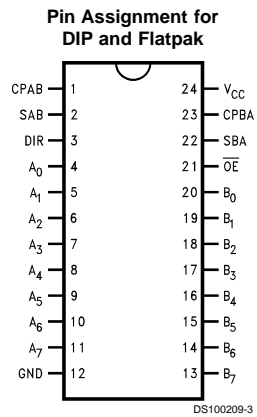
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- A and B output sink capability of 48 mA, source capability of 24 mA
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9457701

### Ordering Code

Military	Package Number	Package Description
54ABT646J-QML	J24A	24-Lead Ceramic Dual-In-Line
54ABT646W-QML	W24C	24-Lead Cerpack
54ABT646E-QML	E28A	28-Lead Ceramic Leadless Chip Carrier, Type C

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## Connection Diagrams



## Pin Descriptions

Pin Names	Description
A <sub>0</sub> -A <sub>7</sub>	Data Register A Inputs/ TRI-STATE Outputs
B <sub>0</sub> -B <sub>7</sub>	Data Register B Inputs/ TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Select Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

## Connection Diagrams (Continued)

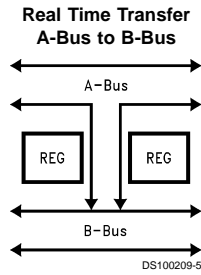


FIGURE 1.

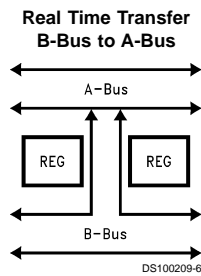


FIGURE 2.

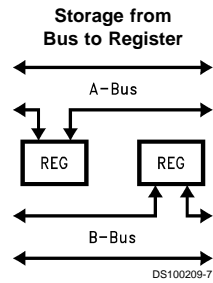


FIGURE 3.

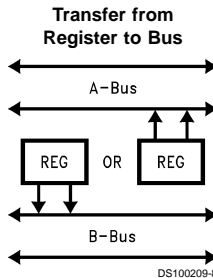


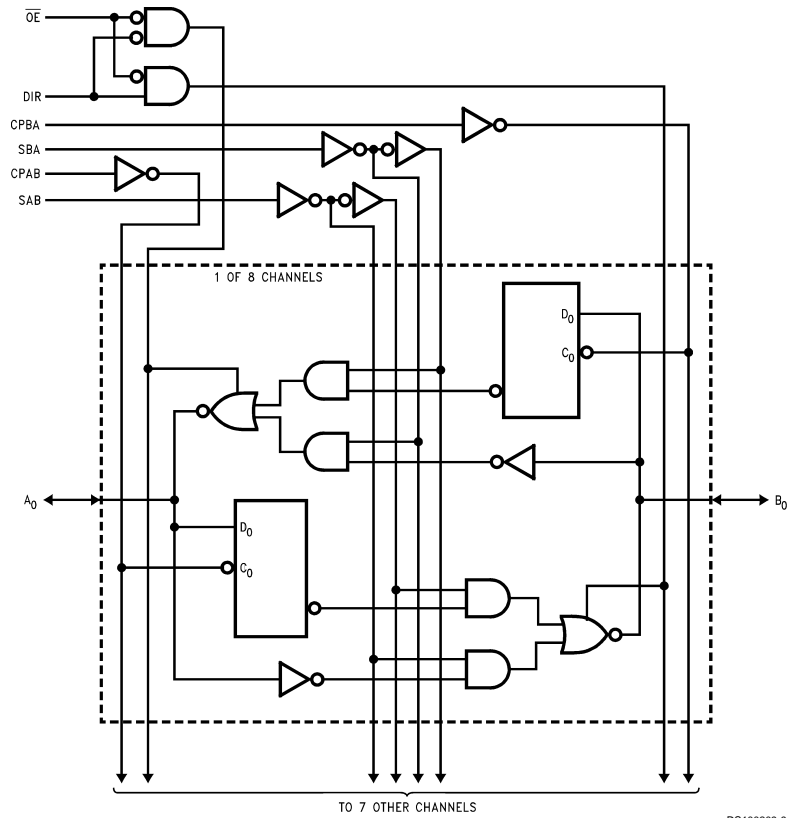
FIGURE 4.

Inputs						Data I/O (Note 1)		Function
O $\overline{E}$	DIR	CPAB	CPBA	SAB	SBA	A $_0$ -A $_7$	B $_0$ -B $_7$	
H	X	H or L	H or L	X	X			Isolation
H	X	↗	X	X	X	Input	Input	Clock A $_n$ Data into A Register Clock B $_n$ Data into B Register
H	X	X	↗	X	X			
L	H	X	X	L	X	Input	Output	A $_n$ to B $_n$ — Real Time (Transparent Mode) Clock A $_n$ Data into A Register
L	H	↗	X	L	X			Clock A $_n$ Data into A Register
L	H	H or L	X	H	X			A Register to B $_n$ (Stored Mode)
L	H	↗	X	H	X			Clock A $_n$ Data into A Register and Output to B $_n$
L	L	X	X	X	L	Output	Input	B $_n$ to A $_n$ — Real Time (Transparent Mode) Clock B $_n$ Data into B Register
L	L	X	↗	X	L			Clock B $_n$ Data into B Register
L	L	X	H or L	X	H			B Register to A $_n$ (Stored Mode)
L	L	X	↗	X	H			Clock B $_n$ Data into B Register and Output to A $_n$

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
↗ = LOW-to-HIGH Transition

**Note 1:** The data output functions may be enabled or disabled by various signals at the  $\overline{O\overline{E}}$  and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

## Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA

Over Voltage Latchup (I/O)

10V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	ABT646			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8		V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54ABT	2.5		V		I <sub>OH</sub> = -3 mA, (A <sub>n</sub> , B <sub>n</sub> )
		54ABT	2.0		Min		I <sub>OH</sub> = -24 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA, (A <sub>n</sub> , B <sub>n</sub> )
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, (Non-I/O Pins) All Other Pins Grounded
I <sub>IH</sub>	Input HIGH Current		5		μA	Max	V <sub>IN</sub> = 2.7V (Non-I/O Pins) (Note 5)
			5				V <sub>IN</sub> = V <sub>CC</sub> (Non-I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test		7		μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Pins)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)		100		μA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub>	Input LOW Current		-5		μA	Max	V <sub>IN</sub> = 0.5V (Non-I/O Pins) (Note 5)
			-5				V <sub>IN</sub> = 0.0V (Non-I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current		50		μA	0V-5.5V	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> ); $\overline{OE}$ = 2.0V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current		-50		μA	0V-5.5V	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> ); $\overline{OE}$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current	-100	-275		mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current		50		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test		100		μA	0.0V	V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> ); All Others GND
I <sub>CCH</sub>	Power Supply Current		250		μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current		30		mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current		50		μA	Max	Outputs TRI-STATE; All Others GND
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input		2.5		mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Other Outputs at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 5)	No Load	0.18		mA/MHz	Max	Outputs Open OE and DIR = GND, Non-I/O = GND or V <sub>CC</sub> (Note 4) One Bit toggling, 50% duty cycle

## DC Electrical Characteristics (Continued)

**Note 4:** For 8-bit toggling,  $I_{CCD} < 1.4$  mA/MHz.

**Note 5:** Guaranteed but not tested.

## AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50$ pF			
		Min	Max		
$f_{max}$	Max Clock Frequency	125		MHz	
$t_{PLH}$	Propagation Delay	2.2	8.8	ns	Figure 8
$t_{PHL}$	Clock to Bus	1.7	8.8		
$t_{PLH}$	Propagation Delay	1.5	7.9	ns	Figure 8
$t_{PHL}$	Bus to Bus	1.5	7.9		
$t_{PLH}$	Propagation Delay	1.5	8.1	ns	Figure 8
$t_{PHL}$	SBA or SAB to $A_n$ to $B_n$	1.5	8.9		
$t_{PZH}$	Enable Time	1.0	7.3	ns	Figure 10
$t_{PZL}$	$\overline{OE}$ to $A_n$ or $B_n$	1.9	8.8		
$t_{PHZ}$	Disable Time	1.5	9.3	ns	Figure 10
$t_{PLZ}$	$\overline{OE}$ to $A_n$ or $B_n$	1.5	9.3		
$t_{PZH}$	Enable Time	1.0	7.7	ns	Figure 10
$t_{PZL}$	DIR to $A_n$ or $B_n$	2.2	9.5		
$t_{PHZ}$	Disable Time	1.5	8.7	ns	Figure 10
$t_{PLZ}$	DIR to $A_n$ or $B_n$	1.5	9.2		

## AC Operating Requirements

Symbol	Parameter	54ABT		Units	Fig. No.
		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50$ pF			
		Min	Max		
$t_S(H)$	Setup Time, HIGH	3.5		ns	Figure 11
$t_S(L)$	or LOW Bus to Clock				
$t_H(H)$	Hold Time, HIGH	1.0		ns	Figure 11
$t_H(L)$	or LOW Bus to Clock				
$t_W(H)$	Pulse Width, HIGH	4.0		ns	Figure 9
$t_W(L)$	HIGH or LOW				

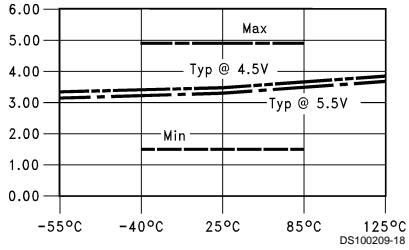
## Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
$C_{IN}$	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ (non I/O pins)
$C_{I/O}$ (Note 6)	Output Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ ( $A_n$ , $B_n$ )

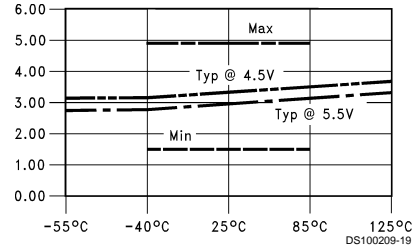
**Note 6:**  $C_{I/O}$  is measured at frequency,  $f = 1$  MHz, per MIL-STD-883B, Method 3012.

## Capacitance (Continued)

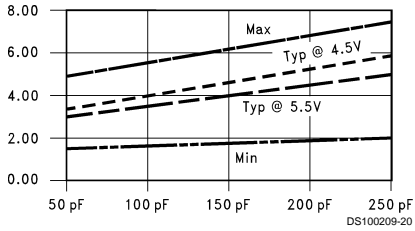
**$t_{PLH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 Clock to Bus



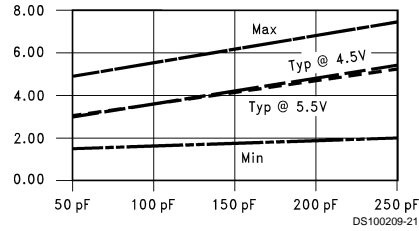
**$t_{PHL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 Clock to Bus



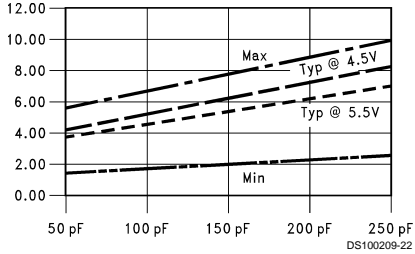
**$t_{PLH}$  vs Load Capacitance**  
 1 Output Switching,  $T_A = 25^\circ\text{C}$   
 Clock to Bus



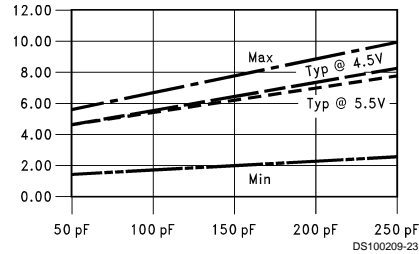
**$t_{PHL}$  vs Load Capacitance**  
 1 Output Switching,  $T_A = 25^\circ\text{C}$   
 Clock to Bus



**$t_{PLH}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$   
 Clock to Bus



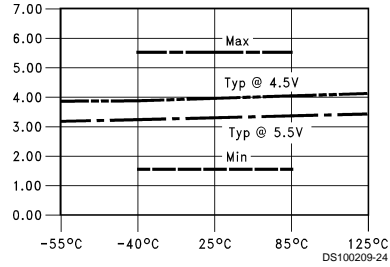
**$t_{PHL}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$   
 Clock to Bus



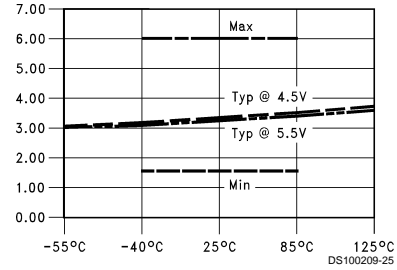
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## Capacitance (Continued)

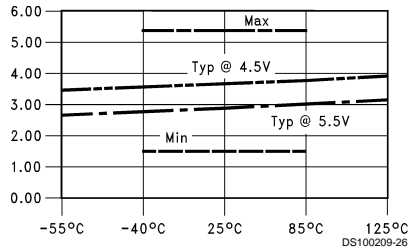
**$t_{PZL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 OE to Bus



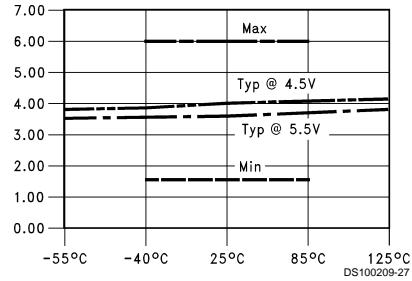
**$t_{PLZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 OE to Bus



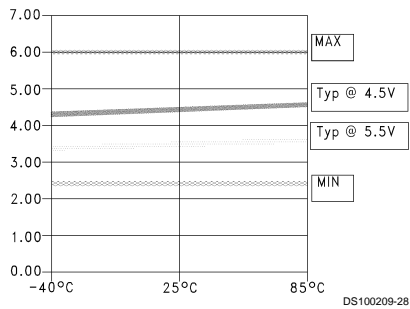
**$t_{PZH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



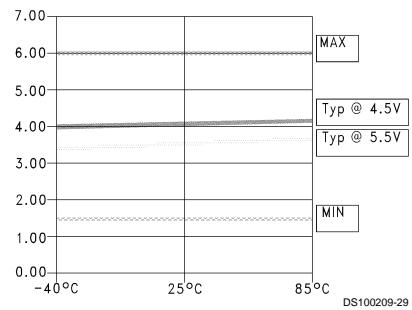
**$t_{PHZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching  
 OE to Bus



**$t_{PZH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching  
 OE to Bus



**$t_{PHZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching  
 OE to Bus

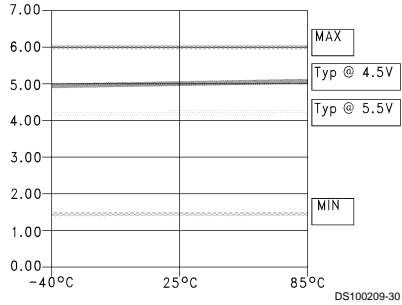


Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

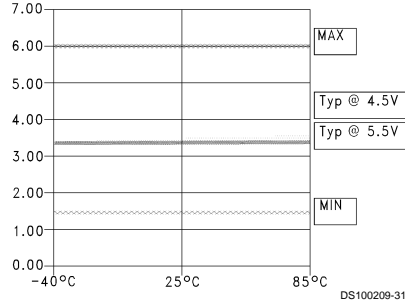


## Capacitance (Continued)

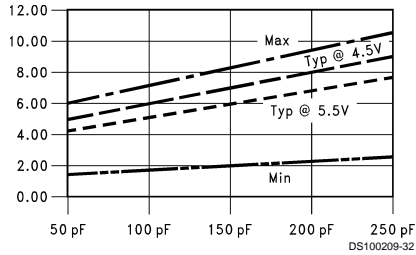
**$t_{PZL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching  
 OE to Bus



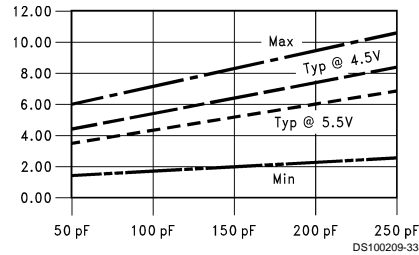
**$t_{PLZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching  
 OE to Bus



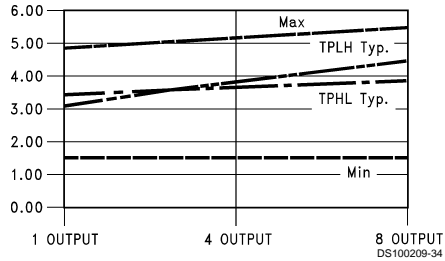
**$t_{PZL}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$   
 OE to Bus



**$t_{PZH}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$   
 OE to Bus



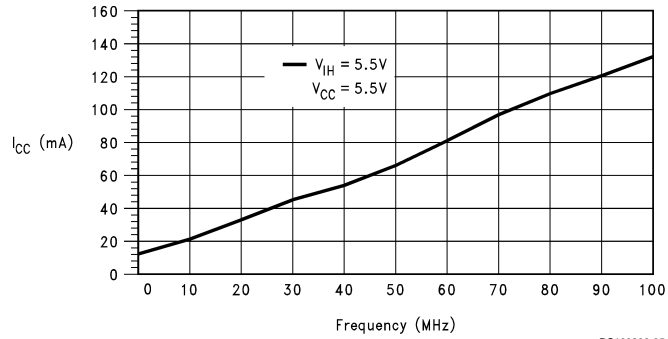
**$t_{PLH}$  and  $t_{PHL}$  vs Number Output Switching**  
 $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$   
 $C_L = 50$  pF, Clock to Bus



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

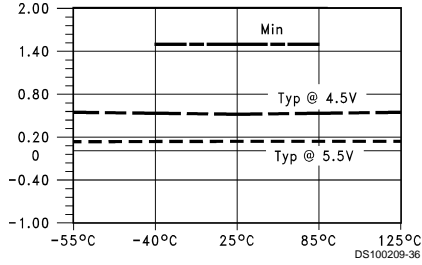
## Capacitance (Continued)

$I_{CC}$  vs Frequency, Average,  
 $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.5\text{V}$   
 All Outputs Unloaded/Unterminated;  
 All Outputs Switching in phase @50% Duty Cycle



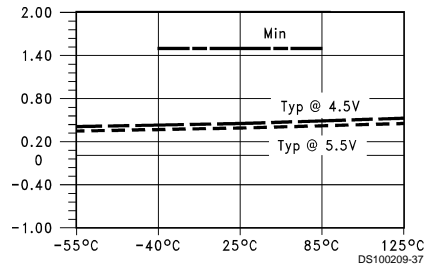
DS100209-35

$t_{SET}$  LOW vs Temperature ( $T_A$ )  
 $C_L = 50\text{ pF}$ , 1 Output Switching  
 Bus to Clock



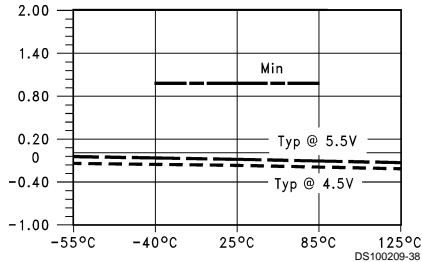
DS100209-36

$t_{SET}$  HIGH vs Temperature ( $T_A$ )  
 $C_L = 50\text{ pF}$ , 1 Output Switching  
 Bus to Clock



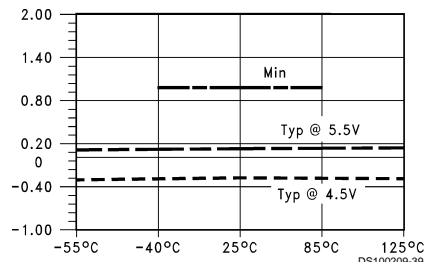
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$t_{HOLD}$  LOW vs Temperature ( $T_A$ )  
 $C_L = 50\text{ pF}$ , 1 Output Switching  
 Bus to Clock



DS100209-38

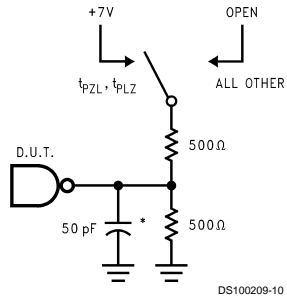
$t_{HOLD}$  HIGH vs Temperature ( $T_A$ )  
 $C_L = 50\text{ pF}$ , 1 Output Switching  
 Bus to Clock



DS100209-39

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

## AC Loading



\*Includes jig and probe capacitance

FIGURE 5. Standard AC Test Load

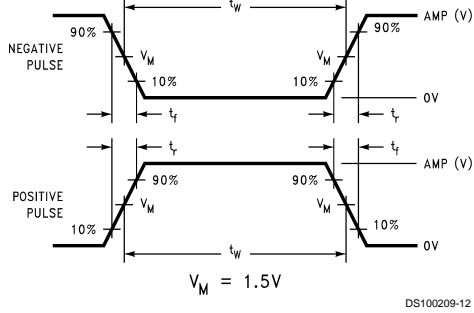


FIGURE 6. Test Input Signal Levels  
Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 7. Test Input Signal Requirements

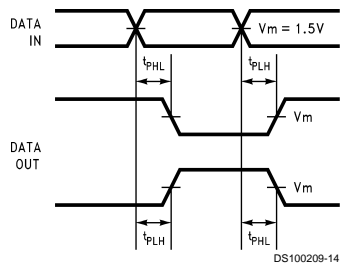


FIGURE 8. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

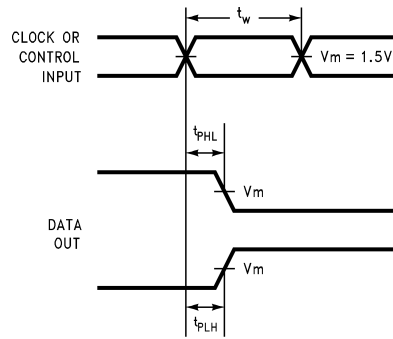


FIGURE 9. Propagation Delay,  
Pulse Width Waveforms

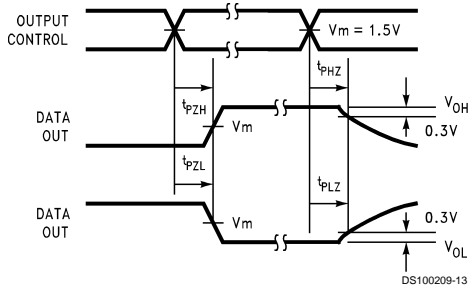


FIGURE 10. TRI-STATE Output HIGH  
and LOW Enable and Disable Times

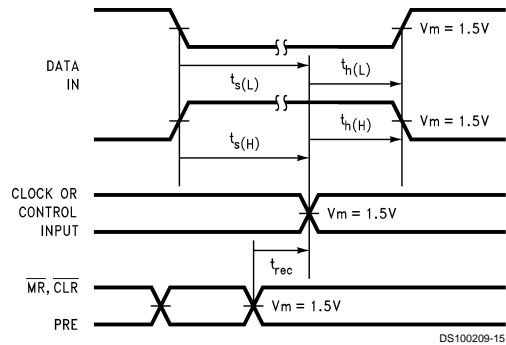
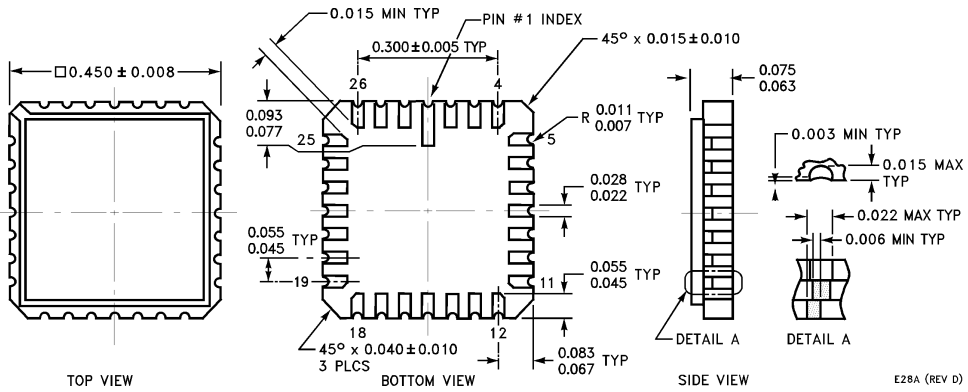


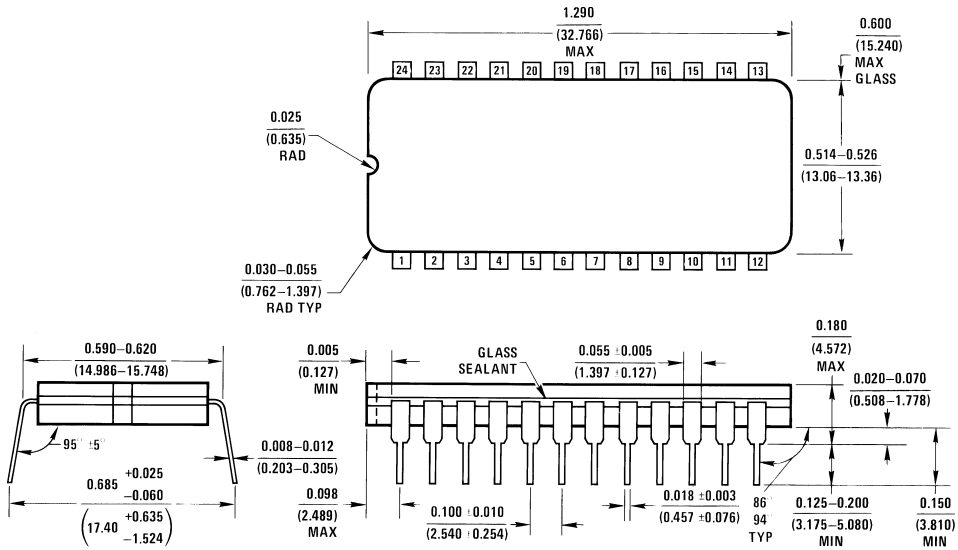
FIGURE 11. Setup Time, Hold Time  
and Recovery Time Waveforms



**Physical Dimensions** inches (millimeters) unless otherwise noted

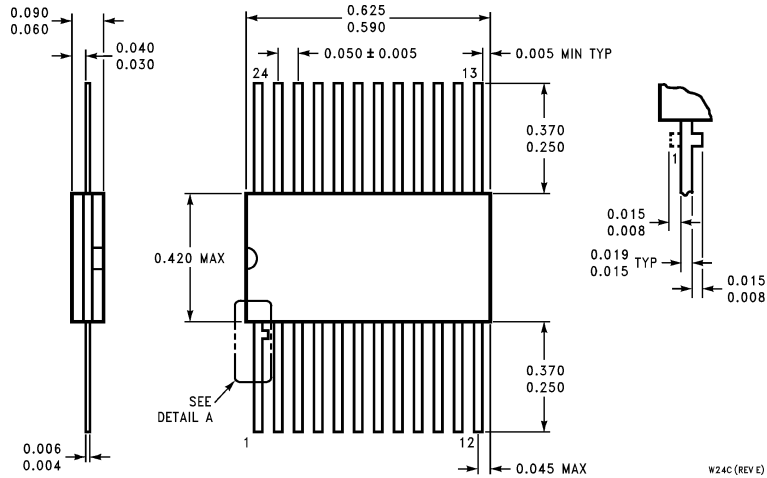


**28-Lead Ceramic Leadless Chip Carrier (L)**  
NS Package Number E28A



**24-Lead Ceramic Dual-in-Line Package (D)**  
NS Package Number J24A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24-Lead Ceramic Flatpak Package (F)**  
**NS Package Number W24C**

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