

## 54ABT273 Octal D-Type Flip-Flop

### General Description

The 'ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

- Buffered common clock
- Buffered, asynchronous Master Reset
- See 'ABT377 for clock enable version
- See 'ABT373 for transparent latch version
- See 'ABT374 for TRI-STATE® version
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9321701

### Features

- Eight edge-triggered D flip-flops

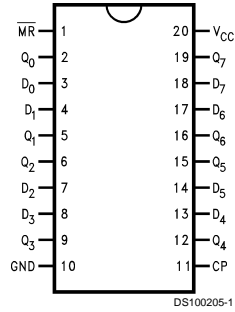
### Ordering Code

Military	Package Number	Package Description
54ABT273J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT273W-QML	W20A	20-Lead Cerpack
54ABT273E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

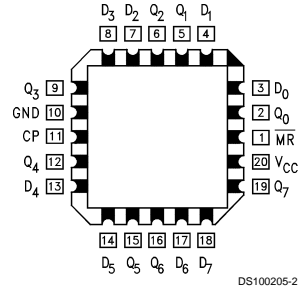
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## Connection Diagrams

Pin Assignment for DIP and Flatpack



Pin Assignment for LCC



Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
$\overline{\text{MR}}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
Q <sub>0</sub> –Q <sub>7</sub>	Data Outputs

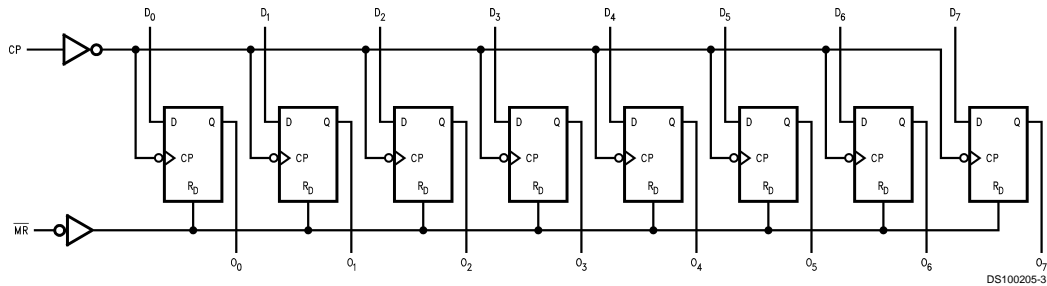
## Truth Table

### Mode Select-Function Table

Operating Mode	Inputs			Output
	$\overline{\text{MR}}$	CP	D <sub>n</sub>	Q <sub>n</sub>
Reset (Clear)	L	X	X	L
Load "1"	H	↗	h	H
Load "0"	H	↗	l	L

H = HIGH Voltage Level steady state  
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
L = LOW Voltage Level steady state  
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition  
X = Immaterial  
↗ = LOW-to-HIGH clock transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +4.75V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

DC Latchup Source Current (Across Comm Operating Range)	-500 mA
Over Voltage Latchup	V <sub>CC</sub> + 4.5V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	ABT273			Units	V <sub>CC</sub>	Conditions	
		Min	Typ	Max				
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal	
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal	
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54ABT	2.5				I <sub>OH</sub> = -3 mA	
		54ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA	
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA	
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V (Note 4)	
				5			V <sub>IN</sub> = V <sub>CC</sub>	
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V	
I <sub>IL</sub>	Input LOW Current			-5	μA	Max	V <sub>IN</sub> = 0.5V (Note 4)	
				-5			V <sub>IN</sub> = 0.0V	
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded	
I <sub>OS</sub>	Output Short-Circuit Current	-100	-275		mA	Max	V <sub>OUT</sub> = 0.0V	
I <sub>CEX</sub>	Output High Leakage Current		50		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>	
I <sub>CCH</sub>	Power Supply Current		50		μA	Max	All Outputs HIGH	
I <sub>CCL</sub>	Power Supply Current		30		mA	Max	All Outputs LOW	
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	Outputs Enabled		1.5		mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V
								Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub>	No Load		0.3	mA/ MHz	Max	Outputs Open (Note 3) One Bit Toggling, 50% Duty Cycle	

Note 3: For 8 bits toggling, I<sub>CCD</sub> < 0.5 mA/MHz.

Note 4: Guaranteed but not tested.

## AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
$f_{\text{max}}$	Max Clock Frequency	150		MHz
$t_{\text{PLH}}$	Propagation Delay	1.0	7.0	ns
$t_{\text{PHL}}$	CP to $O_n$	1.0	7.5	
$t_{\text{PHL}}$	Propagation Delay MR to $O_n$	1.0	8.2	ns

## AC Operating Requirements

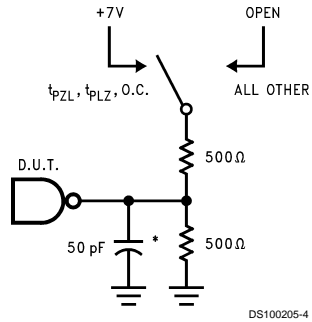
Symbol	Parameter	54ABT		Units
		$T_A = -55^\circ\text{C to }+125^\circ\text{C}$ $V_{CC} = 4.5\text{V to }5.5\text{V}$ $C_L = 50\text{ pF}$		
		Min	Max	
$t_s(\text{H})$	Setup Time, HIGH	2.0		ns
$t_s(\text{L})$	or LOW $D_n$ to CP	2.5		
$t_h(\text{H})$	Hold Time, HIGH	1.4		ns
$t_h(\text{L})$	or LOW $D_n$ to CP	1.4		
$t_w(\text{H})$	Pulse Width, CP,	3.3		ns
$t_w(\text{L})$	HIGH or LOW	3.3		
$t_w(\text{L})$	Master Reset Pulse Width, LOW	3.3		ns
$t_{\text{REC}}$	Recovery Time $\overline{\text{MR}}$ to CP	2.0		ns

## Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
$C_{\text{IN}}$	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$
$C_{\text{OUT}}$ (Note 5)	Output Capacitance	9	pF	$V_{CC} = 5.0\text{V}$

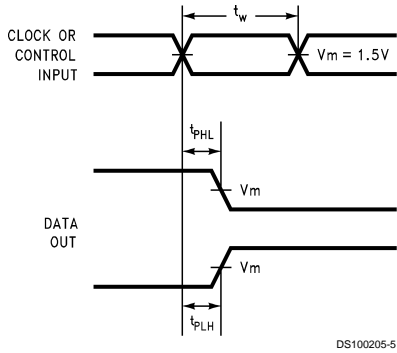
**Note 5:**  $C_{\text{OUT}}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.

# AC Loading

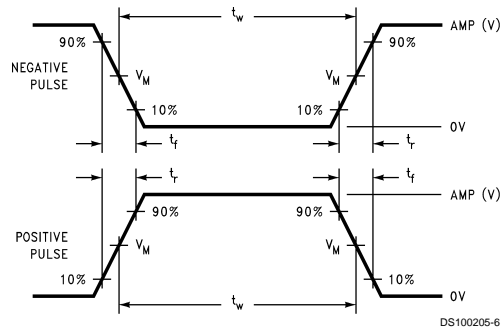


\*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**



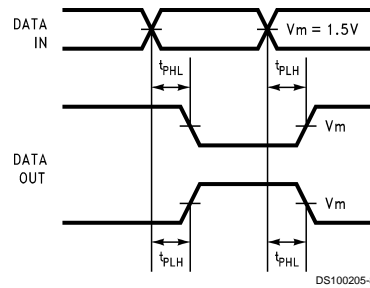
**FIGURE 2. Propagation Delay, Pulse Width Waveforms**



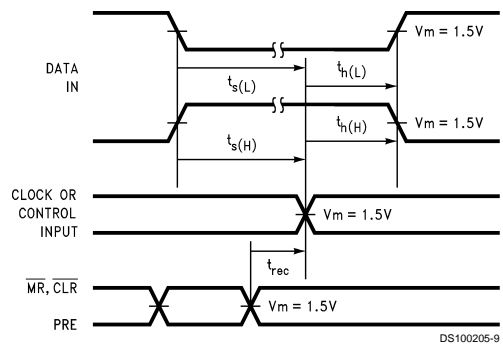
**FIGURE 3. V<sub>M</sub> = 1.5V Input Pulse Requirements**

Amplitude	Rep. Rate	t <sub>w</sub>	t <sub>r</sub>	t <sub>f</sub>
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

**FIGURE 4. Test Input Signal Requirements**



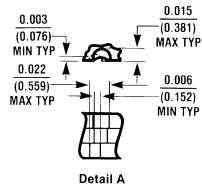
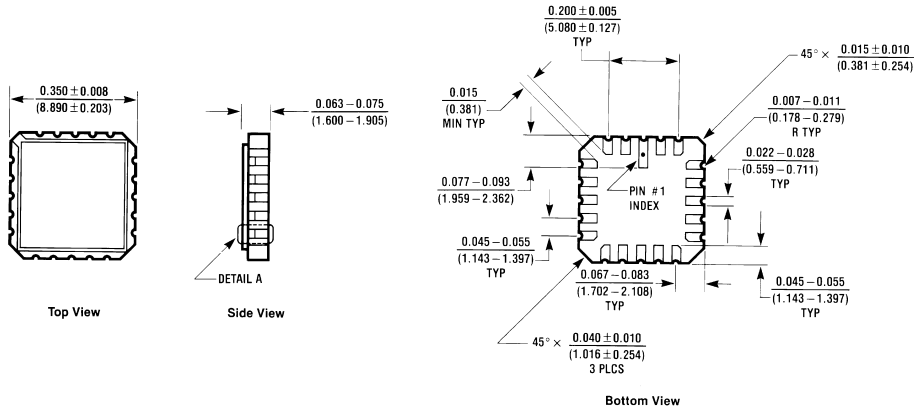
**FIGURE 5. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms**

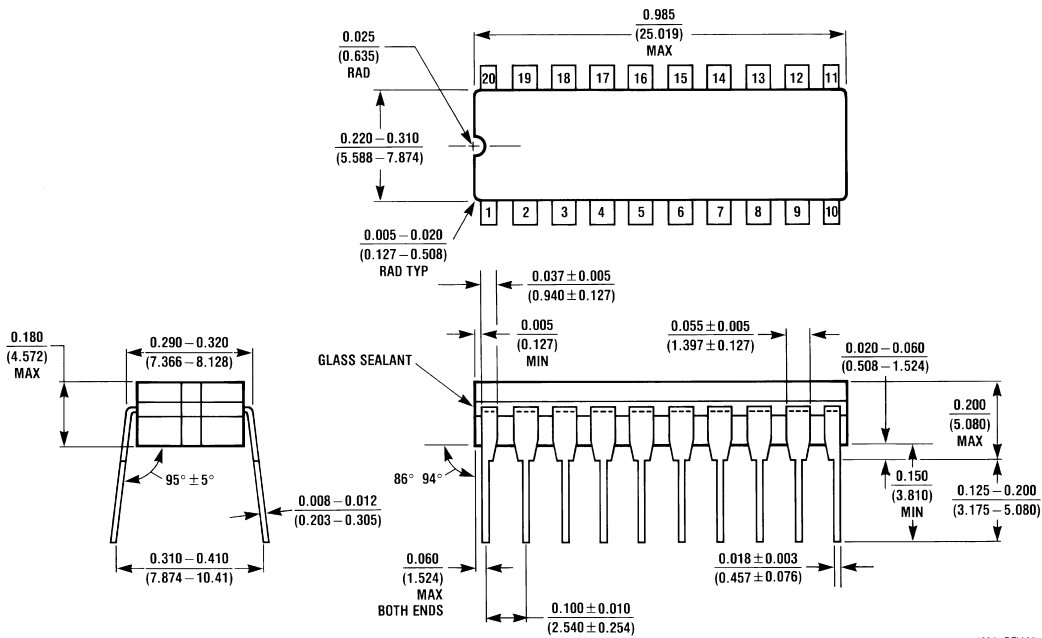


**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

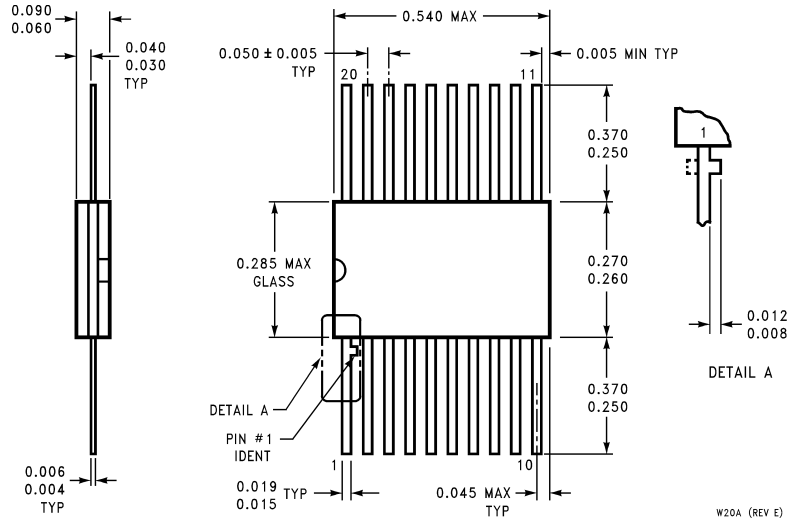
**20-Terminal Ceramic Chip Carrier (L)**  
 NS Package Number E20A



J20A (REV M)

**20-Lead Ceramic Dual-In-Line (D)**  
 NS Package Number J20A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

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