

# 54ABT16500

## 18-Bit Universal Bus Transceivers with TRI-STATE® Outputs

### General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ( $\overline{\text{OEAB}}$  and  $\overline{\text{OEBA}}$ ), latch-enable ( $\text{LEAB}$  and  $\text{LEBA}$ ), and clock ( $\text{CLKAB}$  and  $\text{CLKBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when  $\text{LEAB}$  is high. When  $\text{LEAB}$  is low, the A data is latched if  $\text{CLKAB}$  is held at a high or low logic level. If  $\text{LEAB}$  is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of  $\text{CLKAB}$ . Output-enable  $\text{OEAB}$  is active-high. When  $\text{OEAB}$  is high, the outputs are active. When  $\text{OEAB}$  is low, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses  $\overline{\text{OEBA}}$ ,  $\text{LEBA}$ , and  $\text{CLKBA}$ . The output enables are complementary ( $\text{OEAB}$  is active high and  $\overline{\text{OEBA}}$  is active low).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9687001

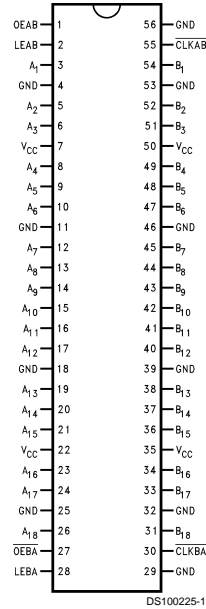
### Ordering Code

| Military        | Package Number | Package Description |
|-----------------|----------------|---------------------|
| 54ABT16500W-QML | WA56A          | 56-Lead Cerpack     |

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## Connection Diagram

Pin Assignment for Cerpack



## Function Table (Note 1)

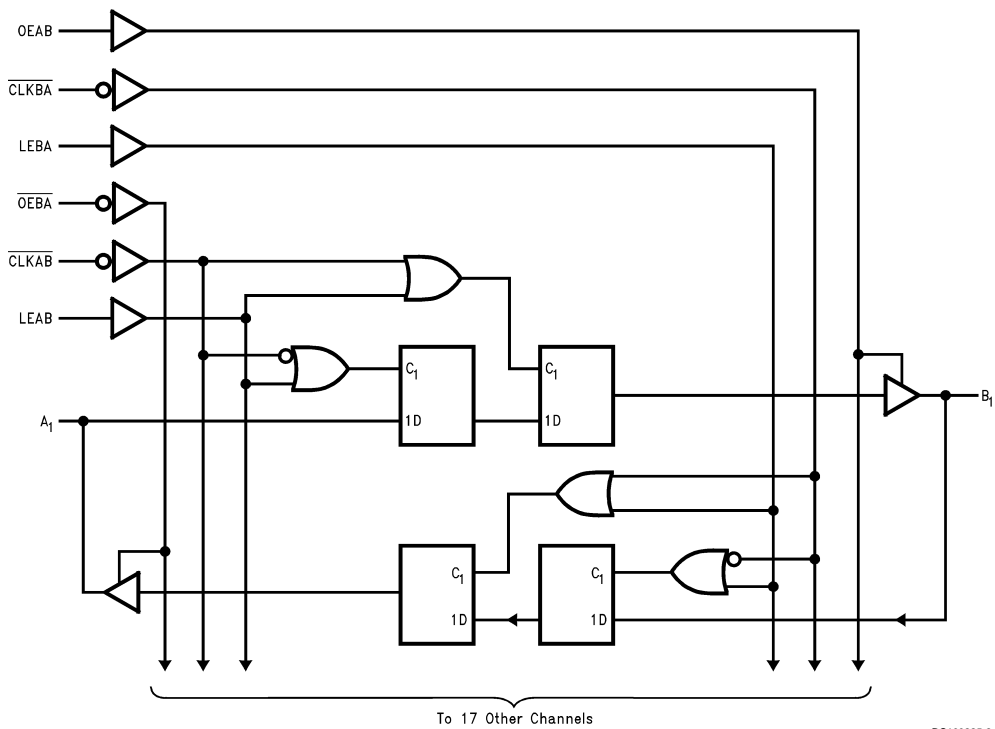
| Inputs |      |       |   | Output                  |
|--------|------|-------|---|-------------------------|
| OEAB   | LEAB | CLKAB | A | B                       |
| L      | X    | X     | X | Z                       |
| H      | H    | X     | L | L                       |
| H      | H    | X     | H | H                       |
| H      | L    | ↓     | L | L                       |
| H      | L    | ↓     | H | H                       |
| H      | L    | H     | X | B <sub>0</sub> (Note 2) |
| H      | L    | L     | X | B <sub>0</sub> (Note 3) |

**Note 1:** A-to-B data flow is shown: B-to-A flow is similar but uses  $\overline{OEBA}$ ,  $\overline{LEBA}$ , and  $\overline{CLKBA}$ .

**Note 2:** Output level before the indicated steady-state input conditions were established.

**Note 3:** Output level before the indicated steady-state input conditions were established, provided that  $\overline{CLKAB}$  was low before  $\overline{LEAB}$  went low.

## Logic Diagram



## Absolute Maximum Ratings (Note 4)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | –65°C to +150°C                      |
| Ambient Temperature under Bias                                   | –55°C to +125°C                      |
| Junction Temperature under Bias                                  |                                      |
| Ceramic  | –55°C to +175°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                      | –0.5V to +7.0V                       |
| Input Voltage (Note 4)   | –0.5V to +7.0V                       |
| Input Current (Note 4)   | –30 mA to +5.0 mA                    |
| Voltage Applied to Any Output in the Disabled or Power-off State | –0.5V to 5.5V                        |
| in the HIGH State  | –0.5V to V <sub>CC</sub>             |
| Current Applied to Output in LOW State (Max)                     | twice the rated I <sub>OL</sub> (mA) |
| DC Latchup Source Current  | –500 mA                              |

Over Voltage Latchup (I/O)

10V

## Recommended Operating Conditions

|                              |                         |
|------------------------------|-------------------------|
| Free Air Ambient Temperature |                         |
| Military                     | –55°C to +125°C         |
| Supply Voltage               |                         |
| Military                     | +4.5V to +5.5V          |
| Minimum Input Edge Rate      | ( $\Delta V/\Delta t$ ) |
| Data Input                   | 50 mV/ns                |
| Enable Input                 | 20 mV/ns                |

**Note 4:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 5:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol                             | Parameter                           | ABT16500 |      |      | Units      | V <sub>CC</sub> | Conditions  |
|------------------------------------|-------------------------------------|----------|------|------|------------|-----------------|---|
|                                    |                                     | Min      | Typ  | Max  |            |                 |   |
| V <sub>IH</sub>                    | Input HIGH Voltage                  | 2.0      |      |      | V          |                 | Recognized HIGH Signal  |
| V <sub>IL</sub>                    | Input LOW Voltage                   |          |      | 0.8  | V          |                 | Recognized LOW Signal   |
| V <sub>CD</sub>                    | Input Clamp Diode Voltage           |          |      | –1.2 | V          | Min             | I <sub>IN</sub> = –18 mA  |
| V <sub>OH</sub>                    | Output HIGH Voltage                 | 2.5      | 2.0  |      | V          | Min             | I <sub>OH</sub> = –3 mA   |
|                                    |                                     |          |      |      | V          | Min             | I <sub>OH</sub> = –24 mA  |
| V <sub>OL</sub>                    | Output LOW Voltage                  |          |      | 0.55 | V          | Min             | I <sub>OL</sub> = 48 mA   |
| I <sub>IH</sub>                    | Input HIGH Current                  |          |      | 5    | μA         | Max             | V <sub>IN</sub> = 2.7V (Note 6)   |
|                                    |                                     |          |      |      | μA         | Max             | V <sub>IN</sub> = V <sub>CC</sub>   |
| I <sub>BVI</sub>                   | Input HIGH Current Breakdown Test   |          |      | 7    | μA         | Max             | V <sub>IN</sub> = 7.0V  |
| I <sub>IL</sub>                    | Input LOW Current                   |          |      | –5   | μA         | Max             | V <sub>IN</sub> = 0.5V (Note 6)   |
|                                    |                                     |          |      |      | μA         | Max             | V <sub>IN</sub> = 0.0V  |
| V <sub>ID</sub>                    | Input Leakage Test                  | 4.75     |      |      | V          | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded                             |
| I <sub>IH</sub> + I <sub>OZH</sub> | Output Leakage Current              |          |      | 50   | μA         | 0 – 5.5V        | V <sub>OUT</sub> = 2.7V; $\overline{OE}$ , OE = 2.0V                            |
| I <sub>IL</sub> + I <sub>OZL</sub> | Output Leakage Current              |          |      | –50  | μA         | 0 – 5.5V        | V <sub>OUT</sub> = 0.5V; $\overline{OE}$ , OE = 2.0V                            |
| I <sub>OS</sub>                    | Output Short-Circuit Current        | –100     | –275 |      | mA         | Max             | V <sub>OUT</sub> = 0V   |
| I <sub>CEX</sub>                   | Output High Leakage Current         |          |      | 50   | μA         | Max             | V <sub>OUT</sub> = V <sub>CC</sub>  |
| I <sub>ZZ</sub>                    | Bus Drainage Test                   |          |      | 100  | μA         | 0.0             | V <sub>OUT</sub> = 5.5V; All Others GND   |
| I <sub>CCH</sub>                   | Power Supply Current                |          |      | 1.0  | mA         | Max             | All Outputs HIGH  |
| I <sub>CCL</sub>                   | Power Supply Current                |          |      | 68   | μA         | Max             | An or Bn Outputs Low  |
| I <sub>CCZ</sub>                   | Power Supply Current                |          |      | 1.0  | mA         | Max             | $\overline{OE}_n$ = V <sub>CC</sub> ,<br>All Others at V <sub>CC</sub> or GND   |
| I <sub>CCT</sub>                   | Additional I <sub>CC</sub> /Input   |          |      | 2.5  | mA         | Max             | V <sub>I</sub> = V <sub>CC</sub> – 2.1V<br>All Others at V <sub>CC</sub> or GND |
| I <sub>CCD</sub>                   | Dynamic I <sub>CC</sub><br>(Note 6) |          |      | 0.23 | mA/<br>MHz | Max             | Outputs Open<br>Transparent Mode<br>One Bit Toggling, 50% Duty Cycle            |

**Note 6:** Guaranteed, but not tested.

## DC Electrical Characteristics

| Symbol           | Parameter                                    | Min | Max  | Units | V <sub>CC</sub> | Conditions<br>C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500Ω |
|------------------|--|-----|------|-------|-----------------|---|
| V <sub>OLP</sub> | Quiet Output Maximum Dynamic V <sub>OL</sub> |     | 1.1  | V     | 5.0             | T <sub>A</sub> = 25°C (Note 7)                              |
| V <sub>OLV</sub> | Quiet Output Minimum Dynamic V <sub>OL</sub> |     | -1.7 | V     | 5.0             | T <sub>A</sub> = 25°C (Note 7)                              |

**Note 7:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol           | Parameter                | 54ABT   |     | Units | Fig. No. |
|------------------|--------------------------|---|-----|-------|----------|
|                  |                          | T <sub>A</sub> = −55°C to +125°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF |     |       |          |
|                  |                          | Min   | Max |       |          |
| f <sub>max</sub> | Maximum Clock Frequency  | 150   |     | MHz   |          |
| t <sub>PLH</sub> | Propagation Delay        | 1.0   | 6.5 | ns    | Figure 4 |
| t <sub>PHL</sub> | A or B to B or A         | 1.0   | 7.0 |       |          |
| t <sub>PLH</sub> | Propagation Delay        | 1.0   | 7.0 | ns    | Figure 4 |
| t <sub>PHL</sub> | LEAB or LEBA to B or A   | 1.0   | 7.8 |       |          |
| t <sub>PLH</sub> | Propagation Delay        | 1.0   | 7.5 | ns    | Figure 4 |
| t <sub>PHL</sub> | CLKAB or CLKBA to B or A | 1.0   | 8.0 |       |          |
| t <sub>PZH</sub> | Propagation Delay        | 1.0   | 6.3 | ns    | Figure 6 |
| t <sub>PZL</sub> | OEAB or OEBA to B or A   | 1.0   | 6.5 |       |          |
| t <sub>PHZ</sub> | Propagation Delay        | 1.0   | 7.2 | ns    | Figure 6 |
| t <sub>PLZ</sub> | OEAB or OEBA to B or A   | 1.0   | 6.8 |       |          |

## AC Operating Requirements

| Symbol             | Parameter                                     | 54ABT   |     | Units | Fig. No. |
|--------------------|---|---|-----|-------|----------|
|                    |   | T <sub>A</sub> = −55°C to +125°C<br>V <sub>CC</sub> = 4.5V–5.5V<br>C <sub>L</sub> = 50 pF |     |       |          |
|                    |   | Min   | Max |       |          |
| t <sub>s</sub> (H) | Setup Time,<br>A to $\overline{\text{CLKAB}}$ | 4.5   |     | ns    | Figure 7 |
| t <sub>s</sub> (L) |   | 4.5   |     |       |          |
| t <sub>h</sub> (H) | Hold Time,<br>A to $\overline{\text{CLKAB}}$  | 0   |     | ns    | Figure 7 |
| t <sub>h</sub> (L) |   | 0   |     |       |          |
| t <sub>s</sub> (H) | Setup Time,<br>B to $\overline{\text{CLKBA}}$ | 4.0   |     | ns    | Figure 7 |
| t <sub>s</sub> (L) |   | 4.0   |     |       |          |
| t <sub>h</sub> (H) | Hold Time,<br>B to $\overline{\text{CLKBA}}$  | 0   |     | ns    | Figure 7 |
| t <sub>h</sub> (L) |   | 0   |     |       |          |
| t <sub>s</sub> (H) | Setup Time, A to LEAB                         | 1.5   |     | ns    | Figure 7 |
| t <sub>s</sub> (L) | or B to LEBA, $\overline{\text{CLK}}$ High    | 1.5   |     |       |          |
| t <sub>h</sub> (H) | Hold Time, A to LEAB                          | 1.5   |     | ns    | Figure 7 |
| t <sub>h</sub> (L) | or B to LEBA, $\overline{\text{CLK}}$ High    | 1.5   |     |       |          |
| t <sub>s</sub> (H) | Setup Time, A to LEAB                         | 4.5   |     | ns    | Figure 7 |
| t <sub>s</sub> (L) | or B to LEBA, $\overline{\text{CLK}}$ Low     | 4.5   |     |       |          |
| t <sub>h</sub> (H) | Hold Time, A to LEAB                          | 1.5   |     | ns    | Figure 7 |
| t <sub>h</sub> (L) | or B to LEBA, $\overline{\text{CLK}}$ Low     | 1.5   |     |       |          |
| t <sub>w</sub> (H) | Pulse Width,<br>LEAB or LEBA, High            | 3.3   |     | ns    | Figure 5 |
| t <sub>w</sub> (L) |   | 3.3   |     |       |          |

## AC Operating Requirements (Continued)

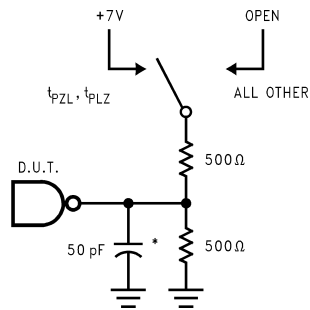
| Symbol          | Parameter                                  | 54ABT   | Units | Fig. No. |
|-----------------|--|---|-------|----------|
|                 |  | $T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$<br>$V_{CC} = 4.5\text{V} - 5.5\text{V}$<br>$C_L = 50 \text{ pF}$ |       |          |
|                 |  | Min                      Max  |       |          |
| $t_w(\text{H})$ | Pulse Width, $\overline{\text{CLKAB}}$     | 3.3   | ns    | Figure 5 |
| $t_w(\text{L})$ | or $\overline{\text{CLKBA}}$ , High or Low | 3.3   |       |          |

## Capacitance

| Symbol                    | Parameter          | Typ  | Units | Conditions, $T_A = 25^{\circ}\text{C}$ |
|---------------------------|--------------------|------|-------|--|
| $C_{\text{IN}}$           | Input Capacitance  | 5.0  | pF    | $V_{CC} = 0.0\text{V}$                 |
| $C_{\text{I/O}}$ (Note 8) | Output Capacitance | 11.0 | pF    | $V_{CC} = 5.0\text{V}$                 |

**Note 8:**  $C_{\text{I/O}}$  is measured at frequency  $f = 1 \text{ MHz}$  per MIL-STD-883B, Method 3012.

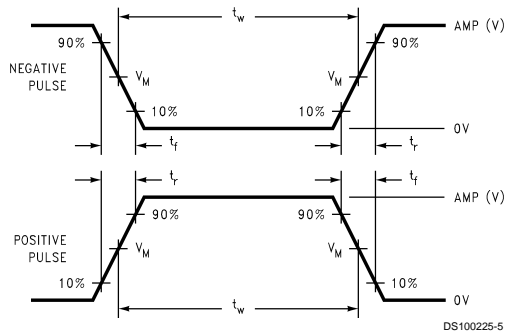
## AC Loading



DS100225-3

\*Includes jig and probe capacitance.

**FIGURE 1. Standard AC Test Load**



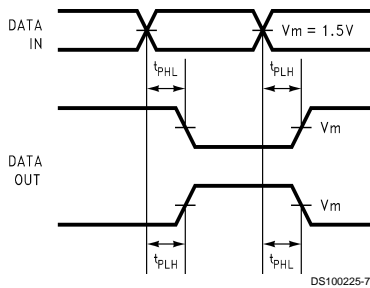
DS100225-5

**FIGURE 2.  $V_m = 1.5V$**

### Input Pulse Requirements

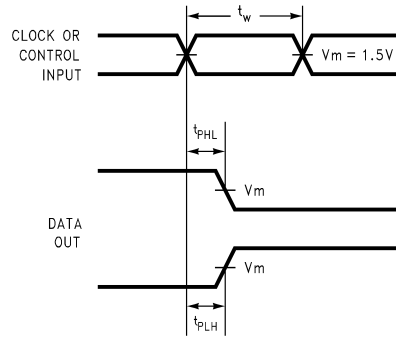
| Amplitude | Rep. Rate | $t_w$  | $t_r$  | $t_f$  |
|-----------|-----------|--------|--------|--------|
| 3.0V      | 1 MHz     | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 3. Test Input Signal Requirements**



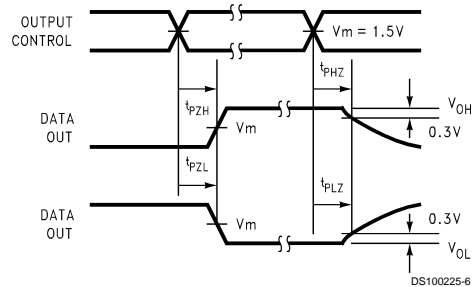
DS100225-7

**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



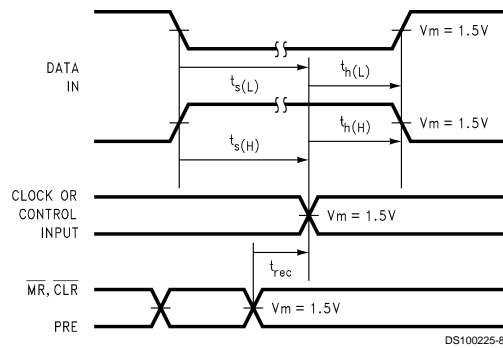
DS100225-4

**FIGURE 5. Propagation Delay, Pulse Width Waveforms**



DS100225-6

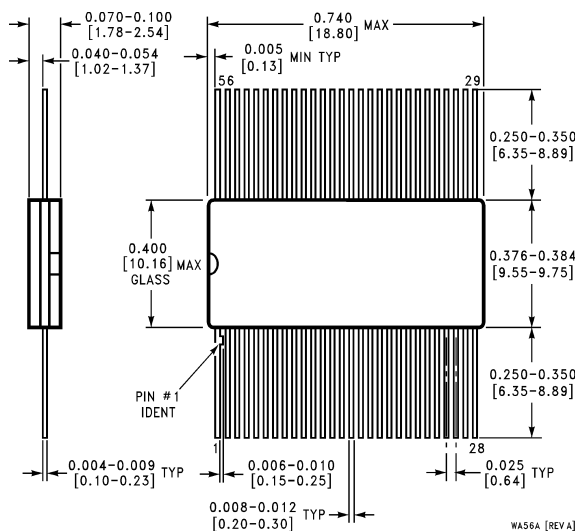
**FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times**



DS100225-8

**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

## Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Cerpack  
NS Package Number WA56A

### LIFE SUPPORT POLICY

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**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

www.national.com

**National Semiconductor Europe**

Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**

Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**

Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179

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