DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD72862

IEEE1394 OHCI HOST CONTROLLER

The μPD72862 is IEEE1394 OHCI-Link controller. The μPD72862 complies with the P1394a draft 2.0 specifications and works up to 400 Mbps.

It supports both of the Cardbus interface and the PCI bus interface.

FEATURES

- Compliant with Link Layer Services as defined in 1394 Open Host Controller Interface specification release 1.0
- Compliant with protocol enhancement as defined in P1394a draft 2.0
- Modular 32-bit host interface compliant to PCI Specification release 2.1
- Supports PCI-Bus Power Management Interface Specification release 1.0
- Supports Cardbus
- Equipped CIS register
- Cycle Master and Isochronous Resource Manager capable
- Compatible to PHY Layer implementation of 100/200/400 Mbps via 2/4/8-bit data interface
- Built-in FIFOs for isochronous transmit (1024 bytes), asynchronous transmit (1024 bytes), and receive (2048 bytes)
- 32-bit CRC generation and checking for receive/transmit packets
- 4-isochronous transmit DMAs and 4-isochronous receive DMAs supported
- Support both IEEE1394-1995 compliant PHY and P1394a compliant PHY
- Internal control and operational registers direct-mapped to PCI configuration space
- 2-wire Serial EEPROM™ interface supported

ORDERING INFORMATION

Part number	Package
μPD72862GC-9EU	100-pin plastic TQFP (Fine pitch) (14 x 14)

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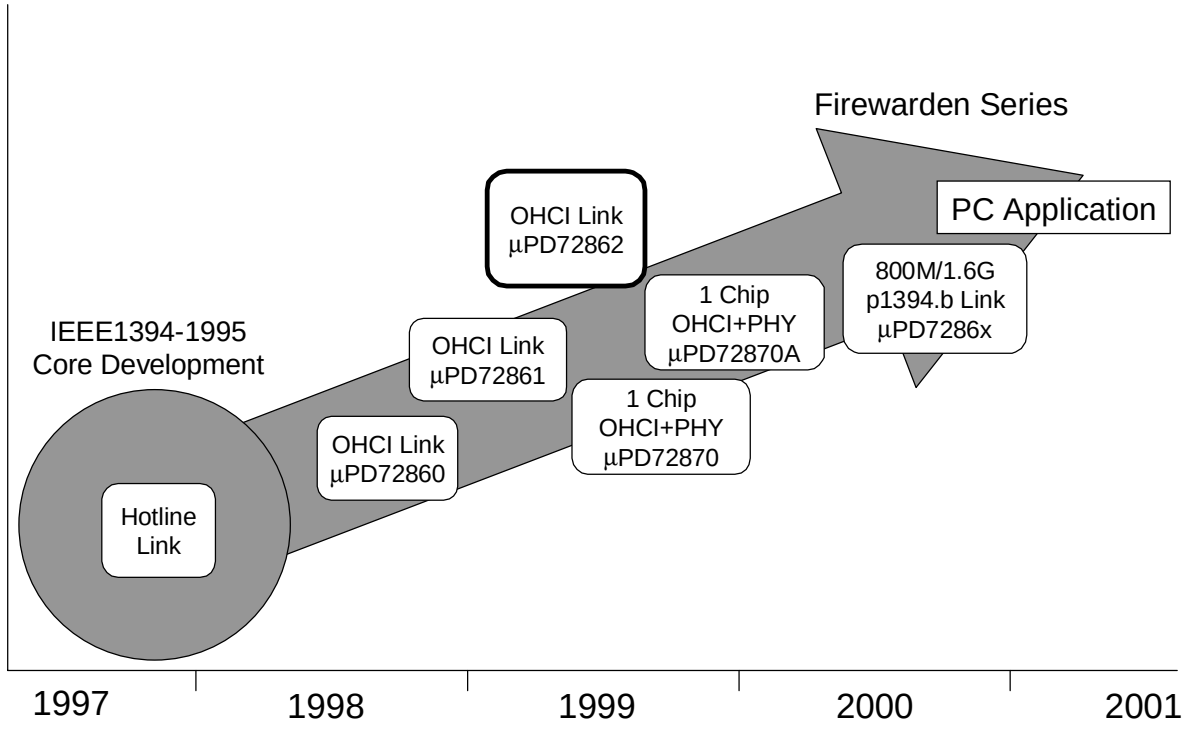
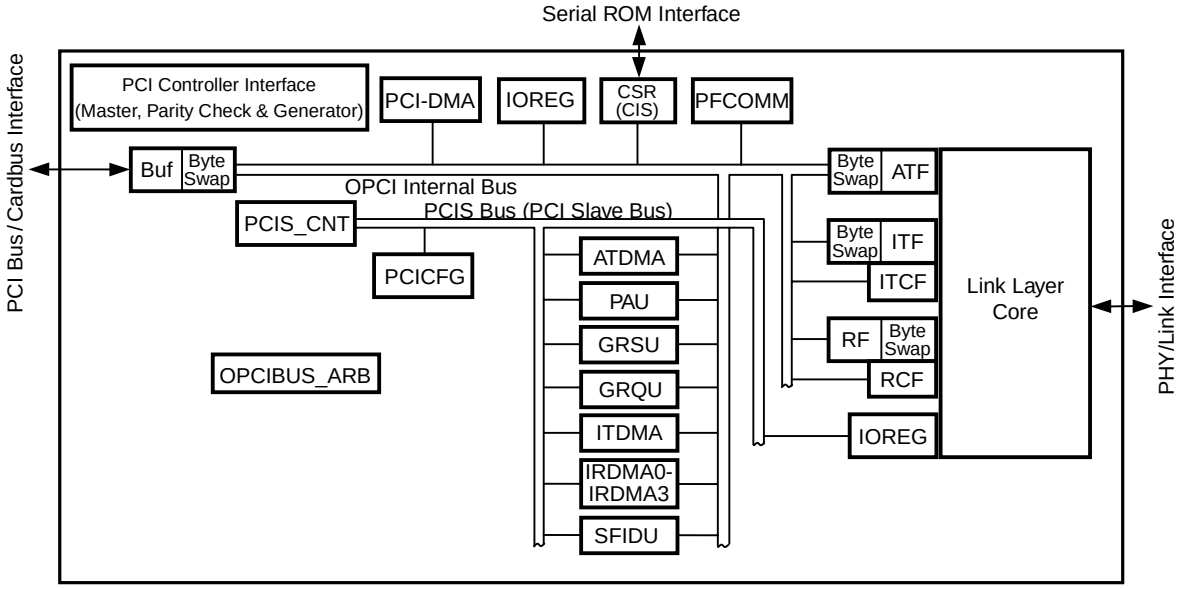
Printed in Japan

The mark ★ shows major revised points.

Firewarden™ ROADMAP



BLOCK DIAGRAM

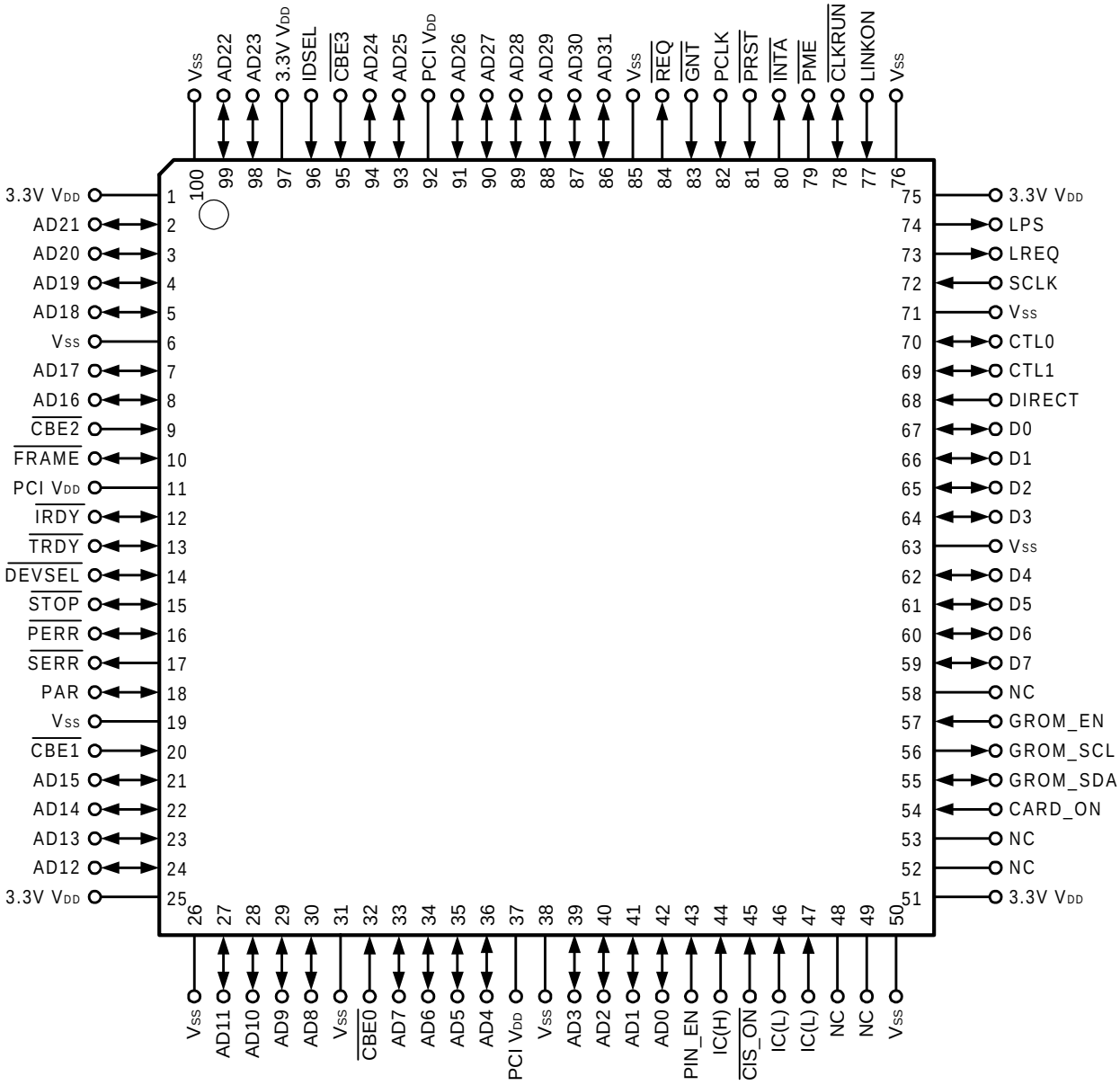


ATDMA	: Asynchronous Transmit DMA
ATF	: Asynchronous Transmit FIFO
CIS	: CIS Register
CSR	: Control and Status Registers
IOREG	: IO Registers
IRDMA	: Isochronous Receive DMA
ITCF	: Isochronous Transmit Control FIFO
ITDMA	: Isochronous Transmit DMA
ITF	: Isochronous Transmit FIFO
OPCIBUS_ARB	: OPCI Internal Bus Arbitration
PAU	: Physical Response and Request Unit
PCICFG	: PCI Configuration Registers
PCIS_CNT	: PHY Control Isochronous Control
PFCOMM	: Pre Fetch Command FIFO
RCF	: Receive Control FIFO
RF	: Receive FIFO
SFIDU	: Self-ID DMA

PIN CONFIGURATION (Top View)

Though the current implementation of the μPD72862 includes signal pins for debugging and testing purpose, the package remains a cost efficient 100-pin TQFP package.

- **100-pin plastic TQFP (Fine pitch) (14 x 14)**



PIN NAME

AD0-AD31	: PCI Multiplexed Address and Data
CARD_ON	: PCI/Card Select
$\overline{\text{CBE0}}$-$\overline{\text{CBE3}}$	: Command/Byte Enables
$\overline{\text{CIS\_ON}}$	: CIS Register ON
$\overline{\text{CLKRUN}}$	: PCICLK Running
CTL0, CTL1	: PHY/Link Bi-directional Control
$\overline{\text{DEVSEL}}$	: Device Select
DIRECT	: Auxiliary PHY/Link Signal
D0-D7	: PHY/Link Bi-directional Data
$\overline{\text{FRAME}}$	: Cycle Frame
$\overline{\text{GNT}}$	: Bus_master Grant
GROM_EN	: Serial EEPROM Enable
GROM_SCL	: Serial EEPROM Clock Output
GROM_SDA	: Serial EEPROM Data Input / Output
IC (H)	: Internally Connected (High Clamped)
IC (L)	: Internally Connected (Low Clamped)
IDSEL	: ID Select
$\overline{\text{INTA}}$	: Interrupt
$\overline{\text{IRDY}}$	: Initiator Ready
LINKON	: Link-On Request
LPS	: Link Power Status
LREQ	: PHY/Link Request
NC	: Non-Connection
PAR	: Parity
PCLK	: PCI Clock
$\overline{\text{PERR}}$	: Parity Error
PIN_EN	: Pin Enable Input
$\overline{\text{PME}}$	: PME Output
$\overline{\text{PRST}}$	: Reset
$\overline{\text{REQ}}$	: Bus_master Request
SCLK	: PHY Clock
$\overline{\text{SERR}}$	: System Error
$\overline{\text{STOP}}$	: PCI Stop
$\overline{\text{TRDY}}$	: Target Ready
V_{DD}	: Supply Voltage
V_{SS}	: Ground

CONTENTS

1. PIN FUNCTIONS

1.1 PCI Bus Interface Signals: (52 pins)

(1/2)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
PAR	I/O	18	PCI/Cardbus	5/3.3	**Parity** is even parity across AD0-AD31 and $\overline{\text{CBE0}}$-$\overline{\text{CBE3}}$. It is an input when AD0-AD31 is an input; it is an output when AD0-AD31 is an output.
AD0-AD31	I/O	2-5, 7, 8, 21-24, 27-30, 33-36, 39-42, 86-91, 93, 94, 98, 99	PCI/Cardbus	5/3.3	**PCI Multiplexed Address and Data**
$\overline{\text{CBE0}}$-$\overline{\text{CBE3}}$	I	9, 20, 32, 95	-	5/3.3	**Command/Byte Enables** are multiplexed Bus Commands & Byte enables.
$\overline{\text{FRAME}}$	I/O	10	PCI/Cardbus	5/3.3	**Cycle Frame** is asserted by the initiator to indicate the cycle beginning and is kept asserted during the burst cycle. ★ If Cardbus mode (CARD_ON = 1), this pin is should be pulled up to V_{DD}.
$\overline{\text{TRDY}}$	I/O	13	PCI/Cardbus	5/3.3	**Target Ready** indicates that the current data phase of the transaction is ready to be completed.
$\overline{\text{IRDY}}$	I/O	12	PCI/Cardbus	5/3.3	**Initiator Ready** indicates that the current bus master is ready to complete the current data phase. During a write, its assertion indicates that the initiator is driving valid data onto the data bus. During a read, its assertion indicates that the initiator is ready to accept data from the currently-addressed target.
$\overline{\text{REQ}}$	O	84	PCI/Cardbus	5/3.3	**Bus_master Request** indicates to the bus arbiter that this device wants to become a bus master.
$\overline{\text{GNT}}$	I	83	-	5/3.3	**Bus_master Grant** indicates to this device that access to the bus has been granted.
IDSEL	I	96	-	5/3.3	**ID Select** when actively driven, indicates that the IUHC is chip-selected for configuration read/write transaction during the phase of device initialization. ★ If Cardbus mode (CARD_ON = 1), this pin is should be pulled up to V_{DD}.
$\overline{\text{DEVSEL}}$	I/O	14	PCI/Cardbus	5/3.3	**Device Select** when actively driven, indicates that the driving device has decoded its address as the target of the current access.
$\overline{\text{STOP}}$	I/O	15	PCI/Cardbus	5/3.3	**PCI Stop** when actively driven, indicates that the target is requesting the current bus master to stop the transaction.

(2/2)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
$\overline{PME}$	O	79	PCI/Cardbus	5/3.3	**PME Output** for power management enable. ★ **Caution The $\overline{PME}$ pin is not an N-channel open drain structure pin. Therefore, when using S3, S4, S5 state in ACPI, a circuit that can separate between the power supply and the $\overline{PME}$ pin externally is needed.** **ACPI: Advanced Configuration and Power Interface. Please refer to ACPI Specification.**
$\overline{CLKRUN}$	I/O	78	PCI/Cardbus	5/3.3	**PCICLK Running** as input, to determine the status of PCLK; as output, to request starting or speeding up clock.
$\overline{INTA}$	O	80	PCI/Cardbus	5/3.3	**Interrupt** the PCI interrupt request A.
$\overline{PERR}$	I/O	16	PCI/Cardbus	5/3.3	**Parity Error** is used for reporting data parity errors during all PCI transactions, except a Special Cycle. It is an output when AD0-AD31 and PAR are both inputs. It is an input when AD0-AD31 and PAR are both outputs.
$\overline{SERR}$	O	17	PCI/Cardbus	5/3.3	**System Error** is used for reporting address parity errors, data parity errors during the Special Cycle, or any other system error where the effect can be catastrophic. When reporting address parity errors, it is an output.
$\overline{PRST}$	I	81	-	5/3.3	**Reset** PCI reset
PCLK	I	82	-	5/3.3	**PCI Clock** 33 MHz system bus clock.

1.2 PCI/Cardbus Select Signals: (2 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
CARD_ON	I	54	-	3.3	**PCI/Card Select** (1:Cardbus, 0:PCI bus)
$\overline{CIS\_ON}$	I	45	-	3.3	**CIS Register ON** CARD_ON / $\overline{CIS\_ON}$ / CIS / $\overline{PME}$ 0 / 1 / off / $\overline{PME}$ 0 / 0 / on / CSTSCHG 1 / X / on / CSTSCHG

1.3 PHY/Link Interface Signals: (15 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
D0-D7	I/O	59-62, 64-67	9mA	3.3	**PHY/Link Bi-directional Data** (ISO-barrier supported)
CTL0,CTL1	I/O	69, 70	9mA	3.3	**PHY/Link Bi-directional Control** (ISO-barrier supported)
LREQ	O	73	9mA	3.3	**PHY/Link Request** (ISO-barrier supported)
LINKON	I	77	-	3.3	**Link-On Request** (ISO-barrier supported)
LPS	O	74	9mA	3.3	**Link Power Status** (ISO-barrier supported)
SCLK	I	72	-	3.3	**PHY Clock** 49.152 MHz (ISO-barrier supported)
DIRECT	I	68	-	3.3	**Auxiliary PHY/Link Signal** is used to determine whether the interconnection between Link and PHY has isolation ('low': ISO-barrier; 'high': no ISO-barrier).

1.4 Serial ROM Interface Signals: (3 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
GROM_SDA	I/O	55	6mA	3.3	**Serial EEPROM Data Input / Output**
GROM_SCL	O	56	6mA	3.3	**Serial EEPROM Clock Output**
GROM_EN	I	57	-	3.3	**Serial EEPROM Enable** ('high': GUID Load enabled; 'low': GUID Load disabled)

1.5 Miscellaneous Signal: (1 pin)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
PIN_EN	I	43	-	5/3.3	**Pin Enable Input** (High clamped)

1.6 IC: (3 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
IC(H)	I	44	-	3.3	**Internally Connected** (High clamped)
IC(L)	I	46, 47	-	3.3	**Internally Connected** (Low clamped)

1.7 NC: (5 pins)

Name	I/O	Pin No.	I_{OL}	Volts(V)	Function
NC	-	48, 49, 52, 53, 58	-	-	**Non- Connection** (Open) Leave them unconnected.

1.8 V_{DD}: (8 pins)

V_{DD} (5 V PCI or 3.3 V PCI) for PCI I/Os: 11, 37, 92

V_{DD} 3 V for digital core & PHY/Link I/Os: 1, 25, 51, 75, 97

1.9 V_{SS}: (11 pins)

V_{SS} : 6, 19, 26, 31, 38, 50, 63, 71, 76, 85, 100

2. REGISTER DESCRIPTIONS

2.1 PCI Bus Mode Configuration Register (CARD_ON=Low)

31 — 24	23 — 16	15 — 08	07 — 00	
DeviceID		VendorID		00H
Status		Command		04H
Class Code			Revision ID	08H
BIST	Header Type	Latency Timer	Cache Line Size	0CH
Base Address 0 (OHCI Registers)				10H
Base Address 1				14H
Base Address 2				18H
Base Address 3				1CH
Base Address 4				20H
Base Address 5				24H
CardBus CIS Pointer				28H
Subsystem ID		Subsystem Vendor ID		2CH
Expansion Rom Base Address Register				30H
000000H			Cap_Ptr	34H
00000000H				38H
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3CH
PCI_OHCI_Control				40H
00000000H				44H
00000000H				48H
00000000H				4CH
Diagnostic register0				50H
Diagnostic register1				54H
Diagnostic register2				58H
Diagnostic register3				5CH
Power Management Capabilities		Next_Item_Ptr	Cap_ID	60H
Data	PMCSR_BSE	Power Management Control/Status		64H
00000000H				68H
00000000H				6CH
User Area (GENERAL_RegisterA)				70H
User Area (GENERAL_RegisterB)				74H
User Area (GENERAL_RegisterC)				78H
User Area (GENERAL_RegisterD)				7CH
00000000H				80H FCH

2.1.1 Offset_00 VendorID Register

This register identifies the manufacturer of the μPD72862. The ID is assigned by the PCI_SIG committee.

Bits	R/W	Description
15-0	R	Constant value of 1033H.

2.1.2 Offset_02 DeviceID Register

This register identifies the type of the device for the μPD72862. The ID is assigned by NEC Corporation.

Bits	R/W	Description
15-0	R	Constant value of 0063H.

2.1.3 Offset_04 Command Register

The register provides control over the device's ability to generate and respond to PCI cycles.

Bits	R/W	Description
0	R	**I/O enable** Constant value of 0. The μPD72862 does not respond to PCI I/O accesses.
1	R/W	**Memory enable** Default value of 1. It defines if the μPD72862 responds to PCI memory accesses. This bit should be set to one upon power-up reset. 0: The μPD72862 does not respond to PCI memory cycles 1: The μPD72862 responds to PCI memory cycles
2	R/W	**Master enable** Default value of 1. It enables the μPD72862 as bus-master on the PCI-bus. 0: The μPD72862 cannot generate PCI accesses by being a bus-master 1: The μPD72862 is capable of acting as a bus-master
3	R	**Special cycle monitor enable** Constant value of 0. The special cycle monitor is always disabled.
4	R/W	**Memory write and invalidate enable** Default value of 0. It enables Memory Write and Invalid Command generation. 0: Memory write must be used 1: The μPD72862, when acts as PCI master, can generate the command
5	R	**VGA color palette invalidate enable** Constant value of 0. VGA color palette invalidate is always disabled.
6	R/W	**Parity error response** Default value of 0. It defines if the μPD72862 responds to $\overline{\text{PERR}}$. 0: Ignore parity error 1: Respond to parity error
7	R	**Stepping enable** Constant value of 0. Stepping is always disabled.
8	R/W	**System error enable** Default value of 0. It defines if the μPD72862 responds to $\overline{\text{SERR}}$. 0: Disable system error checking 1: Enable system error checking
9	R	**Fast back-to-back enable** Constant value of 0. Fast back-to-back transactions are only allowed to the same agent.
15-10	R	**Reserved** Constant value of 000000.

2.1.4 Offset_06 Status Register

This register tracks the status information of PCI-bus related events which are relevant to the μPD72862. "Read" and "Write" are handled somewhat differently.

Bits	R/W	Description
3-0	R	**Reserved** Constant value of 0000.
4	R	**New capabilities** Constant value of 1. It indicates the existence of the Capabilities List.
6,5	R	**Reserved** Constant value of 00.
7	R	**Fast back-to-back capable** Constant value of 1. It indicates that the μPD72862, as a target, cannot accept fast back-to-back transactions when the transactions are not to the same agent.
8	R/W	**Signaled parity error** Default value of 0. It indicates the occurrence of any "Data Parity". 0: No parity detected (default) 1: Parity detected
10,9	R	**DEVSEL timing** Constant value of 01. These bits define the decode timing for $\overline{\text{DEVSEL}}$. 0: Fast (1 cycles) 1: Medium (2 cycles) 2: Slow (3 cycles) 3: undefined
11	R/W	**Signaled target abort** Default value of 0. This bit is set by a target device whenever it terminates a transaction with "Target Abort". 0: The μPD72862 did not terminate a transaction with Target Abort 1: The μPD72862 has terminated a transaction with Target Abort
12	R/W	**Received target abort** Default value of 0. This bit is set by a master device whenever its transaction is terminated with a "Target Abort". 0: The μPD72862 has not received a Target Abort 1: The μPD72862 has received a Target Abort from a bus-master
13	R/W	**Received master abort** Default value of 0. This bit is set by a master device whenever its transaction is terminated with "Master Abort". The μPD72862 asserts "Master Abort" when a transaction response exceeds the time allocated in the latency timer field. 0: Transaction was not terminated with a Master Abort 1: Transaction has been terminated with a Master Abort
14	R/W	**Signaled system error** Default value of 0. It indicates that the assertion of $\overline{\text{SERR}}$ by the μPD72862. 0: System error was not signaled 1: System error was signaled
15	R/W	**Received parity error** Default value of 0. It indicates the occurrence of any $\overline{\text{PERR}}$. 0: No parity error was detected 1: Parity error was detected

2.1.5 Offset_08 Revision ID Register

This register specifies a revision number assigned by NEC Corporation for the μPD72862.

Bits	R/W	Description
7-0	R	Default value of 02H. It specifies the silicon revision. It will be incremented for subsequent silicon revisions.

2.1.6 Offset_09 Class Code Register

This register identifies the class code, sub-class code, and programming interface of the μPD72862.

Bits	R/W	Description
7-0	R	Constant value of 10H. It specifies an IEEE1394 OpenHCI-compliant Host Controller.
15-8	R	Constant value of 00H. It specifies an “IEEE1394” type.
23-16	R	Constant value of 0CH. It specifies a “Serial Bus Controller”.

2.1.7 Offset_0C Cache Line Size Register

This register specifies the system cache line size, which is PC-host system dependent, in units of 32-bit words. The following cache line sizes are supported: 2, 4, 8, 16, 32, 64, and 128. All other values will be recognized as 0, i.e. cache disabled.

Bits	R/W	Description
7-0	R/W	Default value of 00H.

2.1.8 Offset_0D Latency Timer Register

This register defines the maximum amount of time that the μPD72862 is permitted to retain ownership of the bus after it has acquired bus ownership and initiated a subsequent transaction.

Bits	R/W	Description
7-0	R/W	Default value of 00H. It specifies the number of PCI-bus clocks that the μPD72862 may hold the PCI bus as a bus-master.

2.1.9 Offset_0E Header Type Register

Bits	R/W	Description
7-0	R	Constant value of 00H. It specifies a single function device.

2.1.10 Offset_0F BIST Register

Bits	R/W	Description
7-0	R	Constant value of 00H. It specifies whether the device is capable of Built-in Self Test.

2.1.11 Offset_10 Base Address 0 Register

This register specifies the base memory address for accessing all the "Operation registers" (i.e. control, configuration, and status registers) of the μPD72862, while the BIOS is expected to set this value during power-up reset.

Bits	R/W	Description
11-0	R	Constant value of 000H. These bits are "read-only".
31-12	R/W	-

2.1.12 Offset_2C Subsystem Vendor ID Register

This register identifies the subsystem that contains the NEC's μPD72862 function. While the ID is assigned by the PCI_SIG committee, the value should be loaded into the register from the external serial EEPROM after power-up reset. Access to this register through PCI-bus is prohibited.

Bits	R/W	Description
15-0	R	Default value of 1033H.

2.1.13 Offset_2E Subsystem ID Register

This register identifies the type of the subsystem that contains the NEC's μPD72862 function. While the ID is assigned by the manufacturer, the value should be loaded into the register from the external serial EEPROM after power-up reset. Access to this register through PCI-bus is prohibited.

Bits	R/W	Description
15-0	R	Default value of 0063H.

2.1.14 Offset_30 Expansion Rom Base Address Register

This register is not supported by the current implementation of the μPD72862.

Bits	R/W	Description
31-0	R	**Reserved** Constant value of 0.

2.1.15 Offset_34 Cap_Ptr Register

This register points to a linked list of additional capabilities specific to the μPD72862, the NEC's implementation of the 1394 OpenHCI specification.

Bits	R/W	Description
7-0	R	Constant value of 60H. The value represents an offset into the μPD72862's PCI Configuration Space for the location of the first item in the New Capabilities Linked List.

2.1.16 Offset_3C Interrupt Line Register

This register provides the interrupt line routing information specific to the μPD72862, the NEC's implementation of the 1394 OpenHCI specification.

Bits	R/W	Description
7-0	R/W	Default value of 00H. It specifies which input of the host system interrupt controller the interrupt pin of the μPD72862 is connected to.

2.1.17 Offset_3D Interrupt Pin Register

This register provides the interrupt line routing information specific to the μPD72862, the NEC's implementation of the 1394 OpenHCI specification.

Bits	R/W	Description
7-0	R	Constant value of 01H. It specifies PCI $\overline{\text{INTA}}$ is used for interrupting the host system.

2.1.18 Offset_3E Min_Grant Register

This register specifies how long of a burst period the μPD72862 needs, assuming a clock rate of 33MHz. Resolution is in units of ¼ μs. The value should be loaded into the register from the external serial EEPROM upon power-up reset, and access to this register through PCI-bus is prohibited.

Bits	R/W	Description
7-0	R	Default value of 00H. Its value contributes to the desired setting for Latency Timer value.

2.1.19 Offset_3F Max Lat Register

This register specifies how often the μPD72862 needs to gain access to the PCI-bus, assuming a clock rate of 33MHz. Resolution is in units of ¼ μs. The value should be loaded into the register from the external serial EEPROM after hardware reset, and access to this register through PCI-bus is prohibited.

Bits	R/W	Description
7-0	R	Default value of 00H. Its value contributes to the desired setting for Latency Timer value.

2.1.20 Offset_40 PCI_OHCI_Control Register

This register specifies the control bits that are IEEE1394 OpenHCI specific. Vendor options are not allowed in this register. It is reserved for OpenHCI use only.

Bits	R/W	Description
0	R/W	**PCI global SWAP** Default value of 0. When this bit is 1, all quadrates read from and written to the PCI Interface are byte swapped, thus a "PCI Global Swap". PCI addresses for expansion ROM and PCI Configuration registers, are, however, unaffected by this bit. This bit is not required for motherboard implementations.
31-1	R	**Reserved** Constant value of all 0.

2.1.21 Offset_60 Cap_ID & Next_Item_Ptr Register

The Cap_ID signals that this item in the Linked List is the registers defined for PCI Power Management, while the Next_Item_Ptr describes the location of the next item in the μPD72862's Capability List.

Bits	R/W	Description
7-0	R	**Cap_ID** Constant value of 01H. The default value identified the Link List item as being the PCI Power Management registers, while the ID value is assigned by the PCI SIG.
15-8	R	**Next_Item_Ptr** Constant value of 00H. It indicated that there are no more items in the Link List.

2.1.22 Offset_62 Power Management Capabilities Register

This is a 16-bit read-only register that provides information on the power management capabilities of the μPD72862.

Bits	R/W	Description
2-0	R	**version** Constant value of 001. The power management registers are implemented as defined in revision 1.0 of PCI Bus Power Management Interface Specification.
3	R	**PME clock** Constant value of 0.
4	R	**Auxiliary power source** Constant value of 0. The alternative power source is not supported.
5	R	**DIS** Constant value of 0.
8,6	R	**Reserved** Constant value of 000.
9	R	**D1_support** Constant value of 0. The μPD72862 does not support the D1 Power Management state.
10	R	**D2_support** Constant value of 1. The μPD72862 supports the D2 Power Management state.
15-11	R	**PME_support** Constant value of 01100.

2.1.23 Offset_64 Power Management Control/Status Register

This is a 16-bit read-only register that provides control status information of the μPD72862.

Bits	R/W	Description
1,0	R/W	**PowerState** Default value is undefined. This field is used both to determine the current power state of the μPD72862 and to set the μPD72862 into a new power state. As D1 is not supported in the current implementation of the μPD72862, writing of '01' will be ignored. 00: D0 (DMA contexts: ON, Link Layer: ON) 01: Reserved (D1 state not supported) 10: D2 (DMA contexts: OFF, Link Layer: OFF, LPS: OFF, $\overline{\text{PME}}$ will be asserted upon LinkON being active) 11: D3 (DMA contexts: OFF, Link Layer: OFF, LPS: OFF, $\overline{\text{PME}}$ will be asserted upon LinkON being active, Power can be removed)
7-2	R	**Reserved** Constant value of 000000.
8	R/W	**PME_En** Default value of 0. This field is used to enable the specific power management features of the μPD72862.
12-9	R	**Data_Select** Constant value of 0000.
14,13	R	**Data_Scale** Constant value of 00.
15	R/W	**PME_Status** Default value is undefined. A write of '1' clears this bit, while a write of '0' is ignored.

2.2 CardBus Mode Configuration Register (CARD_ON=High)

31 – 24	23 – 16	15 – 08	07 – 00	
DeviceID		VendorID		00H
Status		Command		04H
Class Code			Revision ID	08H
BIST	Header Type	Latency Timer	Cache Line Size	0CH
Base Address 0 (OHCI Registers)				10H
Base Address 1 (CardBus Status Reg) Note				14H
Base Address 2 (CardBus Status Reg) Note				18H
Base Address 3				1CH
Base Address 4				20H
Base Address 5				24H
CardBus CIS Pointer Note				28H
Subsystem ID		Subsystem Vendor ID		2CH
Expansion Rom Base Address Register				30H
000000H			Cap_Ptr	34H
00000000H				38H
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3CH
PCI_OHCI_Control				40H
00000000H				44H
00000000H				48H
00000000H				4CH
Diagnostic register0				50H
Diagnostic register1				54H
Diagnostic register2				58H
Diagnostic register3				5CH
Power Management Capabilities		Next_Item_Ptr	Cap_ID	60H
Data	PMCSR_BSE	Power Management Control/Status		64H
00000000H				68H
00000000H				6CH
User Area (GENERAL_RegisterA)				70H
User Area (GENERAL_RegisterB)				74H
User Area (GENERAL_RegisterC)				78H
User Area (GENERAL_RegisterD)				7CH
CIS Area Note				80H – FCH

Note Different from PCI Bus Mode Configuration Register.

2.2.1 Offset_14/18 Base_Address_1/2 Register (CardBus Status Registers)

Bits	R/W	Description
7-0	R	Constant value of 00.
31-8	R/W	-

(1) Function Event Register (FER) (Base Address 1 (2)+ 0H)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup
14-5	R	Reserved. Read only as '0'
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

(2) Function Event Mask Register (FEMR) (Base Address 1 (2)+ 4H)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup Mask
5	R	BAM. Read only as '0'
6	R	PWM. Read only as '0'
13-7	R	Reserved. Read only as '0'
14	R/W	Wakeup Mask
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

(3) Function Reset Status Register (FRSR) (Base Address 1 (2)+ 8H)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup Mask
14-5	R	Reserved. Read only as '0'
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

(4) Function Force Event Register (FFER) (Base Address 1 (2)+ CH)

Bits	R/W	Description
0	R	Write Protect (No Use). Read only as '0'
1	R	Ready Status (No Use). Read only as '0'
2	R	Battery Voltage Detect 2 (No Use). Read only as '0'
3	R	Battery Voltage Detect 1 (No Use). Read only as '0'
4	R/W	General Wakeup Mask
14-5	-	No Use
15	R/W	Interrupt
31-16	R	Reserved. Read only as '0'

2.2.2 Offset_28 Cardbus CIS Pointer

This register specifies start memory address of the Cardbus CIS Area.

Bits	R/W	Description
31-0	R	Starting Pointer of CIS Area. Constant value of 00000080H.

2.2.3 Offset_80 CIS Area

The μPD72862 supports external Serial ROM(AT24C02 compatible) interface.

CIS Area Register can be loaded from external Serial ROM in the CIS area when CARD_ON are HIGH.

CARD_ON	$\overline{\text{CIS\_ON}}$	Bus	CIS	FUNCTION
0	1	PCI	OFF	$\overline{\text{PME}}$
0	0	PCI	ON	CSTSCHG
1	X	Cardbus	ON	CSTSCHG

3. SERIAL ROM INTERFACE

The μPD72862 provides a serial ROM interface to initialize the 1394 Global Unique ID Register and the PCI/Cardbus Mode Configuration registers from a serial EEPROM.

3.1 Serial EEPROM Register

Register Address	Register Name	R/W
Base address + 0x930	SUBID register	R/W
Base address + 0x934	LATVAL register	R/W
Base address + 0x938	W_GUIDHi register	R/W
Base address + 0x93C	W_GUIDLo register	R/W
Base address + 0x940	Parameters Write register	R/W
Base address + 0x95C	W_GENERAL register	R/W
Base address + 0x960	W_PHYS register	R/W
Base address + 0x984	W_CIS register	R/W

Remark Base address : Base Address 0 in Configuration register

3.2 Serial EEPROM Register Description

(1) SUBID register (Base address + 0x930)

31	16	15	0
W_SUBSYSID		W_SUBVNDID	

Field	Bits	R/W	Default value	Description
W_SUBSYSID	31-16	R/W	0063H	Subsystem ID value. The value is loaded into Subsystem ID register in Configuration register (offset+2CH bit 31-16).
W_SUBVNDID	15-0	R/W	1033H	Subsystem Vendor ID value. The value is loaded into Subsystem Vendor ID register in Configuration register (Offset+2CH bit 15-0).

(2) LATVAL register (Base address + 0x934)

31	24	23	16	15	12	11	10	4	3	0
W_MAXLAT		W_MINGNT		- 0 -		1	- 0 -		W_MAX_REC	

Field	Bits	R/W	Default value	Description
W_MAXLAT	31-24	R/W	00H	Max Latency value. The value is loaded into Max Latency register in Configuration register (Offset+3CH bit 31-24).
W_MINGNT	23-16	R/W	00H	Min Grant value. The value is loaded into Min Grant register in Configuration register (Offset+3CH bit 23-16).
-	15-12	-	-	Reserved. Write 0 to these bits.
	11	-	-	Reserved. Write 1 to this bit.
	10-4	-	-	Reserved. Write 0 to these bits.
W_MAX_REC	3-0	R/W	9H	MAX__REC value. The value is loaded into the max_rec field of OHCI BusOption register in OHCI register (Offset+020H bit 15-12).

(3) W_GUIDHi register (Base address + 0x938)

31	0
W_GUIDHi	

Field	Bits	R/W	Default value	Description
W_GUIDHi	31-0	R/W	Undefined	GlobalUniqueIDHi value. The value is loaded into OHCI GlobalUniqueIDHi register in OHCI register (Offset+024H bit 31-0). Please refer to the 1394 Open Host Controller Interface Specification/Release 1.0 [5.5.5].

(4) W_GUIDLo register (Base address + 0x93C)

31	0
W_GUIDLo	

Field	Bits	R/W	Default value	Description
W_GUIDLo	31-0	R/W	Undefined	GlobalUniqueIDLo value. The value is loaded into GlobalUniqueIDLo register in OHCI register (Offset+028H bit 31-0). Please refer to the 1394 Open Host Controller Interface Specification/Release 1.0 [5.5.5].

(5) Parameters Write register (Base address + 0x940)

31	7	6	4	3	1	0
- 0 -		PAGE_S		- 0 -		PAR_W

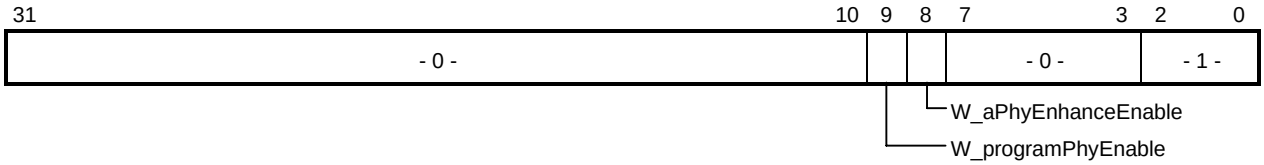
Field	Bits	R/W	Default value	Description
-	31-7	-	-	Reserved. Write 0 to these bits.
PAGE_S	6-4	R/W	000	Write register select page. The bit field returns zero when read. 000: Select SUBID register and LATVAL register. 001: Select W_GUIDHi register and W_GUIDLo register. 010: Select W_GENERAL register (W_GENERAL_0 and W_GENERAL_1). 011: Select W_GENERAL register (W_GENERAL_2 and W_GENERAL_3). 100: Select W_PHYS register (W_ programPhyEnable, W_aPhyEnhanceEnable). 101: Select W_CIS register (W_CIS_EVEN - W_CIS_ODD).
-	3-1	-	-	Reserved. Write 0 to these bits.
PAR_W	0	R/W	0	Write control signal. The bit field returns zeros when read. 1: Write the value of select page defined PAGE_S. One write transaction is the units of 8 byte. 0: Ignored.

(6) W_GENERAL register (Base address + 0x950 - 0x95C)

31	0
W_GENERAL_0 (Base address + 0x950) - W_GENERAL_3 (Base address + 0x95C)	

Field	Bits	R/W	Default value	Description
W_GENERAL_0 - W_GENERAL_3	31-0	R/W	Undefined	User define value. The value is loaded into GENERAL_registerA - D in Configuration register (Offset+70H - 7BH).

(7) W_PHYS register (Base address + 0x960)



Field	Bits	R/W	Default value	Description
-	31-10	-	-	Reserved. Write 0 to these bits.
W_programPhyEnable	9	R/W	1	programPhyEnable bit. The bit is loaded into HCControl registers in OHCI register ((Offset+50H bit 23) and (54H bit 23)). Please refer to the 1394 Open Host Controller Interface Specification/Release 1.0 [5.7]. 1: P1394a enhancement is supported. 0. P1394a enhancement is not supported.
W_aPhyEnhanceEnable	8	R/W	0	aPhyEnhanceEnable bit. The bit is loaded into HCControl registers in OHCI register ((Offset+50H bit 23) and (54H bit 23)).
-	7-3	-	-	Reserved. Write 0 to these bits.
	2-0	-	-	Reserved. Write 1 to these bits.

(8) W_CIS register (Base address + 0x980 - 0x984)

31	0
W_CIS_EVEN (Base address + 0x980) - W_CIS_ODD (Base address + 0x984)	

Field	Bits	R/W	Default value	Description
W_CIS_EVEN - W_CIS_ODD	31-0	R/W	Undefined	CIS Area value. The value is loaded into CIS Area in Configuration register (Offset+80H - FCH).

Table 3-1. Serial EEPROM Memory Map

Byte address	Bit 7	6	5	4	3	2	1	0
0	W_SUBSYSID(31 : 24)							
1	W_SUBSYSID(23 : 16)							
2	W_SUBVNDID(15 : 8)							
3	W_SUBVNDID(7 : 0)							
4	W_MAXLAT(31 : 24)							
5	W_MINGNT(23 : 16)							
6	0	0	0	0	1	0	0	0
7	0	0	0	0	W_MAX_REC(3 : 0)			
8	W_GUIDHi(31 : 24)							
9	W_GUIDHi(23 : 16)							
A	W_GUIDHi(15 : 8)							
B	W_GUIDHi(7 : 0)							
C	W_GUIDLo(31 : 24)							
D	W_GUIDLo(23 : 16)							
E	W_GUIDLo(15 : 8)							
F	W_GUIDLo(7 : 0)							
10	W_GENERAL_0(31 : 24)							
11	W_GENERAL_0(23 : 16)							
12	W_GENERAL_0(15 : 8)							
13	W_GENERAL_0(7 : 0)							
:	:							
:	:							
1C	W_GENERAL_3(31 : 24)							
1D	W_GENERAL_3(23 : 16)							
1E	W_GENERAL_3(15 : 8)							
1F	W_GENERAL_3(7 : 0)							
20	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	WPE	WPEE
23	0	0	0	0	0	1	1	1
:	:							
:	:							
28	W_CIS_0(31 : 24)							
29	W_CIS_0(23 : 16)							
2A	W_CIS_0(15 : 8)							
2B	W_CIS_0(7 : 0)							
:	:							
:	:							
A4	W_CIS_31(31 : 24)							
A5	W_CIS_31(23 : 16)							
A6	W_CIS_31(15 : 8)							
A7	W_CIS_31(7 : 0)							

WPE: W_programPhyEnable, WPEE: W_aPhyEnhanceEnable

3.3 Load Control

GROM_EN	CARD_ON	$\overline{\text{CIS\_ON}}$	Description
0	X	X	No loading.
1	0	1	W_SUBSYSID, W_SUBVNDID, W_MAXLAT, W_MINGNT, W_MAX_REC, W_GUIDHi/Lo, W_GENERAL_0 - W_GENERAL_3, W_programPhyEnable, W_aPhyEnhanceEnable are loaded.
1	0	0	All parameters (W_SUBSYSID, W_SUBVNDID, W_MAXLAT, W_MINGNT, W_MAX_REC, W_GUIDHi/Lo, W_GENERAL_0 - W_GENERAL_3, W_programPhyEnable, W_aPhyEnhanceEnable, W_CIS_EVEN - W_CIS_ODD) are loaded.
1	1	X	

3.4 Programming Sequence Example

The example of programming sequence to the serial EEPROM is shown below.

(1) Write SUBID register. **Note1**
(2) Write LATVAL register. **Note1**
(3) Write PAGE_S = 000 and PAR_W = 1 on Parameters Write register. **Note1**
(4) Wait over 13 ms for serial EEPROM access time. **Note1**
(5) Write W_GUIDHi register. **Note2**
(6) Write W_GUIDLo register. **Note2**
(7) Write PAGE_S = 001 and PAR_W = 1 on Parameters Write register. **Note2**
(8) Wait over 13 ms for serial EEPROM access time. **Note2**
(9) Write W_GENERAL register (W_GENERAL_0, W_GENERAL_1). **Note3**
(10) Write PAGE_S = 010 and PAR_W = 1 on Parameters Write register. **Note3**
(11) Wait over 13 ms for serial EEPROM access time. **Note3**
(12) Write W_GENERAL register (W_GENERAL_2, W_GENERAL_3). **Note4**
(13) Write PAGE_S = 011 and PAR_W = 1 on Parameters Write register. **Note4**
(14) Wait over 13 ms for serial EEPROM access time. **Note4**
(15) Write W_PHYS register (W_programPhyEnable, W_aPhyEnhanceEnable). **Note5**
(16) Write PAGE_S = 100 and PAR_W = 1 on Parameters Write register. **Note5**
(17) Wait over 13 ms for serial EEPROM access time. **Note5**
(18) Write W_CIS register (W_CIS_EVEN, W_CIS_ODD). **Note6**
(19) Write PAGE_S = 101 and PAR_W = 1 on Parameters Write register. **Note6**
(20) Wait over 13 ms for serial EEPROM access time. **Note6**
(21) Repeat (18)-(20) 15 times.
(22) Complete to write parameters into Serial EEPROM.
(23) Parameters are loaded from serial EEPROM after PCI reset.

Notes 1. If none of W_SUBSYSID, W_SUBVNDID, W_MAXLAT, W_MINGNT, W_MAX_REC in serial EEPROM are changed, (1)-(4) transactions don't need.
2. If none of W_GUIDHi, W_GUIDLo in serial EEPROM are changed, (5)-(8) transactions don't need.
3. If none of W_GENERAL_0, W_GENERAL_1 in serial EEPROM are changed, (9)-(11) transactions don't need.
4. If none of W_GENERAL_2, W_GENERAL_3 in serial EEPROM are changed, (12)-(14) transactions don't need.

Notes 5. If none of W_programPhyEnable, W_aPhyEnhanceEnable in serial EEPROM are changed, (15)-(17) transactions don't need.

6. If none of W_CIS_0 - W_CIS_31 in serial EEPROM are changed, (18)-(21) transactions don't need.

4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I	LVTTL @ (V_I < 0.5 V + V_{DD})	–0.5 to +4.6	V
		PCI @ (V_I < 3.0 V + V_{DD})	–0.5 to +6.6	V
Output voltage	V_O	LVTTL @ (V_O < 0.5 V + V_{DD})	–0.5 to +4.6	V
		PCI @ (V_O < 3.0 V + V_{DD})	–0.5 to +6.6	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Ranges

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Used to clamp reflection on PCI bus.	4.5 to 5.5	V
			3.0 to 3.6	V
Operating ambient temperature	T_A		0 to +70	°C

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, T_A= 0°C to +70°C)

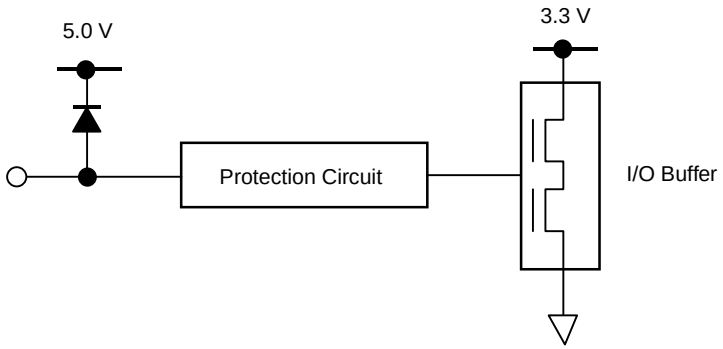
	Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
	High-level input voltage	V_{IH}			2.0		V_{DD}+0.5	V
	Low-level input voltage	V_{IL}			–0.5		+0.8	V
	High-level output current	I_{OH}	V_{OH} =2.4 V	Pin No.48,49,52,53,58	–3			mA
				Pin No.55,56	–6			mA
				Pin No.74	–9			mA
	Low-level output current	I_{OL}	V_{OL} =0.4 V	Pin No.48,49,52,53,58	3			mA
				Pin No.55,56	6			mA
				Pin No.74	9			mA
★	Input leakage current	I_L	V_{IN} = V_{DD} or GND				±10.0	μA
★	Supply current	I_{DD}	V_{DD} = 3.3 V D0 (Power State: 00) LPS = H			145		mA
	PCI interface							
	High-level input voltage	V_{IH}			2.0		5.5	V
	Low-level input voltage	V_{IL}			–0.5		+0.8	V
	High-level output current	I_{OH}	V_{OH} = 2.4 V		–2			mA
	Low-level output current	I_{OL}	V_{OL} = 0.4 V		9			mA
★	Input leakage current	I_L	V_{IN} = V_{DD} or GND				±10.0	μA
	PHY/Link interface							
	Positive trigger voltage	V_P			1.7		3.1	V
	Negative trigger voltage	V_N			0.2		1.6	V
	High-level output current	I_{OH}	V_{OH} = 2.4 V		–9			mA
	Low-level output current	I_{OL}	V_{OL} = 0.4 V		9			mA

Remarks 1. Digital core runs at 3.3 V.

2. PCI Interface can run at 5 or 3.3 V, depending on the choice of 5 V-PCI or 3.3 V-PCI.

3. All other I/Os are 3.3 V driving, and 5 V tolerant.

4. 5 V are used only for 5 V-PCI clamping diode.



AC Characteristics

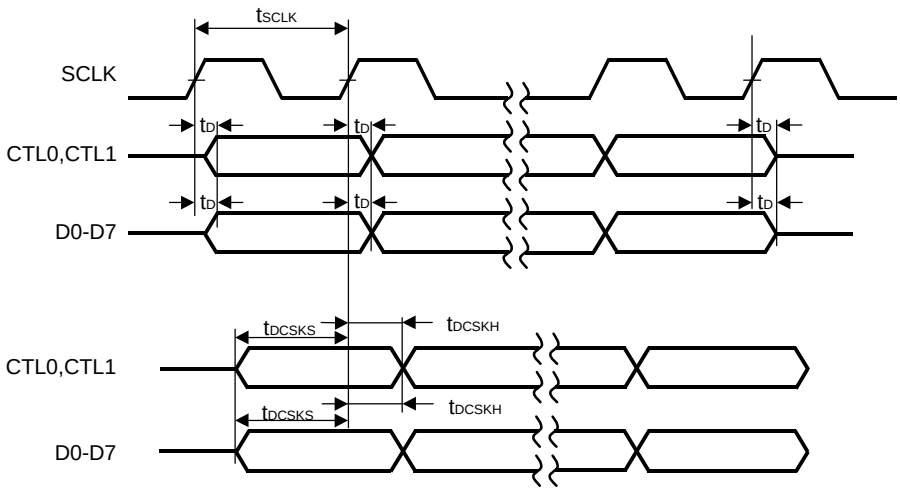
PCI Interface

See PCI local bus specification Revision 2.1.

PHY/Link Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D,CTL setup time to SCLK rise	t_{DCSKS}		6			ns
D,CTL hold time to SCLK rise	t_{DCSKH}		0			ns
SCLK rise to D,CTL,LREQ out	t_D	C_L = 10 pF	1		10	ns
SCLK cycle time	t_{SCLK}		20.345			ns

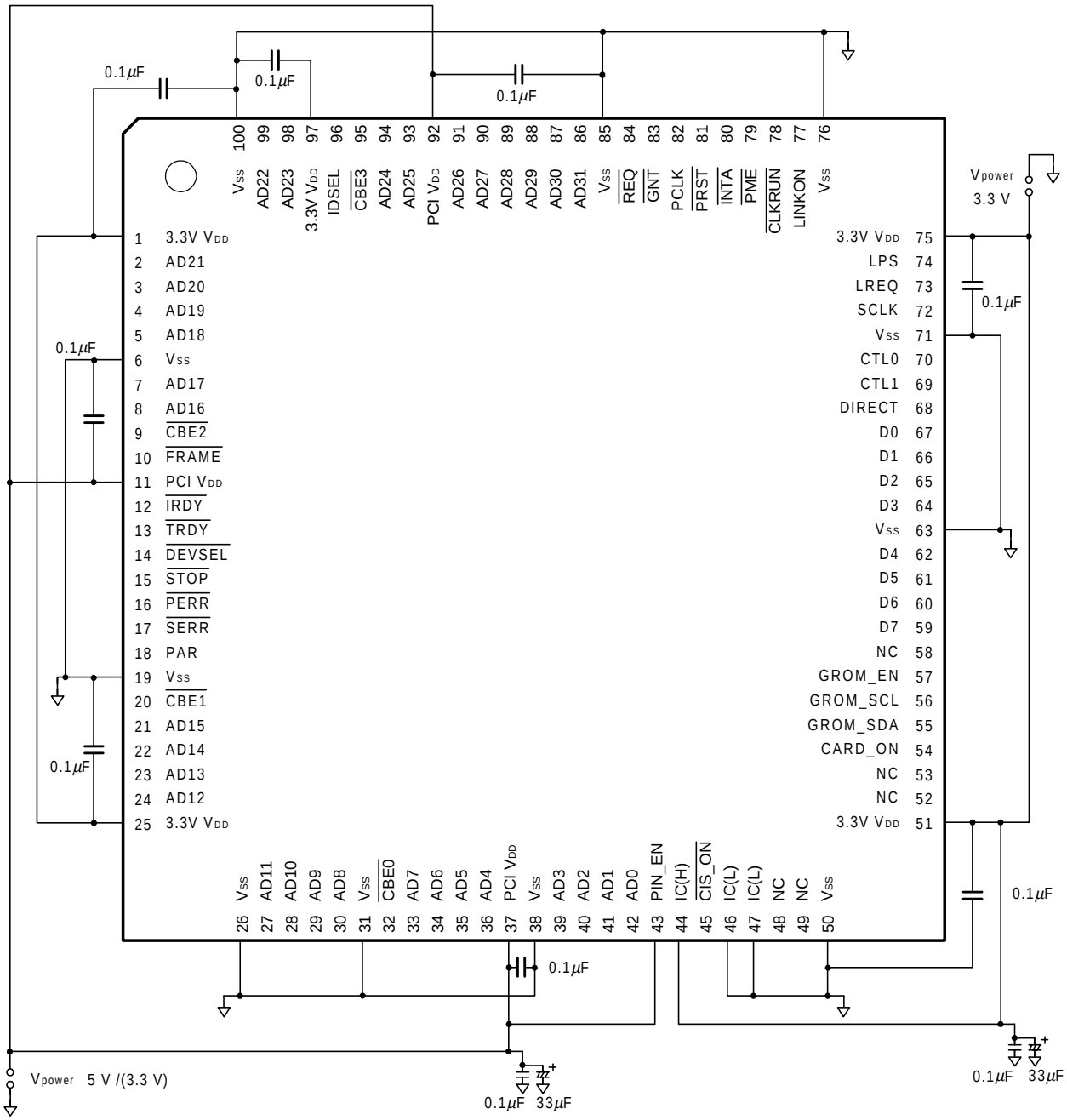
PHY/Link Interface Timing



Serial ROM Interface

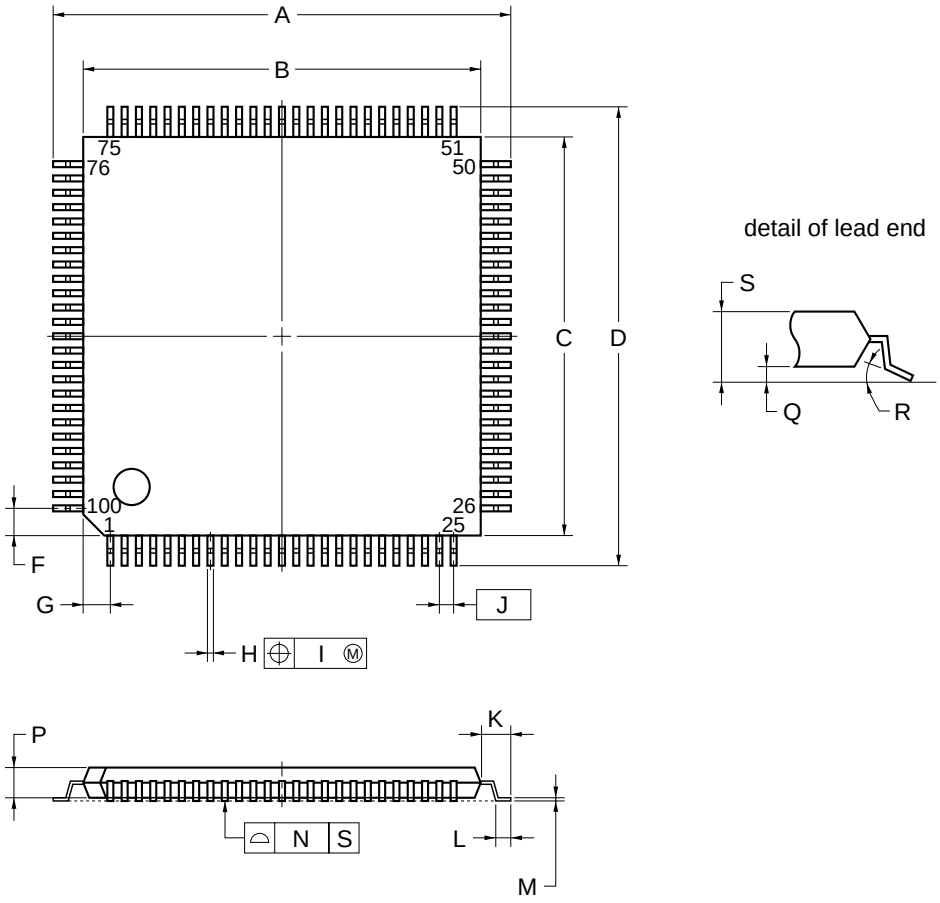
See AT24C01A/02/04/08/16 Spec. Sheet.

5. APPLICATION CIRCUIT EXAMPLE



6. PACKAGE DRAWING

100-PIN PLASTIC TQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.0
G	1.0
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

S100GC-50-9EU-2

★ 7. RECOMMENDED SOLDERING CONDITIONS

The μPD72850A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 7-1. Surface Mounting Type Soldering Conditions

μPD72862GC-9EU : 100-pin plastic TQFP (Fine pitch) (14 x 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher). Count: three times or less Exposure limit: 3 days[Note] (after that prebake at 125°C for 10 hours)	IR35-103-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher). Count: three times or less Exposure limit: 3 days[Note] (after that prebake at 125°C for 10 hours)	VP15-103-3
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M7 98.8