NEC

MOS INTEGRATED CIRCUIT

# μPD72850A

## IEEE1394 400Mbps PHY

The μPD72850A is the 3-port physical layer LSI which complies with the P1394a draft 2.0 specifications.
The μPD72850A works up to 400 Mbps. It is an upgrade of NEC's μPD72850.

### FEATURES

- The Three-port Physical Layer LSI complies to IEEE P1394a draft 2.0
- Connection debounce
- Arbitration enhancements
  - Arbitrated short bus reset
  - Ack-accelerated arbitration
  - Fly-by concatenation
  - Multiple-speed packet concatenation
  - Arbitration enhancements and cycle start (controlled by the Link layer)
- Performance optimization via PHY pinging
- Priority arbitration (controlled by the Link layer)
- Data rate: 393.216 / 196.608 / 98.304 Mbps
- Compliant with Suspend/Resume function as defined in P1394a draft 2.1
- 3.3 V single power supply
- Electrical isolated Link interface
- 24.576 MHz crystal clock generation, 393.216 MHz PLL multiplying frequency
- System power management by signaling of node power class information
- Cable power monitor (CPS) is equipped
- Fully interoperable with IEEE1394 std 1394 Link (FireWire™, i.LINK™)
- Cable bias and terminal voltage driver supply function (for 3-port each)
- Separate digital power and analog GND
- Enable/Disable port control switch when power supply is powered on
- Support Suspend/Resume Off mode (Compliant with P1394a draft 1.3)
- Number of supported port are selectable
  - 1port, 2port, 3port. This selection is only under Suspend/Resume Off mode
- Compliant with MD8405E (FUJIFILM MICRODEVICES CO., LTD)

### ORDERING INFORMATION

| Part number | Package |
|---|---|
| μPD72850AGK-9EU | 80-pin plastic TQFP (Fine pitch) (12 x 12 mm) |



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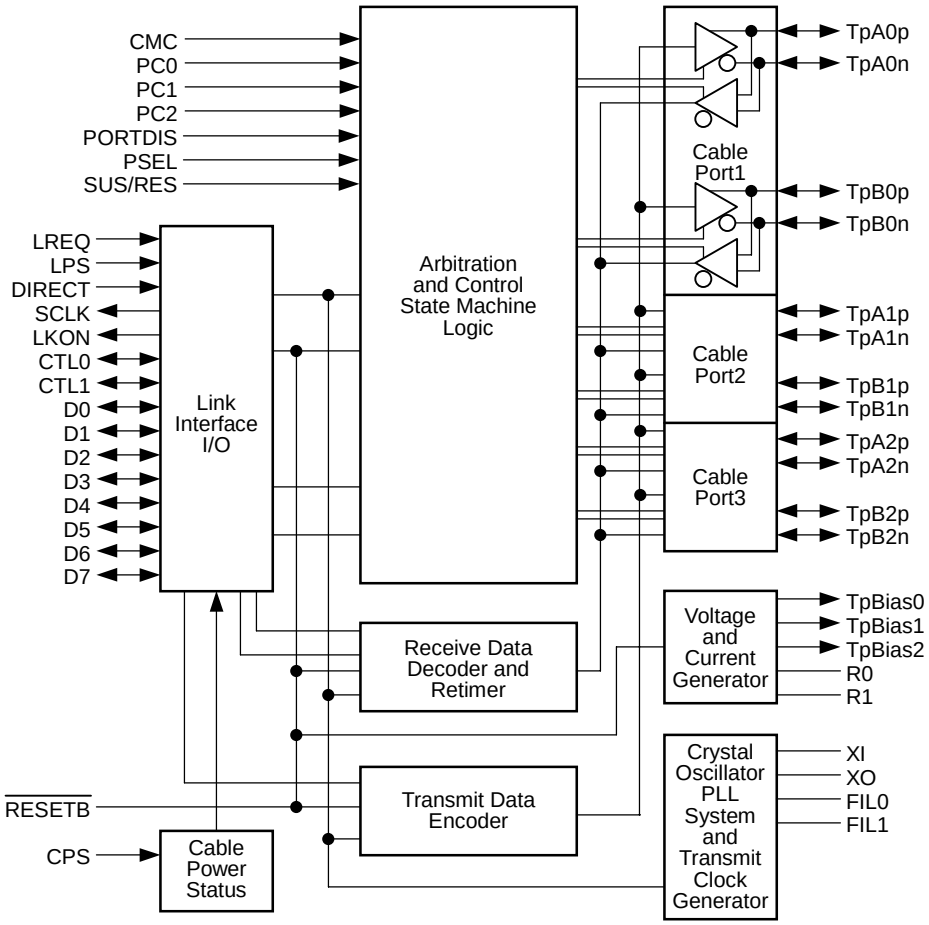
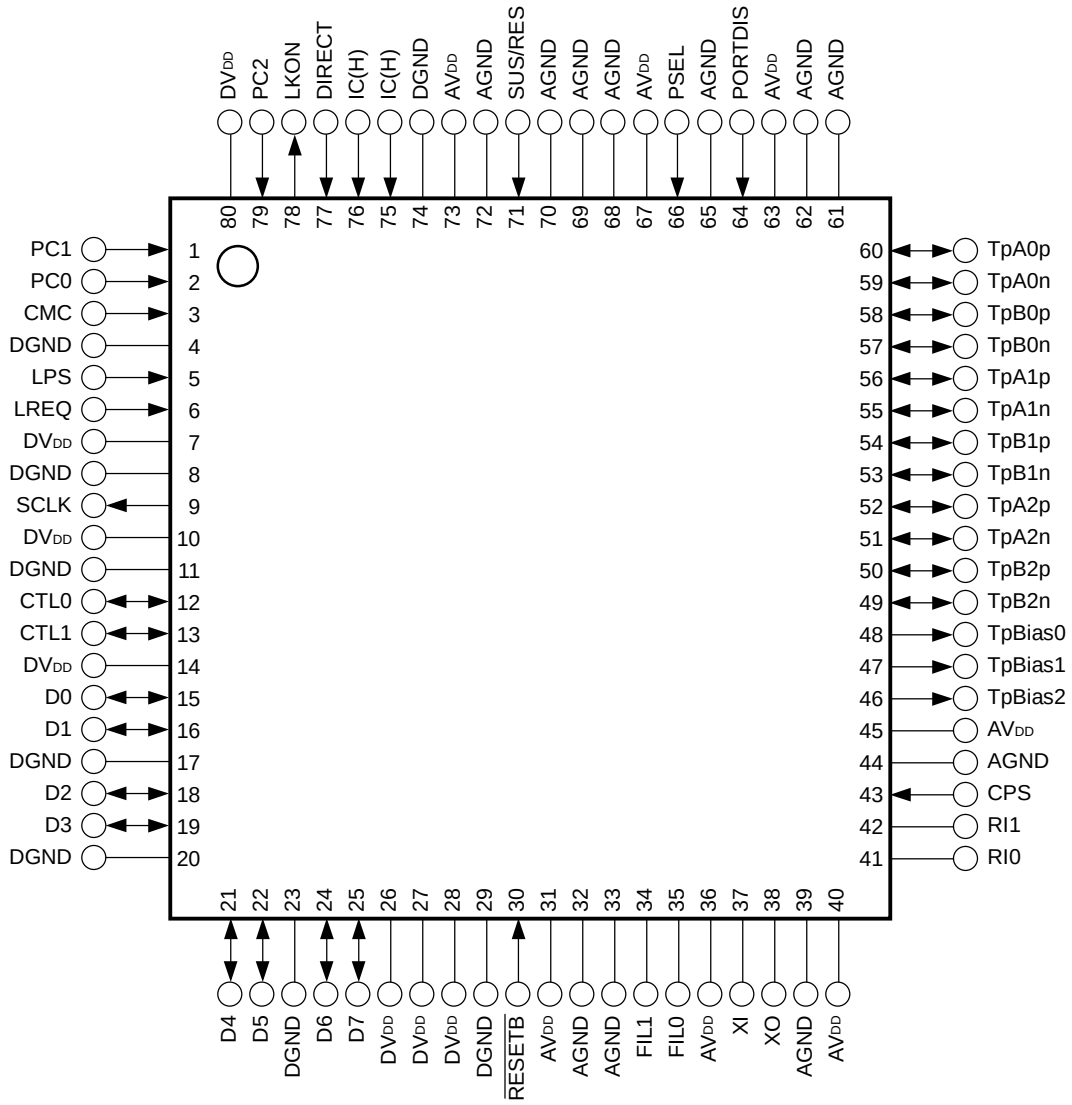
## BLOCK DIAGRAM



**PIN CONFIGURATION (Top View)**

- **80-pin plastic TQFP (Fine pitch) (12 x 12 mm)**



**PIN NAME**

| | |
|---|---|
| AGND | : Analog GND |
| $AV_{DD}$ | : Analog Power |
| CMC | : Configuration Manager Capable |
| CPS | : Cable Power Status |
| CTL0 | : Link Interface Control (bit 0) |
| CTL1 | : Link Interface Control (bit 1) |
| D0-D7 | : Data Input/Output |
| DGND | : Digital GND |
| Direct | : PHY/Link Isolation Barrier Control Input |
| $DV_{DD}$ | : Digital $V_{DD}$ |
| FIL0 | : APLL Filter Ground |
| FIL1 | : APLL Filter |
| IC(H) | : Internally Connected (High Clamped) |
| LKON | : Link-on Signal Output |
| LPS | : Link Power Status Input |
| LREQ | : Link Request Input |
| PC0-PC2 | : Power Class Set Input |
| PORTDIS | : Port Disable |
| PSEL | : Support Number of Port Select |
| $\overline{\text{RESETB}}$ | : Power on Reset Input |
| RI0 | : Reference Power Set, Connect Resistor 0 |
| RI1 | : Reference Power Set, Connect Resistor 1 |
| SCLK | : Link Control Output Clock |
| SUS/RES | : Suspend/Resume Function Select |
| TpA0n | : First Port Twisted Pair Cable A Negative Phase I/O |
| TpA0p | : First Port Twisted Pair Cable A Positive Phase I/O |
| TpA1n | : Second Port Twisted Pair Cable A Negative Phase I/O |
| TpA1p | : Second Port Twisted Pair Cable A Positive Phase I/O |
| TpA2n | : Third Port Twisted Pair Cable A Negative Phase I/O |
| TpA2p | : Third Port Twisted Pair Cable A Positive Phase I/O |
| TpB0n | : First Port Twisted Pair Cable B Negative Phase I/O |
| TpB0p | : First Port Twisted Pair Cable B Positive Phase I/O |
| TpB1n | : Second Port Twisted Pair Cable B Negative Phase I/O |
| TpB1p | : Second Port Twisted Pair Cable B Positive Phase I/O |
| TpB2n | : Third Port Twisted Pair Cable B Negative Phase I/O |
| TpB2p | : Third Port Twisted Pair Cable B Positive Phase I/O |
| TpBias0 | : First port Twisted Pair Output |
| TpBias1 | : Second Port Twisted Pair Output |
| TpBias2 | : Third Port Twisted Pair Output |
| XI | : Crystal Oscillator Connection XI |
| XO | : Crystal Oscillator Connection XO |

**CONTENTS**

# 1. PIN FUNCTIONS

## 1.1 Cable Interface Pins

| Name | Pin No. | I/O | Function |
|---|---|---|---|
| TpA0p | 60 | I/O | First port twisted pair cable A positive phase I/O |
| TpA0n | 59 | I/O | First port twisted pair cable A negative phase I/O |
| TpB0p | 58 | I/O | First port twisted pair cable B positive phase I/O |
| TpB0n | 57 | I/O | First port twisted pair cable B negative phase I/O |
| TpA1p | 56 | I/O | Second port twisted pair cable A positive phase I/O |
| TpA1n | 55 | I/O | Second port twisted pair cable A negative phase I/O |
| TpB1p | 54 | I/O | Second port twisted pair cable B positive phase I/O |
| TpB1n | 53 | I/O | Second port twisted pair cable B negative phase I/O |
| TpA2p | 52 | I/O | Third port twisted pair cable A positive phase I/O |
| TpA2n | 51 | I/O | Third port twisted pair cable A negative phase I/O |
| TpB2p | 50 | I/O | Third port twisted pair cable B positive phase I/O |
| TpB2n | 49 | I/O | Third port twisted pair cable B negative phase I/O |
| PORTDIS | 64 | I | Port disable.<br>SUS/RES(71pin)="1"<br>This selected state will be loaded to Disabled bit which allocated PHY register Port Status Page when power-on reset.<br>The PORTDIS pin is ignored except power-on reset.<br>1: All 3 ports will be disabled.<br>0: All 3 ports will be enabled.<br><br>SUS/RES(71pin)="0"<br>Combination with PSEL(66pin) input the supported number of port will be selected.<br>Please refer to PSEL. |
| PSEL | 66 | I | Supported number of Port select (This function will be activated only under SUS/RES="0").<br><br>1Port(Port0): 64pin 0, 66pin 1<br>2Port(Port0,1): 64pin 1, 66pin 0<br>3Port(Port0-2): 64pin 0, 66pin 0<br><br>When SUS/RES="1", this pin should be connected to AGND. |
| SUS/RES | 71 | I | Suspend/Resume function select<br>1: Suspend/Resume on (P1394a draft 2.1 compliant)<br>0: Suspend/Resume off (P1394a draft 1.3 compliant) |
| CPS | 43 | I | Power cable status.<br>Connect to the cable through a 390 kΩ resistor.<br>0: Cable power fail<br>1: Cable power on |

### 1.2 Link Interface Pins

| Name | Pin No. | I/O | Function |
|---|---|---|---|
| D0 | 15 | I/O | Data input/output (bit 0) |
| D1 | 16 | I/O | Data input/output (bit 1) |
| D2 | 18 | I/O | Data input/output (bit 2) |
| D3 | 19 | I/O | Data input/output (bit 3) |
| D4 | 21 | I/O | Data input/output (bit 4) |
| D5 | 22 | I/O | Data input/output (bit 5) |
| D6 | 24 | I/O | Data input/output (bit 6) |
| D7 | 25 | I/O | Data input/output (bit 7) |
| CTL0 | 12 | I/O | Link interface control (bit 0) |
| CTL1 | 13 | I/O | Llink interface control (bit 1) |
| LREQ | 6 | I | Link request input |
| SCLK | 9 | O | Link control output clock<br>LPS 1: 49.152 MHz output<br>LPS 0: Clamp to 0 (The clock signal will be output within 25 μsec after change to “0”) |
| LPS | 5 | I | Link power status input<br>0: Link power off<br>1: Link power on (PHY/Link direct connection)<br>Clock signal of about 300 kHz (if isolation) |
| LKON | 78 | O | Link-on signal output pin<br>Link-on signal is 6.144 MHz clock output.<br>Please refer to **4.2 Link-on Indication**. |
| Direct | 77 | I | PHY/Link isolation barrier control input<br>0: Isolation barrier<br>1: PHY/Link direct connection |

### 1.3 Control Pins

| Name | Pin No. | I/O | Function |
|---|---|---|---|
| PC0 | 2 | I | Power class set input<br>This pin status will be loaded to Pwr_class bit which allocated to PHY register 4H.<br>IEEE1394-1995 chapter [4.3.4.1] |
| PC1 | 1 | I | |
| PC2 | 79 | I | |
| CMC | 3 | I | Configuration manager capable setting.<br>This pin status will be loaded to Contender bit which allocated to PHY register 4H.<br>0: Non contender<br>1: Contender |
| $\overline{\text{RESETB}}$ | 30 | I | Power on reset input.<br>Connect to DGND through a 0.1 μF capacitor.<br>0: Reset<br>1: Normal |

### 1.4 IC

| Name | Pin No. | I/O | Function |
|---|---|---|---|
| IC | 75, 76 | I | Internally Connected (High Clamped) |

### 1.5 Power Supply Pins

| Name | Pin No. | I/O | Function |
|---|---|---|---|
| $AV_{DD}$ | 31, 36 | - | Analog power 1 (APLL, OSC) |
| | 40, 45 | - | Analog power 2 (Bias) |
| | 63, 67, 73 | - | Analog power 3 (Cable Interface) |
| AGND | 32, 33 | - | Analog GND1 (PLL, OSC) |
| | 39, 44 | - | Analog GND2 (Bias) |
| | 61 | - | Analog GND3 (Common) |
| | 62 | - | Analog GND4 (Speed signal) |
| | 65, 68-70, 72 | - | Analog GND5 (Port) |
| $DV_{DD}$ | 7, 10, 14, 26-28, 80 | - | Digital $V_{DD}$ |
| DGND | 4, 8, 11, 17, 20, 23, 29, 74 | - | Digital GND |

### 1.6 Other Pins

| Name | Pin No. | I/O | Function |
|---|---|---|---|
| TpBias0 | 48 | O | First port twisted pair output |
| TpBias1 | 47 | O | Second port twisted pair output |
| TpBias2 | 46 | O | Third port twisted pair output |
| RI0 | 41 | - | Resistor connection pin0 for reference current generator.<br>Please connect to RI1 pin via 9.1 kΩ resistor. |
| RI1 | 42 | - | Resistor connection pin1 for reference current generator.<br>Please connect to RI0 pin via 9.1 kΩ resistor. |
| FIL1 | 34 | - | APLL filter (No need to assemble) |
| FIL0 | 35 | - | APLL filter ground (No need to assemble) |
| XI | 37 | - | Crystal oscillator connection XI |
| XO | 38 | - | Crystal oscillator connection XO |

## 2. PHY REGISTERS

### 2.1 Complete Structure for PHY Registers

**Figure 2-1. Complete Structure of PHY Registers**

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 0000 | Physical_ID | | | | | | R | PS |
| 0001 | RHB | IBR | Gap_count | | | | | |
| 0010 | Extended (7) | | | Reserved | Total_ports | | | |
| 0011 | Max_speed | | | Reserved | Delay | | | |
| 0100 | Link_active | Contender | Jitter | | | Pwr_class | | |
| 0101 | Resume_int | ISBR | Loop | Pwr_fail | Timeout | Port_event | Enab_accel | Enab_multi |
| 0110 | Reserved | | | | | | | |
| 0111 | Page_select | | | Reserved | Port_select | | | |
| 1000 | Register0 (page_select) | | | | | | | |
| 1001 | Register1 (page_select) | | | | | | | |
| 1010 | Register2 (page_select) | | | | | | | |
| 1011 | Register3 (page_select) | | | | | | | |
| 1100 | Register4 (page_select) | | | | | | | |
| 1101 | Register5 (page_select) | | | | | | | |
| 1110 | Register6 (page_select) | | | | | | | |
| 1111 | Register7 (page_select) | | | | | | | |

**Table 2-1. Bit Field Description (1/2)**

| Field | Size | R/W | Reset value | Description |
|---|---|---|---|---|
| Physical_ID | 6 | R | 000000 | Physical_ID value selected from Self_ID period. |
| R | 1 | R | 0 | If this bit is 1, the node is root.<br>1: Root<br>0: Not root |
| PS | 1 | R | | Cable power status.<br>1: Cable power on<br>0: Cable power off |
| RHB | 1 | R/W | 0 | Root Hold -off bit. If 1, becomes root at the bus reset. |
| IBR | 1 | R/W | 0 | Initiate bus reset.<br>Setting to 1 begins a long bus reset.<br>Long bus reset signal duration: 166 μsec.<br>Returns to 0 at the beginning of bus reset. |
| Gap_count | 6 | R/W | 111111 | Gap count value.<br>It is updated by the changes of transmitting and receiving the PHY configuration packet Tx/Rx.<br>The value is maintained after first bus reset.<br>After the second bus reset it returns to reset value. |
| Extended | 3 | R | 111 | Shows the extended register map. |
| Total_ports | 4 | R | 0011 | Supported port number.<br>When SUS/RES(71pin)="1"<br>0011 : 3 ports<br><br>When SUS/RES(71pin)="0"<br>Combination with PSEL(66pin) input the supported number of port will be selected. Please refer to **1.1 Cable Interface Pins**.<br>0001 : 1 port<br>0010 : 2 port<br>0011 : 3 port |
| Max_speed | 3 | R | 010 | Indicate the maximum speed that this node supports.<br>010: 98.304, 196.608 and 393.216 Mbps |
| Delay | 4 | R | 0010 | Indicate worst case repeating delay time. 144+(2 x 20)=184 nsec |
| Link_active | 1 | R/W | 1 | Link active.<br>1 : Enable<br>0 : Disable<br>The logical AND status of this bit and LPS pin.<br>State will be referred to "L bit" of Self-ID Packet#0. |
| Contender | 1 | R/W | See Description | Contender.<br>"1" indicate this node support bus manager function. This bit will be referred to "C bit" of Self-ID Packet#0.<br>The reset data is depending on CMC pin setting.<br>CMC pin condition<br>1: Pull up (Contender)<br>0: Pull down (Non Contender) |
| Jitter | 3 | R | 010 | The difference of repeating time (Max.-Min.). (2+1) x 20=60 nsec |

**Table 2-1. Bit Field Description (2/2)**

| Field | Size | R/W | Reset value | Description |
|---|---|---|---|---|
| Pwr_class | 3 | R/W | See Description | Power class.<br>Please refer to IEEE1394 -1995 [4.3.4.1].<br>This bit will be referred to Pwr field of Self-ID Packet#0.<br>The reset data will be determined by PC0-PC2 Pin status. |
| Resume_int | 1 | R/W | 0 | Resume interrupt enable. When set to 1, if any one port does resume, the Port_event bit becomes 1. |
| ISBR | 1 | R/W | 0 | Initiate short (arbitrated) bus reset.<br>Setting to 1 acquires the bus and begins short bus reset.<br>Short bus reset signal output : 1.3 μsec<br>Returns to 0 at the beginning of the bus reset. |
| Loop | 1 | R/W | 0 | Loop detection output.<br>1: Detection<br>Writing 1 to this bit clears it to 0.<br>Writing 0 has no effect. |
| Pwr_fail | 1 | R/W | 0 | Power cable disconnect detect.<br>It becomes 1 when there is a change from 1 to 0 in the CPS bit.<br>Writing 1 to this bit clears it to 0.<br>Writing 0 has no effect. |
| Timeout | 1 | R/W | 0 | Arbitration state machine time-out.<br>Writing 1 to this bit clears it to 0.<br>Writing 0 has no effect. |
| Port_event | 1 | R/W | 0 | Set to 1 when the Int_Enable bit in the register map of each port is 1 and there is a change in the ports connected, Bias, Disabled and Fault bits.<br>Set to 1 when the Resume_int bit is 1 and any one port does resume.<br>Writing 1 to this bit clears it to 0.<br>Writing 0 has no effect. |
| Enab_accel | 1 | R/W | 0 | Enables arbitration acceleration.<br>Ack-acceleration and Fly-by arbitration are enabled.<br>1: Enabled<br>0: Disabled<br>If this bit changes while the bus request is pending, the operation is not guaranteed. |
| Enab_multi | 1 | R/W | 0 | Enable multi-speed packet concatenation.<br>Setting this bit to 1 follows multi-speed transmission.<br>When this bit is set to 0,the packet will be transmitted with the same speed as the first packet. |
| Page_select | 3 | R/W | 000 | Select page address between 1000 to 1111.<br>000: Port Status Page<br>001: Vendor Definition Page<br>Others: Unused |
| Port_select | 4 | R/W | 0000 | Port Selection.<br>Selecting 000 (Port Status Page) with the page selection selects the port.<br>0000: Port 0<br>0001: Port 1<br>0010: Port 2<br>Others: Unused |
| Reserved | - | R | 000… | Reserved. Read as 0. |

## 2.2 Port Status Page (Page 000)

**Figure 2-2. Port Status Page**

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 1000 | AStat | | BStat | | Child | Connected | Bias | Disabled |
| 1001 | Negotiated_speed | | | Int_enable | Fault | Reserved | | |
| 1010 | Reserved | | | | | | | |
| 1011 | Reserved | | | | | | | |
| 1100 | Reserved | | | | | | | |
| 1101 | Reserved | | | | | | | |
| 1110 | Reserved | | | | | | | |
| 1111 | Reserved | | | | | | | |

**Table 2-2. Bit Field Description**

| Field | Size | R/W | Reset value | Description |
|---|---|---|---|---|
| AStat | 2 | R | XX | A port status value.<br>00:---, 10: “0”<br>01: “1”, 11: “Z” |
| BStat | 2 | R | XX | B port status value.<br>00:---, 10: “0”<br>01: “1”, 11: “Z” |
| Child | 1 | R | | Child node status value.<br>1: Connected to child node<br>0: Connected to parent node |
| Connected | 1 | R | 0 | Connection status value.<br>1: Connected<br>0: Disconnected |
| Bias | 1 | R | | Bias voltage status value.<br>1: Bias voltage<br>0: No bias voltage |
| Disabled | 1 | R/W | See Description | The reset value is set by the PORTDIS pin.<br>1: Disable |
| Negotiated_ Speed | 3 | R | | Shows the maximum data transfer rate of the node connected to this port.<br>000: 100 Mbps<br>001: 200 Mbps<br>010: 400 Mbps |
| Int_enable | 1 | R/W | 0 | The Port_event is set to 1 by a change to 1 of the Connected, Bias, Disable, and Fault bits. |
| Fault | 1 | R/W | 0 | Set to 1 if an error occurs during Suspend/Resume.<br>Writing 1 to this bit clears it to 0.<br>Writing 0 has no effect. |
| Reserved | - | R | 000… | Reserved. Read as 0. |

## 2.3 Vendor ID Page (Page 001)

**Figure 2-3. Vendor ID Page**

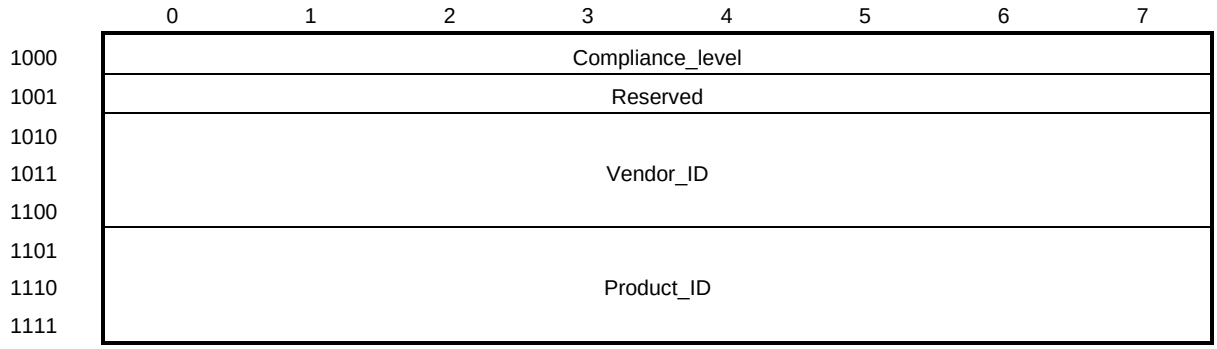



**Table 2-3. Bit Field Description**

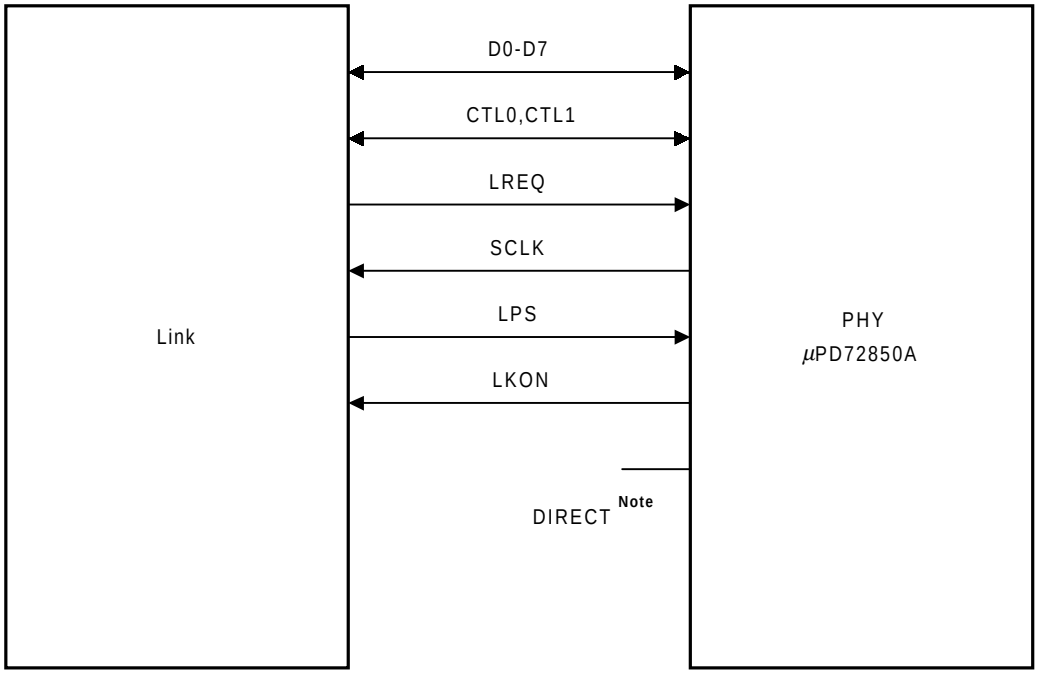
| Field | Size | R/W | Reset value | Description |
|---|---|---|---|---|
| Compliance_level | 8 | R | 00000001 | According to IEEE P1394a. |
| Vendor_ID | 24 | R | 00004CH | Company ID Code value, NEC IEEE OUI. |
| Product_ID | 24 | R | | Product code. |
| Reserved | - | R | 000… | Reserved. Read as 0. |

# 3. INTERNAL FUNCTION

## 3.1 Link Interface

### 3.1.1 Connection Method

**Figure 3-1. PHY/Link Connection Method**




**Note** Clamping to $V_{DD}$ provides direct connection to Link.
Clamping to GND connects through isolation barrier to Link.
The isolation barrier connection circuit is described in **3.1.7 Isolation Barrier.**

### 3.1.2 LPS (Link Power Status)

LPS is a function to monitor the On/Off status of the Link power supply. After 1.2 μsec or more, LPS is Low, the PHY/Link is reset and D and CTL are output Low (when the isolation barrier is Hi-Z). After 2.5 μsec or more, LPS is Low, moreover, the PHY stops the supply of SCLK and SCLK outputs Low (when the isolation barrier is Hi-Z).

### 3.1.3 LREQ, CTL0,CTL1, and D0-D7 Pins

LREQ : Indicates that a request is received from Link.

CTL0,CTL1 : Bi-directional pin which controls the functions between the PHY/Link interface.

D0-D7 : Bi-directional pin which controls the data Transfer/Receive status signal, and the speed code Transfer/Receive status signal.

### 3.1.4 SCLK

49.152 MHz clock supplied by PHY for the PHY/Link interface synchronization.

### 3.1.5 LKON

When the Link power is off, it outputs a clock of 6.144 MHz. LKON outputs under the following conditions: LPS is Low and the internal PHY register of the Link_active bit is 0.

- Link-on packet is received.
- Any bit of Loop, Pwr_fail, Timeout or Port_event is the PHY internal register becomes 1, and moreover either LPS or Link_active bit is 0.

When LPS is asserted, LKON returns to Low.

### 3.1.6 Direct

Set Direct to Low for using the isolation barrier.

### 3.1.7 Isolation Barrier

The IEEE1394 cable holds signals for Data/Strobe in addition to power and ground.

When the ground potential is different between connecting devices, the DC and AC current flows through the ground line in the cable and there is a possibility of malfunction due to ground difference between the two PHY.

The μPD72850A uses the isolation barrier to couple the AC between the PHY/Link interface to overcome the ground difference problem. Connecting the Direct pin to Low enables the digital differential circuit of the μPD72850A. The differential circuit propagates only the change in the signal; the interface will be driven only during transitions High → Low or Low → High. The interface will assume the high impedance state when there is no signal change. The μPD72850A uses Schmitt trigger input buffers for D, CTL, LREQ and LPS pins to prevent noise when the bus assumes a high impedance state.

The digital differential circuit and the Schmitt trigger input buffers are needed on the Link layer controller LSI to implement the isolation barrier.

**Figure 3-2. Waveforms of the Isolation Barrier**

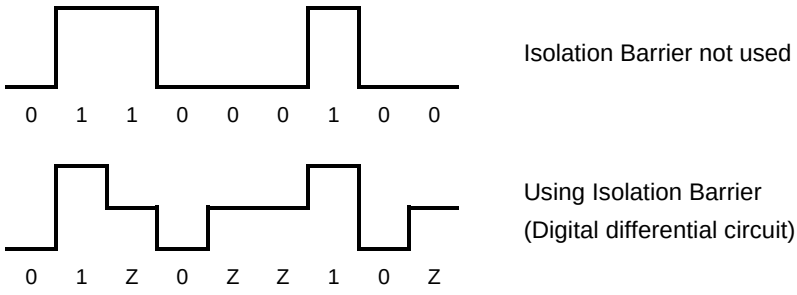
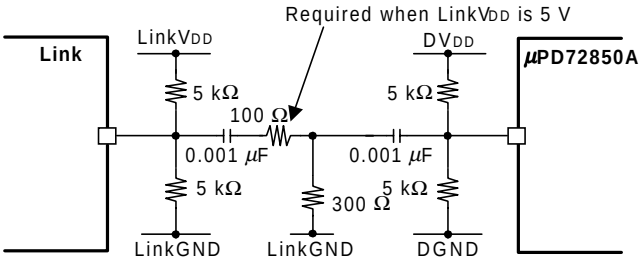
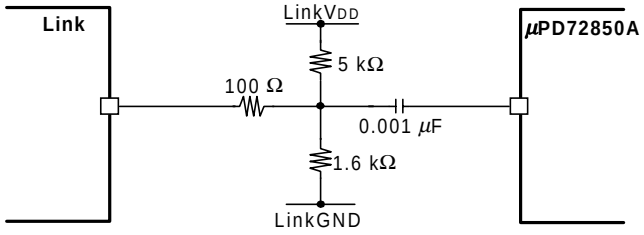


**Figure 3-3. Isolation Barrier Circuits**

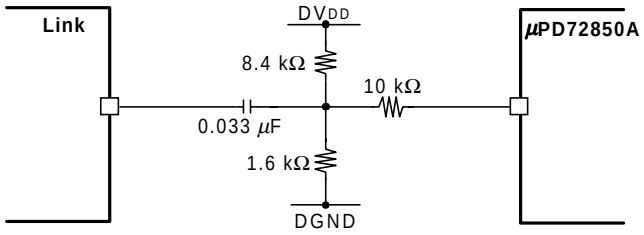
**(a) CTL0,CTL1, D0-Dn Isolation Barrier Circuit**



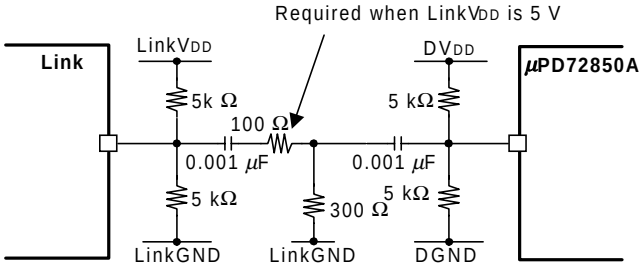

**(b) Link-on Isolation Barrier Circuit**




**(c) LPS Isolation Barrier Circuit**




**(d) LREQ Isolation Barrier Circuit**

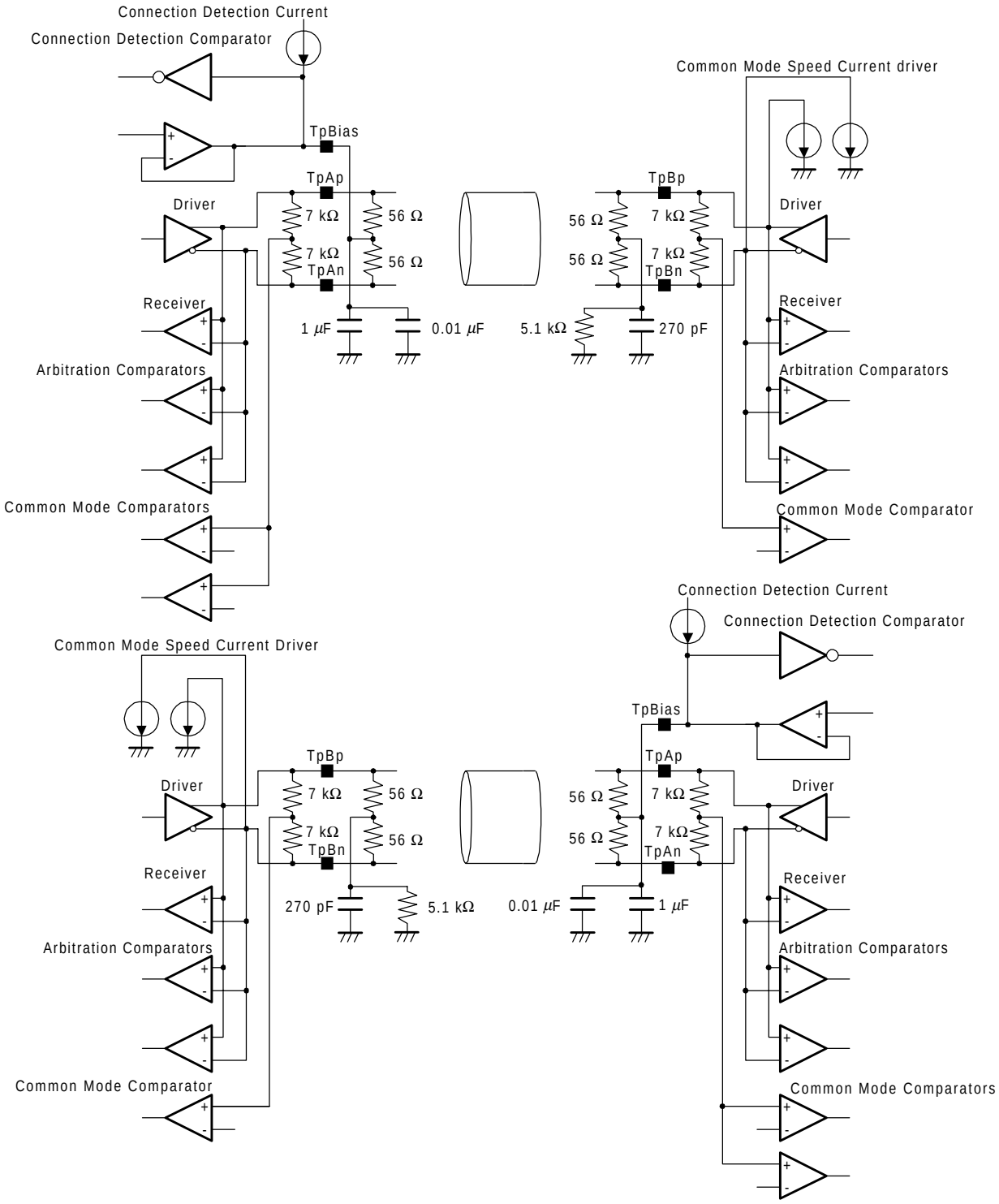



**(e) SCLK Isolation Barrier Circuit**

## 3.2 Cable Interface

### 3.2.1 Connections

**Figure 3-4. Cable Interface**



#### 3.2.2 Cable Interface Circuit

Each port is configured with two twisted-pairs of TpA and TpB.

TpA and TpB are used to monitor the state of the Transmit/Receive line, control signals, data and cables.

During transmission to the IEEE1394 bus, the Data/Strobe signal received from the Link layer controller is encoded, converted from parallel to serial and transmitted.

While receiving from the IEEE1394 bus, the Data/Strobe signal from TpA, TpB is converted from serial to parallel after synchronization by SCLK, then transmitted to the Link layer controller in 2/4/8 bits according to the data rate of 100/200/400 Mbps.

The bus arbitration for TpA and TpB and the state of the line are monitored by the built-in comparator. The state of the IEEE1394 bus is transmitted to the state machine in the LSI.

#### 3.2.3 Unused Ports

TpAp, TpAn : Not connected

TpBp, TpBn : AGND

TpBias : Connected to AGND using a 1.0 μF load capacitor

#### 3.2.4 CPS

An external resistance of 390 kΩ is connected in series to the power cable to monitor the power of the power cable. If the cable power falls under 7.5 V there is an indication to the Link layer controller that the power has failed.

### 3.3 Suspend/Resume

#### 3.3.1 Suspend/Resume On Mode (SUS/RES = “H”)

There are two ways of transition from the active status to the suspended status.

One is when the receipt of a remote command packet that sets the initiate suspend command. After that, the PHY transmits a remote confirmation packet with the ok bit set, subsequently signals TX_SUSPEND to the connected peer PHY with the port which specified by the port field in the remote command packet, and then the PHY port transitions to the suspended state.

The other is when the receipt of a RX_SUSPEND or RX_DISABLE_NOTIFY signal. When the port observes RX_SUSPEND, it transmits TX_SUSPEND to the active ports.

The TX_SUSPEND transmitted propagates until it reaches a leaf node. The PHY port transitions to the suspended state. The propagation of the suspended domain may be blocked by a PHY compliant with IEEE Std 1394-1995, a disabled or a suspended port.

Any one of a number of reasons may cause a suspended port to attempt to resume normal operations:

- Bias is detected and there is no fault condition;
- A resume packet is received or transmitted by the PHY;
- A remote command packet that sets the resume port command is received; or
- Either port of a node without active ports detects bias.

#### 3.3.2 Suspend/Resume Off Mode (SUS/RES = “L”)

- Remote command packet is ignored.
- Resume packet is ignored.
- Disabled, Int_enable and resume_int bits in PHY register are ignored.
- Responses to Remote access packet.
- Detects the connection of the port in TpBias.

## 3.4 PLL and Crystal Oscillation Circuit

### 3.4.1 Crystal Oscillation Circuit

To supply the clock of 24.576 MHz ± 100 ppm, use an external capacitor of 10 pF and a crystal of 50 ppm.

### 3.4.2 PLL

The crystal oscillator multiplies the 24.576 MHz frequency by 16 (393.216 MHz).

## 3.5 PC0-PC2, CMC

CMC shows the bus manager function which corresponds to the c bit of the Self_ID packet and the Contender bit in the PHY register when the input is High.

The value of CMC can be changed with software through the Link layer; this pin sets the initial value during Power-on Reset. Use a pull-up or pull-down resistor of 10 kΩ, based on the device's specification.

The PC0-PC2 pin corresponds to the power field of the Self_ID packet and Pwr_class in the PHY register. Refer to Section 4.3.4.1 of the IEEE1394-1995 specification for information regarding the Pwr_class. The value of Pwr can be changed with software through the Link layer controller; this pin sets the initial value during Power-on Reset. Use a pull-up or pull-down resistor of 10 kΩ based on the application.

## 3.6 $\overline{\text{RESETB}}$

Connect an external capacitor of 0.1 μF between the pins $\overline{\text{RESETB}}$ and GND. If the voltage drops below 0 V, a reset pulse is generated. All of the circuits are initialized, including the contents of the PHY register.

## 3.7 RI1, RI0

Connect an external resistor of 9.1 kΩ to limit the LSI's current.

## 4. PHY/LINK INTERFACE

### 4.1 Initialization of Link Power Status (LPS) and PHY/Link Interface

The LPS pin monitors the On/Off status of the Link power state. This pin is used during the PHY/Link interface Enable/Disable (initialization).

**Reset**

When the LPS input pin is Low for TLPS_RESET:

- CTL0,CTL1 and D0-D7 output Low (When the isolation barrier is Hi-Z).
- SCLK continuously supplies the clock signal to the Link.

**Disable**

When the LPS input pin is Low for TLPS_DISABLE:

- CTL0,CTL1, D0-D7 continue to output Low as TLPS_RESET has already occurred (When the isolation barrier is Hi-Z).
- SCLK to Link stops and it outputs Low (When the isolation barrier is Hi-Z).

**Table 4-1. LPS Timing Parameters**

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| LPS = Low propagation delay (with isolation barrier) | $t_{LPSL}$ | 0.09 | 1.00 | μs |
| LPS = High propagation delay (with isolation barrier) | $t_{LPSH}$ | 0.09 | 1.00 | μs |
| Reset active | $t_{LPS\_RESET}$ | 1.2 | 2.75 | μs |
| Disable active | $t_{LPS\_DISABLE}$ | 25 | 30 | μs |
| Setup time when using isolation barrier | $t_{RESTORE}$ | 15 | 20 | μs |

**Figure 4-1. LPS Waveform when Connected to Isolation Barrier**

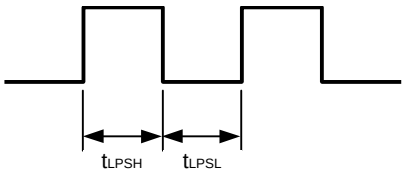
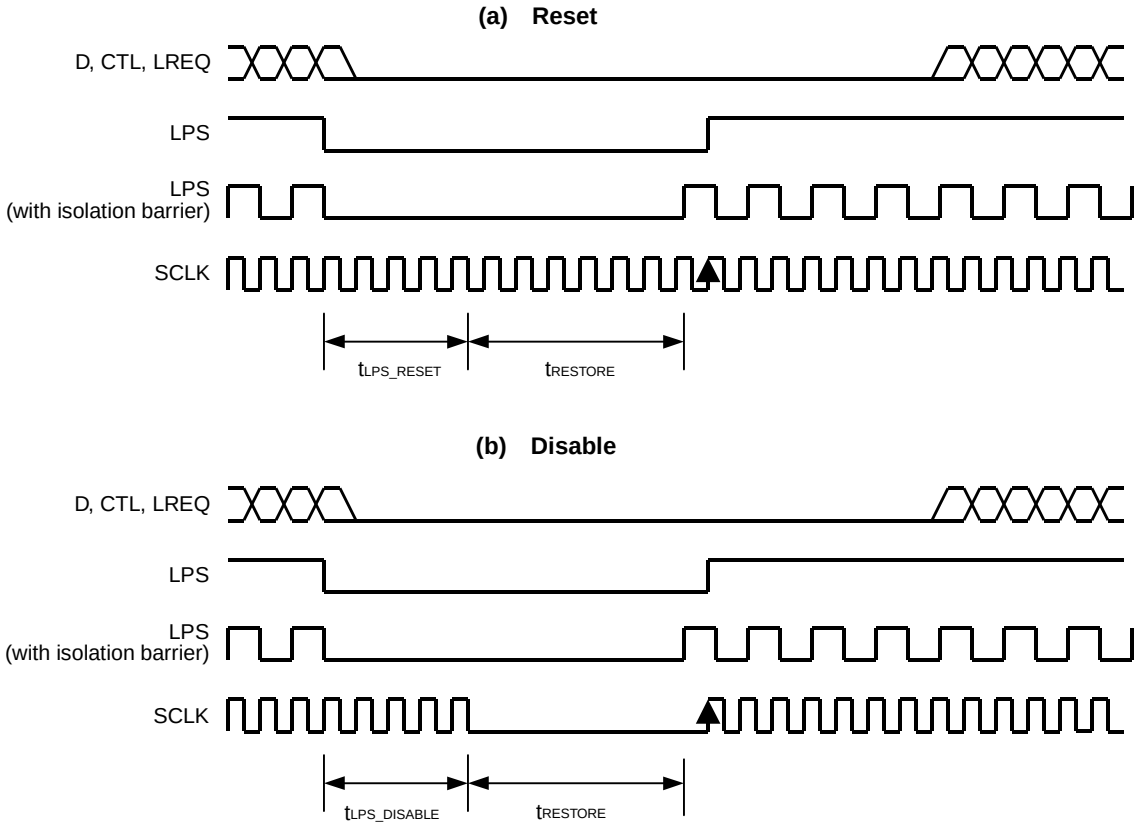


**Figure 4-2. PHY/Link Interface Reset and Disable**




## 4.2 Link-on Indication

When the power supply of Link is off (LPS is Low and the internal PHY register Link_active bit is 0), the pin LKON outputs High according to the following conditions: (With isolation barrier, it outputs a clock of 6.144 MHz)

- Link-on packet is received.
- When any bit of the μPD72850A PHY register's loop, Pwr fail, Timeout or Port_event becomes 1, and either LPS or the Link_active bit is 0.

**Table 4-2. Link-on Timing**

| Parameter | MIN. | MAX. | Unit |
|---|---|---|---|
| Frequency | 4 | 8 | MHz |
| Duty Cycle | 40 | 60 | % |
| Propagation delay before the Link becomes active (LPS is asserted and the Link_active bit in the PHY register is 1). | | 500 | ns |

- If LPS or the Link_active bit is 0, the Link is considered inactive.
  When the Link is inactive and any of Loop, PWR_fail, Timeout, Port_event becomes 1, then Link-on is asserted High.
- When the Link is active (both LPS and Link_active become 1) and Loop, Pwr_fail, Timeout and Port_event become 1, Status transfer is sent on the PHY/Link interface.

• The μPD72850A activates the PHY/Link interface when LPS is 1, regardless of the value of the Link active bit.

## 4.3 PHY/Link Interface Operation (CTL0, CTL1, LREQ, D0-D7)

The PHY/Link Interface consists of the following operations:

• Status transfer to the Link layer controller by CTL
• Transmit packet
• Receive packet
• Request from the Link layer controller by LREQ

### 4.3.1 CTL0,CTL1

CTL0,CTL1 controls the PHY/Link interface as shown in the Table 4-3.

**Table 4-3. CTL Controls PHY**

| CTL0,CTL1 | Type | Content |
|---|---|---|
| 00 | Idle | PHY is in idle function |
| 01 | Status | PHY transmitting status information to Link |
| 10 | Receive | PHY receiving data from the Link |
| 11 | Grant | PHY allows Link to transmit data |

This is the operation by which, after Grant, the Link obtains the right to control the interface.

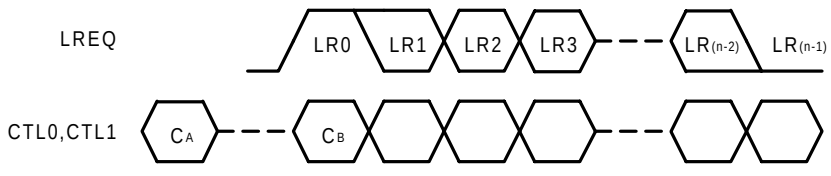
**Table 4-4. CTL Controls Link**

| CTL0,CTL1 | Type | Content |
|---|---|---|
| 00 | Idle | Link completes the packet transmission and releases the PHY/Link interface. |
| 01 | Hold | 1) Link transmits Hold until the data is ready for transmission.<br>2) Link transmits the interface connect packet. |
| 10 | Transmit | Link transmits the data to PHY. |
| 11 | - | Not used. |

### 4.3.2 LREQ

Access to the PHY register and the bus is controlled from the Link layer controller through the LREQ pin of PHY.

**Figure 4-3. LREQ and CTL Timing**




$C_A$ : CTL before generation of LREQ
$C_B$ : CTL during LREQ execution

### (1) LREQ format

• **Bus Request**

**Table 4-5. Bus Request Format**

| Bit | Type | Content |
|---|---|---|
| 0 | start | Signal that starts a request : 1 |
| 1-3 | request | Bus request type:<br>000: ImmReq acknowledge packet transmit<br>001: IsoReq isochronous packet transmit<br>010: PriReq cycle start packet transmit<br>011: FairReq asynchronous packet transmit |
| 4-6 | speed | Transmit speed:<br>000: 100 Mbps<br>010: 200 Mbps<br>100: 400 Mbps<br>other: reserved |
| 7 | stop | End request signal : 0 (optional) |

• **PHY Register Read Request**

**Table 4-6. Read Request Register Format**

| Bit | Type | Content |
|---|---|---|
| 0 | start | Signal that starts a request : 1 |
| 1-3 | request | Read Request.<br>100 : ReadReq |
| 4-7 | access address | PHY register address. |
| 8 | stop | End request signal : 0 |

• **PHY Register Write Request**

**Table 4-7. Write Request Register Format**

| Bit | Type | Content |
|---|---|---|
| 0 | start | Signal that starts a request : 1 |
| 1-3 | request | Write Request.<br>101 : WriteReq |
| 4-7 | access address | PHY register address. |
| 8-15 | write data | Write data. |
| 16 | stop | End request signal : 0 |

• **Acceleration Controller**

**Table 4-8. Acceleration Controller Request Format**

| Bit | Type | Content |
|---|---|---|
| 0 | start | Signal that starts a request : 1 |
| 1-3 | request | 110 : Acc Ctrl accelerate controller |
| 4 | access address | 0: Accelerate disable<br>1: Accelerate enable |
| 5 | stop | End request signal : 0 |

**Table 4-9. Request Type List**

| Bit | Type | Content |
|---|---|---|
| 000 | ImmReq | Used to acknowledge packet transmit.<br>When Idle is detected, PHY immediately controls the bus. |
| 001 | IsoReq | Used to transmit isochronous packet.<br>PHY does arbitration after isochronous gap is detected and acquires the bus. |
| 010 | PriReq | Used for Cycle master request. |
| 011 | FairReq | Fair request. |
| 100 | RdReg | PHY register read request. |
| 101 | WrReg | PHY register write request. |
| 110 | AccCtrl | Disable/enable of arbitration acceleration. |
| 111 | - | Unused. |

For the Link to execute Priority request and Fair, start the request using LREQ when CTL0,CTL1 becomes idle, after one clock. When request is acknowledged, the μPD72850A outputs Grant to CTL0,CTL1.
The Link of cycle master uses PriReq to transmit the cycle start packet. IsoReq transmits the isochronous packet.
IsoReq becomes effective only as follows:

- The transmission of the cycle start packet is performed on the same isochronous period as Receive. (The period until the subaction gap is detected.)
- During isochronous packet Transmit or Receive.

The μPD72850A cancels IsoReq with the subaction gap detection or bus reset. To meet the timing, do not issue the IsoReq to PHY when CRC operation is performed.
The Link cancel method is described later.
After the packet is received, Link issues ImmReq as the acknowledge packet transmission. The purpose is to prevent another node from detecting subaction gap as ACK_RESPONSE_TIME. The μPD72850A acquires the bus after packet receive and returns Grant to CTL0,CTL1. When CRC fails, before Link detects Grant, assert 3 Idle cycles to CTL0,CTL1.
When the bus reset is generated, the unprocessed requests are canceled.
The μPD72850A updates the data of the Write request register and the contents of the Read register are changed. The contents of the register of the specified address are output to the Link as a status transfer in the Read request register, When the status transmission is interrupted by transmitting/receiving packets, the status transmission will re-start from the first bit after completing the transmit/receive of the packets.

The bus request (ImmReq, IsoReq, PriReg, FairReq) is completed (in case of ImmReq, IsoReq, when the subaction gap is detected) when the packet is transmitted or canceled by canceling the bus request.

**(2) LREQ rules**

The Link request and the status of the serial bus are asynchronous; the bus request can be canceled by the status of the serial bus.

The following rules apply to a request by LREQ:

- Link cannot issue a bus request (ImmReq, IsoReq, PriReq, FairReq) if Grant is given to an LREQ request or until the Link's request is canceled. The request can be canceled by the μPD72850A if it detects subaction gap at ImmReq, IsoReq.
- Do not issue a RdReg or WrReg request when the status transmission is not completed by the Read request register.
- All of the bus requests (ImmReq, IsoReq, PriReq, FairReq) are canceled by a bus reset.

In addition, there is a limitation in the request of LREQ according to the state of CTL as shown in Table 4-10.

**Table 4-10. Rules for Other Requests**

| Request | State of CTL in $C_A$ to which LREQ is allowed when PHY drives CTL | LREQ issues permission when Link drives CTL | Note |
|---|---|---|---|
| Fair, Priority | Idle, Status | wrong | Fair, Priority request cannot be issued until the unprocessed bus request is completed. |
| Immediate | Receive, Idle | wrong | Link issues the request after completing the decoding of Destination_ID, when the acknowledge packet is ready. After the packet is received, it is necessary to transmit the first bit of the request within four cycles. |
| Isochronous | any | correct | If the isochronous packet transmission is prepared for the isochronous period, it is issued.<br>Do not issue the request to transmit the isochronous packet appending to the currently transmitted isochronous packet (Using Hold). |
| Register Read<br>Register Write | any | correct | Do not issue this request if the unprocessed Read request has not been completed. |
| AccCtrl | any | correct | To set acceleration bit 0:<br>When the isochronous period starts, if the Enab_accel bit is one, Cycle slave should adjust accelerate bit to 0.<br><br>To set acceleration bit 1:<br>Do not set the cycle master.<br>It is issued when the isochronous period ends. |

**Table 4-11. PHY Operation Before LREQ Request to the CTL Function Changes**

| Request | State of CTL in C B after LREQ was issued | Operation of the PHY (μPD72850A) |
|---|---|---|
| Fair, Priority | Receive | • Hold the request if the acceleration of arbitration packet transmitted with enable is 8 bits (ACK).<br>Except for 8 bits, the requests are ignored.<br>• Ignore the request when the acceleration of arbitration is disabled. |
| | Grant | Arbitration Won. |
| | Idle, Status | Excluding when the bus reset is generated, Hold the requests. |
| Immediate | Grant | |
| | Receive | The packet is being transmitted to Link. Request Hold. |
| | Idle, Status | Excluding when the bus reset is generated, hold the request. |
| Isochronous | Transmit Idle (driven by Link) | Request Hold. |
| | Grant | Arbitration Won. |
| | Receive | Request Hold. |
| | Status | Request is ignored when sub-action gap is detected. |
| | Idle | |
| Register Read | Any (driven by Link) | |
| | Grant | Request Hold. |
| | Receive | Request Hold. |
| | Status | Hold the request until the corresponding register value is returned. |
| | Idle | |
| Register Write, Acceleration control | Any | Request is completed. |

### 4.3.3 PHY/Link Interface Timing

#### (1) SCLK timing

**Table 4-12. SCLK Timing**

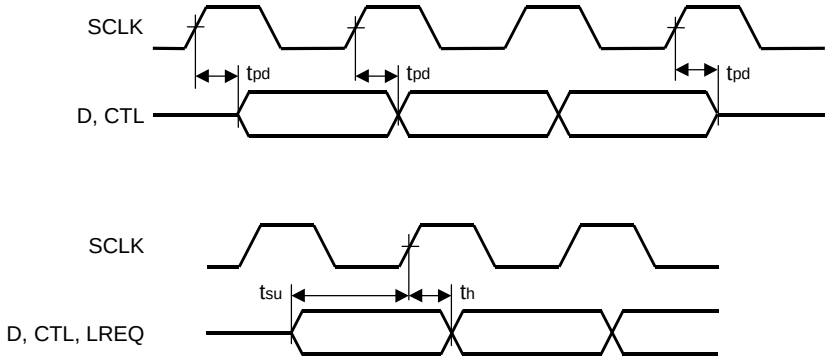
| Timing Constant | Comment | MIN. | MAX. | Unit |
|---|---|---|---|---|
| BUS_TO_LINK_DELAY | Period from receiving RX_DATA_PREFIX until Receive to CTL is output. | 2 | 9 | SCLK cycle |
| DATA_PREFIX_TO_GRANT | Period when the Grant is output to CTL after TX_DATA_PREFIX is output to a port. | | 25 | SCLK cycle |
| LINK_TO_BUS_DELAY | Period when TX_DATA_END is output to all ports after transmitting the packet by Link after idle was asserted to CTL. | 2 | 5 | SCLK cycle |
| MAX_HOLD | Maximum period when Hold can be asserted by Link to confirm Grant. | | 47 | SCLK cycle |

**(2) AC timing**

**Table 4-13. PHY/Link Interface Timing**

| Parameter | Symbol | MIN. | MAX. | Unit |
|---|---|---|---|---|
| D, CTL propagation delay | $t_{pd}$ | 0.5 | 13.5 | ns |
| D, CTL, LREQ setup time | $t_{su}$ | 6 | | ns |
| D, CTL, LREQ Hold time | $t_h$ | 0 | | ns |

**Figure 4-4. PHY/Link Interface AC Timing**




## 4.4 Acceleration Control

Enable of ack-acceleration and fly-by on the same isochronous period may create a problem. The isochronous cycle may extend unintentionally when transmitting the asynchronous packet by a node using ack-acceleration and fly-by.

To avoid this problem, Link should control Disable/Enable of these enhancements (ack-Acceleration, fly-by), by Acceleration Control requests. Cycle master cannot issue the Acceleration Control request.

The enhancements should not be used from the generation of the local cycle synchronization event to the confirmation of cycle start. In this period, all Links except for Cycle Master use Acceleration Control as follows:

- Do not issue Fair nor Priority request to Link after generating local cycle synchronization, if the Acceleration Control request's Accelerate bit is not set to 0.
- Link must not use Hold when transmitting continuous primary asynchronous packet after the Acknowledge packet, except after ack_pending to complete the split transaction.
- Ending the Link during the isochronous period issues the acceleration control request to set the Accelerate bit to 1, enabling these enhancements.

The μPD72850A does not require setting the Acceleration Control during isochronous transmit to enable the isochronous request fly-by acceleration.

It is not necessary to issue Acceleration Control request when the cycle master is absent from the serial bus. These enhancements are enabled if the Enab_accel bit in the PHY register is set. The μPD72850A supports Variable Acceleration controlled by the Acceleration Control during power-on reset.

### 4.5 Transmit Status

Pin D0,D1 of the μPD72850A transmits status information to the Link. Status is asserted to CTL while transmitting Status. The status transmission is interrupted if the serial bus receives a packet which contains states other than status to CTL. Between two status transmissions, assert Idle to CTL for at least one SCLK cycle.

The μPD72850A transmits status in 16 bits as follows:

- In response to the register request
- After deciding the new Physical_ID for the Self_ID period resetting the bus (after a Self_ID packet is transmitted)

The event indication is the only 4-bit transmission of the μPD72850A.

**Figure 4-5. Status Timing**

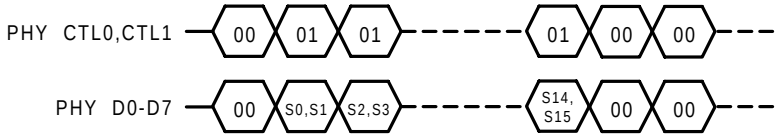



**Table 4-14. Status Data Format**

| Bit(s) | Name | Description |
|---|---|---|
| 0 | ARB_RESET_GAP | Arbitration Reset gap detect |
| 1 | SUBACTION_GAP | Subaction gap detect |
| 2 | BUS_RESET_START | Bus reset detect |
| 3 | Phy_interrupt | Either of the following states is detected:<br>• The topology of the bus is a loop<br>• Voltage drop on the power cable<br>• Arbitration state machine timeout<br>• Port Event |
| 4-7 | Address | PHY register address |
| 8-15 | Data | Register data |

The bits already transmitted are set to 0.

**Example** If the status transmission is interrupted after S0,S1 bit was transmitted, then in the next status transfer, S0,S1 becomes 0.

Therefore one of the following situations will occur when the μPD72850A re-transmits status after an interruption of the status transmission:

- At least one bit of S0-S3 is 1
- The PHY register data contains the interrupt status information

The status transmission always begins with S0,S1.

If the Link executes read request, and Subaction gap and arbitration reset gap are detected, priority is given to the transmission of gap status, postponing the response to the register read request.

### 4.6 Transmit

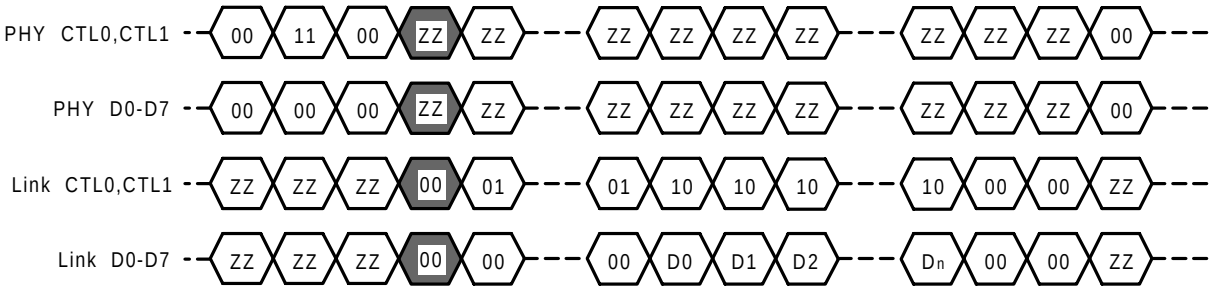
The μPD72850A arbitrates the serial bus using Link's LREQ.

- When the μPD72850A acquires the bus, a Grant period of 1 SCLK is executed to CTL0,CTL1. After that, an Idle period of 1 SCLK cycle is executed.
- Link controls the interface executing Idle, Hold of Transmit to CTL0,CTL1 after 1 SCLK cycle when Grant from PHY is detected.
- Before asserting Hold and Transmit, assert 1 Idle cycle. Do not execute Idle for 2 or more cycles.
- If the packet transmit is not ready, the Hold period can be extended up to MAX_HOLD.
- The μPD72850A outputs DATA_PREFIX to the serial bus while Hold is being asserted to CTL.
- When the packet transmit is ready, Link outputs the first bit of the packet and Transmit is asserted to CTL at the same time.
- After transmitting the last bit of the packet, Link outputs for Idle or Hold to CTL for 1 cycle. After that, it outputs Idle for 1 cycle.

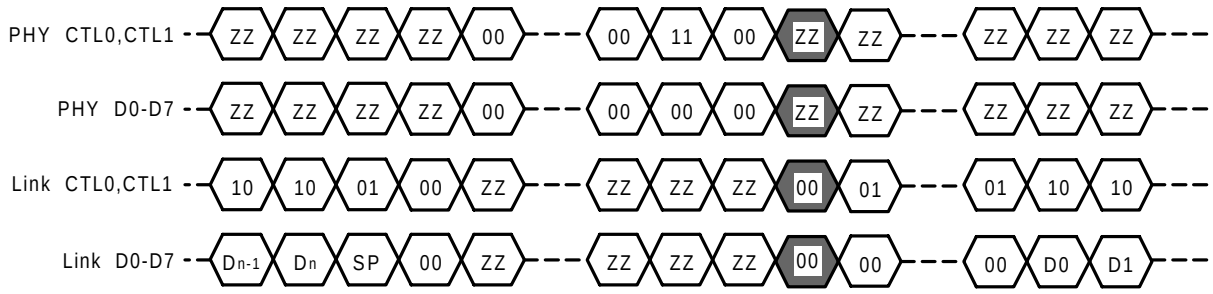
When PHY/Link releases the bus, output Low to CTL and D0-D7 within 1 cycle.

**Figure 4-6. Transmit Timing**

**(a) Single Packet**




**(b) Concatenated Packet**




**Note** In case of packet transmission after Grant, before actual transmission, Hold does not need to be asserted.

Link can transmit continuous packets without releasing the bus.

- Hold is asserted to CTL. This function is used when the Link transmits continuous packets after acknowledge and isochronous packets. Link outputs the transfer rate signal of the following packet to D0-D7 and asserts Hold simultaneously.
- After Hold is detected by MIN_PACKET_SEPARATION, the μPD72850A outputs Grant to CTL.

- Link controls the interface by generating Idle, Hold or Transmit to CTL0,CTL1, after 1 SCLK cycle when Grant from PHY is detected.
- Assert 1 Idle cycle before asserting Hold and Transmit (do not output 2 or more Idle cycles). When the packet transmission is not ready, assert Hold. The Hold output period after Grant is detected should not exceed the period provided by MAX_HOLD.

The following limitations exist though Link can transmit the concatenated packet with a different transfer rate. Link cannot transmit other than S100 connecting packets after S100 (concatenated) packets have been transmitted. A new request to transmit must be issued in order to transmit S100 packets at a transfer rate of S200 or more.

If the En_Multi bit in the PHY register is 0, the μPD72850A assumes the same speed as the first packet, for all of the concatenated packets.

At the end of packet transmission, Link asserts Idle to CTL for a period of 2 cycles.

After sampling Idle from Link, the μPD72850A asserts Idle to CTL for a period of 1 cycle.

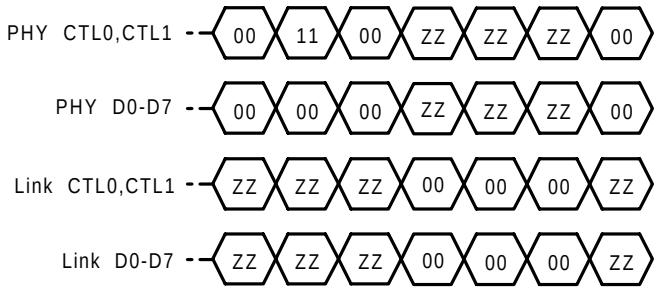
### 4.7 Cancel

This section describes how Link operates, when after the bus has been acquired by the request of LREQ, there is no data transmission. In this case, a Null packet with no data is transmitted to the serial bus (DATA_PREFIX → DATA_END).

Following are two method for canceling the Link:

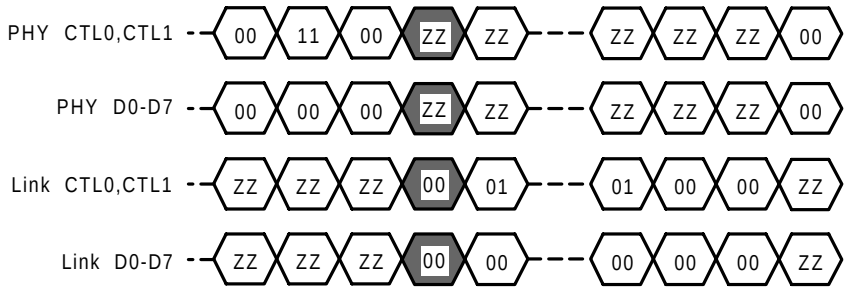
1. As explained in Section 4.6, the Link outputs Idle or Hold, then outputs Transmit to CTL after confirming Grant. Here, the Link asserts Idle for two cycles to CTL, then switches to high impedance.
   The μPD72850A confirms Cancel at the second Idle cycle. To prevent the bus from switching to high impedance, a third Idle cycle is needed.

**Figure 4-7. Link Cancel Timing (After Grant)**




2. To cancel after asserting Hold, assert Idle between two cycles; it switches to high impedance. This method cancels the packet transmission connection (concatenated) after Grant is received. The μPD72850A cancels with the next Idle cycle of Hold. To prevent CTL from switching to high impedance, assert a second Idle cycle.

**Figure 4-8. Link Cancel Timing (After Hold)**

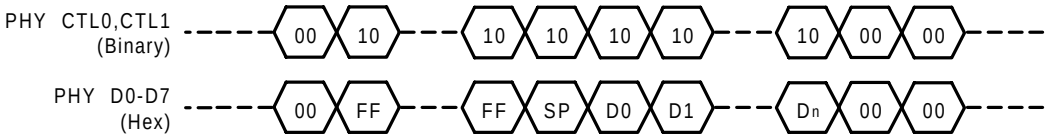



## 4.8 Receive

This section shows the operation when the packet is received from the serial bus.

- When the μPD72850A detects DATA_PREFIX on the serial bus, it asserts receive to CTL and all of the D pins assume the logic value of 1.
- The μPD72850A shows the speed code of the transfer rate ahead of the packet using bits D0-D7. Transmitting the speed code with the speed signal is the protocol of the PHY/Link interface. The speed code is not included in the CRC calculation.
- The μPD72850A continues to assert Receive to CTL until the packet is finally transmitted.
- Idle is asserted to CTL, indicating completion of the packet transmission.

**Figure 4-9. Receive Timing**




The packet transfer rate of the serial bus depends on the topology of the bus. The μPD72850A checks if the node can receive at the faster transfer rate. At this time, DATA_PREFIX → DATA_END is transmitted to the μPD72850A. After DATA_PREFIX is transmitted to the Link, Receive from the serial bus is completed, asserting Idle.

Table 4-15 shows the speed code encoding.

**Table 4-15. Speed Encoding**

| D0-D7 | | Data rate |
|---|---|---|
| Transmitted | Observed | |
| 00000000 | 00xxxxxx | S100 |
| 01000000 | 0100xxxx | S200 |
| 01010000 | 01010000 | S400 |
| 11111111 | 11xxxxxxxx | Data Prefix |

## 5. CABLE PHY PACKET

The node on the serial bus transmits and receives the PHY packet to control the bus.

The PHY packet is composed of 2 quadlets (64-bit); the second quadlet (32-bit) contains the inverse value of the first quadlet.

The PHY packet is transmitted at a transfer rate of S100. All of the PHY packets received from the serial bus are transmitted to the Link.

Though the PHY packet from the μPD72850A is transmitted to the Link, the PHY packet which was transmitted from the Link of the node is not transmitted to the Link.

There are four types of PHY packets, as follows:

- Self_ID packet
- Link-on packet
- PHY configuration packet
- Extended PHY packet

The Self_ID packet transmitted automatically by the μPD72850A is also transmitted to the Link of a local node.

The μPD72850A PHY packet Receive from the serial bus operates similar to the PHY packet transmitted by the Link (when the packet transmission to the Link is executed).

### 5.1 Self_ID Packet

During the Self_ID phase of the initialization or when the Ping packet responds, the μPD72850A transmits the Self_ID packet.

**Figure 5-1. Self_ID Packet Format**

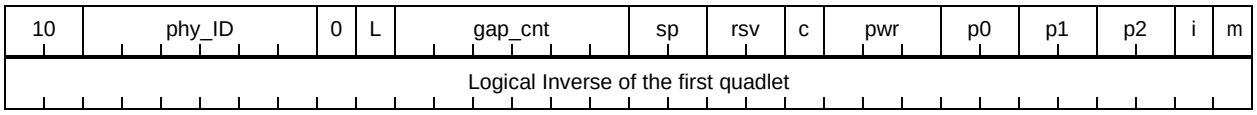



**Table 5-1. Self_ID Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the node. |
| L | Logical product of Link_active and LPS in the PHY register. |
| gap_cnt | Gap_count value in the PHY register. |
| sp | Physpeed 10 (corresponds to 98.304, 196.608, 393.216 Mbps). |
| c | C bit values in the PHY register. |
| pwr | pwr value in the PHY register.<br>000: The node does not need the power supply. No power repeat.<br>001: Obtains power supply for the node. Can supply 15W or more.<br>010: Obtains power supply for the node. Can supply 30W or more.<br>011: Obtains power supply for the node. Can supply 45W or more.<br>100: The node consumes 3W maximum power.<br>110: The node consumes 3W maximum power. At least 3W are necessary to enable Link.<br>111: The node consumes 3W maximum power. At least 7W are necessary to enable Link. |
| i | It shows that the node issued Bus Reset and the bus was reset. |
| m | Read as 0. |
| rsv | Read as 00. |

## 5.2 Link-on Packet

The μPD72850A outputs the Link-on signal of 6.144 MHz from the pin LKON when receiving the Link-on packet.

**Figure 5-2. Link-on Packet Format**

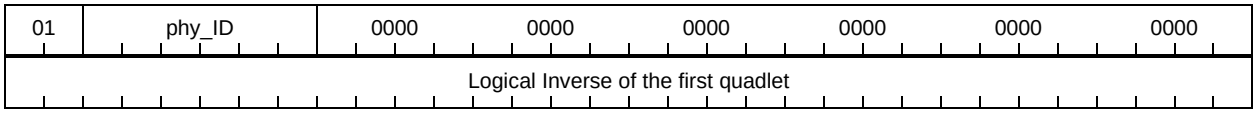



**Table 5-2. Link-on Packet**

| Field | Description |
|---|---|
| phy_ID | Physical_ID of the destination of the Link-on packet |

## 5.3 PHY Configuration Packet

Use the PHY configuration packet to set the gap count for the bus.

**Figure 5-3. PHY Configuration Packet Format**

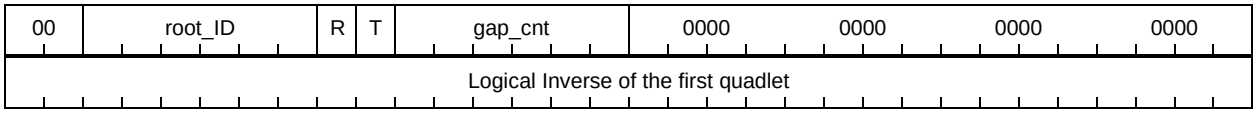



**Table 5-3. PHY Configuration Packet**

| Field | Description |
|---|---|
| root_ID | Sets the Physical_ID node as root contender (for the next reset). |
| R | When this bit is set to 1 and the Phyisical_ID of the node corresponds to the rootID of this packet, the μPD72850A sets the force_root bit. The force_root bit is cleared if there is discrepancy. |
| T | If this bit is 1, the gap_cnt value of this packet is used as the gap_count value. The gap_count value must not be cleared by the following bus reset, set the gap_count_reset_disable flag in the μPD72850A to TRUE. |
| gap_cnt | When this packet is received, the gap count is set to this value. While it remains effective for the next bus reset, it will be cleared by the second bus reset to 3FH. |

**Remark** Applying 0 to both R,T, regards the following packets as extended PHY packets, the PHY configuration is not recognized.

## 5.4 Extended PHY Packet

An extended PHY packet is defined when both the R (in the PHY configuration packet) and T bits are transmitted as 0. The extended PHY packet does not influence the force_root_bit and the gap_count bit on any node.

Following are the types of extended PHY packets:

- Ping packet
- Remote access packet
- Remote reply packet
- Remote command packet
- Remote confirmation packet
- Resume packet

### 5.4.1 Ping Packet

When the μPD72850A receives the Ping packet, it will transmit the Self_ID packet within the RESPONSE_TIME.

**Figure 5-4. Ping Packet Format**

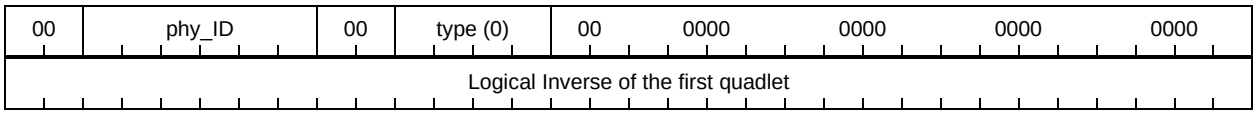



**Table 5-4. Ping Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the destination node of the Ping packet |
| type | Indicates that there is a Ping packet with a value of 0 |

### 5.4.2 Remote Access Packet

The Remote access packet reads information in the PHY register of another node. The PHY specified by the Remote access packet transmits the value in the register using the Remote Reply packet.

**Figure 5-5. Remote Access Packet Format**

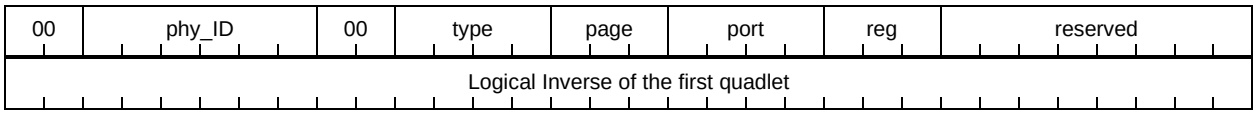



**Table 5-5. Remote Access Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the destination node of the Remote access packet |
| type | 1 = read register (base register), 5 = read register (page register) |
| page | Specifies the page of the PHY register |
| port | Specifies the register of each port in the PHY register |
| reg | Specifies the address when reading the base register.<br>In case of the Page and port registers, specifies the address with 1000+reg. |

### 5.4.3 Remote Reply Packet

The μPD72850A transmits the value in the register by using the Remote reply packet as a response to the Remote access packet.

**Figure 5-6. Remote Reply Packet Format**

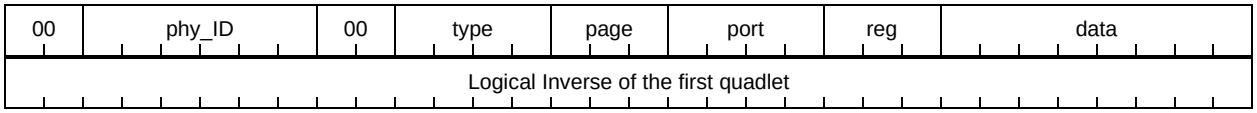



**Table 5-6. Remote Reply Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the node (Node's original packet transmit) |
| type | 3 = register read (base register), 7 = read register (page register) |
| page | Used when specifying the page of the PHY register |
| port | Used to specify the register of each port in the PHY register |
| reg | Specifies the address when reading the base register.<br>In case of the Page and port registers, specify the address with 1000+reg. |
| data | Contents of the specified register |

### 5.4.4 Remote Command Packet

Use the Remote command packet to operate the function of the port of the PHY of another node.

**Figure 5-7. Remote Command Packet Format**

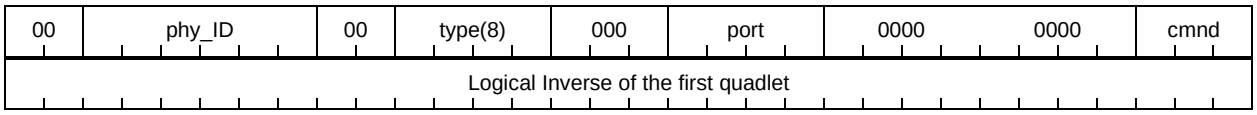



**Table 5-7. Remote Command Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the destination packet |
| type | Extended PHY packet type; set to 8 for Remote command packet |
| port | Port of the PHY of the operating node |
| cmnd | Command<br>0: NOP<br>1: Disables the port after transmission of the TX_DISABLE_NOTIFY<br>2: Suspend initiator<br>4: Clears to 0 the Fault bit of the port<br>5: Enables the port<br>6: Resumes the port |

### 5.4.5 Remote Confirmation Packet

The μPD72850A transmits the Remote confirmation when the Remote command packet is received, responding whether Cmnd can be executed.

**Figure 5-8. Remote Confirmation Packet Format**

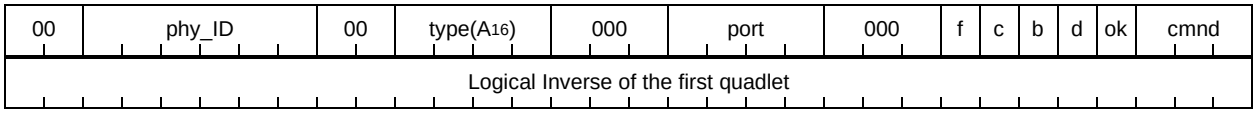



**Table 5-8. Remote Confirmation Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the node (node's original packet transmit) |
| type | Extended PHY packet type; set to $A_{16}$ for Remote confirmation packet |
| port | Port set from the Remote command packet |
| f | Fault bit value of the PHY register of this port |
| c | Connected bit value of the PHY register of this port |
| b | Bias bit value of the PHY register of this port |
| d | Disable bit value of the PHY register of this port |
| ok | 1 indicates executing; otherwise it is 0 |
| cmnd | Specifies the command value with the Remote command packet |

### 5.4.6 Resume Packet

When the μPD72850A receives the Resume packet, all of the ports that were suspended resume the connection. The Resume packet does the broadcast.

**Figure 5-9. Resume Packet Format**

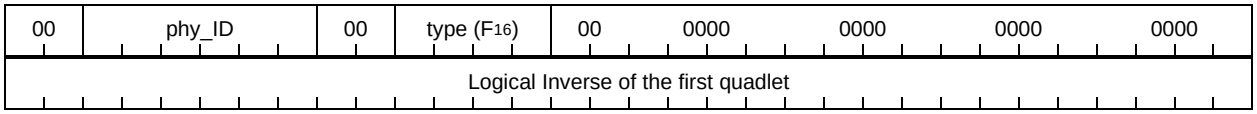



**Table 5-9. Resume Packet**

| Field | Description |
|---|---|
| phy_ID | Physical ID of the original packet transmit |
| type | Extended PHY packet type; set to $F_{16}$ for Resume packet |

## 6. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DDm}$ | | –0.5 to +4.6 | V |
| Input voltage | $V_{IN}$ | | –0.5 to $V_{DD}$+0.5 | V |
| Output voltage | $V_{OUT}$ | | –0.5 to $V_{DD}$+0.5 | V |
| Storage temperature | $T_{stg}$ | | –40 to +125 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

### Recommended Operating Ranges

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | 3.0 | 3.3 | 3.6 | V |
| Operating temperature | $T_A$ | | 0.0 | | 70.0 | °C |
| Power dissipation | $P_D$ | | | | 0.9 | W |

## DC Characteristics

### Common

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_{DD}$ | 3-port, S400, $V_{DD}$ = 3.6 V | | | 240 | mA |
| | | 1-port transmit or receive, S400, $V_{DD}$ = 3.3 V | | 135 | | mA |

### PHY/Link Interface

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| High-level output voltage (Undifferentiated) | $V_{OH}$ | $I_{OH}$ = –4 mA | 2.8 | | | V |
| High-level output voltage (Differentiated) | $V_{OHD}$ | $I_{OH}$ = –9 mA | $V_{DD}$–0.4 | | | V |
| Low-level output voltage (Undifferentiated) | $V_{OL}$ | $I_{OH}$ = 4 mA | | | 0.4 | V |
| Low-level output voltage (Differentiated) | $V_{OLD}$ | $I_{OH}$ = 9 mA | | | 0.4 | V |
| High-level input voltage (Undifferentiated) | $V_{IH}$ | | 2.6 | | $V_{DD}$+10% | V |
| Low-level input voltage (Undifferentiated) | $V_{IL}$ | | | | 0.7 | V |
| Input rising threshold voltage (LPS) | $V_{LIT+}$ | | | | $V_{LREF}$+1 | V |
| Input falling threshold voltage (LPS) | $V_{LIT-}$ | | $V_{LREF}$ +0.2 | | | V |
| Hysteresis input rising threshold voltage(Differentiated) | $V_{IT+}$ | | $V_{REF}$ +0.3 | | $V_{REF}$ +0.9 | V |
| Hysteresis input falling threshold voltage(Differentiated) | $V_{IT-}$ | | $V_{REF}$ –0.9 | | $V_{REF}$ –0.3 | V |
| Reference voltage | $V_{REF}$ | | $V_{DD}$/2±1% | | | V |
| Reference voltage (LPS) | $V_{LREF}$ | | 0.5 | | 1.6 | V |
| Input capacitance | $C_{IN}$ | | | | 7.5 | pF |

### Cable Interface

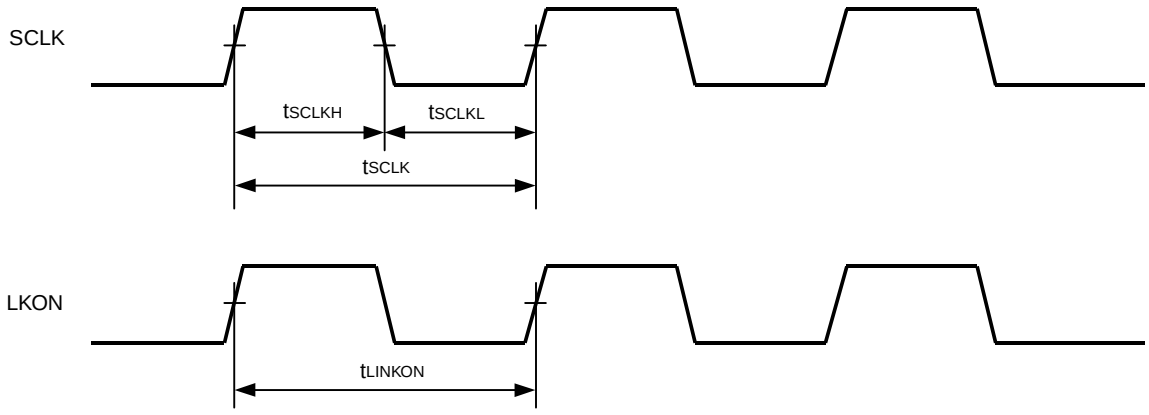
| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Differential input voltage | $V_{ID}$ | Cable input, 100 Mbps operation | 142 | | 260 | mV |
| | | Cable input, 200 Mbps operation | 132 | | 260 | mV |
| | | Cable input, 400 Mbps operation | 118 | | 260 | mV |
| TpB common mode input voltage | $V_{ICM}$ | 100 Mbps speed signaling off | 1.165 | | 2.515 | V |
| | | 200 Mbps speed signaling | 0.935 | | 2.515 | V |
| | | 400 Mbps speed signaling | 0.523 | | 2.515 | V |
| Differential output voltage | $V_{OD}$ | Cable output (Test load 55Ω) | 172.0 | | 265.0 | mV |
| TpA common mode output voltage | $V_{OCM}$ | 100 Mbps speed signaling off | 1.665 | | 2.015 | V |
| | | 200 Mbps speed signaling | 1.438 | | 2.015 | V |
| | | 400 Mbps speed signaling | 1.030 | | 2.015 | V |
| TpA common mode output current | $I_{CM}$ | 100 Mbps speed signaling off | –0.81 | | +0.44 | mA |
| | | 200 Mbps speed signaling | –4.84 | | –2.53 | mA |
| | | 400 Mbps speed signaling | –12.40 | | –8.10 | mA |
| Power status threshold voltage | $V_{TH}$ | CPS | | | 7.5 | V |
| TpBias output voltage | $V_{TPBIAS}$ | | 1.665 | | 2.015 | V |

## AC Characteristics

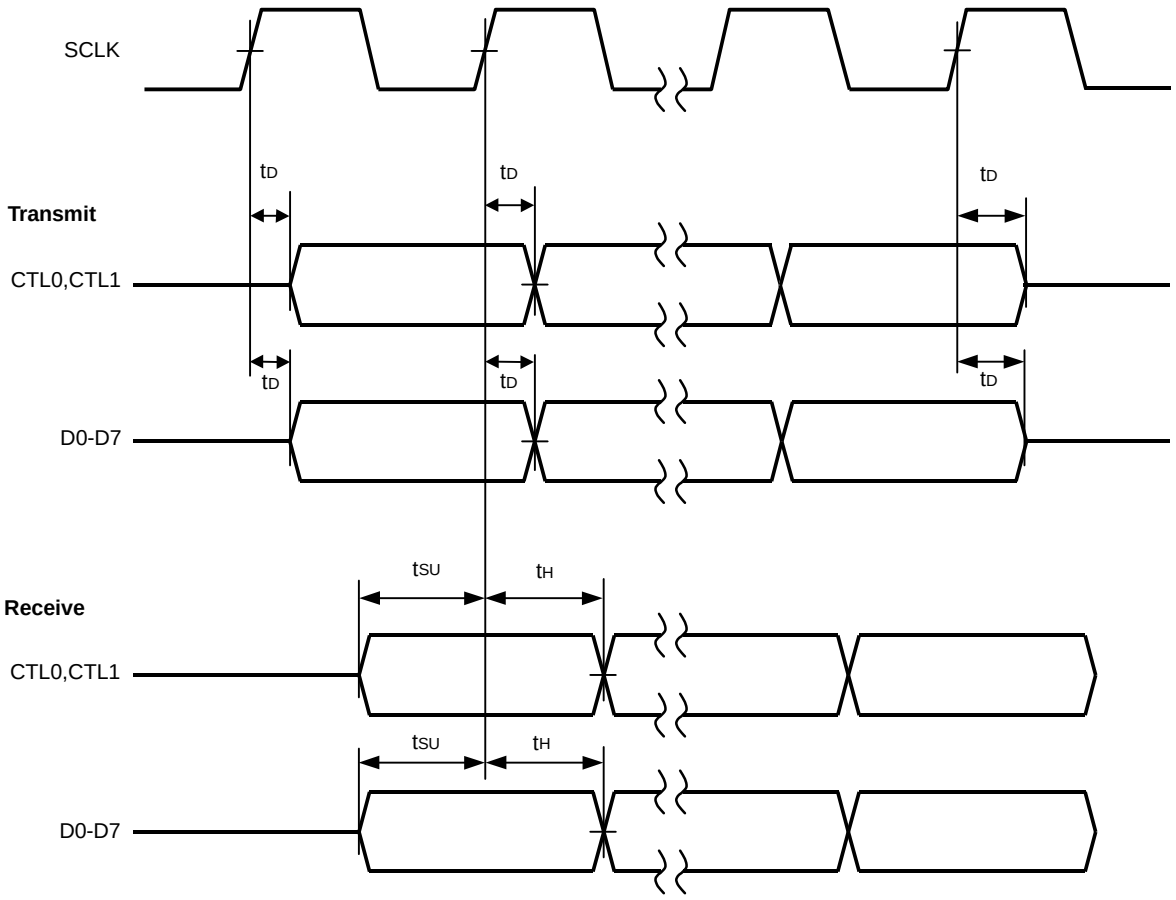
### PHY/Link Interface

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| D, CTL, LREQ setup time | $t_{SU}$ | | 6 | | | ns |
| D, CTL, LREQ hold time | $t_{HD}$ | | 0 | | | ns |
| D, CTL output timing | $t_{D}$ | | 2 | | 12 | ns |
| SCLK cycle time | $t_{SCLK}$ | | 20 | | | ns |
| SCLK high level time | $t_{SCLKH}$ | | 9 | | 11 | ns |
| SCLK low level time | $t_{SCLKL}$ | | 9 | | 11 | ns |
| LKON cycle time | $t_{LINKON}$ | | 160 | | | ns |

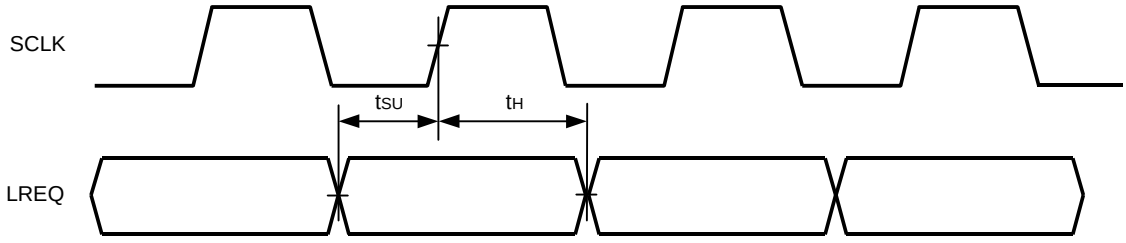
### Link Interface Timing (SCLK, LKON)



**Link Interface Timing (CTL, D)**




**Link Interface Timing (LREQ)**

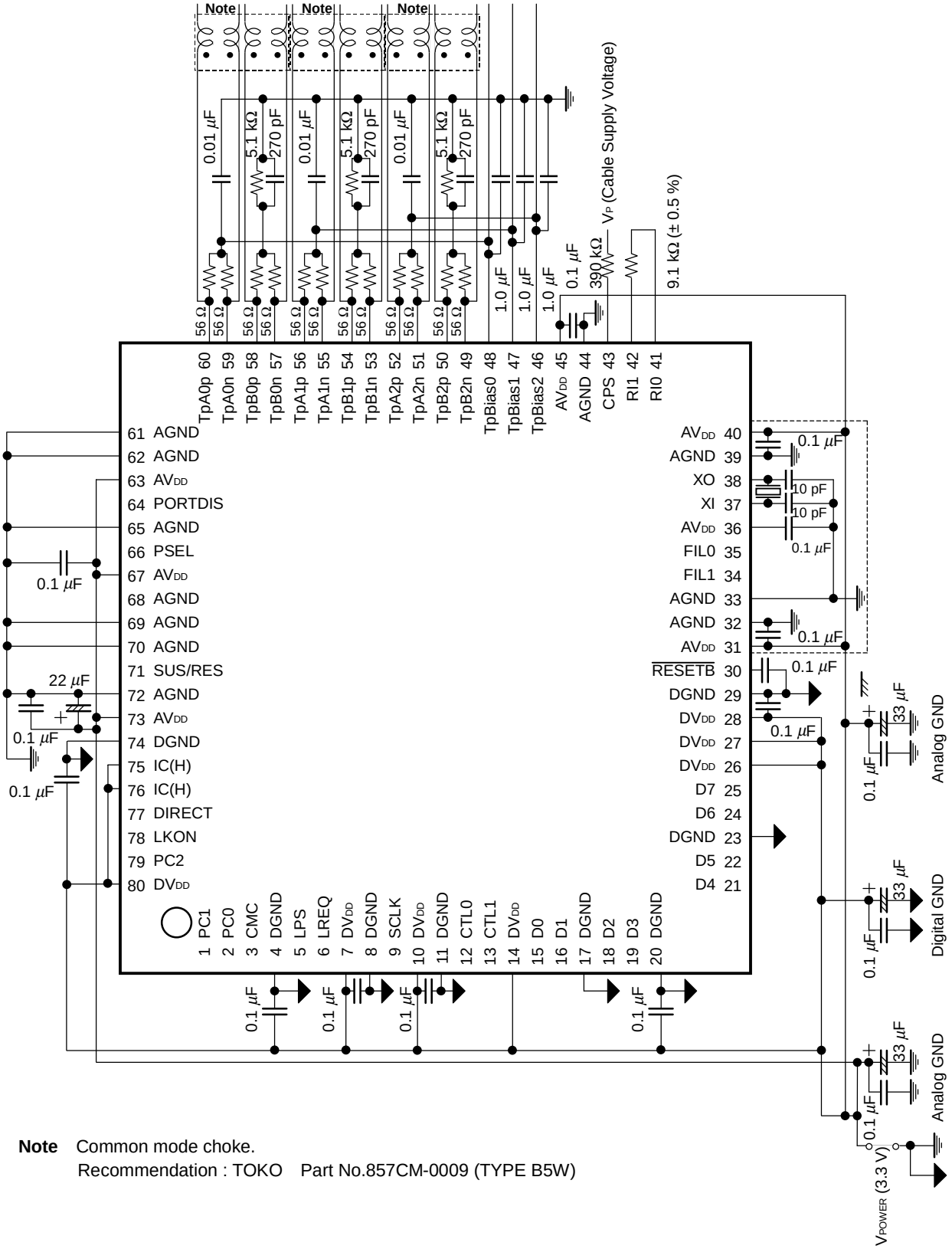


**Cable Interface**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| TpA, TpB transfer jitter | $t_{JITTER}$ | Between TpA and TpB | | | ±0.15 | ns |
| TpA strobe, TpB data transfer | $t_{SKEW}$ | Between TpA and TpB | | | ±0.10 | ns |
| TPA, TPB rise time/fall time | $t_R/t_F$ | 10% to 90%, via 55Ω and 10 pF | | | 1.2 | ns |

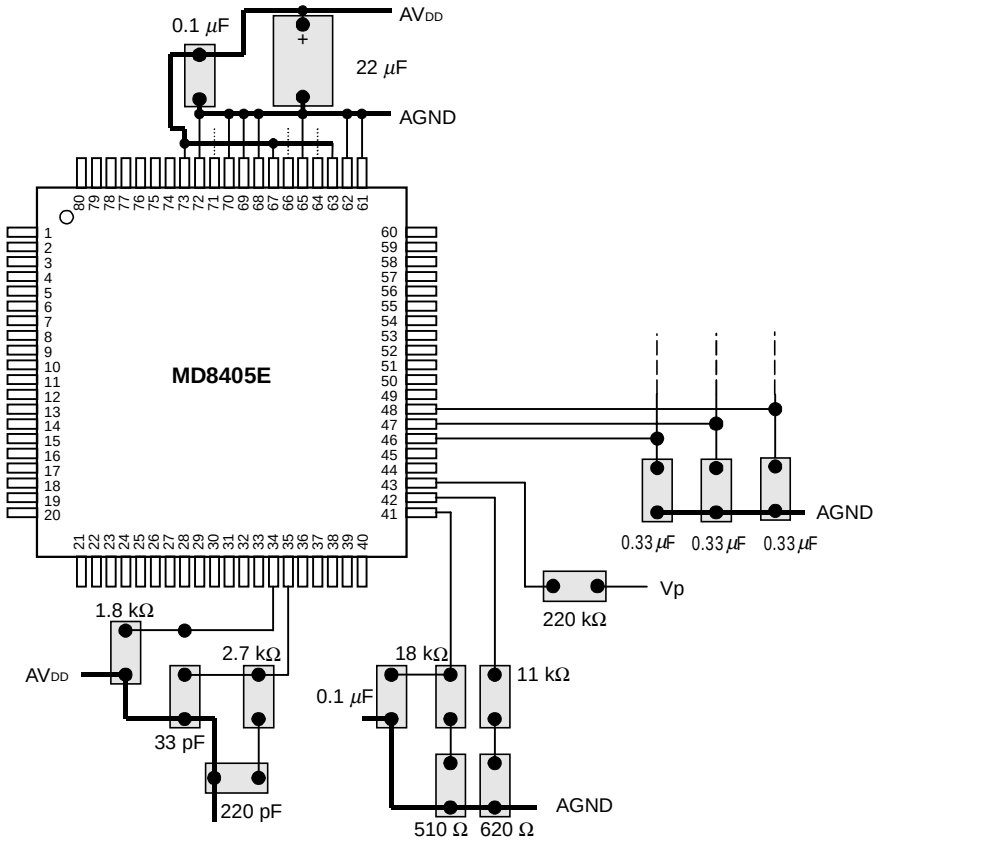
## 7. APPLICATION CIRCUIT EXAMPLE

### 7.1 IEEE1394 Interface

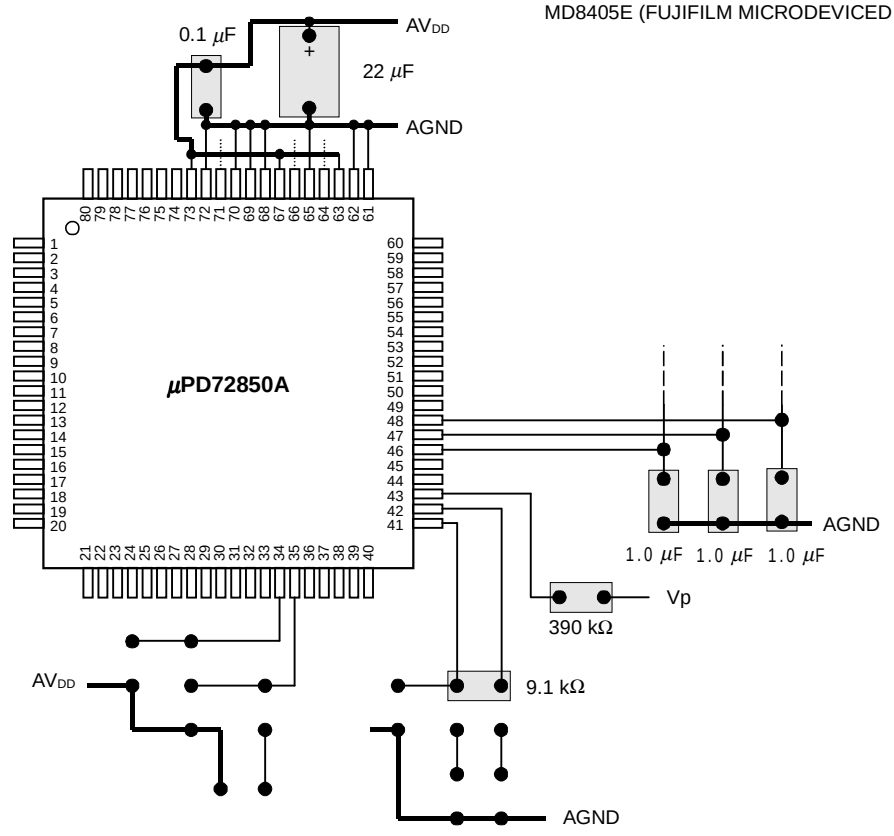



**Note** Common mode choke.
Recommendation : TOKO Part No.857CM-0009 (TYPE B5W)

### 7.2 NEC/FFM Board Sharing

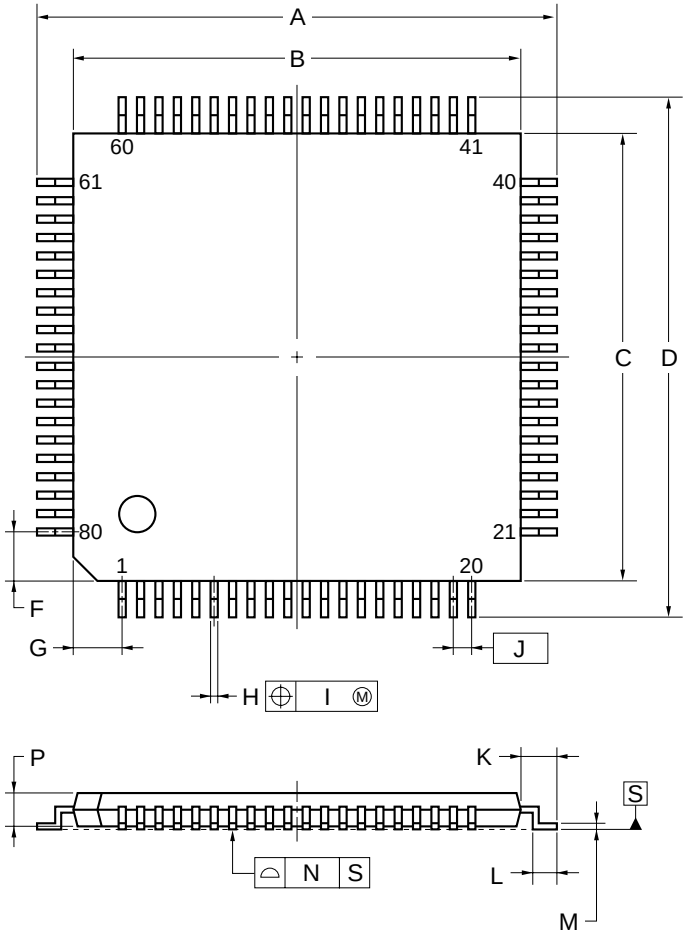



MD8405E (FUJIFILM MICRODEVICED CO.,LTD)

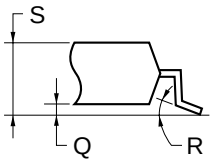


## 8. PACKAGE DRAWING

## 80-PIN PLASTIC TQFP (FINE PITCH) (12x12)




detail of lead end




**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 14.0±0.2 |
| B | 12.0±0.2 |
| C | 12.0±0.2 |
| D | 14.0±0.2 |
| F | 1.25 |
| G | 1.25 |
| H | 0.22±0.05 |
| I | 0.10 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | 0.145±0.05 |
| N | 0.10 |
| P | 1.0±0.05 |
| Q | 0.1±0.05 |
| R | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |
| S | 1.2 MAX. |

**S80GK-50-9EU-1**

## 9. RECOMMENDED SOLDERING CONDITIONS

The μPD72850A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Table 9-1. Surface Mounting Type Soldering Conditions**

**μPD72850AGK-9EU : 80-pin plastic TQFP (Fine pitch) (12 x 12 mm)**

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher).<br>Count: three times or less<br>Exposure limit: 3 days[Note] (after that prebake at 125°C for 10 hours) | IR35-103-3 |
| Partial heating | Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row) | — |

**Note** After opening the dry pach, store it at 25°C or less and 65% RH or less for the allowable storage period.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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M7 98.8