NEC

MOS INTEGRATED CIRCUIT

μPD23C16343, 23C16383

16M-BIT MASK-PROGRAMMABLE ROM
1M-WORD BY 16-BIT
PAGE ACCESS MODE

Description

The μPD23C16343 and μPD23C16383 are 16,777,216 bits mask-programmable ROM. The word organization is 1,048,576 words by 16 bits.

The active levels of OE (Output Enable Input) can be selected with mask-option.

The μPD23C16343 and μPD23C16383 are packed in 48-pin PLASTIC TSOP(I) and 48-pin TAPE FBGA.

Features

- Pin compatible with NOR Flash Memory
- Word organization
  - 1,048,576 words by 16 bits
- Page access mode
  - 4 word random page access (μPD23C16343)
  - 8 word random page access (μPD23C16383)
- Operating supply voltage : V_{CC} = 2.7 V to 3.6 V
- Input / output supply voltage : $V_{CC}Q$ = 1.65 V to 1.95 V

Operating supply voltage V_{CC}	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)		Standby current (CMOS level input) μA (MAX.)
		μPD23C16343	μPD23C16383	
3.3 V ± 0.3 V	85 / 25	40	55	30
3.0 V ± 0.3 V	90 / 25			

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Ordering Information

Part Number	Package
μPD23C16343GZ-xxx-MJH	48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)
μPD23C16343F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)
μPD23C16383GZ-xxx-MJH	48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)
μPD23C16383F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)

(xxx : ROM code suffix No.)

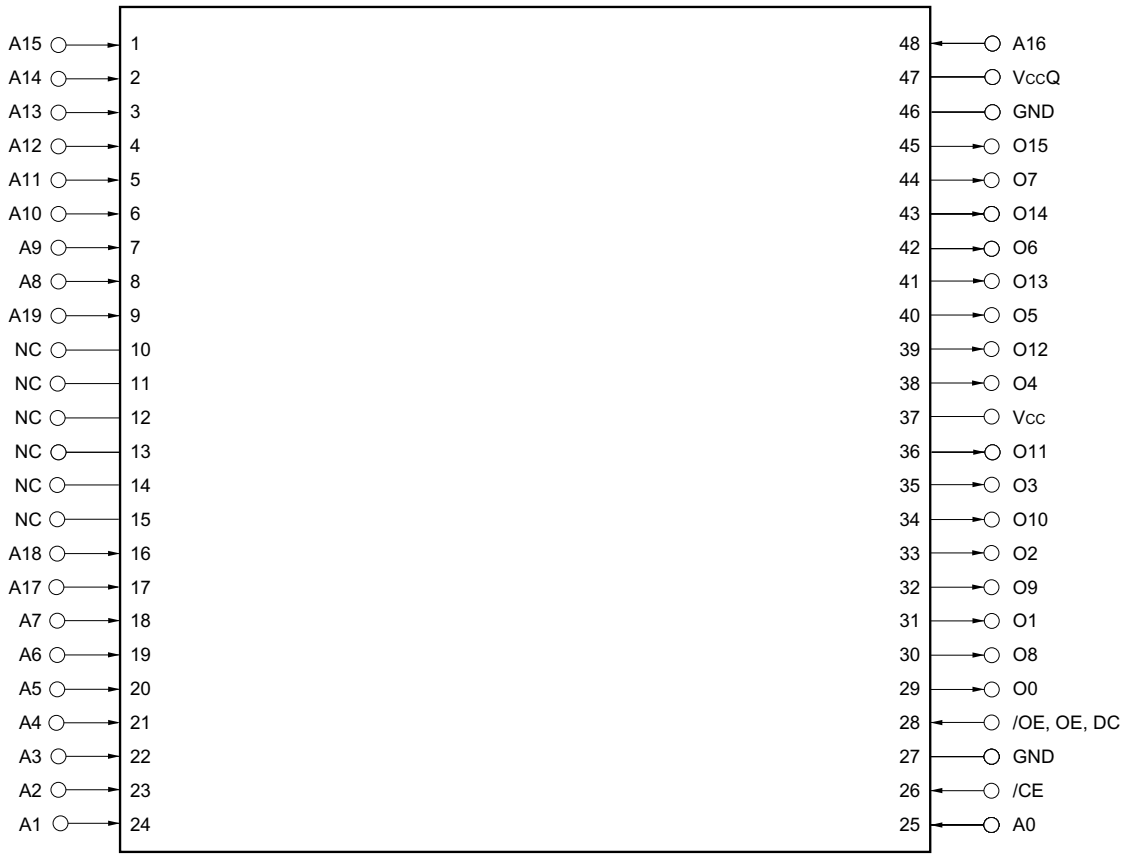
Pin Configurations (Marking Side)

/xxx indicates active low signal.

48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

[μPD23C16343GZ-xxx-MJH]

[μPD23C16383GZ-xxx-MJH]



A0 - A19	: Address inputs
O0 - O15	: Data outputs
/CE	: Chip Enable
/OE, OE	: Output Enable
Vcc	: Supply voltage
VccQ	: Input / output supply voltage
GND	: Ground
NC [Note]	: No Connection
DC	: Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

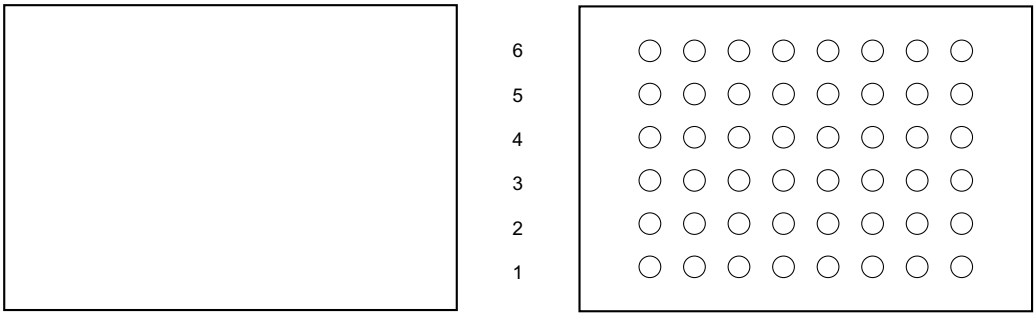
Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin TAPE FBGA (8 x 6)

[μPD23C16343F9-xxx-BC3]

[μPD23C16383F9-xxx-BC3]

Top View **Bottom View**



	A	B	C	D	E	F	G	H
6	A13	A12	A14	A15	A16	$V_{CC}Q$	O15	GND
5	A9	A8	A10	A11	O7	O14	O13	O6
4	NC	NC	NC	A19	O5	O12	V_{CC}	O4
3	NC	NC	A18	NC	O2	O10	O11	O3
2	A7	A17	A6	A5	O0	O8	O9	O1
1	A3	A4	A2	A1	A0	/CE	/OE, OE	GND

	H	G	F	E	D	C	B	A
6	GND	O15	$V_{CC}Q$	A16	A15	A14	A12	A13
5	O6	O13	O14	O7	A11	A10	A8	A9
4	O4	V_{CC}	O12	O5	A19	NC	NC	NC
3	O3	O11	O10	O2	NC	A18	NC	NC
2	O1	O9	O8	O0	A5	A6	A17	A7
1	GND	/OE, OE	/CE	A0	A1	A2	A4	A3

A0 - A19	: Address inputs
O0 - O15	: Data outputs
/CE	: Chip Enable
/OE, OE	: Output Enable
V_{CC}	: Supply voltage
$V_{CC}Q$	: Input / output supply voltage
GND	: Ground
NC [Note]	: No Connection
DC	: Don't Care

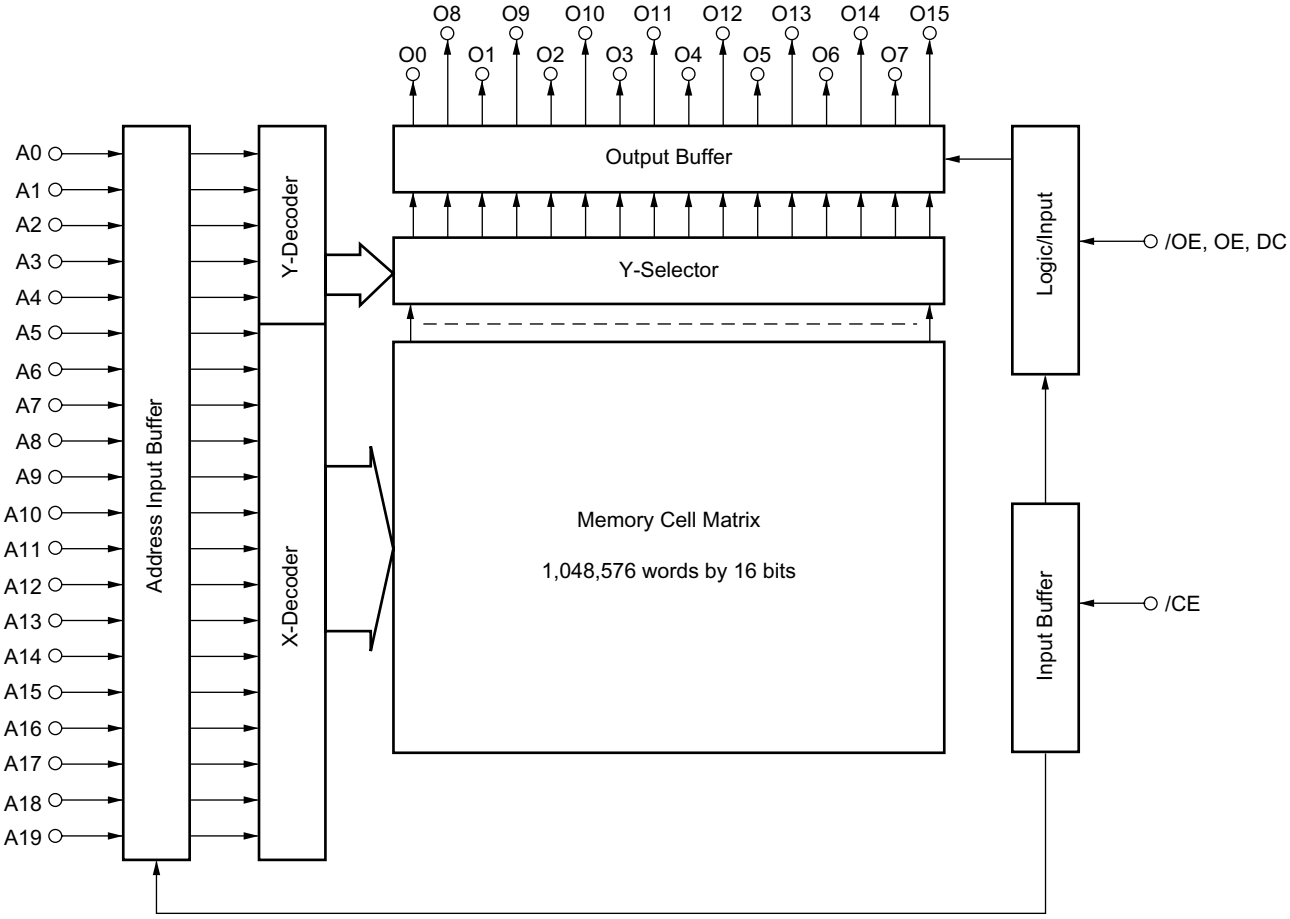
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the index mark.

Input / Output Pin Functions

Pin name	Input / Output	Function
A0 to A19 (Address inputs)	Input	Address input pins. A0 to A19 are used as 20 bits address signals.
O0 to O15 (Data outputs)	Output	Data output pins. 16 bits data outputs to O0 to O15.
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High impedance **Low level** : Data out
/OE, OE, DC (Output Enable, Don't care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
$V_{CC}Q$	–	Input / output supply voltage
GND	–	Ground
NC	–	Not internally connected. (The signal can be connected.)

Block Diagram



Mask Option

The active levels of output enable pin (/OE, OE, DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE, OE, DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High impedance
H	H or L	Standby	High impedance

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High impedance
	H		Data out
H	H or L	Standby	High impedance

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High impedance

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input / output supply voltage	V_{CCQ}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CCQ}+0.3	V
Output voltage	V_O		–0.3 to V_{CCQ}+0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V, V_{CCQ} = 1.65 to 1.95 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}			0.8 V_{CCQ}		V_{CCQ} + 0.3	V
Low level input voltage	V_{IL}	V_{CCQ} = 1.8 V ± 0.15 V		–0.3		0.2 V_{CCQ}	V
High level output voltage	V_{OH}	I_{OH} = –100 μA		0.8 V_{CCQ}			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA				0.2 V_{CCQ}	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CCQ}		–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CCQ}, Chip deselected		–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode),	μPD23C16343			40	mA
		I_O = 0 mA	μPD23C16383			55	
Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)				30	μA

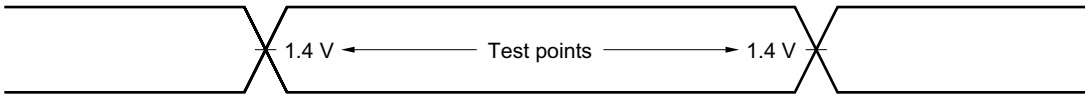
AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V, $V_{CC}Q$ = 1.65 to 1.95 V)

Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	t_{ACC}				90			85	ns
Page access time	t_{PAC}				25			25	ns
Chip enable access time	t_{CE}				90			85	ns
Output enable access time	t_{OE}				25			25	ns
Output hold time	t_{OH}		0			0			ns
Output disable time	t_{DF}		0		25	0		25	ns

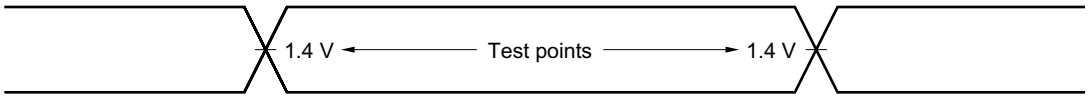
Remark t_{DF} is the time from inactivation of /CE or /OE, OE to high-impedance state output.

AC Test Conditions

Input waveform (Rise / Fall time ≤ 5 ns)



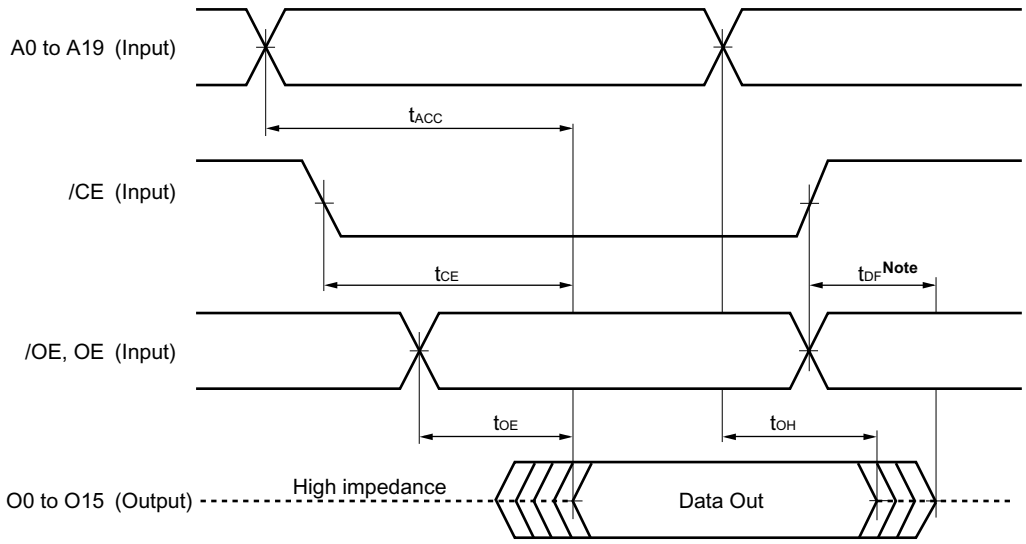
Output waveform



Output load

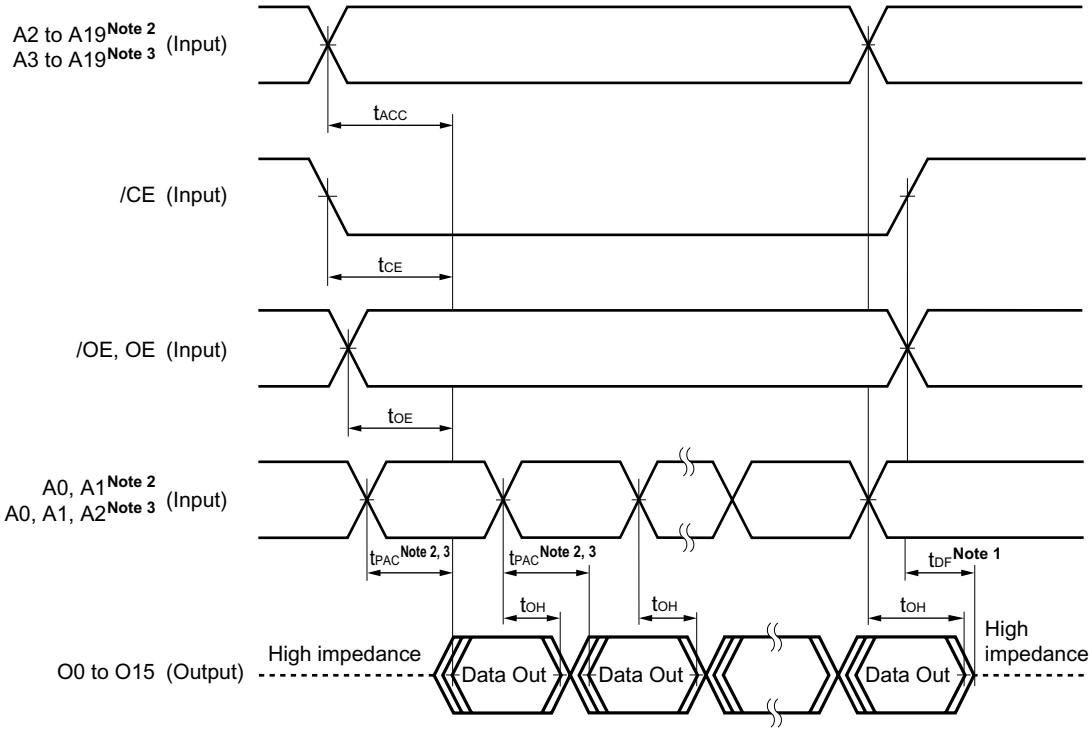
1TTL + 100 pF

Read Cycle Timing Chart 1



Note t_{DF} is specified when one of /CE, /OE, OE is inactivated.

Read Cycle Timing Chart 2 (Page Access Mode)



Notes 1. t_{DF} is specified when one of /CE, /OE, OE is inactivated.

2. The definition of page access time is as follows.

[μPD23C16343]

Page access time	Upper address (A2 to A19) inputs condition	/CE input condition	/OE, OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A0, A1)

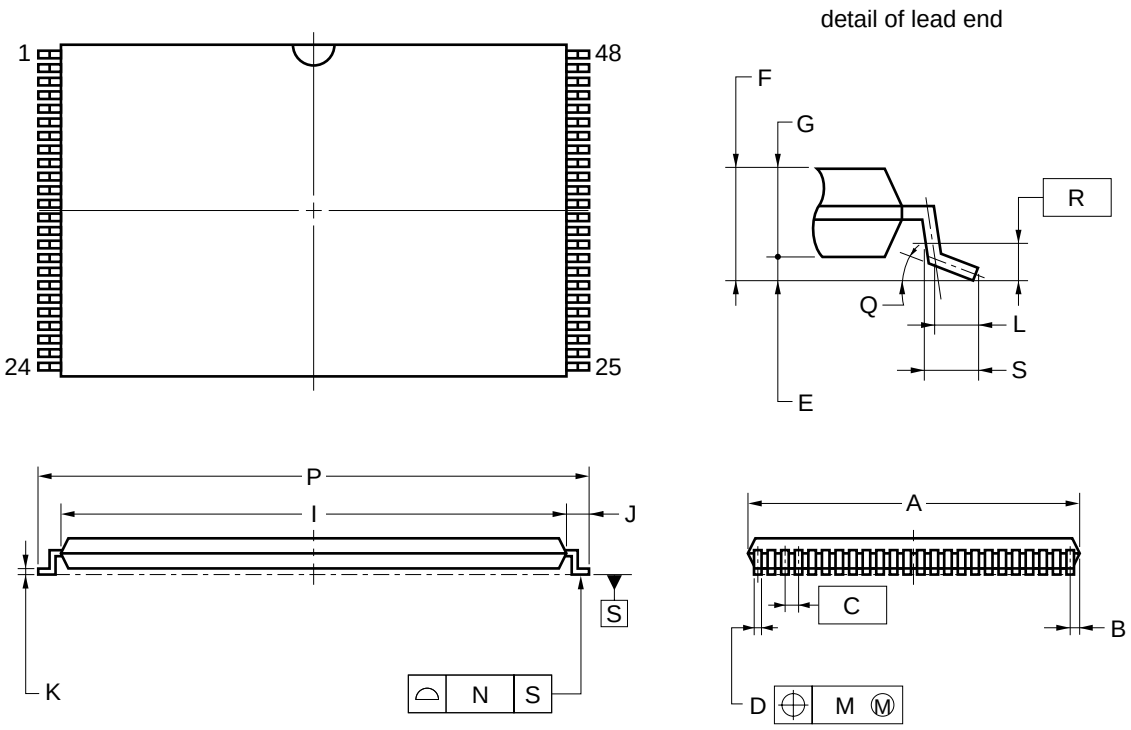
3. The definition of page access time is as follows.

[μPD23C16383]

Page access time	Upper address (A3 to A19) inputs condition	/CE input condition	/OE, OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A0, A1, A2)

Package Drawings

48-PIN PLASTIC TSOP (I) (12x20)



NOTES

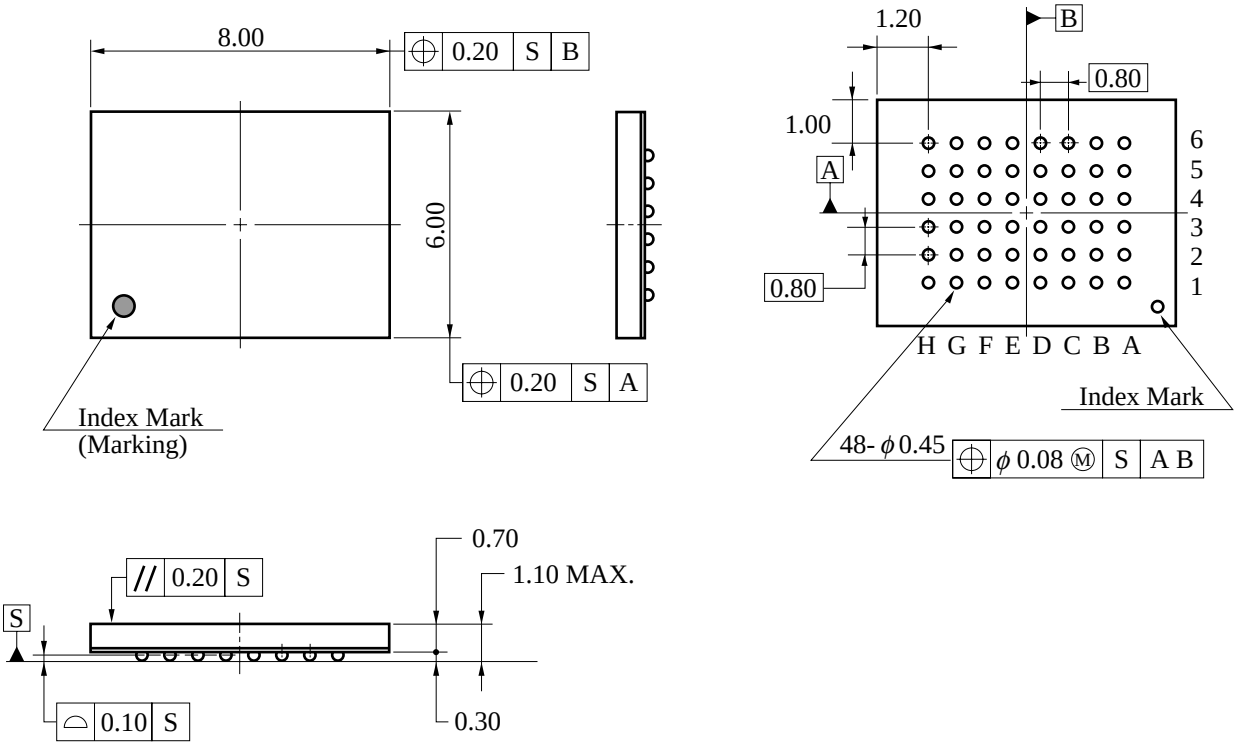
1) Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

2) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GZ-50-MJH-1

48-PIN TAPE FBGA (8x6) (unit: mm)



This package drawing is a preliminary version. It may be changed in the future.

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C16343 and μPD23C16383.

Types of Surface Mount Device

μPD23C16343GZ-MJH : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)
μPD23C16343F9-BC3 : 48-pin TAPE FBGA (8 x 6)
μPD23C16383GZ-MJH : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)
μPD23C16383F9-BC3 : 48-pin TAPE FBGA (8 x 6)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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