

## 8-BIT SINGLE-CHIP MICROCONTROLLER

The  $\mu$ PD178004, 178006, 178016 and 178018 are 8-bit single-chip CMOS microcontrollers that incorporate hardware for digital tuning systems.

The CPU uses the 78K/0 architecture and high-speed access to internal memory and control of peripheral hardware are easy to implement. Also, the instructions used are the high-speed 78K/0 instructions, suitable for system control.

The rich assortment of peripheral hardware includes an input/output port, 8-bit timer, A/D converter, serial interface, power-ON clear circuits, as well as a pre-scaler for digital tuning, a PLL frequency synthesizer and a frequency counter.

The  $\mu$ PD178P018, one-time PROM or EPROM versions which can be operated in the same supply voltage range as for the mask ROM versions, and various development tools, are also available.

**For more information on functions, refer to the following User's Manuals. Be sure to read them when designing.**

**$\mu$ PD178018 Subseries User's Manual: U11410E**  
**78K/0 Series User's Manual Instruction: IEU-1372**

## FEATURES

- Internal high-capacity ROM and RAM

Items Product Name	Program Memory ROM	Data Memory		
		Internal High-Speed RAM	Buffer RAM	Internal Expanded RAM
$\mu$ PD178004	32 Kbytes	1024 bytes	32 bytes	Not provided
$\mu$ PD178006	48 Kbytes			2048 bytes
$\mu$ PD178016				
$\mu$ PD178018	60 Kbytes			

- Instruction Cycle: 0.44  $\mu$ s (4.5-MHz crystal oscillator used)
- Large array of on-chip peripheral hardware  
General-purpose input/output port, A/D converter, serial interface, timer, frequency counter, power-ON clear circuits.
- On-chip hardware for a PLL frequency synthesizer.  
Dual modulus pre-scaler, programmable divider, phase comparator, charge pump.
- Vector Interrupts: 17
- Supply Voltage:  $V_{DD} = 4.5$  to 5.5 V (during PLL operation)  
 $V_{DD} = 3.5$  to 5.5 V (during CPU operation, when the system clock is  $f_x/2$  or lower)  
 $V_{DD} = 4.5$  to 5.5 V (during CPU operation, when the system clock is  $f_x$ )

The information in this document is subject to change without notice.

**APPLICATIONS**

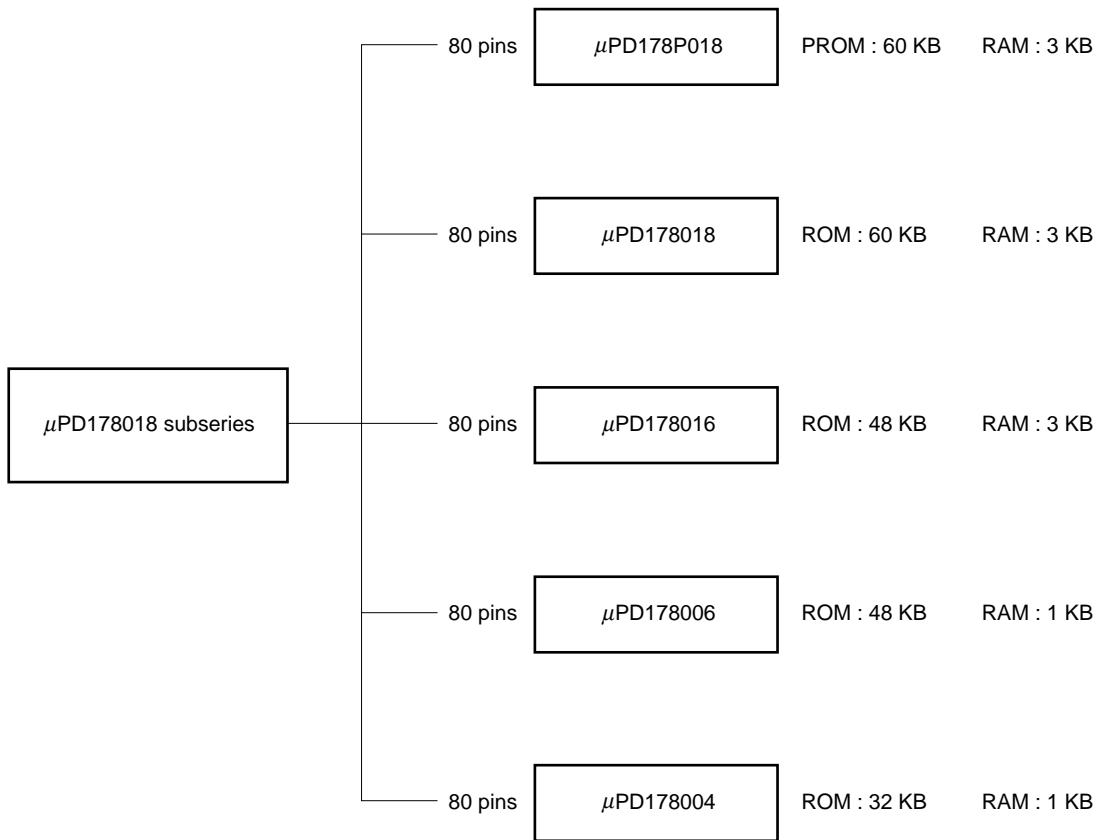
Car stereo, home stereo systems.

**ORDERING INFORMATION**

Part Number	Package
μPD178004GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178006GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178016GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178018GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)

**Remark** xxx denotes the ROM code number. Also, the ROM code number becomes Exx when the I<sup>2</sup>C bus is used.

**μPD178018 SUBSERIES EXPANSION**



OUTLINE OF FUNCTION

(1/2)

Product name		μPD178004	μPD178006	μPD178016	μPD178018
Internal memory	ROM (ROM configuration)	32 Kbytes (mask ROM)	48 Kbytes (mask ROM)		60 Kbytes (mask ROM)
	Internal high-speed RAM	1024 bytes			
	Buffer RAM	32 bytes			
	Internal expansion RAM	None		2048 bytes	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		With variable instruction execution time function 0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (with 4.5-MHz crystal resonator)			
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operation</li> <li>• Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulation (set, reset, test, Boolean operation)</li> <li>• BCD adjustment, etc.</li> </ul>			
I/O port		Total : 62 pins CMOS input : 1 pin CMOS I/O : 54 pins N-ch open-drain I/O : 4 pins N-ch open-drain output : 3 pins			
A/D converter		8-bit resolution × 6 channels			
Serial interface		<ul style="list-style-type: none"> <li>• 3-wire/SBI/2-wire/I<sup>2</sup>C bus<sup>Note</sup> mode selectable : 1 channel</li> <li>• 3-wire serial I/O mode (with automatic transfer/receive function of up to 32 byte) : 1 channel</li> </ul>			
Timer		<ul style="list-style-type: none"> <li>• Basic timer (timer carry FF (10 Hz)) : 1 channel</li> <li>• 8-bit timer/event counter : 2 channels</li> <li>• 8-bit timer (D/A converter: PWM output): 1 channel</li> <li>• Watchdog timer : 1 channel</li> </ul>			
Buzzer (BEEP) output		1.5 kHz, 3 kHz, 6 kHz			
Vectored interrupt	Maskable interrupt	Internal: 8, external: 7			
	Non-maskable interrupt	Internal: 1			
	Software interrupt	Internal: 1			
Test input		Internal: 1			
PLL frequency synthesizer	Division mode	Two types <ul style="list-style-type: none"> <li>• Direct division mode (VCOL pin)</li> <li>• Pulse swallow mode (VCOH and VCOL pins)</li> </ul>			
	Reference frequency	12 types selectable by program (1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50 kHz)			
	Charge pump	Error out output: 2			
	Phase comparator	Unlock detectable by program			
Frequency counter		<ul style="list-style-type: none"> <li>• Frequency measurement                             <ul style="list-style-type: none"> <li>• AMIFC pin: for 450-kHz count</li> <li>• FMIFC pin: for 450-kHz/10.7-MHz count</li> </ul> </li> </ul>			
D/A converter (PWM output)		8-/9-bit resolution × 3 channels (shared by 8-bit timer)			

**Note** When using the I<sup>2</sup>C bus mode (including when this mode is implemented by program without using the peripheral hardware), consult your local NEC sales representative when you place an order for mask.

(2/2)

Item	Product name	μPD178004	μPD178006	μPD178016	μPD178018
Standby function		<ul style="list-style-type: none"> <li>• HALT mode</li> <li>• STOP mode</li> </ul>			
Reset		<ul style="list-style-type: none"> <li>• Reset by <math>\overline{\text{RESET}}</math> pin</li> <li>• Internal reset by watchdog timer</li> <li>• Reset by power-ON clear circuit (3-value detection)                             <ul style="list-style-type: none"> <li>• Detection of less than 4.5 V<sup>Note</sup> (CPU clock: <math>f_x</math>)</li> <li>• Detection of less than 3.5 V<sup>Note</sup> (CPU clock: <math>f_x/2</math> or less and on power application)</li> <li>• Detection of less than 2.5 V<sup>Note</sup> (in STOP mode)</li> </ul> </li> </ul>			
Power supply voltage		<ul style="list-style-type: none"> <li>• <math>V_{DD} = 4.5</math> to 5.5 V (with PLL operating)</li> <li>• <math>V_{DD} = 3.5</math> to 5.5 V (with CPU operating, CPU clock: <math>f_x/2</math> or less)</li> <li>• <math>V_{DD} = 4.5</math> to 5.5 V (with CPU operating, CPU clock: <math>f_x</math>)</li> </ul>			
Package		<ul style="list-style-type: none"> <li>• 80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)</li> </ul>			

**Note** These voltage values are maximum values. The reset is actually executed at a voltage lower than these values.

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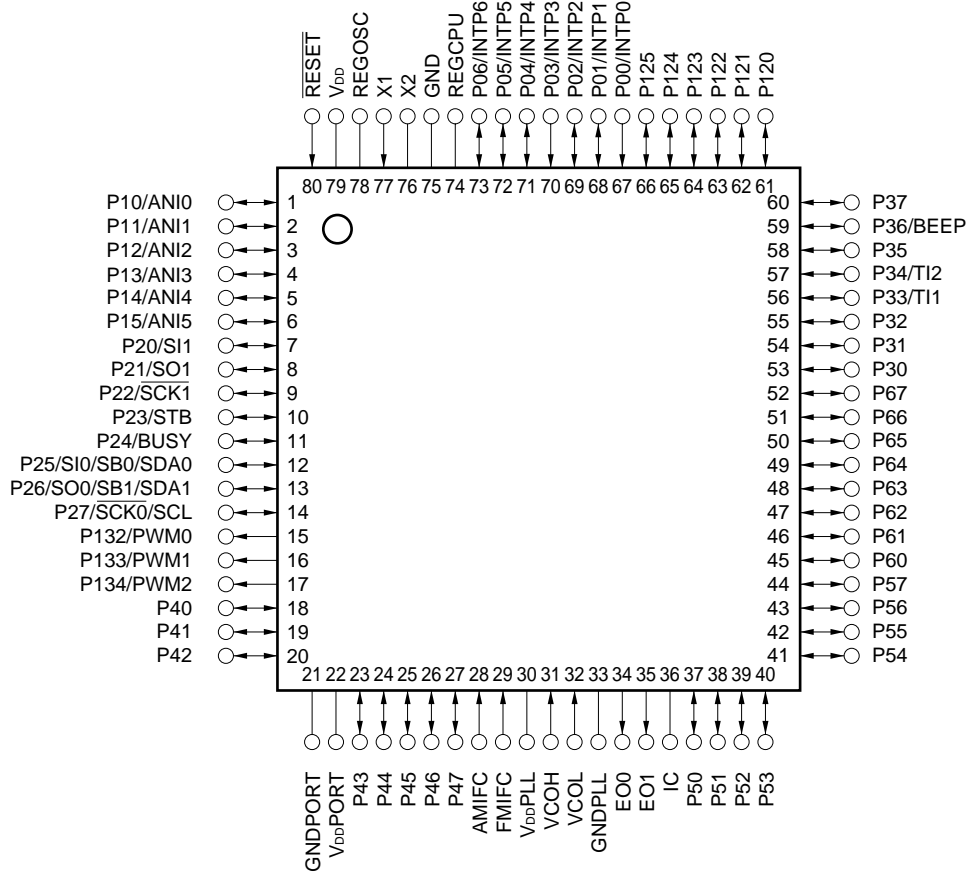
**APPENDIX B. RELATED DOCUMENTS ..... 50**

1. PIN CONFIGURATION (TOP VIEW)

• 80-PIN PLASTIC QFP (14 × 14 mm, 0.65 mm pitch)

μPD178004GC-xxx-3B9, 178006GC-xxx-3B9

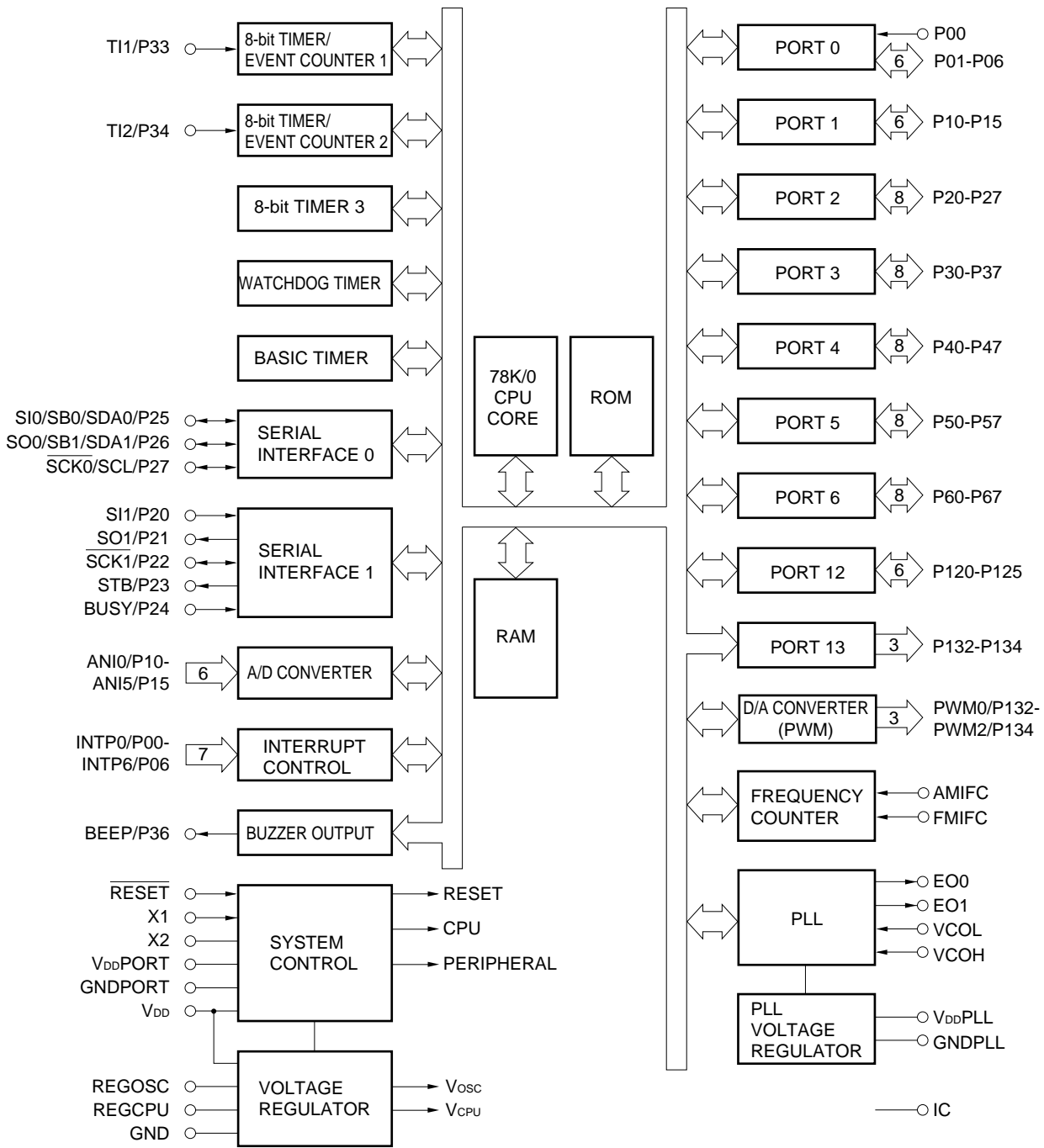
μPD178016GC-xxx-3B9, 178018GC-xxx-3B9



- Cautions**
1. Connect the Internally Connected (IC) pin to GND directly.
  2. Connect V<sub>DD</sub>PORT and V<sub>DD</sub>PLL pins to V<sub>DD</sub>.
  3. Connect the GNDPORT and GNDPLL pins to GND.
  4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1-μF capacitor.

AMIFC	: AM Intermediate Frequency Counter Input	P132-P134	: Port 13
AN10-AN15	: A/D Converter Input	PWM0-PWM2	: PWM Output
BEEP	: Buzzer Output	REGCPU	: Regulator for CPU Power Supply
BUSY	: Busy Output	REGOSC	: Regulator for Oscillator Circuit
EO0, EO1	: Error Out Output	RESET	: Reset Input
FMIFC	: FM Intermediate Frequency Counter Input	SB0, SB1	: Serial Data Bus Input/Output
GND	: Ground	SCK0, SCK1	: Serial Clock Input/Output
GNDPLL	: PLL Ground	SCL	: Serial Clock Input/Output
GNDPORT	: Port Ground	SDA0, SDA1	: Serial Data Input/Output
IC	: Internally Connected	SI0, SI1	: Serial Data Input
INTP0-INTP6	: Interrupt Inputs	SO0, SO1	: Serial Data Output
P00-P06	: Port 0	STB	: Strobe Output
P10-P15	: Port 1	TI1, TI2	: Timer Clock Input
P20-P27	: Port 2	VCOL, VCOH	: Local Oscillator Input
P30-P37	: Port 3	V <sub>DD</sub>	: Power Supply
P40-P47	: Port 4	V <sub>DD</sub> PLL	: PLL Power Supply
P50-P57	: Port 5	V <sub>DD</sub> PORT	: Port Power Supply
P60-P67	: Port 6	X1, X2	: Crystal Oscillator Connection
P120-P125	: Port 12		

2. BLOCK DIAGRAM



**Remark** The internal ROM and RAM capacities depend on the version.



### 3. PIN FUNCTION LIST

#### 3.1 PORT PINS

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0.	Input only	Input	INTP0
P01-P06	I/O	7-bit input/output port.	Input/output mode can be specified bit-wise.	Input	INTP1-INTP6
P10-P15	I/O	Port 1. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	ANI0-ANI5
P20	I/O	Port 2. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK}}1$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK}}0/\text{SCL}$
P30-P32	I/O	Port 3. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P33					TI1
P34					TI2
P35					—
P36					BEEP
P37					—
P40-P47	I/O	Port 4. 8-bit input/output port. Input/output mode can be specified in 8-bit units. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50-P57	I/O	Port 5. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P60-P63	I/O	Port 6. 8-bit input/output port. Input/output mode can be specified bit-wise.	Middle voltage N-ch open drain input/output port. LEDs can be driven directly.	Input	—
P64-P67					
P120-P125	I/O	Port 12. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P132-P134	Output	Port 13. 3-bit output port. N-ch open-drain output port.		—	PWM0-PWM2

3.2 PINS OTHER THAN PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0-INTP6	Input	External maskable interrupt inputs with specifiable valid edges (rising edge, falling edge, both rising and falling edges).	Input	P00-P06
SI0	Input	Serial interface serial data input	Input	P25/SB0/SDA0
SI1				P20
SO0	Output	Serial interface serial data output	Input	P26/SB1/SDA1
SO1				P21
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{\text{SCK0}}$	I/O	Serial interface serial clock input/output	Input	P27/SCL
$\overline{\text{SCK1}}$				P22
SCL				P27/ $\overline{\text{SCK0}}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
TI1	Input	External count clock input to 8-bit timer (TM1)	Input	P33
TI2		External count clock input to 8-bit timer (TM2)		P34
BEEP	Output	Buzzer output	Input	P36
ANI0-ANI5	Input	A/D converter analog input	Input	P10-P15
PWM0-PWM2	Output	PWM output	—	P132-P134
EO0, EO1	Output	Error out output from charge pump of the PLL frequency synthesizer	—	—
VCOL	Input	Inputs PLL local band frequency (In HF, MF mode)	—	—
VCOH	Input	Inputs PLL local band frequency (In VHF mode)	—	—
AMIFC	Input	Inputs AM intermediate frequency counter	—	—
FMIFC	Input	Inputs FM intermediate frequency counter	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	System clock oscillation resonator connection	—	—
X2	—		—	—
REGOSC	—	Oscillation regulator. Connected to GND via a 0.1-μF capacitor.	—	—
REGCPU	—	CPU power supply regulator. Connected to GND via a 0.1-μF capacitor.	—	—
V <sub>DD</sub>	—	Positive power supply	—	—
GND	—	Ground	—	—
V <sub>DD</sub> PORT	—	Positive power supply for port block	—	—
GNDPORT	—	Ground for port block	—	—
V <sub>DD</sub> PLL	—	Positive power supply for PLL	—	—
GNDPLL	—	Ground for PLL	—	—
IC	—	Internally connected. Connected to GND or GNDPORT.	—	—

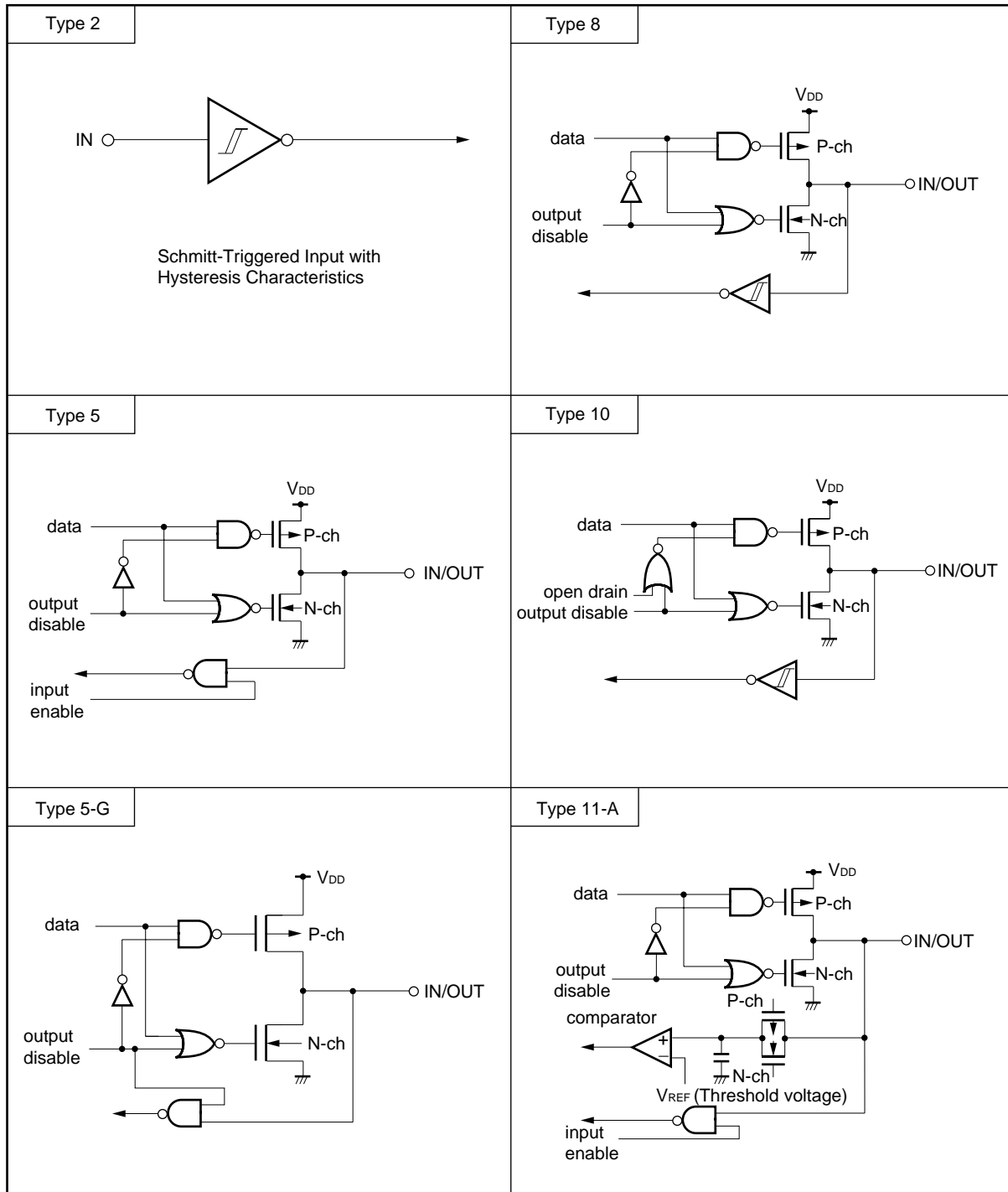
**3.3 INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS**

Table 3-1 shows the input/output circuit types of pins and the recommended conditions for unused pins. Refer to Figure 3-1 for the configuration of the input/output circuit of each type.

**Table 3-1. I/O Circuit Type of Each Circuit**

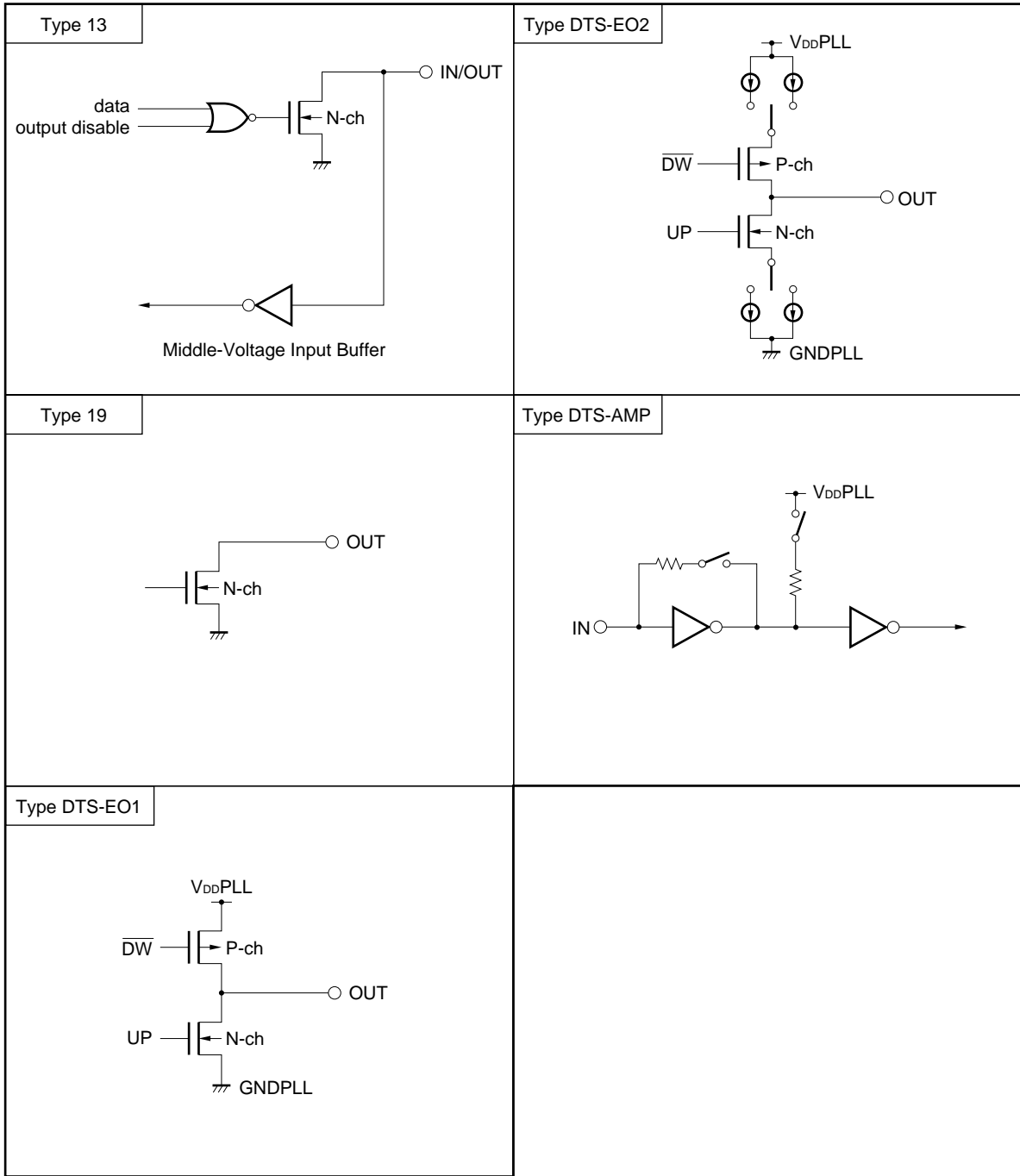
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	2	Input	Connected to GND or GNDPORT
P01/INTP1-P06/INTP6	8	I/O	Set in general-purpose input port mode by software and individually connected to V <sub>DD</sub> , V <sub>DD</sub> PORT, GND, or GNDPORT via resistor.
P10/ANI0-P15/ANI5	11-A		
P20/SI1	8		
P21/SO1	5		
P22/SCK1	8		
P23/STB	5		
P24/BUSY	8		
P25/SI0/SB0/SDA0 P26/SO0/SB1/SDA1 P27/SCK0/SCL	10		
P30-P32	5		
P33/TI1, P34/TI2	8		
P35 P36/BEEP P37	5		
P40-P47	5-G		
P50-P57	5		
P60-P63	13		
P64-P67 P120-P125	5		
P132/PWM0-P134/PWM2	19		
EO0	DTS-EO1		
EO1	DTS-EO2		
VCOL, VCOH AMIFC, FMIFC	DTS-AMP	Input	Set to disabled status by software and open
IC	—	—	Connected to GND or GNDPORT directly

Figure 3-1. Pin Input/Output Circuit of List (1/2)



**Remark** All V<sub>DD</sub> and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V<sub>DD</sub>PORT and GNDPORT, respectively.

Figure 3-1. Pin Input/Output Circuit of List (2/2)

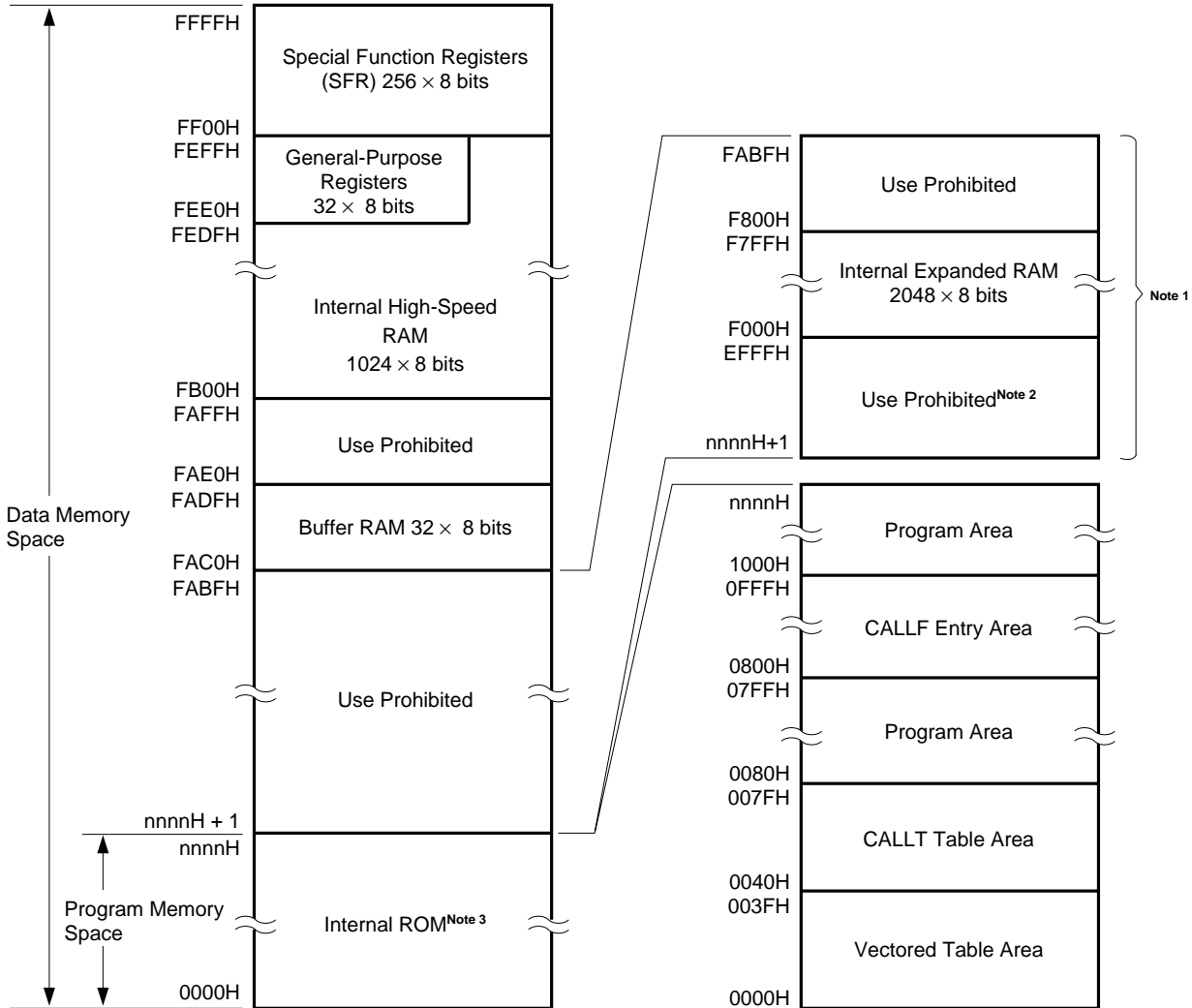


**Remark** All V<sub>DD</sub> and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V<sub>DD</sub>PORT and GNDPORT, respectively.

4. MEMORY SPACE

Figure 4-1 shows the μPD178004, 178006, 178016 and 178018 memory map.

Figure 4-1. Memory Map



- Notes**
1. Available only for μPD178016 and 178018
  2. The μPD178018 does not contain this use prohibited area.
  3. The internal ROM capacity depends on the version (see the table below).

Corresponding Product Name	Internal ROM Last Address nnnnH
μPD178004	7FFFH
μPD178006, 178016	BFFFH
μPD178018	EFFFH

## 5. PERIPHERAL HARDWARE FUNCTION FEATURES

### 5.1 PORTS

The following 3 types of I/O ports are available.

- CMOS input (P00) : 1
  - CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 12) : 54
  - N-channel open-drain input/output (P60 to P63) : 4
  - N-ch open drain output (Port 13) : 3
- 
- Total : 62

**Table 5-1. Port Functions**

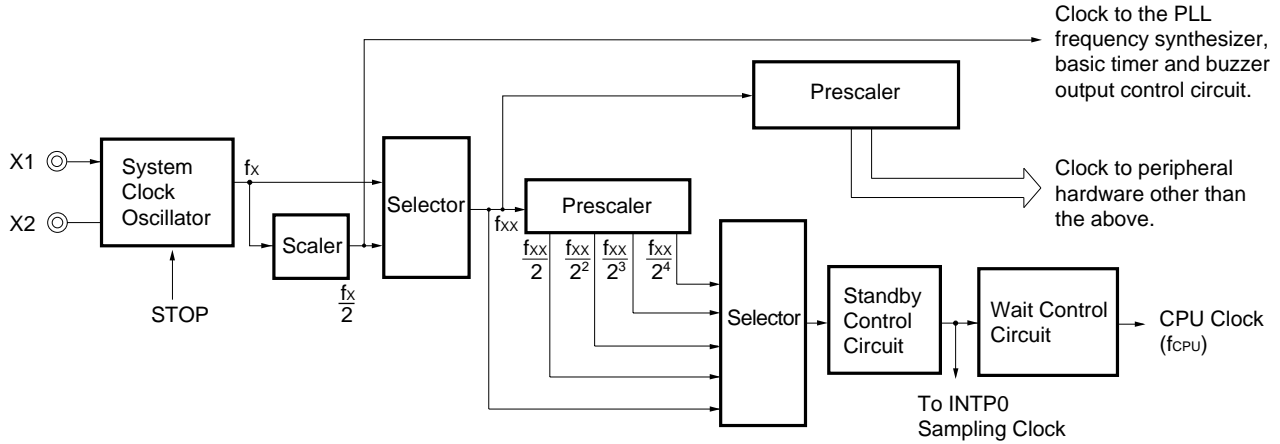
Name	Pin Name	Function
Port 0	P00	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise.
Port 1	P10 to P15	Input/output port pins. Input/output specifiable bit-wise.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. LED direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise.
Port 12	P120 to P125	Input/output port pins. Input/output specifiable bit-wise.
Port 13	P132 to P134	N-ch open drain output port.

**5.2 CLOCK GENERATOR**

The instruction execution time can be changed as follows.

0.44  $\mu$ s/0.88  $\mu$ s/1.78  $\mu$ s/3.56  $\mu$ s/7.11  $\mu$ s/14.22  $\mu$ s (@ 4.5-MHz crystal oscillator with system clock.)

**Figure 5-1. Clock Generator Block Diagram**



**5.3 TIMER**

The  $\mu$ PD178004, 178006, 178016 and 178018 incorporate 5 channels of the timer.

- Basic timer : 1 channel
- 8-bit timer/event counter : 2 channel
- 8-bit timer (D/A converter) <sup>Note</sup> : 1 channel
- Watchdog timer : 1 channel

**Note** Used is shared with the 8/9-bit resolution  $\times$  3-channel D/A converter (PWM output).

**FIGURE 5-2. Basic Timer Block Diagram**

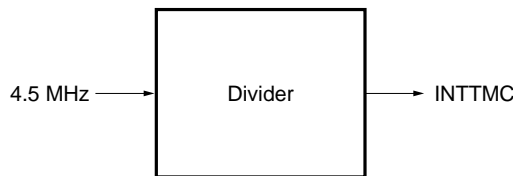




Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

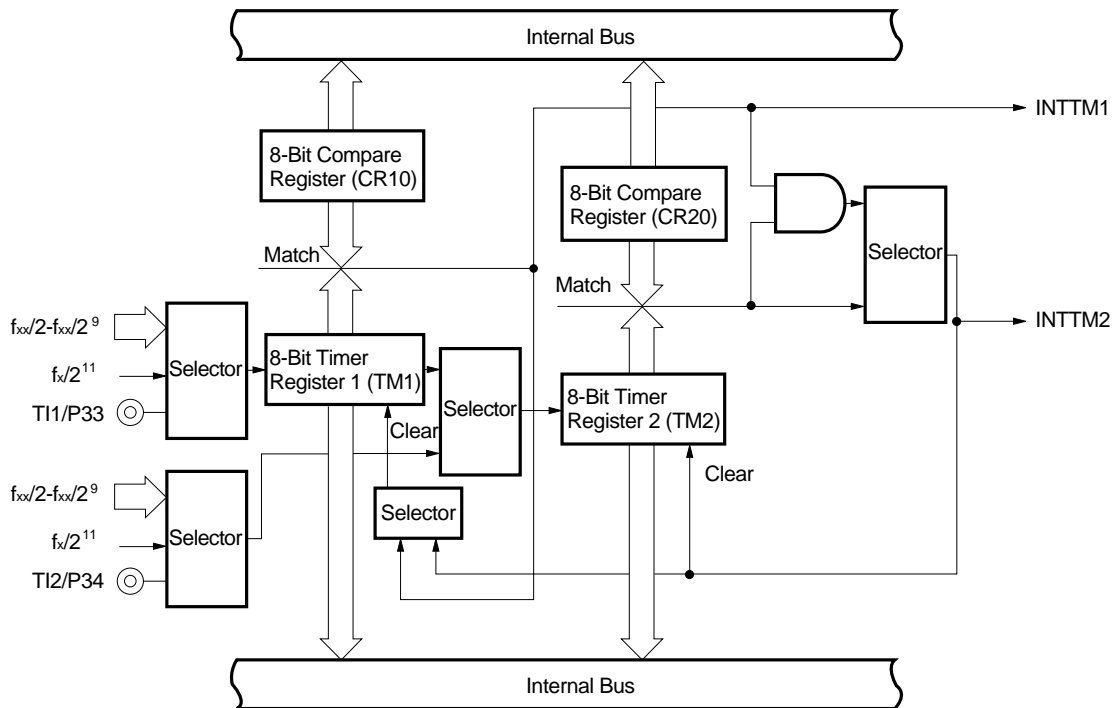
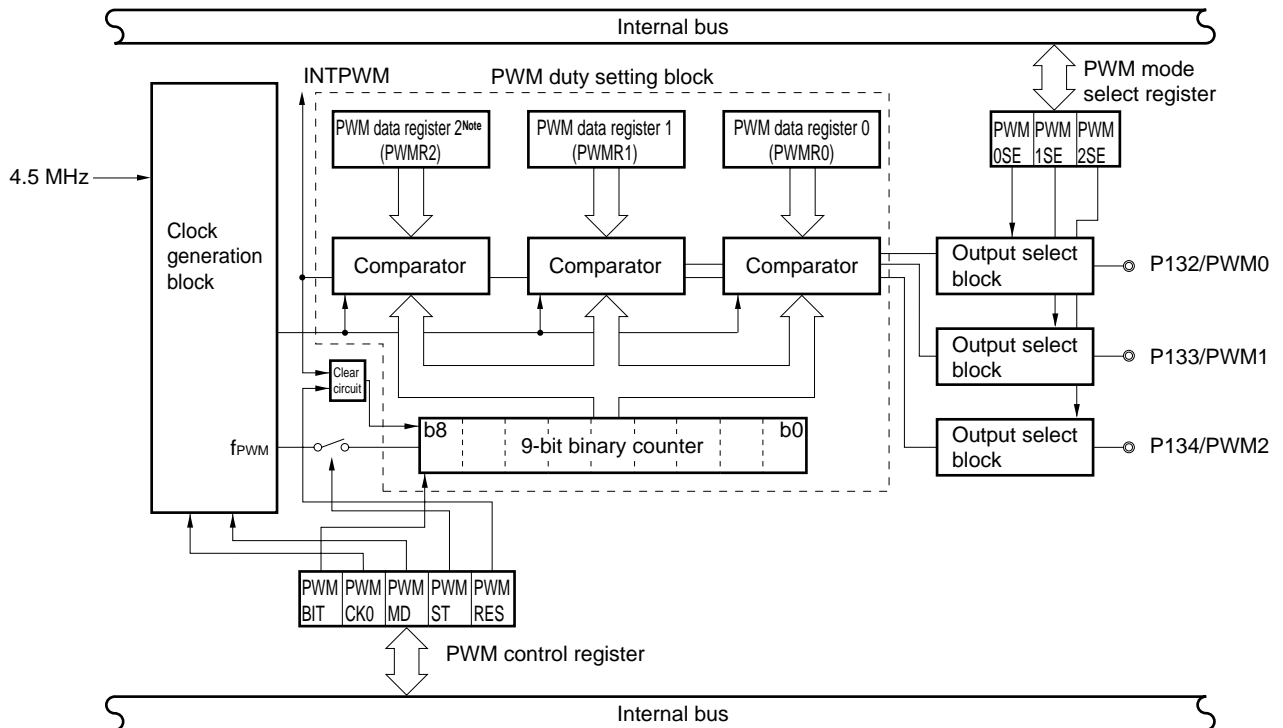
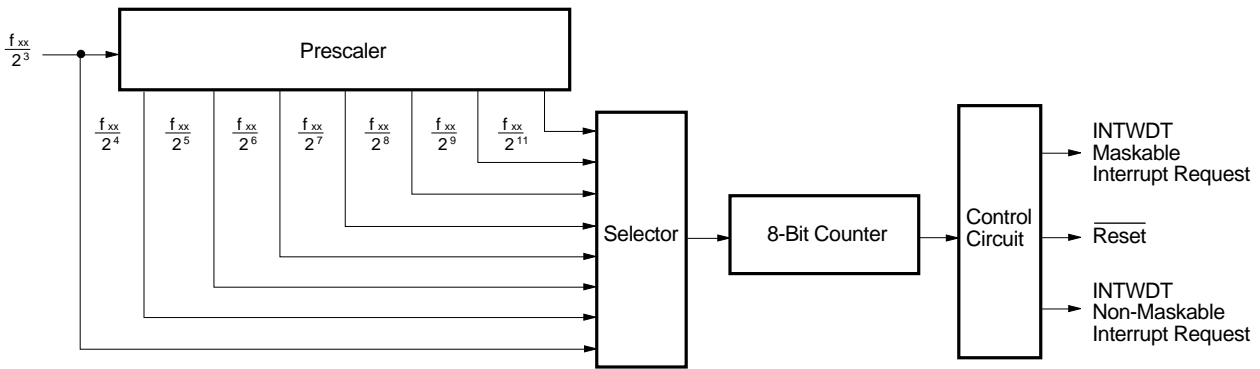


Figure 5-4. 8-Bit Timer (D/A Converter) Block Diagram



**Note** The PWM data register 2 (PWMR2) is multiplexed with the PWM timer register (PWMTMR).

Figure 5-5. Watchdog Timer Block Diagram

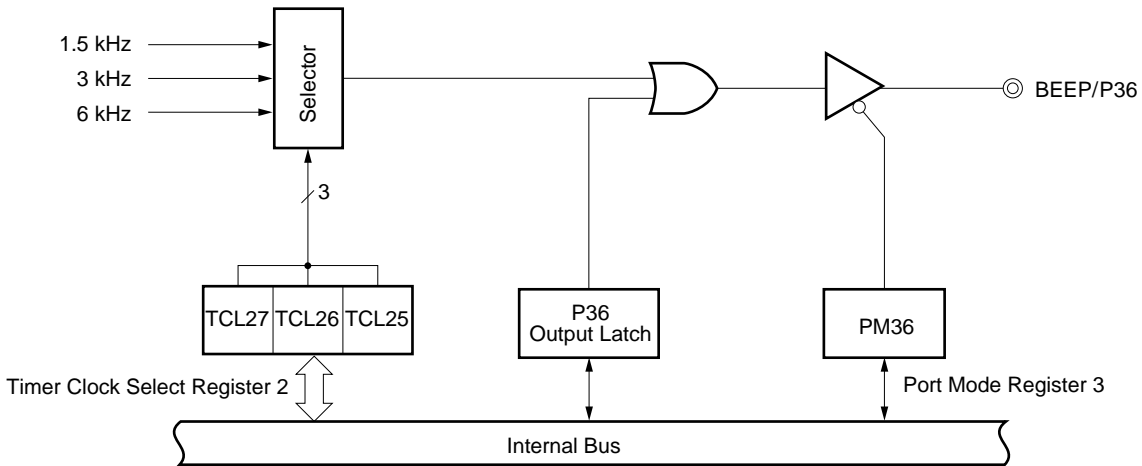


**5.4 BUZZER OUTPUT CONTROL CIRCUIT**

The clock with the following frequency can be output as a buzzer output.

- 1.5 kHz/3 kHz/6 kHz (@ 4.5-MHz crystal oscillator with system clock)

Figure 5-6. Buzzer Output Control Circuit Block Diagram



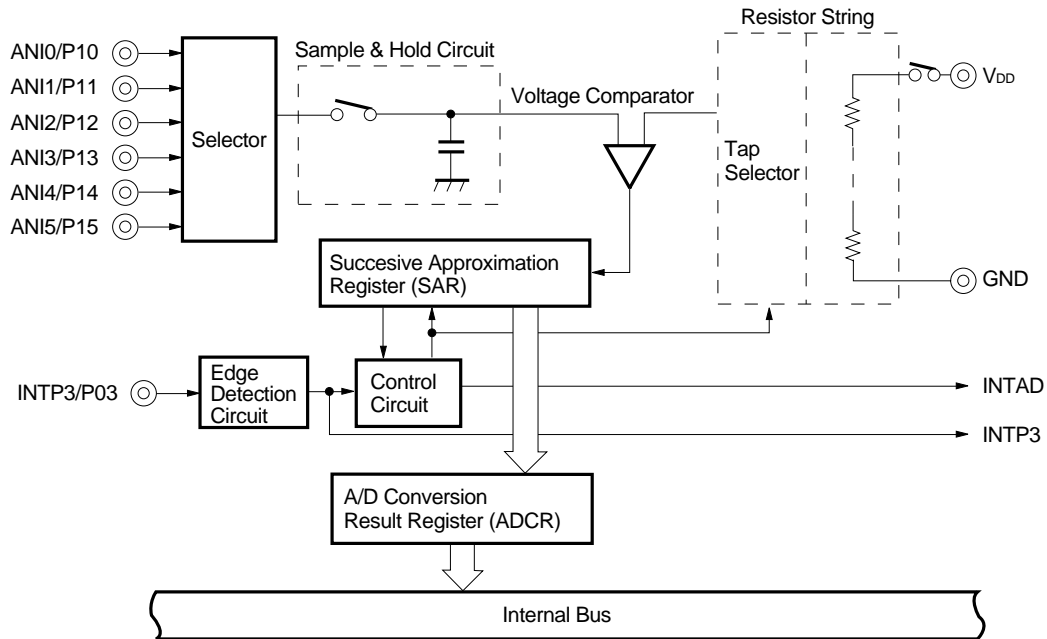
### 5.5 A/D CONVERTER

An A/D converter of 8-bit resolution × 6 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-7. A/D Converter Block Diagram



### 5.6 SERIAL INTERFACES

2 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1

Table 5-2. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	○ (MSB/LSB first switchable)	○ (MSB/LSB first switchable)
3-wire serial I/O mode with automatic transmission/ reception function	—	○ (MSB/LSB first switchable)
SBI (serial bus interface) mode	○ (MSB first)	—
2-wire serial I/O mode	○ (MSB first)	—
I <sup>2</sup> C Bus Mode	○ (MSB first)	—

Figure 5-8. Serial Interface Channel 0 Block Diagram

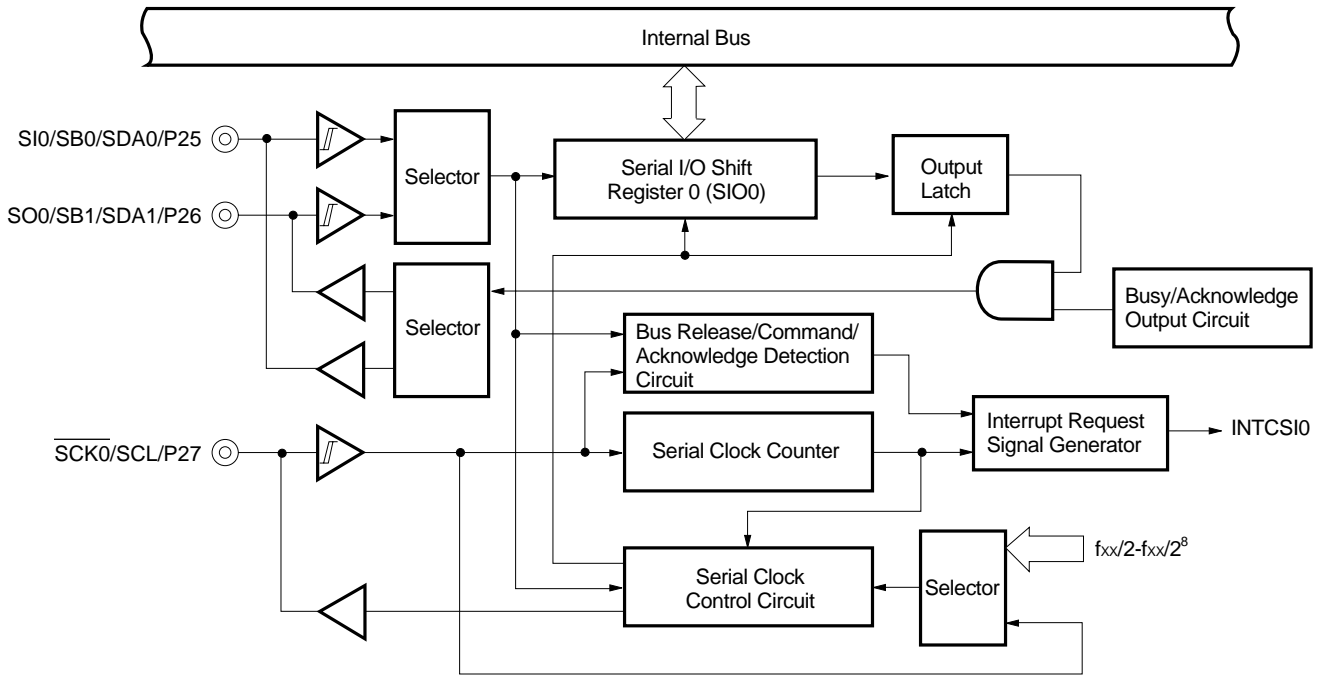
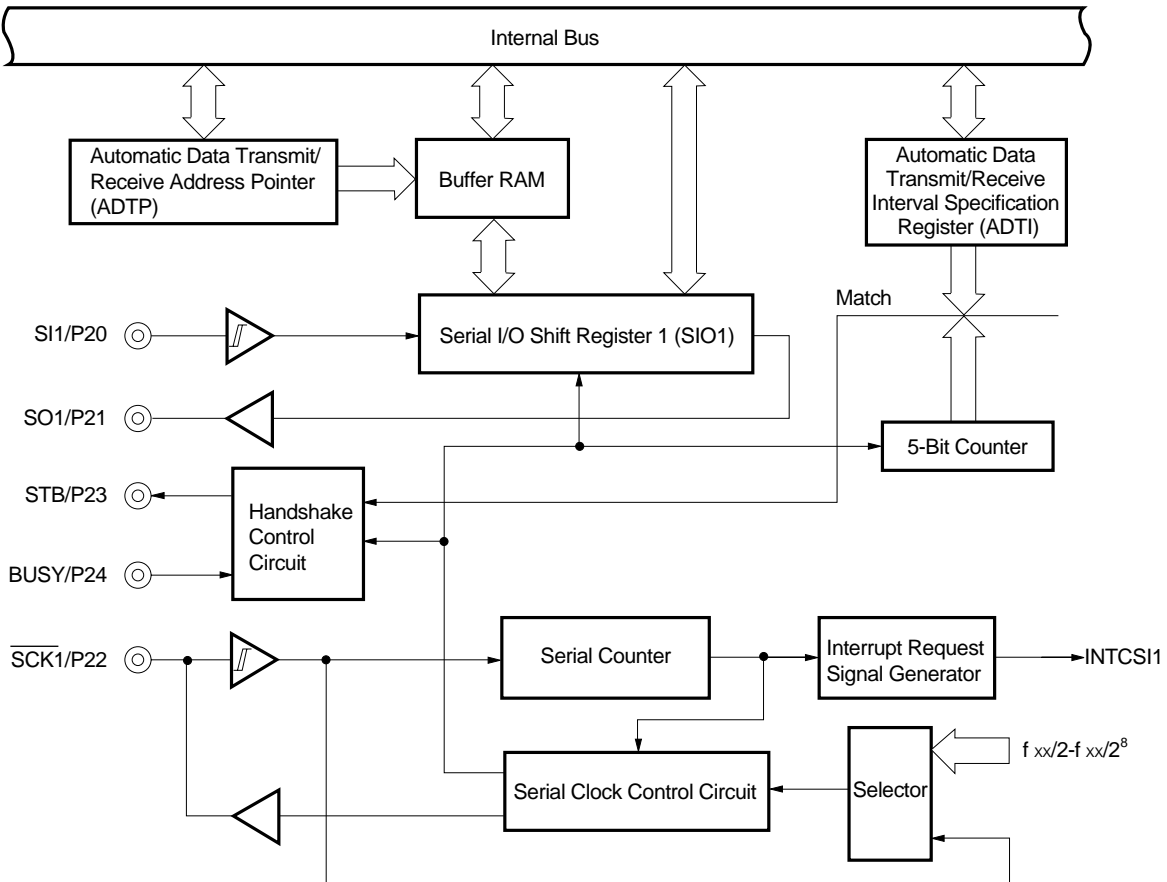
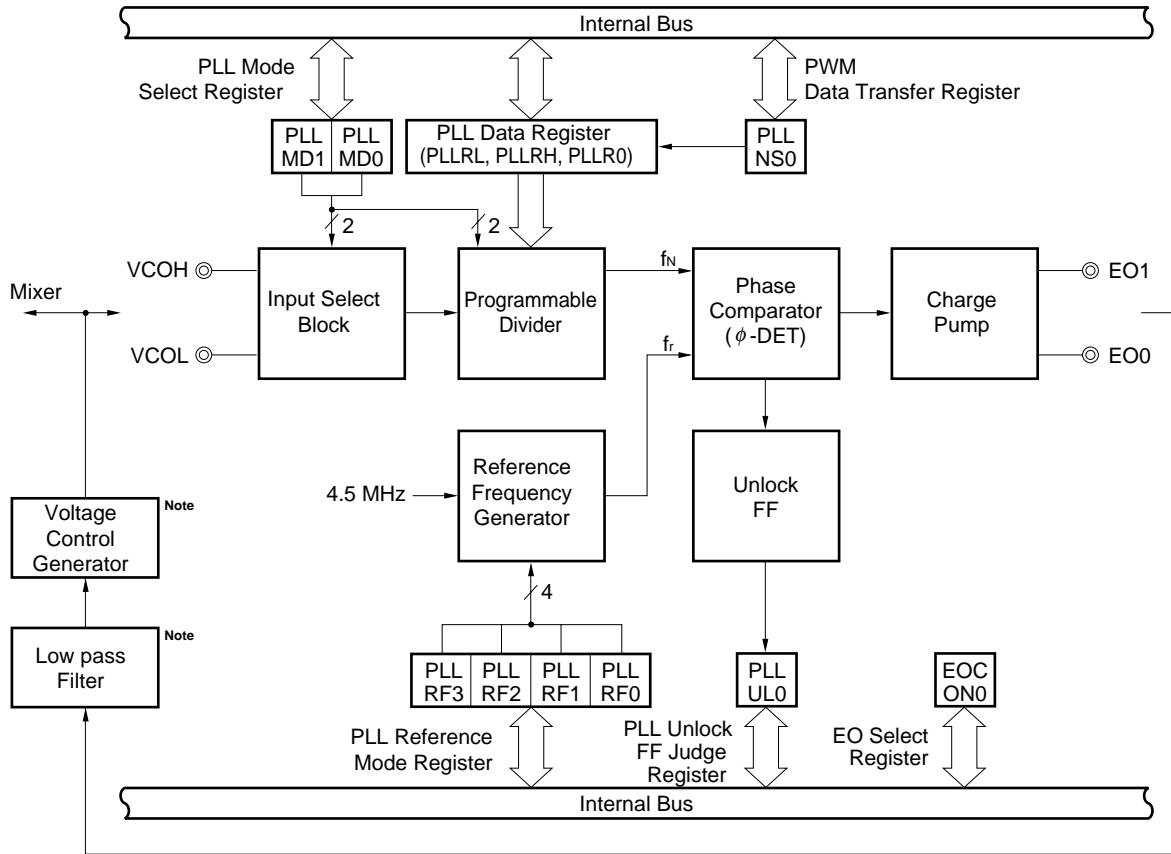


Figure 5-9. Serial Interface Channel 1 Block Diagram



5.7 PLL FREQUENCY SYNTHESIZER

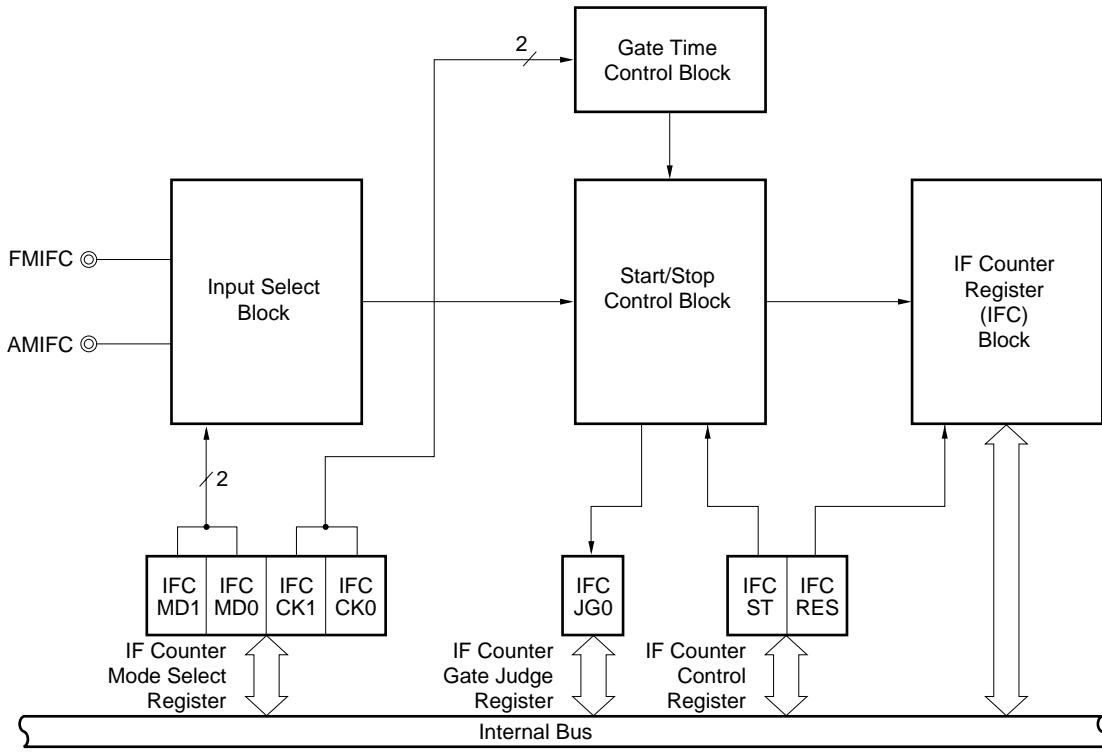
Figure 5-10. PLL Frequency Synthesizer Block Diagram



**Note** External circuit

5.8 FREQUENCY COUNTER

Figure 5-11. Frequency Counter Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are 17 interrupt functions of three different kinds, as shown below.

- Non-maskable interrupt : 1
- Maskable interrupt : 15
- Software interrupt : 1

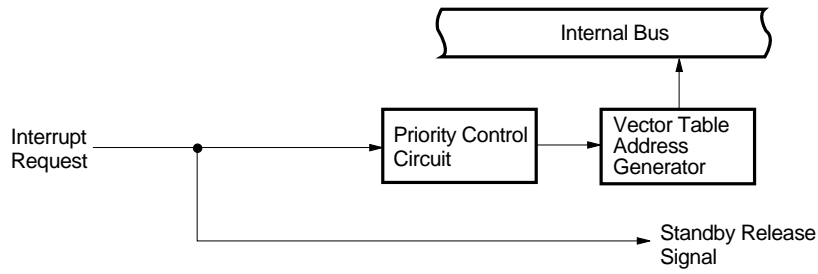
Table 6-1. Interrupt Source List

Interrupt Type	Note 1 Default Priority	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type <sup>Note 2</sup>		
		Name	Trigger					
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)		
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			External	0006H 0008H 000AH 000CH 000EH 0010H 0012H	(B)
	1	INTP0	Pin input edge detection	Internal	0014H 0016H 0018H 001AH 001CH 001EH 0020H			(C)
	2	INTP1						(D)
	3	INTP2						
	4	INTP3						
	5	INTP4						
	6	INTP5						
	7	INTP6						
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H 0016H 0018H 001AH 001CH 001EH 0020H			
	9	INTCSI1	End of serial interface channel 1 transfer					
	10	INTTMC	Generation of match signal of basic timer					
	11	INTPWM	Generation of match signal of 8-bit timer					
	12	INTTM1	Generation of match signal of 8-bit timer/ event counter 1					
	13	INTTM2	Generation of match signal of 8-bit timer/ event counter 2					
14	INTAD	End of conversion by A/D converter						
Software	—	BRK	BRK instruction execution	Internal	003EH	(E)		

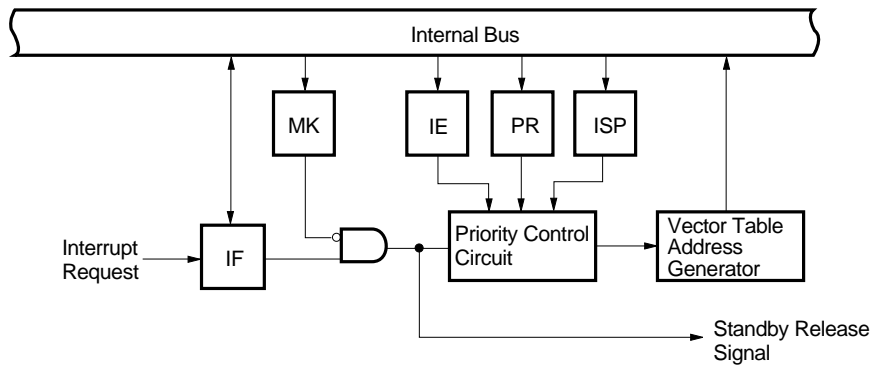
- Notes**
1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 14, the lowest.
  2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration(1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

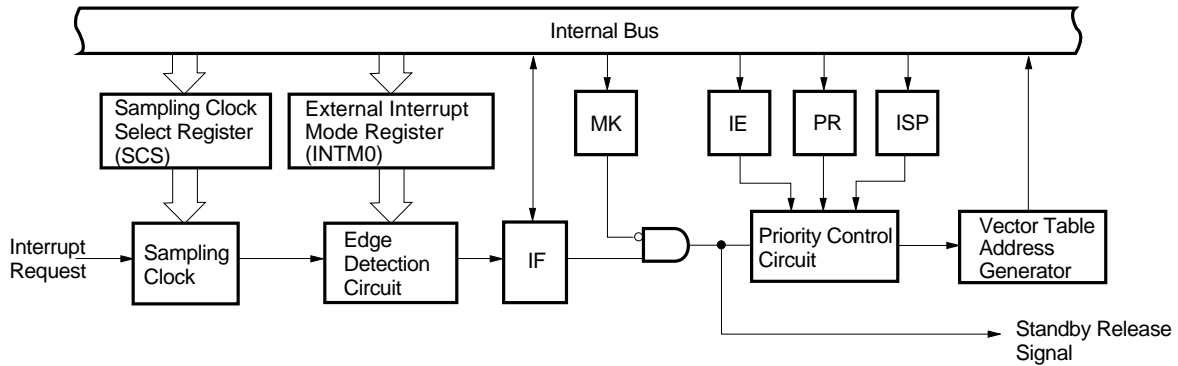
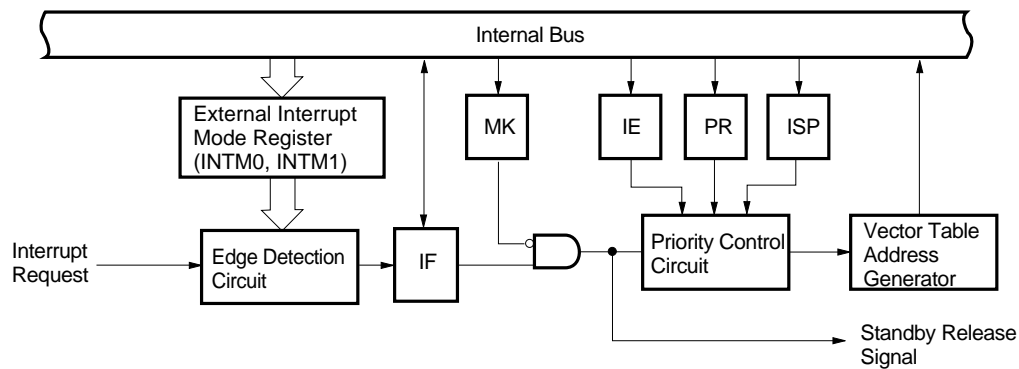


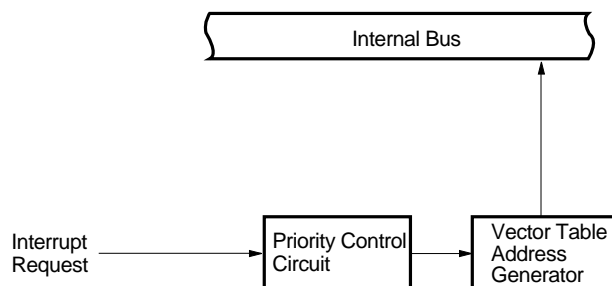


Figure 6-1. Interrupt Function Basic Configuration(2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

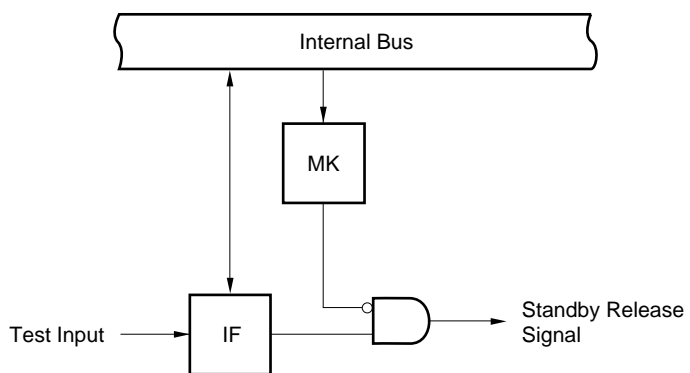
6.2 TEST FUNCTIONS

There is a test function as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag

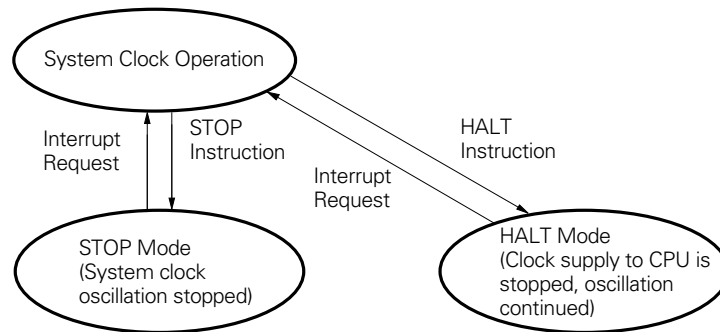
MK : Test mask flag

## 7. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.  
The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The system clock oscillation is stopped. All operations by the system clock are stopped and current consumption can be considerably reduced.

Figure 7-1. Stand-by Function



## 8. RESET FUNCTION

There are the following three reset methods.

- External reset input by  $\overline{\text{RESET}}$  pin
- Internal reset by watchdog timer runaway time detection
- Internal reset by Power-On Clear (POC).

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand First Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B,C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

**(2) 16-bit instructions**

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second Operand First Operand	#word	AX	rp <sup>Note</sup>	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW <sup>Note</sup>						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

**Note** Only when rp = BC, DE or HL

**(3) Bit manipulation instructions**

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

**(4) Call instruction/branch instructions**

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second Operand First Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

**(5) Other instructions**

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Parameter	Symbol	Test Conditions		Rating	Unit
Power supply voltage	V <sub>DD</sub>			-0.3 to + 7.0	V
Input voltage	V <sub>I1</sub>	Excluding P60 to P63		-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>I2</sub>	P60 to P63	N-ch Open-drain	-0.3 to +16	V
Output voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> + 0.3	V
Output withstand voltage	V <sub>BDS</sub>	P132 to P134	N-ch Open-drain	16	V
Analog input voltage	V <sub>AN</sub>	P10 to P15	Analog input pin	-0.3 to V <sub>DD</sub> + 0.3	V
Output current high	I <sub>OH</sub>	1 pin		-10	mA
		P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P125 total		-15	mA
		P10 to P15, P20 to P27, P40 to P47, P50 to P55, P132 to P134 total		-15	mA
Output current low	I <sub>OL</sub> <b>Note</b>	1 pin	Peak value	15	mA
			Effective value	7.5	mA
Operating ambient temperature	T <sub>A</sub>			-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Note** Effective value should be calculated as follows: [Effective value] = [Peak value] × √duty

**Caution** Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED SUPPLY VOLTAGE RANGES (T<sub>A</sub> = -40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V <sub>DD1</sub>	During CPU operation and PLL operation.	4.5		5.5	V
	V <sub>DD2</sub>	While the CPU is operating and the PLL is stopped. Cycle Time: T <sub>CY</sub> ≥ 0.89 μs	3.5		5.5	V
	V <sub>DD3</sub>	While the CPU is operating and the PLL is stopped. Cycle Time: T <sub>CY</sub> = 0.44 μs	4.5		5.5	V

**Remark** T<sub>CY</sub>: Cycle Time (Minimum instruction execution time)

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.5 to 5.5 V)

(1/3)

\*

\*

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage high	V <sub>IH1</sub>	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125	0.7 V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH2</sub>	P00 to P06, P20, P22, P24 to P27, P33, P34, RESET	0.85 V <sub>DD</sub>		V <sub>DD</sub>	V	
	V <sub>IH3</sub>	P60 to P63 (N-ch Open-drain)	0.7 V <sub>DD</sub>		15	V	
Input voltage low	V <sub>IL1</sub>	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125	0		0.3 V <sub>DD</sub>	V	
	V <sub>IL2</sub>	P00 to P06, P20, P22, P24 to P27, P33, P34, RESET	0		0.15 V <sub>DD</sub>	V	
	V <sub>IL3</sub>	P60 to P63 (N-ch Open-drain)	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.3 V <sub>DD</sub>	V
			3.5 V ≤ V <sub>DD</sub> < 4.5 V	0		0.2 V <sub>DD</sub>	V
Output voltage high	V <sub>OH1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 1.0			V	
		3.5 V ≤ V <sub>DD</sub> < 4.5 V I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.5			V	
Output voltage low	V <sub>OL1</sub>	P50 to P57, P60 to P63	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OH</sub> = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P120 to P125, P132 to P134	V <sub>DD</sub> = 4.5 to 5.5 V, I <sub>OL</sub> = 1.6 mA			0.4	V
	V <sub>OL2</sub>	SB0, SB1, SCK0	V <sub>DD</sub> = 4.5 to 5.5 V, open-drain pulled-up (R = 1 KΩ)			0.2 V <sub>DD</sub>	V

**Remark** The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

DC CHARACTERISTICS (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.5 to 5.5 V)

(2/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I <sub>LIH1</sub>	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, <u>RESET</u>	V <sub>IN</sub> = V <sub>DD</sub>			3	μA
	I <sub>LIH2</sub>	P60 to P63	V <sub>IN</sub> = 15 V			80	μA
Input leakage current low	I <sub>LIL1</sub>	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, <u>RESET</u>	V <sub>IN</sub> = 0 V			-3	μA
	I <sub>LIL2</sub>	P60 to P63				-3 <sup>Note</sup>	μA
Output leakage current high	I <sub>LOH</sub>	P132 to P134	V <sub>OUT</sub> = 15 V			3	μA
Output leakage current low	I <sub>LOL</sub>	P132 to P134	V <sub>OUT</sub> = 0 V			-3	μA
Output off leak current	I <sub>LOF</sub>	EO0, EO1	V <sub>OUT</sub> = V <sub>DD</sub> , V <sub>OUT</sub> = 0 V			±1	μA

**Note** When an input instruction is executed, the low-level input leakage current for P60 to P63 becomes -200 μA (MAX.) only in one clock cycle (at no wait). It remains at -3 μA (MAX.) for other than an input instruction.

**Remark** The characteristics of an alternate function pin and a port pin are the same unless specified otherwise.

\* REFERENCE CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>DD</sub> = 5 V)

(1/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output current high	I <sub>OH1</sub>	EO0	V <sub>OUT</sub> = V <sub>DD</sub> -1 V		-4		mA
		EO1 (EOCON0 = 1)			-6		mA
		EO1 (EOCON0 = 0)			-2		mA
Output current low	I <sub>OL1</sub>	EO0	V <sub>OUT</sub> = 1 V		6		mA
		EO1 (EOCON0 = 1)			8		mA
		EO1 (EOCON0 = 0)			3		mA



**DC CHARACTERISTICS** (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.5 to 5.5 V)

(3/3)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Power Supply <sup>Note 1</sup> Current	I <sub>DD1</sub>	While the CPU is operating and the PLL is stopped		2.5	15	mA	
	I <sub>DD2</sub>	f <sub>X</sub> = 4.5 MHz operation		4.0	27	mA	
	I <sub>DD3</sub>	While the CPU is operating and the PLL is stopped HALT Mode		0.7	1.5	mA	
	I <sub>DD4</sub>	Pin X1 sine wave input V <sub>IN</sub> = V <sub>DD</sub> . f <sub>X</sub> = 4.5 MHz operation		1.0	2.0	mA	
Data Hold Power Supply Voltage	V <sub>DR1</sub>	When the crystal is oscillating		4.5		5.5	V
	V <sub>DR2</sub>			3.5		5.5	V
	V <sub>DR3</sub>	When the crystal oscillator is stopped When power off by Power On Clear is detected		2.6		5.5	V
Data Hold Power Supply Current	I <sub>DR1</sub>	While the crystal oscillator is stopped		2	4	μA	
	I <sub>DR2</sub>			2	30	μA	

**Notes** 1. The port current is not included.

2. When the Processor Clock Control register (PCC) is set at 00H, and the Oscillation Mode Select register (OSMS) is set at 00H.

3. When PCC is set at 00H and OSMS is set at 01H.

**Remarks** 1. T<sub>CY</sub>: Cycle Time (Minimum instruction execution time)

2. f<sub>X</sub>: System clock oscillator frequency.

**REFERENCE CHARACTERISTICS** (T<sub>A</sub> = 25°C, V<sub>DD</sub> = 5 V)

(2/2)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Current	I <sub>DD5</sub>	During CPU operation and PLL operation. VCOH pin sine wave input f <sub>IN</sub> = 130 MHz, V <sub>IN</sub> = 0.15 V <sub>P-P</sub>		7		mA

**Note** When the Processor Clock Control register (PCC) is set at 00H, and the Oscillation Mode Select register (OSMS) is set at 01H.

**Remark** T<sub>CY</sub>: Cycle Time (Minimum instruction execution time)

AC CHARACTERISTICS

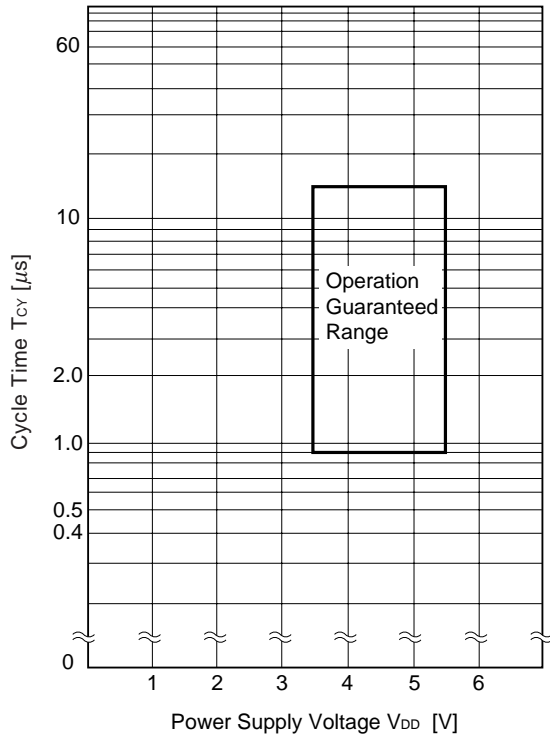
(1) BASIC OPERATION (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T <sub>CY</sub>	f <sub>XX</sub> = f <sub>X</sub> /2 <sup>Note 1</sup> , f <sub>X</sub> = 4.5 MHz operation	0.89		14.22	μs
		f <sub>XX</sub> = f <sub>X</sub> <sup>Note 2</sup> , f <sub>X</sub> = 4.5 MHz operation	4.5 ≤ V <sub>DD</sub> ≤ 5.5 V	0.44	7.11	μs
			3.5 ≤ V <sub>DD</sub> < 4.5 V	0.89	7.11	μs
T11, T12 input frequency	f <sub>TI</sub>	4.5 ≤ V <sub>DD</sub> ≤ 5.5 V	0		4.5	MHz
		3.5 V ≤ V <sub>DD</sub> ≤ 4.5 V	0		275	kHz
T11, T12 input high/ low-level width	t <sub>TIH</sub> ,	4.5 ≤ V <sub>DD</sub> ≤ 5.5 V	111			ns
	t <sub>TIL</sub>	3.5 V ≤ V <sub>DD</sub> ≤ 4.5 V	1.8			μs
Interrupt input high/ low-level width	T <sub>INTH</sub> ,	INTP0	8/f <sub>sam</sub> <sup>Note 3</sup>			μs
	T <sub>INTL</sub>					
RESET low level width	t <sub>RSL</sub>		10			μs

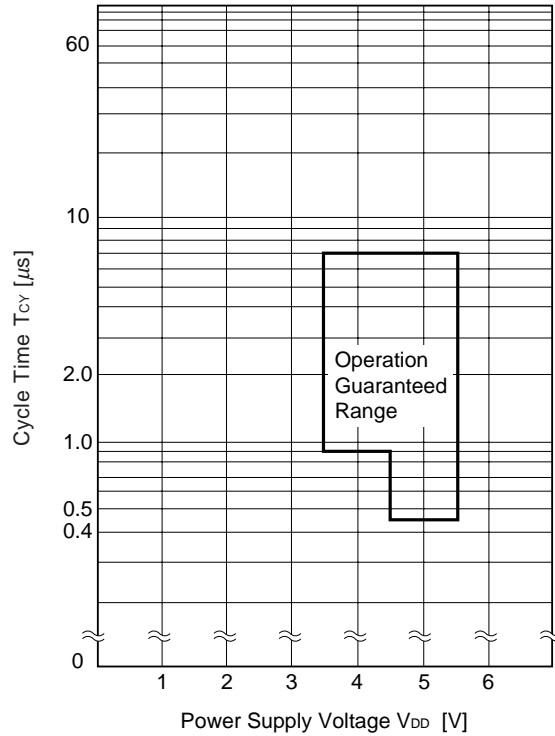
- Notes**
1. When oscillation mode selection (OSMS) register is set at 00H.
  2. When OSMS is set at 01H.
  3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f<sub>sam</sub> is possible between f<sub>XX</sub>/2<sup>N</sup>, f<sub>XX</sub>/32, f<sub>XX</sub>/64 and f<sub>XX</sub>/128 (when N = 0 to 4).

- Remarks**
1. f<sub>XX</sub>: System clock frequency (f<sub>X</sub> or f<sub>X</sub>/2)
  2. f<sub>X</sub>: System clock oscillation frequency

T<sub>CY</sub> vs V<sub>DD</sub> (At F<sub>XX</sub> = F<sub>X</sub>/2 system clock operation)



T<sub>CY</sub> vs V<sub>DD</sub> (At F<sub>XX</sub> = F<sub>X</sub> system clock operation)



(2) SERIAL INTERFACE (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.5 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		3.5 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
$\overline{\text{SCK0}}$ high-/low-level width	t <sub>KH1</sub> ,	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	t <sub>KCY1</sub> /2 - 50			ns
	t <sub>KL1</sub>	3.5 V ≤ V <sub>DD</sub> < 4.5 V	t <sub>KCY1</sub> /2 - 100			ns
SI0 setup time (to $\overline{\text{SCK0}}\uparrow$ )	t <sub>SIK1</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	100			ns
		3.5 V ≤ V <sub>DD</sub> < 4.5 V	150			ns
SI0 hold time (from $\overline{\text{SCK0}}\uparrow$ )	t <sub>KSI1</sub>		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t <sub>KSO1</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the load capacitance of SO0 output line.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t <sub>KCY2</sub>	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		3.5 V ≤ V <sub>DD</sub> < 4.5 V	1600			ns
$\overline{\text{SCK0}}$ high-/low-level width	t <sub>KH2</sub> ,	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	400			ns
	t <sub>KL2</sub>	3.5 V ≤ V <sub>DD</sub> < 4.5 V	800			ns
SI0 setup time (to $\overline{\text{SCK0}}\uparrow$ )	t <sub>SIK2</sub>		100			ns
SI0 hold time (from $\overline{\text{SCK0}}\uparrow$ )	t <sub>KSI2</sub>		400			ns
SO0 output delay time from $\overline{\text{SCK0}}\downarrow$	t <sub>KSO2</sub>	C = 100 pF <sup>Note</sup>			300	ns
$\overline{\text{SCK0}}$ at rising or falling edge time	t <sub>R2</sub> , t <sub>F2</sub>				1000	ns

**Note** C is the load capacitance of SO0 output line.

(iii) SBI mode ( $\overline{\text{SCK0}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY3}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH3}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY3}}/2 - 50$			ns
	$t_{\text{KL3}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	$t_{\text{KCY3}}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{SIK3}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{KSI3}}$		$t_{\text{KCY3}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	$t_{\text{KSO3}}$	$R = 1 \text{ k}\Omega$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	0	250	ns
		$C = 100 \text{ pF}^{\text{Note}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	0	1000	ns
SB0, SB1 $\downarrow$ from $\overline{\text{SCK0}}\uparrow$	$t_{\text{KSB}}$		$t_{\text{KCY3}}$			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1 $\downarrow$	$t_{\text{SBK}}$		$t_{\text{KCY3}}$			ns
SB0, SB1 high-level width	$t_{\text{SBH}}$		$t_{\text{KCY3}}$			ns
SB0, SB1 low-level width	$t_{\text{SBL}}$		$t_{\text{KCY3}}$			ns

**Note** R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(iv) SBI mode ( $\overline{\text{SCK0}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY4}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	3200			ns
$\overline{\text{SCK0}}$ high-/low-level width	$t_{\text{KH4}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
	$t_{\text{KL4}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{SIK4}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{KSI4}}$		$t_{\text{KCY4}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	$t_{\text{KSO4}}$	$R = 1 \text{ k}\Omega$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	0	300	ns
		$C = 100 \text{ pF}^{\text{Note}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	0	1000	ns
SB0, SB1 $\downarrow$ from $\overline{\text{SCK0}}\uparrow$	$t_{\text{KSB}}$		$t_{\text{KCY4}}$			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1 $\downarrow$	$t_{\text{SBK}}$		$t_{\text{KCY4}}$			ns
SB0, SB1 high-level width	$t_{\text{SBH}}$		$t_{\text{KCY4}}$			ns
SB0, SB1 low-level width	$t_{\text{SBL}}$		$t_{\text{KCY4}}$			ns
$\overline{\text{SCK0}}$ at rising or falling edge time	$t_{\text{R4}}, t_{\text{F4}}$				1000	ns

**Note** R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(v) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY5}}$	$R = 1 \text{ k}\Omega$	1600			ns
$\overline{\text{SCK0}}$ high-level width	$t_{\text{KH5}}$	$C = 100 \text{ pF}^{\text{Note}}$	$t_{\text{KCY5}}/2 - 160$			ns
$\overline{\text{SCK0}}$ low-level width	$t_{\text{KL5}}$		$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY5}}/2 - 50$		
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{SIK5}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	$t_{\text{KCY5}}/2 - 100$			ns
		$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{KSI5}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	350			ns
			400			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	$t_{\text{KSO5}}$		0		300	ns

**Note** R and C are the load resistance and load capacitance of  $\overline{\text{SCK0}}$ , SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ( $\overline{\text{SCK0}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
$\overline{\text{SCK0}}$ cycle time	$t_{\text{KCY6}}$		1600			ns	
$\overline{\text{SCK0}}$ high-level width	$t_{\text{KH6}}$		650			ns	
$\overline{\text{SCK0}}$ low-level width	$t_{\text{KL6}}$		800			ns	
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{SIK6}}$		100			ns	
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$ )	$t_{\text{KSI6}}$		$t_{\text{KCY6}}/2$			ns	
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	$t_{\text{KSO6}}$	$R = 1 \text{ k}\Omega$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	0		300	ns
		$C = 100 \text{ pF}^{\text{Note}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	0		500	ns
$\overline{\text{SCK0}}$ at rising or falling edge time	$t_{\text{r6}}, t_{\text{f6}}$				1000	ns	

**Note** R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(vii) I<sup>2</sup>C Bus mode (SCL ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t <sub>KCY7</sub>	R = 1 kΩ C = 100 pF <sup>Note</sup>		10			μs
SCL high-level width	t <sub>KH7</sub>			t <sub>KCY7</sub> - 160			ns
SCL low-level width	t <sub>KL7</sub>			t <sub>KCY7</sub> - 50			ns
SDA0, SDA1 setup time (to SCL↑)	t <sub>SIK7</sub>			200			ns
SDA0, SDA1 hold time (from SCL↓)	t <sub>SI7</sub>			0			ns
SDA0, SDA1 output delay time (from SCL↓)	t <sub>KSO7</sub>		4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		300	ns
			3.5 V ≤ V <sub>DD</sub> < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t <sub>KSB</sub>			200			ns
SCL↓ from SDA0, SDA1↓	t <sub>SBK</sub>			400			ns
SDA0, SDA1 high-level width	t <sub>SBH</sub>			500			ns

**Note** R and C are the load resistance and load capacitance of SCL, SDA0 and SDA1 output line.

(viii) I<sup>2</sup>C Bus mode (SCL ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t <sub>KCY8</sub>			1000			ns
SCL high-/low-level width	t <sub>KH8</sub> , t <sub>KL8</sub>			400			ns
SDA0, SDA1 setup time (to SCL↑)	t <sub>SIK8</sub>			200			ns
SDA0, SDA1 hold time (from SCL↓)	t <sub>SI8</sub>			0			ns
SDA0, SDA1 output delay time from SCL↓	t <sub>KSO8</sub>	R = 1 kΩ	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		300	ns
		C = 100 pF <sup>Note</sup>	3.5 V ≤ V <sub>DD</sub> < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t <sub>KSB</sub>			200			ns
SCL↓ from SDA0, SDA1↓	t <sub>SBK</sub>			400			ns
SDA0, SDA1 high-level width	t <sub>SBH</sub>			500			ns
SCL at rising or falling edge time	t <sub>r8</sub> , t <sub>f8</sub>					1000	ns

**Note** R and C are the load resistance and load capacitance of SDA0 and SDA1 output line.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ( $\overline{\text{SCK1}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY9}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH9}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY9}}/2 - 50$			ns
	$t_{\text{KL9}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	$t_{\text{KCY9}}/2 - 100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{SIK9}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{KSI9}}$		400			ns
SO1 output delay time (from $\overline{\text{SCK1}}\downarrow$ )	$t_{\text{KSO9}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

**Note** C is the load capacitance of SO1 output line.

(ii) 3-wire serial I/O mode ( $\overline{\text{SCK1}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY10}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH10}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
	$t_{\text{KL10}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{SIK10}}$		100			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{KSI10}}$		400			ns
SO1 output delay time (from $\overline{\text{SCK1}}\downarrow$ )	$t_{\text{KSO10}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
$\overline{\text{SCK1}}$ at rising or falling edge time	$t_{\text{R10}}, t_{\text{F10}}$				1000	ns

**Note** C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ( $\overline{\text{SCK1}}$  ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY11}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH11}},$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	$t_{\text{KCY11}}/2 - 50$			ns
	$t_{\text{KL11}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	$t_{\text{KCY11}}/2 - 100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{SIK11}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{KSI11}}$		400			ns
SO1 output delay time (from $\overline{\text{SCK1}}\downarrow$ )	$t_{\text{KSO11}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
STB $\uparrow$ from $\overline{\text{SCK1}}\uparrow$	$t_{\text{SBD}}$		$t_{\text{KCY11}}/2 - 100$		$t_{\text{KCY11}}/2 + 100$	ns
Strobe signal high-level width	$t_{\text{SBW}}$		$t_{\text{KCY11}}/ - 30$		$t_{\text{KCY11}} + 30$	ns
Busy signal setup time (to busy signal detection timing)	$t_{\text{BYS}}$		100			ns
Busy signal hold time (from busy signal detection timing)	$t_{\text{BYH}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	100			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
$\overline{\text{SCK1}}\downarrow$ from busy inactive	$t_{\text{SPS}}$				$2t_{\text{KCY11}}$	ns

**Note** C is the load capacitance of SO1 output line.

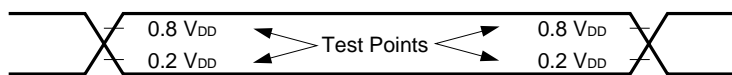
(iv) 3-wire serial I/O mode with automatic transmit/receive function ( $\overline{\text{SCK1}}$  ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	$t_{\text{KCY12}}$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	800			ns
		$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
$\overline{\text{SCK1}}$ high/low-level width	$t_{\text{KH12}},$	$4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	400			ns
	$t_{\text{KL12}}$	$3.5 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{SIK12}}$		100			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$ )	$t_{\text{KSI12}}$		400			ns
SO1 output delay time (from $\overline{\text{SCK1}}\downarrow$ )	$t_{\text{KSO12}}$	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
$\overline{\text{SCK1}}$ at rising or falling edge time	$t_{\text{R12}}, t_{\text{F12}}$				1000	ns

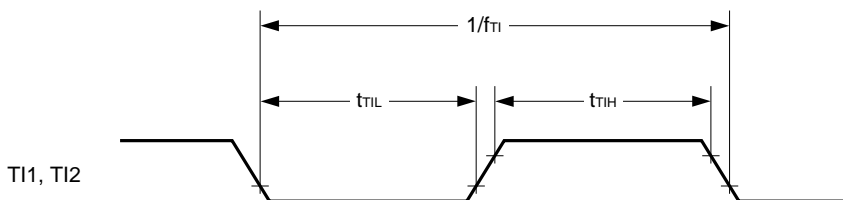
**Note** C is the load capacitance of SO1 output line.



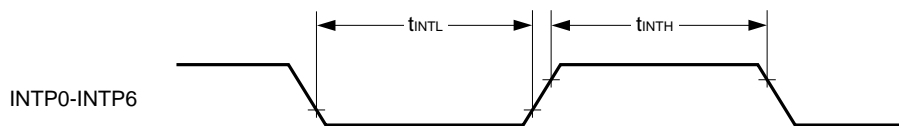
AC TIMING TEST POINT (EXCLUDING X1 INPUT)



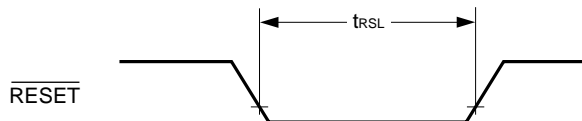
TI Timing



Interrupt Input Timing

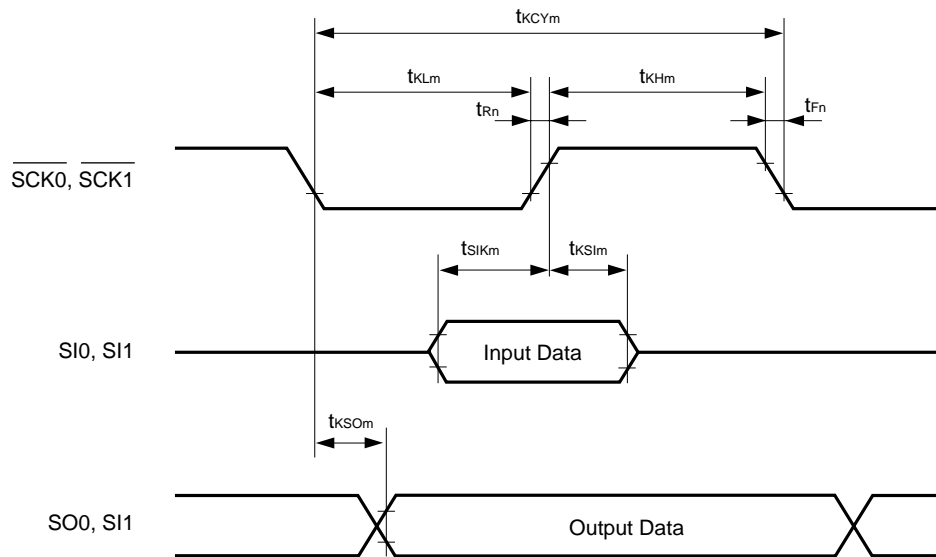


$\overline{\text{RESET}}$  Input Timing



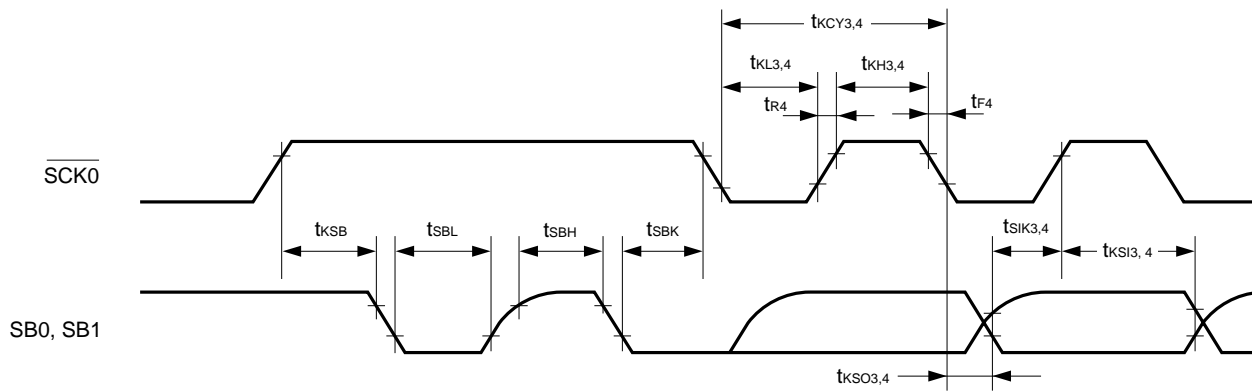
SERIAL TRANSFER TIMING

3-Wire Serial I/O Mode:

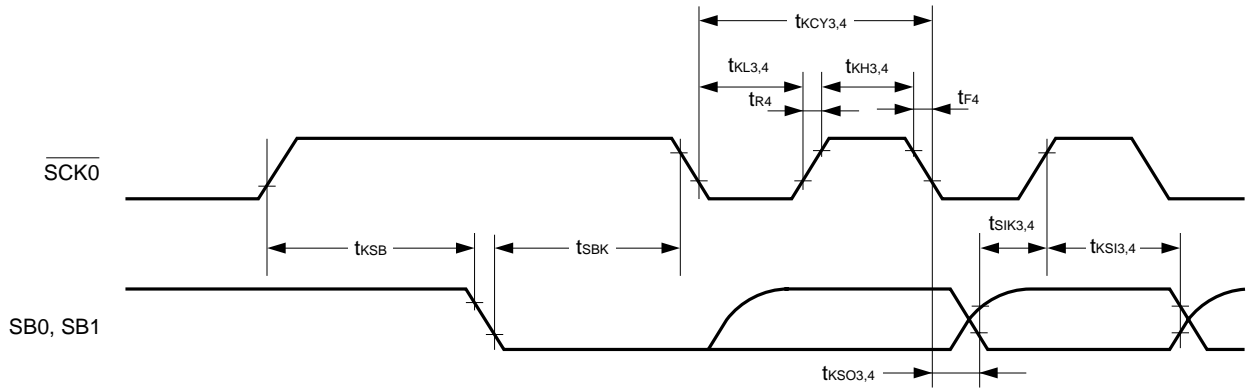


Remark  $m = 1, 2, 9, 10$   
 $n = 2, 10$

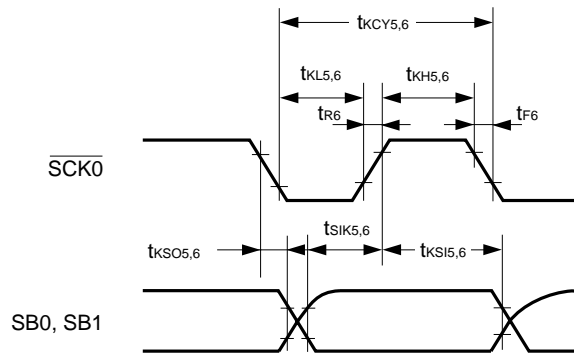
SBI Mode (Bus Release Signal Transfer):



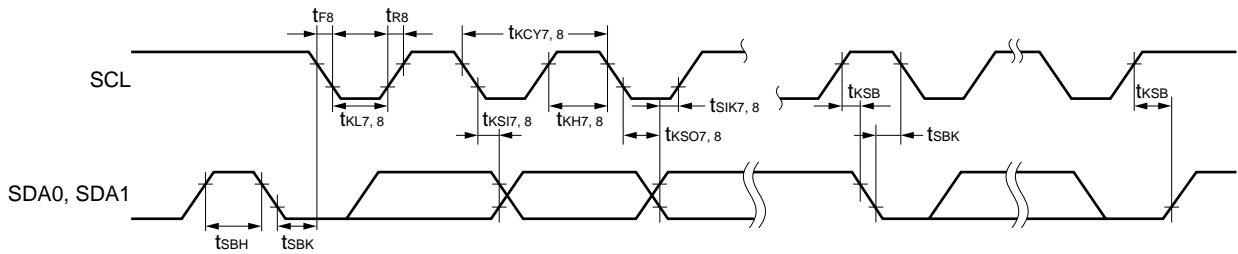
**SBI Mode (Command Signal Transfer):**



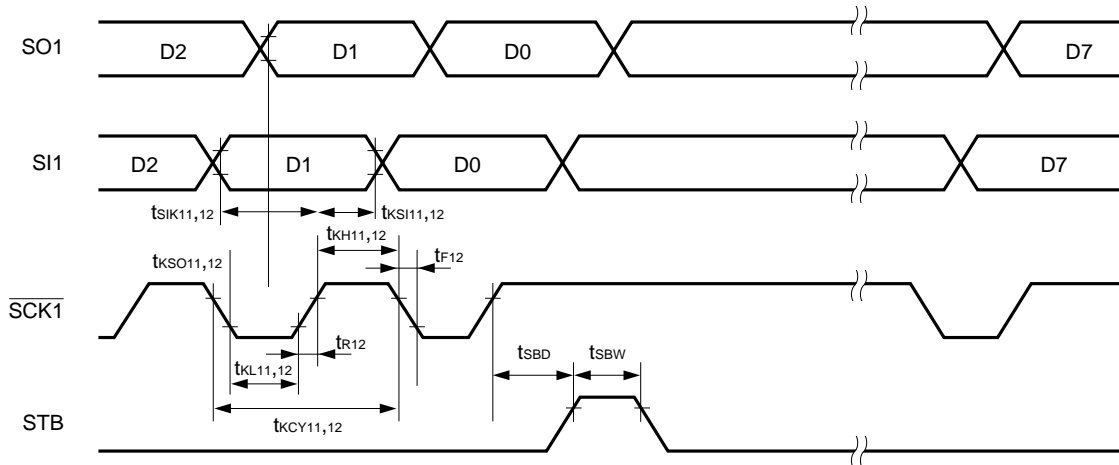
**2-Wire Serial I/O Mode:**



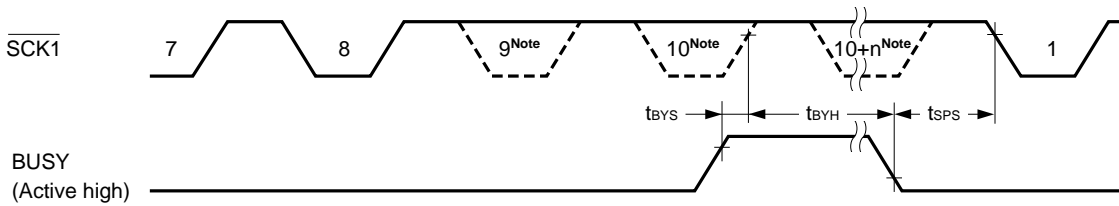
**I<sup>2</sup>C Bus Mode:**



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function:



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing):



**Note** The signal is not actually driven low here; it is shown as such to indicate the timing.

\* **A/D CONVERTER CHARACTERISTICS** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Conversion total error					±3.0	LSB
Conversion time	$t_{CONV}$		22.2		44.4	μs
Sampling time	$t_{SAMP}$		15/ $f_{XX}$			μs
Analog input voltage	$V_{IAN}$		0		$V_{DD}$	V

- \* **Remarks** 1.  $f_{XX}$ : System clock frequency ( $f_x/2$ )  
 2.  $f_x$ : System clock oscillation frequency

\* **PLL CHARACTERISTICS** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	$f_{IN1}$	VCOL Pin MF Mode Sine wave input $V_{IN} = 0.1 V_{p-p}$	0.5		3	MHz
	$f_{IN2}$	VCOL Pin HF Mode Sine wave input $V_{IN} = 0.2 V_{p-p}$	9		55	MHz
	$f_{IN3}$	VCOH Pin VHF Mode Sine wave input $V_{IN} = 0.15 V_{p-p}$	60		160	MHz

\*

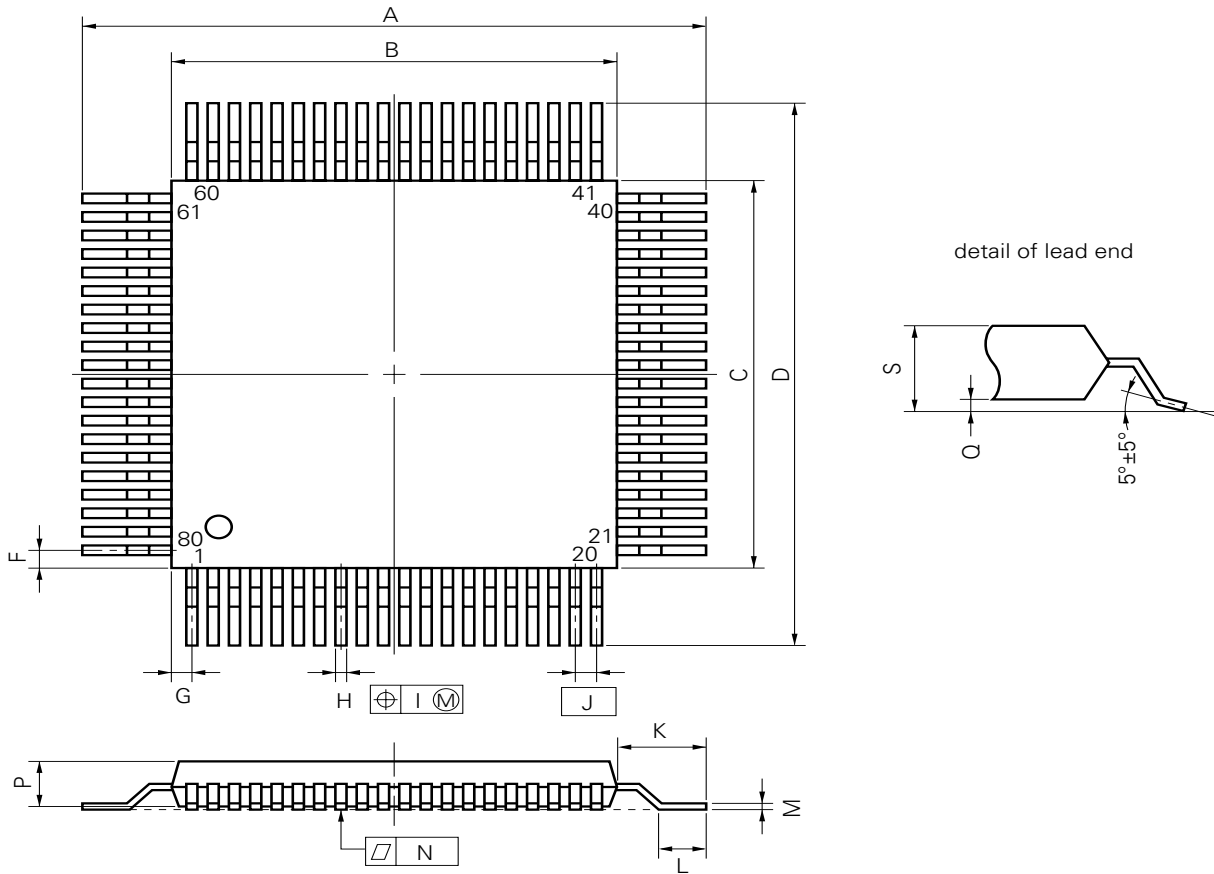
**IFC CHARACTERISTICS** ( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5$  V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	$f_{IN4}$	AMIFC Pin AMIF Count Mode Sine wave input $V_{IN} = 0.1 V_{p-p}$ <sup>Note</sup>	0.4		0.5	MHz
	$f_{IN5}$	FMIFC Pin FMIF Count Mode Sine wave input $V_{IN} = 0.1 V_{p-p}$ <sup>Note</sup>	10		11	MHz
	$f_{IN6}$	FMIFC Pin AMIF Count Mode Sine wave input $V_{IN} = 0.1 V_{p-p}$ <sup>Note</sup>	0.4		0.5	MHz

**Note** The condition of a sine wave input of  $V_{IN} = 0.1 V_{p-p}$  is the standard value for operation of this device during stand-alone operation, so in consideration of the effect of noise, it is recommended that operation be at an input amplitude condition of  $V_{IN} = 0.15 V_{p-p}$ .

11. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14 × 14)



**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S80GC-65-3B9-3

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

**12. RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document “**Semiconductor Device Mounting Technology Manual**” (C10535E).

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 12-1. Surface Mounting Type Soldering Conditions**

**μPD178004GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)**

**μPD178006GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)**

**μPD178016GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)**

**μPD178018GC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature : 260°C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per pin row)	—

**Caution Do not use different soldering method together (except for partial heating).**

**APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD178018 subseries.

**Language Processing Software**

RA78K/0 <sup>Notes 1, 2, 3, 4</sup>	78K/0 series common assembler package
CC78K/0 <sup>Notes 1, 2, 3, 4</sup>	78K/0 series common C compiler package
DF178018 <sup>Notes 1, 2, 3, 4</sup>	μPD178018 subseries common device file
CC78K/0-L <sup>Notes 1, 2, 3, 4</sup>	78K/0 series common C compiler library source file

**PROM Writing Tools**

PG-1500	PROM programmer
PG-178P018GC	Programmer adapters connected to a PG-1500
PA-178P018KK-T	
PG-1500 controller <sup>Notes 1, 2</sup>	PG-1500 control program

**Debugging Tools**

IE-78000-R	In-circuit emulator common to 78K/0 series
* IE-78000-R-A	In-circuit emulator common to 78K/0 series (for the integration debugger)
IE-78000-R-BK	Break board common to 78K/0 series
IE-178018-R-EM	Emulation board common to μPD178018 subseries
EP-78230GC-R	Emulation probe common to μPD78234 subseries
EV-9200GC-80	Socket for mounting on target system board created for 80-pin plastic QFP (GC-3B9 type)
EV-9900	Jig used when removing the μPD178P018KK-T from the EV-9200GC-80.
SM78K0 <sup>Notes 5, 6, 7</sup>	78K/0 series common system simulator
ID78K0 <sup>Notes 4, 5, 6, 7</sup>	Integration debugger for IE-78000-R-A
SD78K/0 <sup>Notes 1, 2</sup>	IE-78000-R screen debugger
DF178018 <sup>Notes 1, 2, 4, 5, 6, 7</sup>	μPD178018 subseries device file

**Real-Time OS**

RX78K/0 <sup>Notes 1, 2, 3, 4</sup>	78K/0 series real-time OS
MX78K0 <sup>Notes 1, 2, 3, 4</sup>	78K/0 series OS

- Notes**
1. PC-9800 series (MS-DOS™) based
  2. IBM PC/AT™ and compatible (PC DOS™/IBM-DOS™/MS-DOS) based
  3. HP9000 series 300™ based
  4. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™) based, EWS-4800 series (EWS-UX/V) based
  5. PC-9800 series (MS-DOS + Windows™) based
  6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
  7. NEWS™ (NEWS-OS™) based



**Fuzzy Inference Development Support System**

FE9000 <sup>Note 1</sup> /FE9200 <sup>Note 2</sup>	Fuzzy knowledge data creation tool
FT9080 <sup>Note 1</sup> /FT9085 <sup>Note 3</sup>	Translator
FI78K0 <sup>Notes 1, 3</sup>	Fuzzy inference module
FD78K0 <sup>Notes 1, 3</sup>	Fuzzy inference debugger

- Notes**
1. PC-9800 series (MS-DOS) based
  2. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
  3. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS) based

- Remarks**
1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.
  2. The RA78K/0, CC78K/0, SD78K/0, ID78K/0, SM78K/0 and RX78K/0 are used in combination with the DF178018.

## APPENDIX B. RELATED DOCUMENTS

## Device Documents

Title		Document No. (Japanese)	Document No. (English)
μPD178018 Subseries User's Manual		U11410J	U11410E
78K/0 Series User's Manual—Instruction		IEU-849	IEU-1372
78K/0 Series Instruction Set		U10904J	—
78K/0 Series Instruction Table		U10903J	—
μPD178018 Subseries Special Function Register Table		To be prepared	—
78K/0 Series Application Note	Basics (II)	U10121J	U10121E

## Development Tool Documents (User's Manual)

Title		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Notes	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		EEU-810	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-178018-R-EM		U10668J	U10668E
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	U11151E
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
* ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	—
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	EEU-1413

**Caution** The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

**Related Documents for Embedded Software (User's Manual)**

Title		Document No. (Japanese)	Document No. (English)
78K/0 Series Realtime OS	Basics	U11537J	—
	Installation	U11536J	—
	Technical	U11538J	—
78K/0 Series OS MX78K0	Basics	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System—Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System—Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System —Fuzzy Inference Debugger		EEU-921	EEU-1458

**Other Documents**

Title	Document No. (Japanese)	Document No. (English)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Guides on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	C11893J	MEI-1202
Microcomputer-related Product Guide (Products by other Manufacturers)	U11416J	—

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[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## Regional Information

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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