NEC

MOS INTEGRATED CIRCUIT

MC-22222361-X

MCP (MULTI-CHIP PACKAGE) FLASH MEMORY AND SRAM
64M-BIT PAGE MODE FLASH MEMORY AND 8M-BIT SRAM

Description

The MC-22222361-X is a stacked type MCP (Multi-Chip Package) of 67,108,864 bits (4,194,304 words by 16 bits) flash memory and 8,388,608 bits (524,288 words by 16 bits) static RAM.

The MC-22222361-X is packaged in a 85-pin TAPE FBGA .

Features

General Features

- Fast access time : t_{ACC} = 80 ns (MAX.) ($V_{CC}f$ = 1.8 V), 85 ns (MAX.) ($V_{CC}f$ = 1.65 V) (Flash Memory),
★ t_{AA} = 55 ns (MAX.) (SRAM)
- Supply voltage : -D80X : 1.8 to 2.1 V (Chip) / 2.7 to 3.1 V (I/O) (Flash Memory), 2.7 to 3.1 V (SRAM)
-E85X : 1.65 to 1.95 V (Chip) / 2.7 to 3.1 V (I/O) (Flash Memory), 2.7 to 3.1 V (SRAM)
- Output Enable input for easy application
- Wide operating temperature : T_A = –25 to +85°C

Flash Memory Features

- Four bank organization enabling simultaneous execution of program / erase and read
- High-speed read with page mode
- Bank organization : 4 banks (8M bits + 24M bits + 24M bits + 8M bits)
- Memory organization : 4,194,304 words × 16 bits
- Sector organization : 142 sectors (4K words × 16 sectors, 32K words × 126 sectors)
  Boot sector allocated to the highest address (sector) and the lowest address (sector)
- 3-state output
- Automatic program
  - Program suspend / resume
- Unlock bypass program
- Automatic erase
  - Chip erase
  - Sector erase (sectors can be combined freely)
  - Erase suspend / resume
- Program / Erase completion detection
  - Detection through data polling and toggle bits
  - Detection through RY (/BY) pin
- Sector group protection
  - Any sector group can be protected
  - Any protected sector group can be temporary unprotected
  - Any sector group can be unprotected
- Sectors can be used for boot application

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The mark ★ shows major revised points.

- Hardware reset and standby using /RESET pin
- Automatic sleep mode
- Boot block sector protect by /WP (ACC) pin
- Extra One Time Protect Sector provided
- Program / erase time
  - Program : 11.0 μs / word (TYP.)
  - Sector erase :

    Program / erase cycle : 100,000 cycles

    0.15 s (TYP.) (4K words sector), 0.5 s (TYP.) (32K words sector)

    Program / erase cycle : 300,000 cycles

    0.5 s (TYP.) (4K words sector), 0.7 s (TYP.) (32K words sector)
- Program / erase cycle : 300,000 cycles (MIN.)

SRAM Features

- Memory organization : 524,288 words $\times$ 16 bits
- Supply current : At operating : 30 mA (MAX.)

  At standby : 15 μA (MAX.)
- Two Chip Enable inputs : /CE1s, CE2s
- Byte data control : /LB, /UB
- Low V_{CC} data retention : 1.5 V (MIN.)

Ordering Information

	Part number	Flash Memory Access time ns (MAX.)	SRAM Access time ns (MAX.)	Operating supply voltage V		Package	Mounted Flash Memory
				Chip	I/O		
★	MC-22222361F9-D80X-CD5	80	55	1.8 to 2.1 (Flash Memory) 2.7 to 3.1 (SRAM)	2.7 to 3.1 (Flash Memory)	85-pin TAPE FBGA (11 $\times$ 8)	μPD29F064115-X
	MC-22222361F9-E85X-CD5	85		1.65 to 1.95 (Flash Memory) 2.7 to 3.1 (SRAM)			

Bus Operations, COMMANDS, HARDWARE SEQUENCE FLAGS, HARD WARE DATA PROTECTION, READ MODE REGISTER SETTINGS, TIMING CHARTS and **FLOW CHARTS** for Flash Memory, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E).**

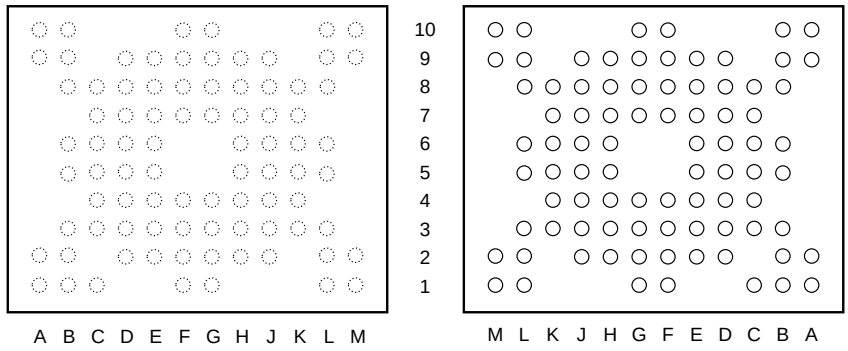
TIMING CHARTS OF SRAM FOR MCP, refer to **SRAM AND MOBILE SPECIFIED RAM TIMING CHARTS FOR MCP Information (M15819E).**

Pin Configuration

/xxx indicates active low signal.

85-pin TAPE FBGA (11 × 8)

Top View **Bottom View**



Top View

	A	B	C	D	E	F	G	H	J	K	L	M
10	NC	NC				NC	NC				NC	NC
9	NC	NC		A15	A21	NC	A16	V_{CCS}	Vss		NC	NC
8		NC	A11	A12	A13	A14	IC	I/O15	I/O7	I/O14	NC	
7			A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5		
6		NC	/WE	CE2s	A20			I/O4	V_{CCS}	$V_{CC}Qf$	NC	
5		NC	/WP(ACC)	/RESET	RY(/BY)			I/O3	$V_{CC}f$	I/O11	NC	
4			/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2		
3		NC	A7	A6	A5	A4	Vss	/OE	I/O0	I/O8	NC	
2	NC	NC		A3	A2	A1	A0	/CEf	/CE1s		NC	NC
1	NC	NC	NC			NC	NC				NC	NC

Common Pins

A0 to A18	:	Address Inputs
I/O0 to I/O15	:	Data Inputs / Outputs
/OE	:	Output Enable Input
/WE	:	Write Enable Input
V_{SS}	:	Ground
NC Note1	:	No Connection
IC Note2	:	Internal Connection

Flash Memory Pins

A19 to A21	:	Address Inputs
/CEf	:	Chip Enable Input
RY (/BY)	:	Ready (Busy) output
/RESET	:	Hardware reset Input
/WP(ACC)	:	Hardware Write Protect (Acceleration) Input
$V_{CC}f$	:	Supply Voltage
$V_{CC}Qf$	:	Input / Output Supply Voltage

SRAM Pins

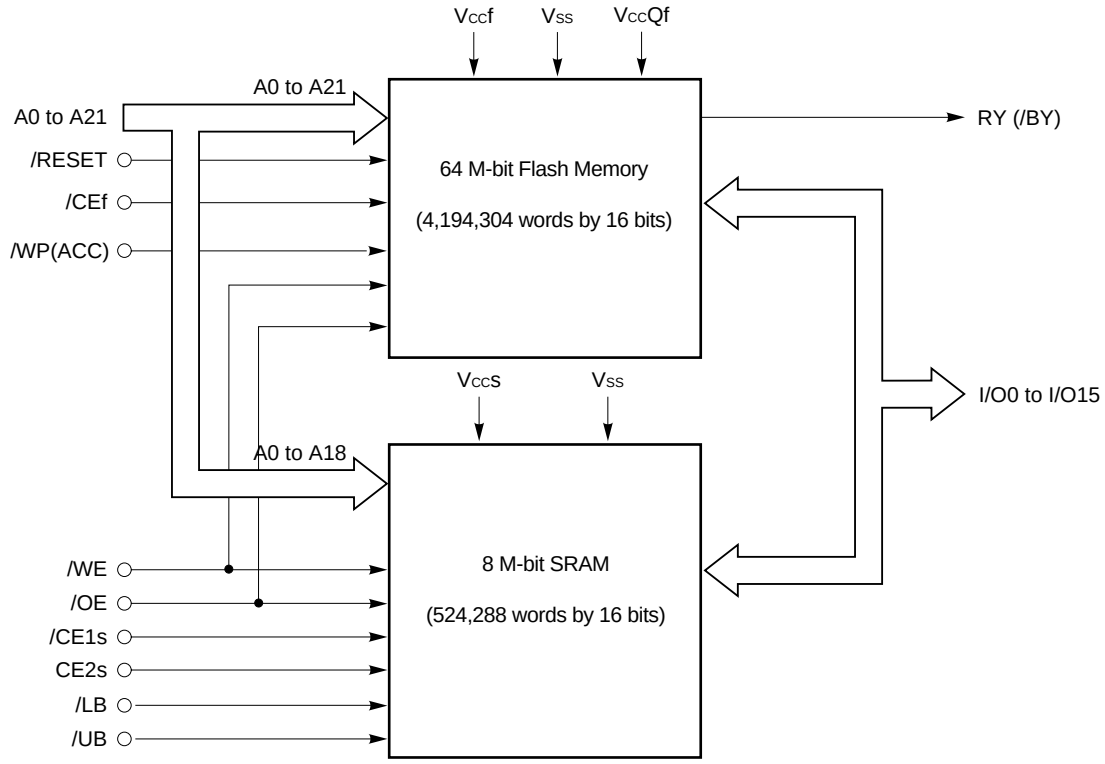
/CE1s	:	Chip Enable 1 Input
CE2s	:	Chip Enable 2 Input
/LB, /UB	:	Byte data select Input
V_{CCS}	:	Supply Voltage

Notes 1. Some signals can be applied because this pin is not internally connected.

2. Any level (Vss, Vccf, Open) can be applied. Do not change the state during operation.

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



Bus Operations

Operation		Flash Memory			SRAM				Common			
		/RESET	/CEf	/WP(ACC)	/CE1s	CE2s	/LB	/UB	/OE	/WE	I/O0 to I/O7	I/O8 to I/O15
Full Standby		H	H	×	H	×	×	×	×	×	High-Z	High-Z
					×	L						
					×	×	H	H				
Output Disable		H	L	×	L	H	×	×	H	H	High-Z	High-Z
Flash Memory												
Word Read [Note 1]		H	L	×	**Note 2**				L	H	Data Out	Data Out
Word Write		H	L	×	**Note 2**				H	L	Data In	Data In
Temporary Sector Group Unprotect		V_{ID}	×	×	**Note 2**				×	×	High-Z or Data In/Out	High-Z or Data In/Out
Automatic Sleep Mode		H	L	×	**Note 2**				L	H	Data Out	Data Out
Boot Block Sector Protect		×	×	L	×	×	×	×	×	×	High-Z or Data In/Out	High-Z or Data In/Out
Accelerated Mode		H	×	V_{ACC}	**Note 2**				×	×	High-Z or Data In/Out	High-Z or Data In/Out
Hardware Reset		L	×	×	×	×	×	×	×	×	High-Z	High-Z
SRAM												
Word Read		**Note 3**			L	H	L	L	L	H	Data Out	Data Out
	Lower byte read							H				High-Z
	Upper byte read						H	L			High-Z	Data Out
Word Write		**Note 3**			L	H	L	L	×	L	Data In	Data In
	Lower byte read							H				High-Z
	Upper byte read						H	L			High-Z	Data In

Caution Other operations except for indicated in this table are inhibited.

Notes 1. When /OE = V_{IL}, V_{IL} can be applied to /WE. When /OE = V_{IH}, a write operation is started. When /WE = V_{IL} and /OE = V_{IL}, a write operation is started.

2. SRAM should be Standby.

3. Flash Memory should be Standby or Hardware reset.

Remarks 1. × : V_{IH} or V_{IL}, H : V_{IH}, L : V_{IL}, V_{ID} : 9.0 to 11.0 V, V_{ACC} : 8.5 to 9.5 V

2. Sector group protection and read the product ID are using a command.

3. If an address is held longer than the minimum read cycle time (t_{RC}) in the flash memory read mode, the automatic sleep mode is set.

Sector Organization / Sector Address Table (Flash Memory)

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank D	4	3FFFFFH 3FF000H	SA141	1	1	1	1	1	1	1	1	1	1
	4	3FEFFFH 3FE000H	SA140	1	1	1	1	1	1	1	1	1	0
	4	3FDFFFH 3FD000H	SA139	1	1	1	1	1	1	1	1	0	1
	4	3FCFFFH 3FC000H	SA138	1	1	1	1	1	1	1	1	0	0
	4	3FBFFFH 3FB000H	SA137	1	1	1	1	1	1	1	0	1	1
	4	3FAFFFH 3FA000H	SA136	1	1	1	1	1	1	1	0	1	0
	4	3F9FFFH 3F9000H	SA135	1	1	1	1	1	1	1	0	0	1
	4	3F8FFFH 3F8000H	SA134	1	1	1	1	1	1	1	0	0	0
	32	3F7FFFH 3F0000H	SA133	1	1	1	1	1	1	0	x	x	x
	32	3EFFFFH 3E8000H	SA132	1	1	1	1	1	0	1	x	x	x
	32	3E7FFFH 3E0000H	SA131	1	1	1	1	1	0	0	x	x	x
	32	3DFFFFH 3D8000H	SA130	1	1	1	1	0	1	1	x	x	x
	32	3D7FFFH 3D0000H	SA129	1	1	1	1	0	1	0	x	x	x
	32	3CFFFFH 3C8000H	SA128	1	1	1	1	0	0	1	x	x	x
	32	3C7FFFH 3C0000H	SA127	1	1	1	1	0	0	0	x	x	x
	32	3B7FFFH 3B8000H	SA126	1	1	1	0	1	1	1	x	x	x
	32	3B7FFFH 3B0000H	SA125	1	1	1	0	1	1	0	x	x	x
	32	3AFFFFH 3A8000H	SA124	1	1	1	0	1	0	1	x	x	x
	32	3A7FFFH 3A0000H	SA123	1	1	1	0	1	0	0	x	x	x
	32	39FFFFH 398000H	SA122	1	1	1	0	0	1	1	x	x	x
	32	397FFFH 390000H	SA121	1	1	1	0	0	1	0	x	x	x
	32	38FFFFH 388000H	SA120	1	1	1	0	0	0	1	x	x	x
	32	387FFFH 380000H	SA119	1	1	1	0	0	0	0	x	x	x
Bank C	32	37FFFFH 378000H	SA118	1	1	0	1	1	1	1	x	x	x
	32	377FFFH 370000H	SA117	1	1	0	1	1	1	0	x	x	x
	32	36FFFFH 368000H	SA116	1	1	0	1	1	0	1	x	x	x
	32	367FFFH 360000H	SA115	1	1	0	1	1	0	0	x	x	x
	32	35FFFFH 358000H	SA114	1	1	0	1	0	1	1	x	x	x
	32	357FFFH 350000H	SA113	1	1	0	1	0	1	0	x	x	x
	32	34FFFFH 348000H	SA112	1	1	0	1	0	0	1	x	x	x
	32	347FFFH 340000H	SA111	1	1	0	1	0	0	0	x	x	x
	32	33FFFFH 338000H	SA110	1	1	0	0	1	1	1	x	x	x
	32	337FFFH 330000H	SA109	1	1	0	0	1	1	0	x	x	x
	32	32FFFFH 328000H	SA108	1	1	0	0	1	0	1	x	x	x
	32	327FFFH 320000H	SA107	1	1	0	0	1	0	0	x	x	x
	32	31FFFFH 318000H	SA106	1	1	0	0	0	1	1	x	x	x

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank C	32	317FFFH 310000H	SA105	1	1	0	0	0	1	0	x	x	x
	32	30FFFFH 308000H	SA104	1	1	0	0	0	0	1	x	x	x
	32	307FFFH 300000H	SA103	1	1	0	0	0	0	0	x	x	x
	32	2FFFFFH 2F8000H	SA102	1	0	1	1	1	1	1	x	x	x
	32	2F7FFFH 2F0000H	SA101	1	0	1	1	1	1	0	x	x	x
	32	2EFFFFH 2E8000H	SA100	1	0	1	1	1	0	1	x	x	x
	32	2E7FFFH 2E0000H	SA99	1	0	1	1	1	0	0	x	x	x
	32	2DFFFFH 2D8000H	SA98	1	0	1	1	0	1	1	x	x	x
	32	2D7FFFH 2D0000H	SA97	1	0	1	1	0	1	0	x	x	x
	32	2CFFFFH 2C8000H	SA96	1	0	1	1	0	0	1	x	x	x
	32	2C7FFFH 2C0000H	SA95	1	0	1	1	0	0	0	x	x	x
	32	2BFFFFH 2B8000H	SA94	1	0	1	0	1	1	1	x	x	x
	32	2B7FFFH 2B0000H	SA93	1	0	1	0	1	1	0	x	x	x
	32	2AFFFFH 2A8000H	SA92	1	0	1	0	1	0	1	x	x	x
	32	2A7FFFH 2A0000H	SA91	1	0	1	0	1	0	0	x	x	x
	32	29FFFFH 298000H	SA90	1	0	1	0	0	1	1	x	x	x
	32	297FFFH 290000H	SA89	1	0	1	0	0	1	0	x	x	x
	32	28FFFFH 288000H	SA88	1	0	1	0	0	0	1	x	x	x
	32	287FFFH 280000H	SA87	1	0	1	0	0	0	0	x	x	x
	32	27FFFFH 278000H	SA86	1	0	0	1	1	1	1	x	x	x
	32	277FFFH 270000H	SA85	1	0	0	1	1	1	0	x	x	x
	32	26FFFFH 268000H	SA84	1	0	0	1	1	0	1	x	x	x
	32	267FFFH 260000H	SA83	1	0	0	1	1	0	0	x	x	x
	32	25FFFFH 258000H	SA82	1	0	0	1	0	1	1	x	x	x
	32	257FFFH 250000H	SA81	1	0	0	1	0	1	0	x	x	x
	32	24FFFFH 248000H	SA80	1	0	0	1	0	0	1	x	x	x
	32	247FFFH 240000H	SA79	1	0	0	1	0	0	0	x	x	x
	32	23FFFFH 238000H	SA78	1	0	0	0	1	1	1	x	x	x
	32	237FFFH 230000H	SA77	1	0	0	0	1	1	0	x	x	x
	32	22FFFFH 228000H	SA76	1	0	0	0	1	0	1	x	x	x
	32	227FFFH 220000H	SA75	1	0	0	0	1	0	0	x	x	x
	32	21FFFFH 218000H	SA74	1	0	0	0	0	1	1	x	x	x
	32	217FFFH 210000H	SA73	1	0	0	0	0	1	0	x	x	x
	32	20FFFFH 208000H	SA72	1	0	0	0	0	0	1	x	x	x
	32	207FFFH 200000H	SA71	1	0	0	0	0	0	0	x	x	x

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank B	32	1FFFFFH 1F8000H	SA70	0	1	1	1	1	1	1	x	x	x
	32	1F7FFFH 1F0000H	SA69	0	1	1	1	1	1	0	x	x	x
	32	1EFFFFH 1E8000H	SA68	0	1	1	1	1	0	1	x	x	x
	32	1E7FFFH 1E0000H	SA67	0	1	1	1	1	0	0	x	x	x
	32	1DFFFFH 1D8000H	SA66	0	1	1	1	0	1	1	x	x	x
	32	1D7FFFH 1D0000H	SA65	0	1	1	1	0	1	0	x	x	x
	32	1CFFFFH 1C8000H	SA64	0	1	1	1	0	0	1	x	x	x
	32	1C7FFFH 1C0000H	SA63	0	1	1	1	0	0	0	x	x	x
	32	1BFFFFH 1B8000H	SA62	0	1	1	0	1	1	1	x	x	x
	32	1B7FFFH 1B0000H	SA61	0	1	1	0	1	1	0	x	x	x
	32	1AFFFFH 1A8000H	SA60	0	1	1	0	1	0	1	x	x	x
	32	1A7FFFH 1A0000H	SA59	0	1	1	0	1	0	0	x	x	x
	32	19FFFFH 198000H	SA58	0	1	1	0	0	1	1	x	x	x
	32	197FFFH 190000H	SA57	0	1	1	0	0	1	0	x	x	x
	32	18FFFFH 188000H	SA56	0	1	1	0	0	0	1	x	x	x
	32	187FFFH 180000H	SA55	0	1	1	0	0	0	0	x	x	x
	32	17FFFFH 178000H	SA54	0	1	0	1	1	1	1	x	x	x
	32	177FFFH 170000H	SA53	0	1	0	1	1	1	0	x	x	x
	32	16FFFFH 168000H	SA52	0	1	0	1	1	0	1	x	x	x
	32	167FFFH 160000H	SA51	0	1	0	1	1	0	0	x	x	x
	32	15FFFFH 158000H	SA50	0	1	0	1	0	1	1	x	x	x
	32	157FFFH 150000H	SA49	0	1	0	1	0	1	0	x	x	x
	32	14FFFFH 148000H	SA48	0	1	0	1	0	0	1	x	x	x
	32	147FFFH 140000H	SA47	0	1	0	1	0	0	0	x	x	x
	32	13FFFFH 138000H	SA46	0	1	0	0	1	1	1	x	x	x
	32	137FFFH 130000H	SA45	0	1	0	0	1	1	0	x	x	x
	32	12FFFFH 128000H	SA44	0	1	0	0	1	0	1	x	x	x
	32	127FFFH 120000H	SA43	0	1	0	0	1	0	0	x	x	x
	32	11FFFFH 118000H	SA42	0	1	0	0	0	1	1	x	x	x
	32	117FFFH 110000H	SA41	0	1	0	0	0	1	0	x	x	x
	32	10FFFFH 108000H	SA40	0	1	0	0	0	0	1	x	x	x
	32	107FFFH 100000H	SA39	0	1	0	0	0	0	0	x	x	x
	32	0FFFFFH 0F8000H	SA38	0	0	1	1	1	1	1	x	x	x
	32	0F7FFFH 0F0000H	SA37	0	0	1	1	1	1	0	x	x	x
	32	0EFFFFH 0E8000H	SA36	0	0	1	1	1	0	1	x	x	x
	32	0E7FFFH 0E0000H	SA35	0	0	1	1	1	0	0	x	x	x

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Bank	Sector Organization K words	Address	Sectors Address	Sector Address Table									
				Bank Address Table									
				A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
Bank B	32	0DFFFFH 0D8000H	SA34	0	0	1	1	0	1	1	x	x	x
	32	0D7FFFH 0D0000H	SA33	0	0	1	1	0	1	0	x	x	x
	32	0CFFFFH 0C8000H	SA32	0	0	1	1	0	0	1	x	x	x
	32	0C7FFFH 0C0000H	SA31	0	0	1	1	0	0	0	x	x	x
	32	0BFFFFH 0B8000H	SA30	0	0	1	0	1	1	1	x	x	x
	32	0B7FFFH 0B0000H	SA29	0	0	1	0	1	1	0	x	x	x
	32	0AFFFFH 0A8000H	SA28	0	0	1	0	1	0	1	x	x	x
	32	0A7FFFH 0A0000H	SA27	0	0	1	0	1	0	0	x	x	x
	32	09FFFFH 098000H	SA26	0	0	1	0	0	1	1	x	x	x
	32	097FFFH 090000H	SA25	0	0	1	0	0	1	0	x	x	x
	32	08FFFFH 088000H	SA24	0	0	1	0	0	0	1	x	x	x
	32	087FFFH 080000H	SA23	0	0	1	0	0	0	0	x	x	x
Bank A	32	07FFFFH 078000H	SA22	0	0	0	1	1	1	1	x	x	x
	32	077FFFH 070000H	SA21	0	0	0	1	1	1	0	x	x	x
	32	06FFFFH 068000H	SA20	0	0	0	1	1	0	1	x	x	x
	32	067FFFH 060000H	SA19	0	0	0	1	1	0	0	x	x	x
	32	05FFFFH 058000H	SA18	0	0	0	1	0	1	1	x	x	x
	32	057FFFH 050000H	SA17	0	0	0	1	0	1	0	x	x	x
	32	04FFFFH 048000H	SA16	0	0	0	1	0	0	1	x	x	x
	32	047FFFH 040000H	SA15	0	0	0	1	0	0	0	x	x	x
	32	03FFFFH 038000H	SA14	0	0	0	0	1	1	1	x	x	x
	32	037FFFH 030000H	SA13	0	0	0	0	1	1	0	x	x	x
	32	02FFFFH 028000H	SA12	0	0	0	0	1	0	1	x	x	x
	32	027FFFH 020000H	SA11	0	0	0	0	1	0	0	x	x	x
	32	01FFFFH 018000H	SA10	0	0	0	0	0	1	1	x	x	x
	32	017FFFH 010000H	SA9	0	0	0	0	0	1	0	x	x	x
	32	00FFFFH 008000H	SA8	0	0	0	0	0	0	1	x	x	x
	4	007FFFH 007000H	SA7	0	0	0	0	0	0	0	1	1	1
	4	006FFFH 006000H	SA6	0	0	0	0	0	0	0	1	1	0
	4	005FFFH 005000H	SA5	0	0	0	0	0	0	0	1	0	1
	4	004FFFH 004000H	SA4	0	0	0	0	0	0	0	1	0	0
	4	003FFFH 003000H	SA3	0	0	0	0	0	0	0	0	1	1
	4	002FFFH 002000H	SA2	0	0	0	0	0	0	0	0	1	0
	4	001FFFH 001000H	SA1	0	0	0	0	0	0	0	0	0	1
	4	000FFFH 000000H	SA0	0	0	0	0	0	0	0	0	0	0

Sector Group Address Table (Flash Memory)

(1/2)

Sector group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA0	0	0	0	0	0	0	0	0	0	0	4K words (1 Sector)	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	4K words (1 Sector)	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	4K words (1 Sector)	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	4K words (1 Sector)	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	4K words (1 Sector)	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	4K words (1 Sector)	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	4K words (1 Sector)	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	4K words (1 Sector)	SA7
SGA8	0	0	0	0	0	0	1	×	×	×	96K words (3 Sectors)	SA8 to SA10
						1	0					
						1	1					
SGA9	0	0	0	0	1	×	×	×	×	×	128K words (4 Sectors)	SA11 to SA14
SGA10	0	0	0	1	0	×	×	×	×	×	128K words (4 Sectors)	SA15 to SA18
SGA11	0	0	0	1	1	×	×	×	×	×	128K words (4 Sectors)	SA19 to SA22
SGA12	0	0	1	0	0	×	×	×	×	×	128K words (4 Sectors)	SA23 to SA26
SGA13	0	0	1	0	1	×	×	×	×	×	128K words (4 Sectors)	SA27 to SA30
SGA14	0	0	1	1	0	×	×	×	×	×	128K words (4 Sectors)	SA31 to SA34
SGA15	0	0	1	1	1	×	×	×	×	×	128K words (4 Sectors)	SA35 to SA38
SGA16	0	1	0	0	0	×	×	×	×	×	128K words (4 Sectors)	SA39 to SA42
SGA17	0	1	0	0	1	×	×	×	×	×	128K words (4 Sectors)	SA43 to SA46
SGA18	0	1	0	1	0	×	×	×	×	×	128K words (4 Sectors)	SA47 to SA50
SGA19	0	1	0	1	1	×	×	×	×	×	128K words (4 Sectors)	SA51 to SA54
SGA20	0	1	1	0	0	×	×	×	×	×	128K words (4 Sectors)	SA55 to SA58
SGA21	0	1	1	0	1	×	×	×	×	×	128K words (4 Sectors)	SA59 to SA62
SGA22	0	1	1	1	0	×	×	×	×	×	128K words (4 Sectors)	SA63 to SA66
SGA23	0	1	1	1	1	×	×	×	×	×	128K words (4 Sectors)	SA67 to SA70

Remark × : V_{IH} or V_{IL}

(2/2)

Sector group	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Size	Sector
SGA24	1	0	0	0	0	×	×	×	×	×	128K words (4 Sectors)	SA71 to SA74
SGA25	1	0	0	0	1	×	×	×	×	×	128K words (4 Sectors)	SA75 to SA78
SGA26	1	0	0	1	0	×	×	×	×	×	128K words (4 Sectors)	SA79 to SA82
SGA27	1	0	0	1	1	×	×	×	×	×	128K words (4 Sectors)	SA83 to SA86
SGA28	1	0	1	0	0	×	×	×	×	×	128K words (4 Sectors)	SA87 to SA90
SGA29	1	0	1	0	1	×	×	×	×	×	128K words (4 Sectors)	SA91 to SA94
SGA30	1	0	1	1	0	×	×	×	×	×	128K words (4 Sectors)	SA95 to SA98
SGA31	1	0	1	1	1	×	×	×	×	×	128K words (4 Sectors)	SA99 to SA102
SGA32	1	1	0	0	0	×	×	×	×	×	128K words (4 Sectors)	SA103 to SA106
SGA33	1	1	0	0	1	×	×	×	×	×	128K words (4 Sectors)	SA107 to SA110
SGA34	1	1	0	1	0	×	×	×	×	×	128K words (4 Sectors)	SA111 to SA114
SGA35	1	1	0	1	1	×	×	×	×	×	128K words (4 Sectors)	SA115 to SA118
SGA36	1	1	1	0	0	×	×	×	×	×	128K words (4 Sectors)	SA119 to SA122
SGA37	1	1	1	0	1	×	×	×	×	×	128K words (4 Sectors)	SA123 to SA126
SGA38	1	1	1	1	0	×	×	×	×	×	128K words (4 Sectors)	SA127 to SA130
SGA39	1	1	1	1	1	0	0	×	×	×	96K words (3 Sectors)	SA131 to SA133
						0	1					
						1	0					
SGA40	1	1	1	1	1	1	1	0	0	0	4K words (1 Sector)	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	4K words (1 Sector)	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	4K words (1 Sector)	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	4K words (1 Sector)	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	4K words (1 Sector)	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	4K words (1 Sector)	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	4K words (1 Sector)	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	4K words (1 Sector)	SA141

Remark × : V_{IH} or V_{IL}

Product ID Code (Flash Memory)

Product ID Code	Code output																
	I/O15	I/O14	I/O13	I/O12	I/O11	I/O10	I/O9	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	HEX
Manufacturer code	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0010H
Device code	0	0	1	0	0	0	1	0	0	0	0	1	1	1	0	0	221CH
Sector group protection	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001H[Note]

Note If 0001H is output, the sector group is protected. If 0000H is output, the sector group is unprotected.

Command Sequence (Flash Memory)

Command sequence	Bus	1st bus Cycle		2nd bus Cycle		3rd bus Cycle		4th bus Cycle		5th bus Cycle		6th bus Cycle	
	Cycle	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset Note1	1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset Note1	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	–	–	–	–
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	–	–	–	–
Program Suspend Note 2	1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Program Resume Note 3	1	BA	30H	–	–	–	–	–	–	–	–	–	–
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend Note 4, 5	1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume Note 4, 6	1	BA	30H	–	–	–	–	–	–	–	–	–	–
Unlock Bypass Set	3	555H	AAH	2AAH	55H	555H	20H	–	–	–	–	–	–
Unlock Bypass Program Note 7	2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock Bypass Chip Erase Note 7	2	×××H	80H	×××H	10H	–	–	–	–	–	–	–	–
Unlock Bypass Sector Erase Note 7	2	×××H	80H	SA	30H	–	–	–	–	–	–	–	–
Unlock Bypass Reset Note 7	2	×××H	90H	×××H	00H Note11	–	–	–	–	–	–	–	–
Product ID / Sector Group Protection Information / Read Mode Register Information	3	555H	AAH	2AAH	55H	(BA) 555H	90H	IA	ID	–	–	–	–
Sector Group Protection Note 8	4	×××H	60H	SPA	60H	SPA	40H	SPA	SD	–	–	–	–
Sector Group Unprotect Note 9	4	×××H	60H	SUA	60H	SUA	40H	SUA	SD	–	–	–	–
Extra One Time Protect Sector Entry	3	555H	AAH	2AAH	55H	555H	88H	–	–	–	–	–	–
Extra One Time Protect Sector Reset Note 10	4	555H	AAH	2AAH	55H	555H	90H	xxxH	00H	–	–	–	–
Extra One Time Protect Sector Program Note 10	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	–	–	–	–
Extra One Time Protect Sector Erase Note 10	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	EOTPSA	30H
Extra One Time Protect Sector Protection Note 10	4	×××H	60H	EOTPSA	60H	EOTPSA	40H	EOTPSA	SD	–	–	–	–
Read Mode Register Set	3	555H	AAH	2AAH	55H	REGD	C0H	–	–	–	–	–	–

Notes 1. Both these read / reset commands reset the device to the read mode.

2. Programming is suspended if B0H is input to the bank address being programmed to in a program operation.

3. Programming is resumed if 30H is input to the bank address being suspended to in a program-suspend operation.

4. If automatic erase resume and suspend are repeated at intervals of less than 100 μs, since it will become suspend operation, without starting automatic erase, the erase operation may not be correctly completed.

5. Erasure is suspended if B0H is input to the bank address being erased in a sector erase operation.

6. Erasure is resumed if 30H is input to the bank address being suspended in a sector-erase-suspend operation.

7. Valid only in the unlock bypass mode.

8. Valid only when /RESET = V_{ID} (except in the Extra One Time Protect Sector mode).

9. The command sequence that protects a sector group is excluded.

10. Valid only in the Extra One Time Protect Sector mode.

11. This command can be used even if this data is F0H.

Remarks 1. The system should generate the following address pattern:

555H or 2AAH (A10 to A0)

2. RA : Read address

RD : Read data

IA : Address input as follows

Information	A21 to A12	A11 to A4	A3 to A0
Manufacturer code	Bank address	Don't care	0000
Device code	Bank address	Don't care	0001
Sector group protection information	Sector group address	Don't care	0010
Read mode register information	Bank address	Don't care	0100

ID : Code output. For the manufacture code, device code and sector group protection information, refer to the **Product ID code (Flash Memory)**. For read mode register information, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

PA : Program address

PD : Program data

SA : Erase sector address. The sector to be erased is selected by the combination of A21 to A12. Refer to the **Sector Organization / Sector Address Table (Flash Memory)**.

BA : Bank address. Refer to the **Sector Organization / Sector Address Table (Flash Memory)**.

SPA : Sector group address to be protected or protection-verified. Set the sector group address (SGA) and (A6, A3, A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}, V_{IH}, V_{IL}).

Sector group protection can be set for each sector group address. For details, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

Refer to the **Sector Group Address Table (Flash Memory)** for the sector group address.

SUA : Sector group address to be unprotected or unprotection-verified. Set the sector group address (SGA) and (A6, A3, A2, A1, A0) = (V_{IH}, V_{IL}, V_{IL}, V_{IH}, V_{IL}).

Sector group unprotect is performed for all sector group using a single command, however, unprotect verification must be performed for each sector group address. For details, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

Refer to the **Sector Group Address Table (Flash Memory)** for the sector group address.

EOTPSA : Extra One Time Protect Sector area addresses. These addresses are 000000H to 007FFFH.

SD : Data for verifying whether sector groups read from the address specified by SPA, SUA, EOTPSA are protected or unprotected.

REGD : Read mode register information. Description for setting, refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

3. The sector group address is don't care except when a program / erase address or read address are selected.

4. For the operation of bus, refer **to PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E)**.

5. × of address bit indicates V_{IH} or V_{IL}.

Electrical Specifications

Before turning on power, input $V_{SS} \pm 0.2$ V to the /RESET pin until $V_{CCf} \geq V_{CCf}$ (MIN.) and keep that state for 200 μs.

Absolute Maximum Ratings

Parameter	Symbol	Condition		Rating	Unit
Supply voltage	V_{CCf}	with respect to V_{SS}		–0.5 to +2.4	V
	V_{CCS}			–0.5 Note 1 to +3.3	
Input / Output supply voltage	V_{CCQf}	with respect to V_{SS}		–0.5 to +4.0	V
Input / Output voltage	V_T	with respect to V_{SS}	/WP(ACC), /RESET	–0.5 Note 2 to +13.0	V
			except /WP(ACC), /RESET	–0.5 Note 1 to V_{CCQf} + 0.4 (3.3 V MAX.), –0.5 Note 1 to V_{CCS} + 0.4 (3.3 V MAX.)	
Ambient operation temperature	T_A			–25 to +85	°C
Storage temperature	T_{stg}			–55 to +125	°C
	T_{bias}	at bias		–25 to +85	

Notes 1. –1.5 V (MIN.) (pulse width ≤ 30 ns)

2. –2.0 V (MIN.) (pulse width ≤ 20 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CCf}	-D80X	1.8		2.1	V
		-E85X	1.65		1.95	
	V_{CCS}		2.7		3.1	
Input / Output supply voltage	V_{CCQf}		2.7		3.1	V
High level input voltage	V_{IH}		2.4		V_{CCQf} +0.4, V_{CCS} +0.4	V
	V_{ID}	High voltage is applied (/RESET)	9.0		11.0	V
Low level input voltage	V_{IL}		–0.3 Note		+0.5	V
Accelerated programming voltage	V_{ACC}	High voltage is applied	8.5		9.5	V
Ambient operating temperature	T_A		–25		+85	°C

Note –1.0 V (MIN.) (pulse width = 20 ns)

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Flash Memory **(1/2)**

Parameter		Symbol	Test condition	-D80X			Unit
				MIN.	TYP.	MAX.	
High level output voltage		V_{OH}	I_{OH} = –0.1 mA	$V_{CC}Qf$–0.1			V
Low level output voltage		V_{OL}	I_{OL} = 0.1 mA			0.1	V
Input leakage current		I_{LI1}	V_{IN} = V_{SS} to $V_{CC}Qf$, $V_{CC}Qf$ = $V_{CC}Qf$ (MAX.)			1.0	μA
	High voltage is applied	I_{LI2}	/RESET = 11.0 V			35	
I/O leakage current		I_{LO}	$V_{I/O}$ = V_{SS} to $V_{CC}Qf$, $V_{CC}Qf$ = $V_{CC}Qf$ (MAX.)			1.0	μA
Power supply current	Read	I_{CC1}	/CEf = V_{IL}, /OE = V_{IH}, Cycle = 5 MHz, I_{OUT} = 0 mA		10	20	mA
	Program, Erase	I_{CC2}	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming / erase			35	mA
	Standby	I_{CC3}	$V_{CC}f$ = $V_{CC}f$ (MAX.), /OE = V_{IL}, /CEf = /RESET = /WP(ACC) = $V_{CC}Qf$ ± 0.3 V		15	25	μA
	Standby / Reset	I_{CC4}	$V_{CC}f$ = $V_{CC}f$ (MAX.), /RESET = V_{SS} ± 0.2 V		15	25	μA
	Automatic sleep mode	I_{CC5}	V_{IH} = $V_{CC}Qf$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V		15	25	μA
	Read during programming	I_{CC6}	V_{IH} = $V_{CC}Qf$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			55	mA
	Read during erasing	I_{CC7}	V_{IH} = $V_{CC}Qf$ ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			55	mA
	Programming during suspend	I_{CC8}	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming during suspend			35	mA
	Accelerated programming	I_{ACC}	/WP (ACC) pin		5	10	mA
			$V_{CC}f$		15	35	
Low $V_{CC}f$ lock-out voltage[Note]		V_{LKO}		1.0			V

Note When $V_{CC}f$ is equal to or lower than V_{LKO}, the device ignores all write cycles. Refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E).**

Remark V_{IN} : Input voltage, $V_{I/O}$: Input / Output voltage

Flash Memory **(2/2)**

Parameter		Symbol	Test condition	-E85X			Unit
				MIN.	TYP.	MAX.	
High level output voltage		V_{OH}	I_{OH} = –0.1 mA	V_{CCQf}–0.1			V
Low level output voltage		V_{OL}	I_{OL} = 0.1 mA			0.1	V
Input leakage current		I_{LI1}	V_{IN} = V_{SS} to V_{CCQf}, V_{CCQf} = V_{CCQf} (MAX.)			1.0	μA
	High voltage is applied	I_{LI2}	/RESET = 11.0 V			35	
I/O leakage current		I_{LO}	$V_{I/O}$ = V_{SS} to V_{CCQf}, V_{CCQf} = V_{CCQf} (MAX.)			1.0	μA
Power supply current	Read	I_{CC1}	/CEf = V_{IL}, /OE = V_{IH}, Cycle = 5 MHz, I_{OUT} = 0 mA		8	15	mA
	Program, Erase	I_{CC2}	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming / erase			25	mA
	Standby	I_{CC3}	V_{CCf} = V_{CCf} (MAX.), /OE = V_{IL}, /CEf = /RESET = /WP(ACC) = V_{CCQf} ± 0.3 V		15	25	μA
	Standby / Reset	I_{CC4}	V_{CCf} = V_{CCf} (MAX.), /RESET = V_{SS} ± 0.2 V		15	25	μA
	Automatic sleep mode	I_{CC5}	V_{IH} = V_{CCQf} ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V		15	25	μA
	Read during programming	I_{CC6}	V_{IH} = V_{CCQf} ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			40	mA
	Read during erasing	I_{CC7}	V_{IH} = V_{CCQf} ± 0.2 V, V_{IL} = V_{SS} ± 0.2 V			40	mA
	Programming during suspend	I_{CC8}	/CEf = V_{IL}, /OE = V_{IH}, Automatic programming during suspend			25	mA
	Accelerated programming	I_{ACC}	/WP (ACC) pin		5	10	mA
			V_{CCf}		12	25	
Low V_{CCf} lock-out voltage[Note]		V_{LKO}		1.0			V

Note When V_{CCf} is equal to or lower than V_{LKO}, the device ignores all write cycles. Refer to **PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information (M15451E).**

Remark V_{IN} : Input voltage, $V_{I/O}$: Input / Output voltage

SRAM

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High level output voltage	V_{OH}	I_{OH} = –0.1 mA	V_{CCs}–0.1			V
Low level output voltage	V_{OL}	I_{OL} = 0.1 mA			0.1	V
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CCs}	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CCs}, /CE1s = V_{IH} or CE2s = V_{IL} or /WE = V_{IL} or /OE = V_{IH}	–1.0		+1.0	μA
Power supply current	I_{CCA1}	/CE1s = V_{IL}, CE2s = V_{IH}, $I_{I/O}$ = 0 mA, Minimum cycle time		–	30	mA
	I_{CCA2}	/CE1s = V_{IL}, CE2s = V_{IH}, $I_{I/O}$ = 0 mA, Cycle time = ∞		–	5	
	I_{CCA3}	/CE1s ≤ 0.2 V, CE2s ≥ V_{CCs} – 0.2 V, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CCs} – 0.2 V, $I_{I/O}$ = 0 mA, Cycle time = 1 μs		–	6	
Standby supply current	I_{SB}	/CE1s = V_{IH} or CE2s = V_{IL} or /LB = /UB = V_{IH}		–	0.6	mA
	I_{SB1}	/CE1s ≥ V_{CCs} – 0.2 V, CE2s ≥ V_{CCs} – 0.2 V		1.0	15	μA
	I_{SB2}	CE2s ≤ 0.2 V		1.0	15	
	I_{SB3}	/LB = /UB ≥ V_{CCs} – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CCs} – 0.2 V		1.0	15	

Remarks 1. V_{IN} : Input voltage, $V_{I/O}$: Input / Output voltage

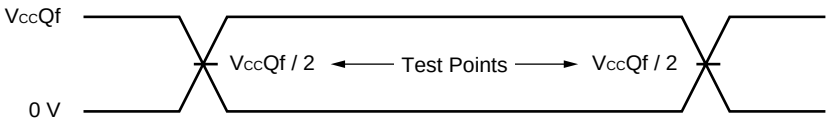
2. This DC Characteristic is in common regardless of product classification.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

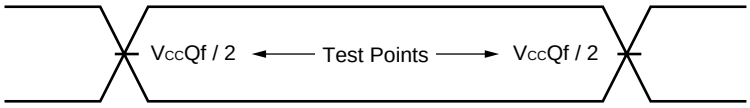
AC Test Conditions

[Flash Memory]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

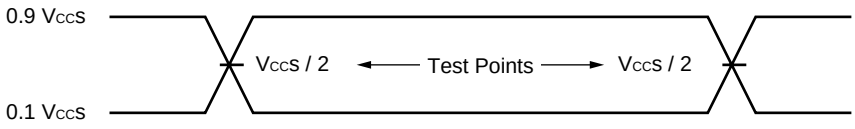


Output Load

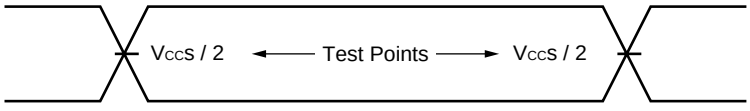
1 TTL + 30 pF

[SRAM]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1 TTL + 30 pF

/CEf, /CE1s, CE2s Timing

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Note
/CEf, /CE1s, CE2s recover time	t_{CCR}		0			ns	

Read Cycle (Flash Memory)

Parameter		Symbol	-D80X		-E85X		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Read cycle time		t_{RC}	80		85		ns	
Address access time		t_{ACC}		80		85	ns	1
Page read cycle		t_{PRC}	30		30		ns	
Page address access time		t_{PACC}		30		30	ns	1
/CEf access time		t_{CEf}		80		85	ns	2
/OE access time		t_{OE}		25		25	ns	
Output disable time		t_{DF}		25		25	ns	
Output hold time		t_{OH}	0		0		ns	
/RESET pulse width		t_{RP}	500		500		ns	
/RESET hold time before read		t_{RH}	50		50		ns	
/RESET low	At automatic mode	t_{READY}		20		20	μs	
to read mode	Except automatic mode			500		500	ns	
/OE low level time from /WE high level		t_{OEH}	20		20		ns	

Notes 1. /CEf = /OE = V_{IL}

2. /OE = V_{IL}

Remark t_{DF} is the time from inactivation of /CEf or /OE to high impedance state output.

Write Cycle (Program /Erase) (Flash Memory) **(1/2)**

Parameter		Symbol	-D80X			-E85X			Unit	Note
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Write cycle time		t_{WC}	80			85			ns	
Address setup time (/WE to address)		t_{AS}	0			0			ns	
Address setup time (/CEf to address)		t_{AS}	0			0			ns	
Address hold time (/WE to address)		t_{AH}	45			45			ns	
Address hold time (/CEf to address)		t_{AH}	45			45			ns	
Input data setup time		t_{DS}	45			45			ns	
Input data hold time		t_{DH}	0			0			ns	
/OE hold time	Read	t_{OEH}	0			0			ns	
	Toggle bit, Data polling		10			10				
Read recovery time before write (/OE to /CEf)		t_{GHEL}	0			0			ns	
Read recovery time before write (/OE to /WE)		t_{GHWL}	0			0			ns	
/WE setup time (/CEf to /WE)		t_{WS}	0			0			ns	
/CEf setup time (/WE to /CEf)		t_{CS}	0			0			ns	
/WE hold time (/CEf to /WE)		t_{WH}	0			0			ns	
/CEf hold time (/WE to /CEf)		t_{CH}	0			0			ns	
Write pulse width		t_{WP}	35			35			ns	
/CEf pulse width		t_{CP}	35			35			ns	
Write pulse width high		t_{WPH}	30			30			ns	
/CEf pulse width high		t_{CPH}	30			30			ns	
Word programming operation time		t_{WPG}		11	200		11	200	μs	
Chip programming operation time		t_{CPG}		47	840		47	840	s	
Sector erase operation time	4K words sector	t_{SER}		0.15	1.0		0.15	1.0	s	1,2
	32K words sector			0.5	1.5		0.5	1.5		
	4K words sector			0.5	3.0		0.5	3.0		1,3
	32K words sector			0.7	5.0		0.7	5.0		
Chip erase operation time		t_{CER}		65.4	205		65.4	205	s	1,2
				96.2	678		96.2	678		1,3
Accelerated programming time		t_{ACCPG}		7	150		7	150	μs	
Program / Erase cycle			300,000			300,000			cycle	
V_{CC}f setup time		t_{VCS}	200			200			μs	
RY (/BY) recovery time		t_{RB}	0			0			ns	
/RESET pulse width		t_{RP}	500			500			ns	
/RESET high-voltage (V_{ID}) hold time from high of RY(/BY) when sector group is temporarily unprotect		t_{RRB}	20			20			μs	
/RESET hold time		t_{RH}	50			50			ns	

Notes 1. The preprogramming time prior to the erase operation is not included.

2. Program / erase cycle : 100,000 cycles

3. Program / erase cycle : 300,000 cycles

Write Cycle (Program / Erase) (Flash Memory) **(2/2)**

Parameter	Symbol	-D80X			-E85X			Unit	Note
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
From completion of automatic program / erase to data output time	t_{EOE}			80			85	ns	
RY (/BY) delay time from valid program or erase operation	t_{BUSY}			80			85	ns	
Address setup time to /OE low in toggle bit	t_{ASO}	15			15			ns	
Address hold time to /CEf or /OE high in toggle bit	t_{AHT}	0			0			ns	
/CEf pulse width high for toggle bit	t_{CEPH}	20			20			ns	
/OE pulse width high for toggle bit	t_{OEPH}	20			20			ns	
Voltage transition time	t_{VLHT}	4			4			μs	1
Rise time to V_{ID} (/RESET)	t_{VIDR}	500			500			ns	
Rise time to V_{ACC} (/WP(ACC))	t_{VACCR}	500			500			ns	
Erase timeout time	t_{TOW}	50			50			μs	2
Erase suspend transition time	t_{SPD}			20			20	μs	2

Notes 1. Sector group protection only.

2. Table only.

Write operation (Program / Erase) Performance (Flash Memory)

Parameter	Description		MIN.	TYP.	MAX.	Unit	Note
Sector erase time	The preprogramming time prior to the erase operation is not included.	4K words sector		0.15	1.0	s	1
		32K words sector		0.5	1.5		
		4K words sector		0.5	3.0		2
		32K words sector		0.7	5.0		
Chip erase time	The preprogramming time prior to the erase operation is not included.			65.4	205	s	1
				96.2	678		2
Word programming time	Excludes system-level overhead			11	200	μs	
Chip programming time	Excludes system-level overhead			47	840	s	
Accelerated programming time	Excludes system-level overhead			7	150	μs	
Program / Erase cycle			300,000			cycle	

Notes 1. Program / erase cycle : 100,000 cycles

2. Program / erase cycle : 300,000 cycles

★ **Read Cycle (SRAM)**

Parameter	Symbol	MIN.	MAX.	Unit	Note
Read cycle time	t_{RC}	55		ns	
Address access time	t_{AA}		55	ns	1
/CE1s access time	t_{CO1}		55	ns	
CE2s access time	t_{CO2}		55	ns	
/OE to output valid	t_{OE}		30	ns	
/LB, /UB to output valid	t_{BA}		55	ns	
Output hold from address change	t_{OH}	5		ns	
/CE1s to output in Low-Z	t_{LZ1}	5		ns	2
CE2s to output in Low-Z	t_{LZ2}	5		ns	
/OE to output in Low-Z	t_{OLZ}	0		ns	
/LB, /UB to output in Low-Z	t_{BLZ}	5		ns	
/CE1s to output in High-Z	t_{HZ1}		20	ns	
CE2s to output in High-Z	t_{HZ2}		20	ns	
/OE to output in High-Z	t_{OHZ}		20	ns	
/LB, /UB to output in High-Z	t_{BHZ}		20	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

★ **Write Cycle (SRAM)**

Parameter	Symbol	MIN.	MAX.	Unit	Note
Write cycle time	t_{WC}	55		ns	
/CE1s to end of write	t_{CW1}	50		ns	
CE2s to end of write	t_{CW2}	50		ns	
/LB, /UB to end of write	t_{BW}	50		ns	
Address valid to end of write	t_{AW}	50		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	45		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	25		ns	
Data hold time	t_{DH}	0		ns	
/WE to output in High-Z	t_{WHZ}		20	ns	1
Output active from end of write	t_{OW}	5		ns	

Note 1. The output load is 1TTL + 5 pF.

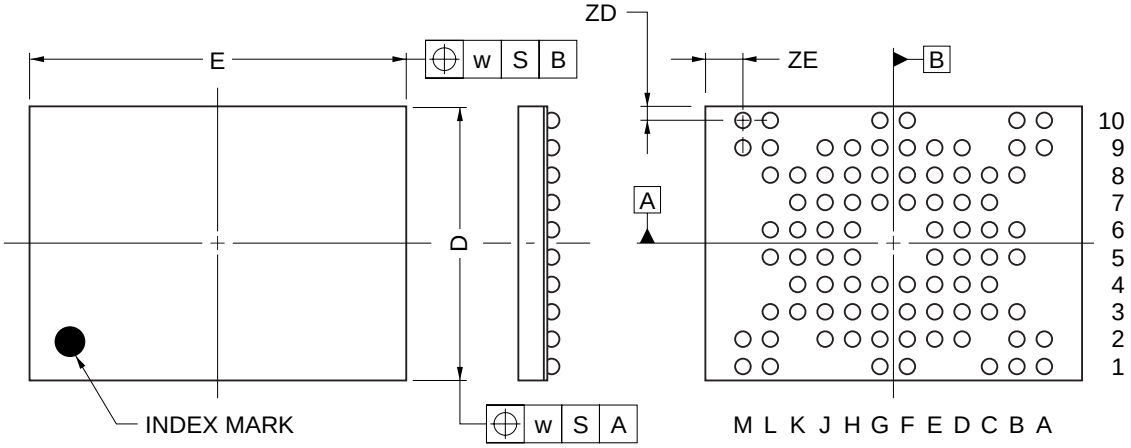
Low V_{CC} Data Retention Characteristics (T_A = –25 to +85°C) (SRAM)

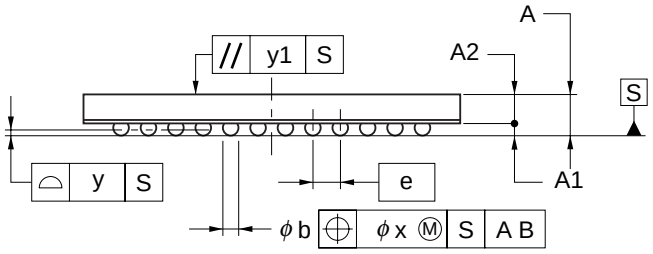
Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	/CE1s ≥ V_{CC}s – 0.2 V, CE2s ≥ V_{CC}s – 0.2 V	1.5		3.1	V
	V_{CCDR2}	CE2s ≤ 0.2 V	1.5		3.1	
	V_{CCDR3}	/LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V	1.5		3.1	
Data retention supply current	I_{CCDR1}	V_{CC}s = 1.5 V, /CE1s ≥ V_{CC}s – 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.5	6.0	μA
	I_{CCDR2}	V_{CC}s = 1.5 V, CE2s ≤ 0.2 V		0.5	6.0	
	I_{CCDR3}	V_{CC}s = 1.5 V, /LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.5	6.0	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		t_{RC} Note			ns

Note t_{RC} : Read cycle time

Package Drawing

85-PIN TAPE FBGA (11x8)





ITEM	MILLIMETERS
D	8.00±0.10
E	11.00±0.10
w	0.20
e	0.80
A	1.11±0.10
A1	0.27±0.05
A2	0.84
b	0.45±0.05
x	0.08
y	0.10
y1	0.20
ZD	0.40
ZE	1.10

P85F9-80-CD5

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the MC-22222361-X.

Type of Surface Mount Device

MC-22222361F9-CD5 : 85-pin TAPE FBGA (11 × 8)

Related Documents

Document Name	Document Number
PAGE MODE FLASH MEMORY, BURST MODE FLASH MEMORY Information	M15451E
SRAM AND MOBILE SPECIFIED RAM TIMING CHARTS FOR MCP Information	M15819E

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
3rd edition/ Sep. 2002	p.2	p.2	Modification	Mounted Flash Memory	μPD29F064115-Y → μPD29F064115-X
	p.3	p.3	Addition	Pin Configuration	Figures of top view and bottom view
	p.13	p.13	Modification	Command Sequence (Flash Memory)	Remark 2: SPA, SUA
	p.16	p.16	Modification Addition	DC Characteristics (SRAM)	I_{SB1}, I_{SB2}, I_{SB3} (TYP.): TBD → 1.0 μA Remark 2
	p.18	p.18	Addition	Read Cycle (Flash Memory)	T_{OEH}
	pp.19, 20	pp.19, 20	Modification	Accelerated programming time (MAX.)	TBD → 150 μs
	p.23	p.23	Modification	Package Drawing	Preliminary version → Standard version
4th edition/ Nov. 2002	pp.1, 2	pp.1, 2	Modification	General Features, Ordering Information	SRAM Access time (MAX.): 70 ns → 55 ns
	p.21	p.21	Modification	Read Cycle (SRAM)	t_{RC} (MIN.): 70 ns → 55 ns t_{AA}, t_{CO1}, t_{CO2}, t_{BA} (MAX.): 70 ns → 55 ns t_{OE} (MAX.): 35 ns → 30 ns t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{BHZ} (MAX.): 25 ns → 20 ns
				Write Cycle (SRAM)	t_{WC} (MIN.): 70 ns → 55 ns t_{CW1}, t_{CW2}, t_{BW}, t_{AW} (MIN.): 55 ns → 50 ns t_{WP} (MIN.): 50 ns → 45 ns t_{DW} (MIN.): 30 ns → 25 ns t_{WHZ} (MAX.): 25 ns → 20 ns

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

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