

**2M-BIT CMOS STATIC RAM
128K-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION**

Description

The μ PD442002-X is a high speed, low power, 2,097,152 bits (131,072 words by 16 bits) CMOS static RAM.

The μ PD442002-X is packed in 48-pin TAPE FBGA.

Features

- 131,072 words by 16 bits organization
- ★ • Fast access time : 50, 55, 70, 85, 100, 120 ns (MAX.)
- Byte data control : /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation
(BB version : $V_{CC} = 2.7$ to 3.6 V, BC version : $V_{CC} = 2.2$ to 3.6 V, DD version : $V_{CC} = 1.8$ to 2.2 V)
- Low V_{CC} data retention : 1.0 V (MIN.)
- Operating ambient temperature : $T_A = -25$ to $+85$ °C
- Output Enable input for easy application

| Part number | Access time ns (MAX.) | Operating supply voltage V | Operating ambient temperature °C | Supply current | | |
|------------------------|-----------------------------------|----------------------------------|--|--|------------------------------|-------------------------------------|
| | | | | At operating mA (MAX.) | At standby μ A (MAX.) | At data retention μ A (MAX.) |
| ★ μ PD442002-BBxxX | 50 ^{Note 1} , 55, 70, 85 | 2.7 to 3.6 | -25 to +85 | 30 ^{Note 2} 35 ^{Note 3} 40 ^{Note 4} | 4 | 2 |
| μ PD442002-BCxxX | 70, 85, 100 | 2.2 to 3.6 | | 30 | | |
| ★ μ PD442002-DDxxX | 85, 100, 120 | 1.8 to 2.2 | | 15 | 3 | |

- ★ **Notes** 1. $V_{CC} \geq 3.0$ V
- ★ 2. Cycle time ≥ 70 ns
- ★ 3. Cycle time = 55 ns
- ★ 4. Cycle time = 50 ns

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

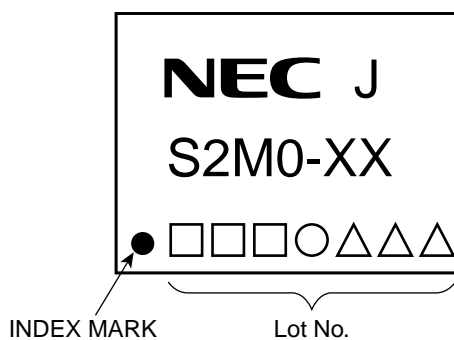
Ordering Information

| Part number | Package | Access time ns (MAX.) | Operating supply voltage V | Operating temperature °C | Remark |
|-------------------------|------------------------|--------------------------|----------------------------------|--------------------------------|------------|
| ★ μPD442002F9-BB55X-BC1 | 48-pin TAPE FBGA (6×8) | 55, 50 ^{Note} | 2.7 to 3.6 | -25 to +85 | BB version |
| μPD442002F9-BB70X-BC1 | | 70 | | | |
| μPD442002F9-BB85X-BC1 | | 85 | | | |
| μPD442002F9-BC70X-BC1 | | 70 | 2.2 to 3.6 | | BC version |
| μPD442002F9-BC85X-BC1 | | 85 | | | |
| μPD442002F9-BC10X-BC1 | | 100 | | | |
| μPD442002F9-DD85X-BC1 | | 85 | 1.8 to 2.2 | | DD version |
| μPD442002F9-DD10X-BC1 | | 100 | | | |
| μPD442002F9-DD12X-BC1 | | 120 | | | |

★ **Note** V_{cc} ≥ 3.0 V

Marking Image

| Part number | Marking (XX) |
|-----------------------|--------------|
| μPD442002F9-BB55X-BC1 | B1 |
| μPD442002F9-BB70X-BC1 | B2 |
| μPD442002F9-BB85X-BC1 | B3 |
| μPD442002F9-BC70X-BC1 | C2 |
| μPD442002F9-BC85X-BC1 | C3 |
| μPD442002F9-BC10X-BC1 | C4 |
| μPD442002F9-DD85X-BC1 | D3 |
| μPD442002F9-DD10X-BC1 | D4 |
| μPD442002F9-DD12X-BC1 | D5 |



Pin Configuration

/xxx indicates active low signal.

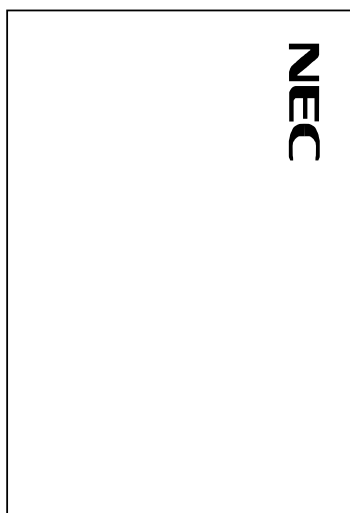
48-pin TAPE FBGA (6x8)

[μPD442002F9-BBxxX-BC1]

[μPD442002F9-BCxxX-BC1]

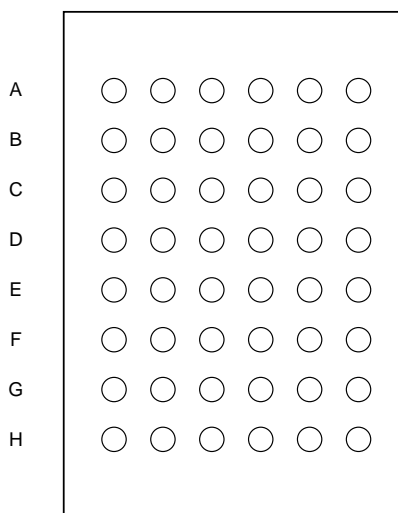
[μPD442002F9-DDxxX-BC1]

Top View



1 2 3 4 5 6

Bottom View



6 5 4 3 2 1

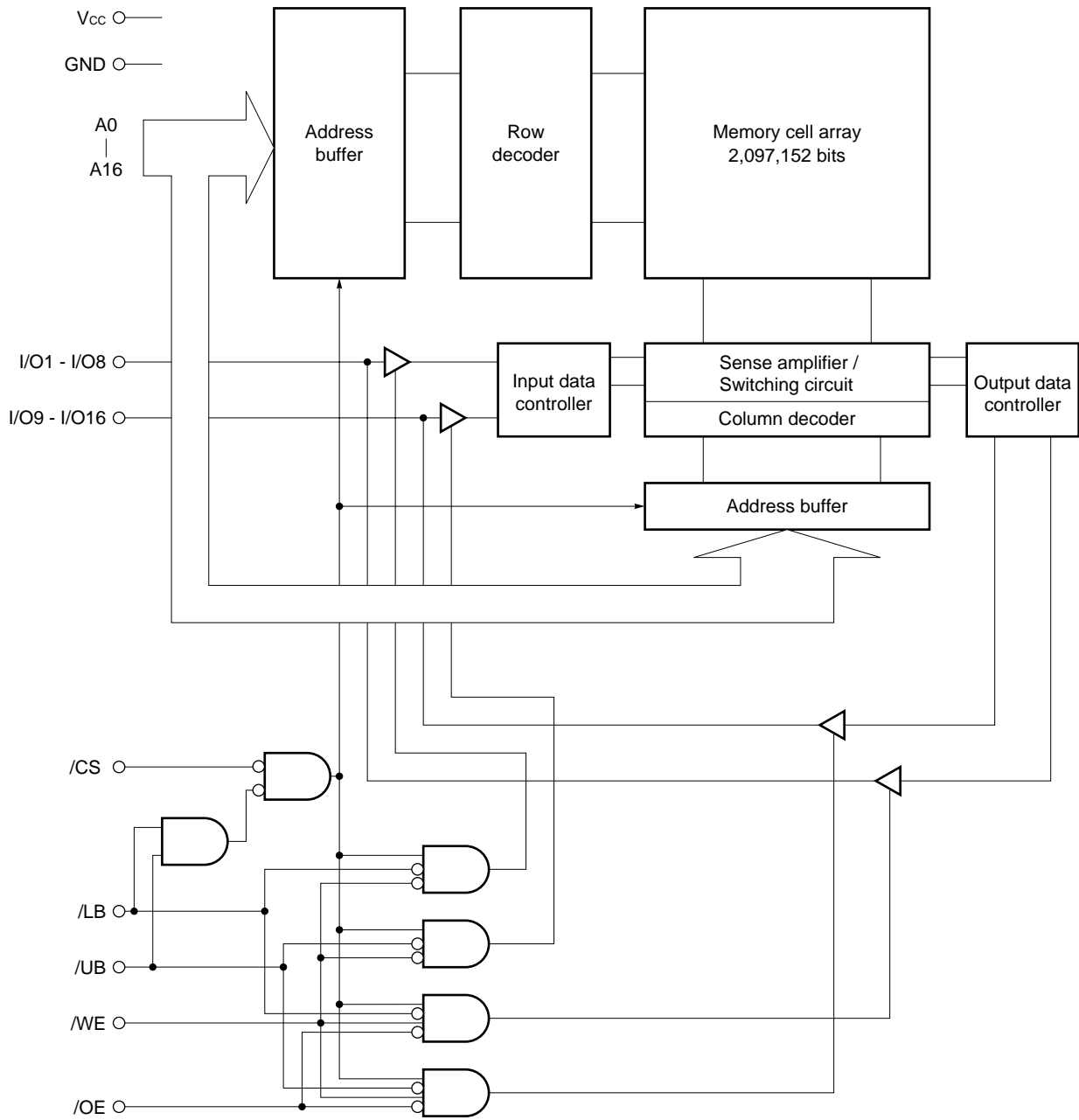
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|-----------------|-------|-----|-----|------|-----------------|
| A | /LB | /OE | A0 | A1 | A2 | NC |
| B | I/O9 | /UB | A3 | A4 | /CS | I/O1 |
| C | I/O10 | I/O11 | A5 | A6 | I/O2 | I/O3 |
| D | GND | I/O12 | NC | A7 | I/O4 | V _{cc} |
| E | V _{cc} | I/O13 | NC | A16 | I/O5 | GND |
| F | I/O15 | I/O14 | A14 | A15 | I/O6 | I/O7 |
| G | I/O16 | NC | A12 | A13 | /WE | I/O8 |
| H | NC | A8 | A9 | A10 | A11 | NC |

| | 6 | 5 | 4 | 3 | 2 | 1 |
|---|-----------------|------|-----|-----|-------|-----------------|
| A | NC | A2 | A1 | A0 | /OE | /LB |
| B | I/O1 | /CS | A4 | A3 | /UB | I/O9 |
| C | I/O3 | I/O2 | A6 | A5 | I/O11 | I/O10 |
| D | V _{cc} | I/O4 | A7 | NC | I/O12 | GND |
| E | GND | I/O5 | A16 | NC | I/O13 | V _{cc} |
| F | I/O7 | I/O6 | A15 | A14 | I/O14 | I/O15 |
| G | I/O8 | /WE | A13 | A12 | NC | I/O16 |
| H | NC | A11 | A10 | A9 | A8 | NC |

- A0 - A16 : Address inputs
- I/O1 - I/O16 : Data inputs / outputs
- /CS : Chip Select
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- V_{cc} : Power supply
- GND : Ground
- NC : No Connection

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



Truth Table

| /CS | /OE | /WE | /LB | /UB | Mode | I/O | | Supply current |
|-----|-----|-----|-----|-----|------------------|------------------|------------------|------------------|
| | | | | | | I/O1 - I/O8 | I/O9 - I/O16 | |
| H | × | × | × | × | Not selected | High impedance | High impedance | I _{SB} |
| × | × | × | H | H | Not selected | High impedance | High impedance | |
| L | H | H | L | × | Output disable | High impedance | High impedance | I _{CCA} |
| | | | × | L | Output disable | High impedance | High impedance | |
| | L | H | L | L | Word read | D _{OUT} | D _{OUT} | |
| | | | L | H | Lower byte read | D _{OUT} | High impedance | |
| | | | H | L | Upper byte read | High impedance | D _{OUT} | |
| | × | L | L | L | Word write | D _{IN} | D _{IN} | |
| | | | L | H | Lower byte write | D _{IN} | High impedance | |
| | | | H | L | Upper byte write | High impedance | D _{IN} | |

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Product | Rating | Unit |
|-------------------------------|------------------|----------------------------------|---|------|
| Supply voltage | V _{CC} | μPD442002-BBxxX, μPD442002-BCxxX | -0.5 ^{Note} to +4.0 | V |
| | | μPD442002-DDxxX | -0.5 ^{Note} to +2.7 | |
| Input / Output voltage | V _T | μPD442002-BBxxX, μPD442002-BCxxX | -0.5 ^{Note} to V _{CC} +0.4 (4.0 V MAX.) | V |
| | | μPD442002-DDxxX | -0.5 ^{Note} to V _{CC} +0.4 (2.7 V MAX.) | |
| Operating ambient temperature | T _A | | -25 to +85 | °C |
| Storage temperature | T _{stg} | | -55 to +125 | °C |

Note -3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Condition | μPD442002-BBxxX | | μPD442002-BCxxX | | μPD442002-DDxxX | | Unit |
|-------------------------------|-----------------|---------------------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Supply voltage | V _{CC} | | 2.7 | 3.6 | 2.2 | 3.6 | 1.8 | 2.2 | V |
| High level input voltage | V _{IH} | 2.7 V ≤ V _{CC} ≤ 3.6 V | 2.4 | V _{CC} +0.4 | 2.4 | V _{CC} +0.4 | - | - | V |
| | | 2.2 V ≤ V _{CC} < 2.7 V | - | - | 2.0 | V _{CC} +0.3 | - | - | |
| | | 1.8 V ≤ V _{CC} < 2.2 V | - | - | - | - | 1.6 | V _{CC} +0.2 | |
| Low level input voltage | V _{IL} | | -0.3 ^{Note} | +0.5 | -0.3 ^{Note} | +0.4 | -0.2 ^{Note} | +0.2 | V |
| Operating ambient temperature | T _A | | -25 | +85 | -25 | +85 | -25 | +85 | °C |

Note -1.0 V (MIN.) (Pulse width : 20 ns)

Capacitance (T_A = 25°C, f = 1 MHz)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|----------------------------|------------------|------------------------|------|------|------|------|
| Input capacitance | C _{IN} | V _{IN} = 0 V | | | 8 | pF |
| Input / Output capacitance | C _{I/O} | V _{I/O} = 0 V | | | 10 | pF |

Remarks 1. V_{IN} : Input voltage

V_{I/O} : Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

| Parameter | Symbol | Test condition | | μPD442002-BBxxX | | | Unit |
|----------------------------|--|---|--------------------|-----------------|------|------|------|
| | | | | MIN. | TYP. | MAX. | |
| Input leakage current | I _{LI} | V _{IN} = 0 V to V _{CC} | | -1.0 | | +1.0 | μA |
| I/O leakage current | I _{LO} | V _{I/O} = 0 V to V _{CC} , /CS = V _{IH} or /WE = V _{IL} or /OE = V _{IH} | | -1.0 | | +1.0 | μA |
| ★ Operating supply current | I _{CCA1} | /CS = V _{IL} , I _{I/O} = 0 mA, Minimum cycle time | Cycle time = 50 ns | | - | 40 | mA |
| | | | Cycle time = 55 ns | | - | 35 | |
| | | | Cycle time ≥ 70 ns | | - | 30 | |
| | I _{CCA2} | /CS = V _{IL} , I _{I/O} = 0 mA, Cycle time = ∞ | | - | 4 | | |
| I _{CCA3} | /CS ≤ 0.2 V, Cycle time = 1 μs, I _{I/O} = 0 mA, V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V | | - | 4 | | | |
| ★ Standby supply current | I _{SB} | /CS = V _{IH} or /LB = /UB = V _{IH} | | | - | 0.6 | mA |
| | I _{SB1} | /CS ≥ V _{CC} - 0.2 V | | | 0.3 | 4 | |
| | I _{SB2} | /LB = /UB ≥ V _{CC} - 0.2 V, /CS ≤ 0.2 V | | | 0.3 | 4 | |
| High level output voltage | V _{OH} | I _{OH} = -0.5 mA | | 2.4 | | | V |
| Low level output voltage | V _{OL} | I _{OL} = 1.0 mA | | | | 0.4 | V |

Remarks 1. V_{IN} : Input voltage

V_{I/O} : Input / Output voltage

2. These DC characteristics are in common regardless of product classification.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

| Parameter | Symbol | Test condition | μPD442002-BCxxX | | | μPD442002-DDxxX | | | Unit | |
|---------------------------|-------------------|---|-------------------------|------|------|-----------------|------|------|------|-----|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | |
| Input leakage current | I _{LI} | V _{IN} = 0 V to V _{CC} | -1.0 | | +1.0 | -1.0 | | +1.0 | μA | |
| I/O leakage current | I _{LO} | V _{I/O} = 0 V to V _{CC} , /CS = V _{IH} or /WE = V _{IL} or /OE = V _{IH} | -1.0 | | +1.0 | -1.0 | | +1.0 | μA | |
| Operating supply current | I _{CCA1} | /CS = V _{IL} , I _{I/O} = 0 mA, Minimum cycle time | V _{CC} ≤ 2.7 V | - | 30 | - | - | - | mA | |
| | | | V _{CC} ≤ 2.2 V | - | - | - | - | 15 | | |
| | | | | - | 4 | - | - | - | | |
| | I _{CCA2} | /CS = V _{IL} , I _{I/O} = 0 mA, Cycle time = ∞ | V _{CC} ≤ 2.7 V | - | 2 | - | - | - | | |
| | | | V _{CC} ≤ 2.2 V | - | - | - | - | 1 | | |
| | | | | - | 4 | - | - | - | | |
| | I _{CCA3} | /CS ≤ 0.2 V, Cycle time = 1 μs, I _{I/O} = 0 mA, V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V | V _{CC} ≤ 2.7 V | - | 3 | - | - | - | | |
| | | | V _{CC} ≤ 2.2 V | - | - | - | - | 3 | | |
| | | | | - | 4 | - | - | - | | |
| Standby supply current | I _{SB} | /CS = V _{IH} or /LB = /UB = V _{IH} | V _{CC} ≤ 2.7 V | - | 0.6 | - | - | - | mA | |
| | | | V _{CC} ≤ 2.2 V | - | - | - | - | 0.6 | | |
| | | | | 0.3 | 4 | - | - | - | | |
| | I _{SB1} | /CS ≥ V _{CC} - 0.2 V | V _{CC} ≤ 2.7 V | 0.25 | 3.5 | - | - | - | μA | |
| | | | V _{CC} ≤ 2.2 V | - | - | 0.2 | 3 | - | | |
| | | | | 0.3 | 4 | - | - | - | | |
| | I _{SB2} | /LB = /UB ≥ V _{CC} - 0.2 V, /CS ≤ 0.2 V | V _{CC} ≤ 2.7 V | 0.25 | 3.5 | - | - | - | μA | |
| | | | V _{CC} ≤ 2.2 V | - | - | 0.2 | 3 | - | | |
| | | | | 0.3 | 4 | - | - | - | | |
| High level output voltage | V _{OH} | I _{OH} = -0.5 mA | 2.4 | | | - | | | V | |
| | | | V _{CC} ≤ 2.7 V | 1.8 | | | - | | | |
| | | | V _{CC} ≤ 2.2 V | - | | 1.5 | | | | |
| Low level output voltage | V _{OL} | I _{OL} = 1.0 mA | | | 0.4 | | | - | V | |
| | | | V _{CC} ≤ 2.7 V | | | 0.4 | | | | - |
| | | | V _{CC} ≤ 2.2 V | | | - | | | | 0.4 |

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Remarks 1. V_{IN} : Input voltage

V_{I/O} : Input / Output voltage

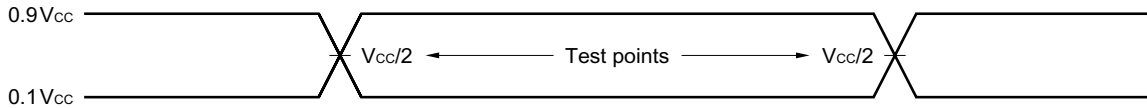
2. These DC characteristics are in common regardless of product classification.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

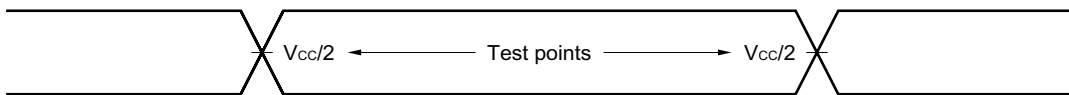
AC Test Conditions

[μ PD442002-BB55X, μ PD442002-BB70X, μ PD442002-BB85X]

Input Waveform (Rise and Fall Time \leq 5 ns)



Output Waveform

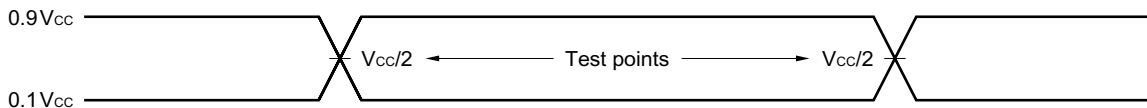


Output Load

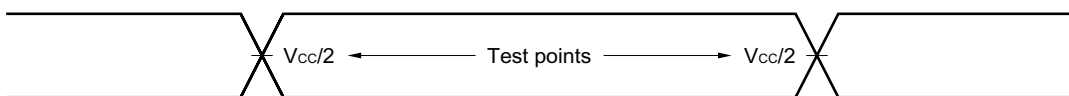
1TTL + 50 pF

[μ PD442002-BC70X, μ PD442002-BC85X, μ PD442002-BC10X]

Input Waveform (Rise and Fall Time \leq 5 ns)



Output Waveform

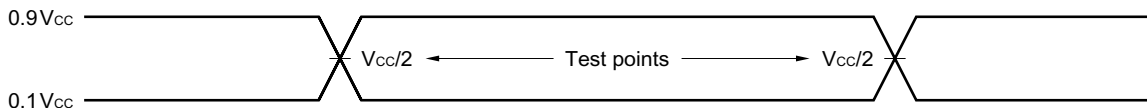


Output Load

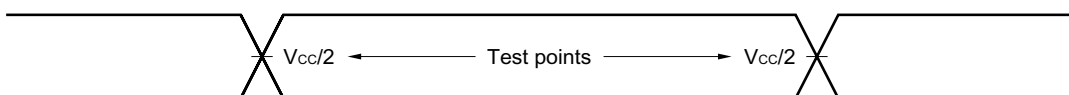
1TTL + 30 pF

[μ PD442002-DD85X, μ PD442002-DD10X, μ PD442002-DD12X]

Input Waveform (Rise and Fall Time \leq 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

★ Read Cycle (1/3) (BB version)

| Parameter | Symbol | μPD442002-BB55X | | | | μPD442002 | | μPD442002 | | Unit | Condition |
|--------------------------------------|------------------|-------------------------|------|------|------|-----------|------|-----------|------|------|-----------|
| | | V _{CC} ≥ 3.0 V | | | | -BB70X | | -BB85X | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | t _{RC} | 50 | | 55 | | 70 | | 85 | | ns | |
| Address access time | t _{AA} | | 50 | | 55 | | 70 | | 85 | ns | Note 1 |
| /CS access time | t _{ACS} | | 50 | | 55 | | 70 | | 85 | ns | |
| /OE to output valid | t _{OE} | | 30 | | 30 | | 35 | | 40 | ns | |
| /LB, /UB to output valid | t _{BA} | | 50 | | 55 | | 70 | | 85 | ns | |
| Output hold from address change | t _{OH} | 10 | | 10 | | 10 | | 10 | | ns | |
| /CS to output in low impedance | t _{LZ} | 10 | | 10 | | 10 | | 10 | | ns | Note 2 |
| /OE to output in low impedance | t _{OLZ} | 5 | | 5 | | 5 | | 5 | | ns | |
| /LB, /UB to output in low impedance | t _{BLZ} | 10 | | 10 | | 10 | | 10 | | ns | |
| /CS to output in high impedance | t _{HZ} | | 20 | | 20 | | 25 | | 30 | ns | |
| /OE to output in high impedance | t _{OHZ} | | 20 | | 20 | | 25 | | 30 | ns | |
| /LB, /UB to output in high impedance | t _{BHZ} | | 20 | | 20 | | 25 | | 30 | ns | |

- Notes**
1. The output load is 1TTL + 50 pF.
 2. The output load is 1TTL + 5 pF.

Read Cycle (2/3) (BC version)

| Parameter | Symbol | μPD442002 | | μPD442002 | | μPD442002 | | Unit | Condition |
|--------------------------------------|------------------|-----------|------|-----------|------|-----------|------|------|-----------|
| | | -BC70X | | -BC85X | | -BC10X | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | t _{RC} | 70 | | 85 | | 100 | | ns | |
| Address access time | t _{AA} | | 70 | | 85 | | 100 | ns | Note 1 |
| /CS access time | t _{ACS} | | 70 | | 85 | | 100 | ns | |
| /OE to output valid | t _{OE} | | 35 | | 40 | | 50 | ns | |
| /LB, /UB to output valid | t _{BA} | | 70 | | 85 | | 100 | ns | |
| Output hold from address change | t _{OH} | 10 | | 10 | | 10 | | ns | |
| /CS to output in low impedance | t _{LZ} | 10 | | 10 | | 10 | | ns | Note 2 |
| /OE to output in low impedance | t _{OLZ} | 5 | | 5 | | 5 | | ns | |
| /LB, /UB to output in low impedance | t _{BLZ} | 10 | | 10 | | 10 | | ns | |
| /CS to output in high impedance | t _{HZ} | | 25 | | 30 | | 35 | ns | |
| /OE to output in high impedance | t _{OHZ} | | 25 | | 30 | | 35 | ns | |
| /LB, /UB to output in high impedance | t _{BHZ} | | 25 | | 30 | | 35 | ns | |

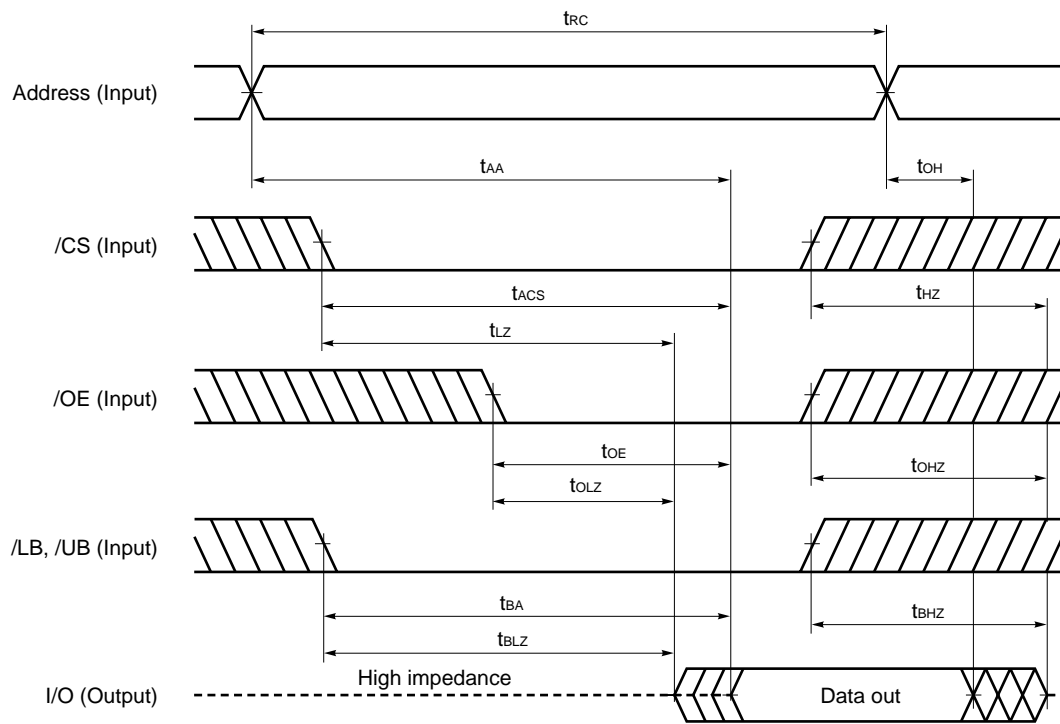
- Notes**
1. The output load is 1TTL + 30 pF.
 2. The output load is 1TTL + 5 pF.

Read Cycle (3/3) (DD version)

| Parameter | Symbol | μPD442002 -DD85X | | μPD442002 -DD10X | | μPD442002 -DD12X | | Unit | Condition |
|--------------------------------------|------------------|---------------------|------|---------------------|------|---------------------|------|------|---------------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | t _{RC} | 85 | | 100 | | 120 | | ns | |
| Address access time | t _{AA} | | 85 | | 100 | | 120 | ns | Note 1 |
| /CS access time | t _{ACS} | | 85 | | 100 | | 120 | ns | |
| /OE to output valid | t _{OE} | | 40 | | 50 | | 60 | ns | |
| /LB, /UB to output valid | t _{BA} | | 85 | | 100 | | 120 | ns | |
| Output hold from address change | t _{OH} | 10 | | 10 | | 10 | | ns | |
| /CS to output in low impedance | t _{LZ} | 10 | | 10 | | 10 | | ns | Note 2 |
| /OE to output in low impedance | t _{OLZ} | 5 | | 5 | | 5 | | ns | |
| /LB, /UB to output in low impedance | t _{BLZ} | 10 | | 10 | | 10 | | ns | |
| /CS to output in high impedance | t _{HZ} | | 30 | | 35 | | 40 | ns | |
| /OE to output in high impedance | t _{OHZ} | | 30 | | 35 | | 40 | ns | |
| /LB, /UB to output in high impedance | t _{BHZ} | | 30 | | 35 | | 40 | ns | |

- Notes**
1. The output load is 1TTL + 30 pF.
 2. The output load is 1TTL + 5 pF.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

★ Write Cycle (1/3) (BB version)

| Parameter | Symbol | μPD442002-BB55X | | | | μPD442002 | | μPD442002 | | Unit | Condition |
|---------------------------------|------------------|-------------------------|------|------|------|-----------|------|-----------|------|------|-------------|
| | | V _{CC} ≥ 3.0 V | | | | -BB70X | | -BB85X | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | t _{WC} | 50 | | 55 | | 70 | | 85 | | ns | |
| /CS to end of write | t _{CW} | 45 | | 50 | | 55 | | 70 | | ns | |
| /LB, /UB to end of write | t _{BW} | 45 | | 50 | | 55 | | 70 | | ns | |
| Address valid to end of write | t _{AW} | 45 | | 50 | | 55 | | 70 | | ns | |
| Address setup time | t _{AS} | 0 | | 0 | | 0 | | 0 | | ns | |
| Write pulse width | t _{WP} | 40 | | 45 | | 50 | | 55 | | ns | |
| Write recovery time | t _{WR} | 0 | | 0 | | 0 | | 0 | | ns | |
| Data valid to end of write | t _{DW} | 25 | | 25 | | 30 | | 35 | | ns | |
| Data hold time | t _{DH} | 0 | | 0 | | 0 | | 0 | | ns | |
| /WE to output in high impedance | t _{WHZ} | | 20 | | 20 | | 25 | | 30 | ns | Note |
| Output active from end of write | t _{OW} | 5 | | 5 | | 5 | | 5 | | ns | |

Note The output load is 1TTL + 5 pF.

Write Cycle (2/3) (BC version)

| Parameter | Symbol | μPD442002 | | μPD442002 | | μPD442002 | | Unit | Condition |
|---------------------------------|------------------|-----------|------|-----------|------|-----------|------|------|-------------|
| | | -BC70X | | -BC85X | | -BC10X | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | t _{WC} | 70 | | 85 | | 100 | | ns | |
| /CS to end of write | t _{CW} | 55 | | 70 | | 80 | | ns | |
| /LB, /UB to end of write | t _{BW} | 55 | | 70 | | 80 | | ns | |
| Address valid to end of write | t _{AW} | 55 | | 70 | | 80 | | ns | |
| Address setup time | t _{AS} | 0 | | 0 | | 0 | | ns | |
| Write pulse width | t _{WP} | 50 | | 55 | | 60 | | ns | |
| Write recovery time | t _{WR} | 0 | | 0 | | 0 | | ns | |
| Data valid to end of write | t _{DW} | 30 | | 35 | | 40 | | ns | |
| Data hold time | t _{DH} | 0 | | 0 | | 0 | | ns | |
| /WE to output in high impedance | t _{WHZ} | | 25 | | 30 | | 35 | ns | Note |
| Output active from end of write | t _{OW} | 5 | | 5 | | 5 | | ns | |

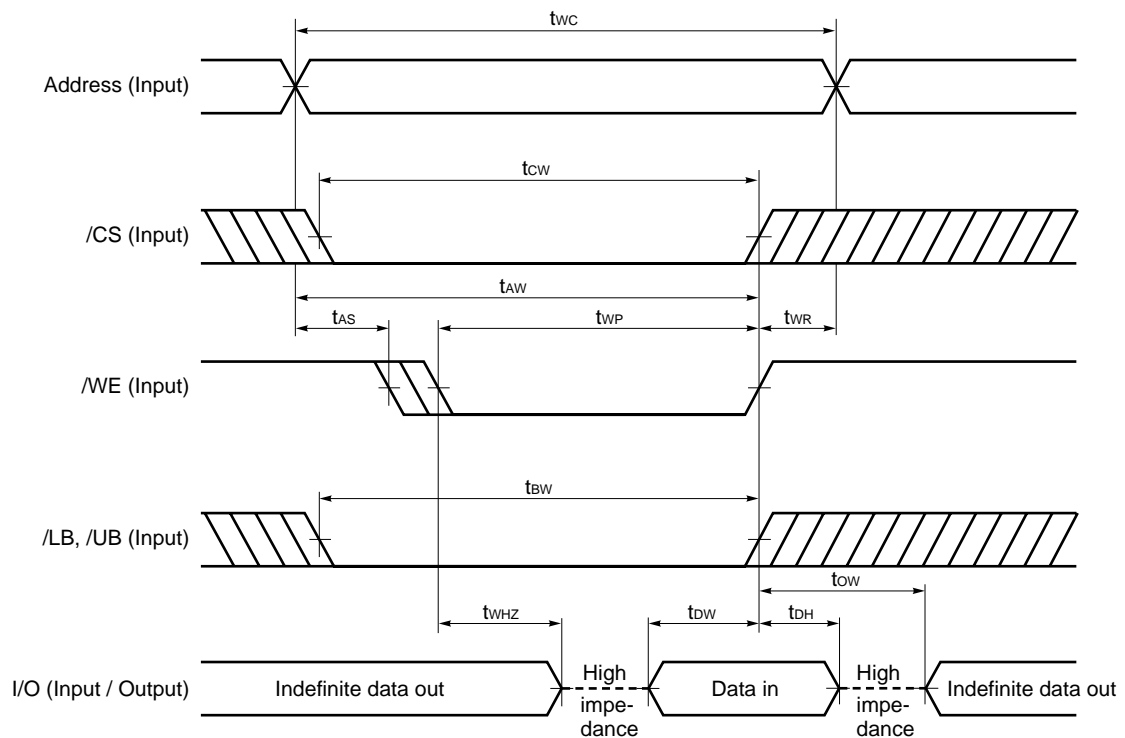
Note The output load is 1TTL + 5 pF.

Write Cycle (3/3) (DD version)

| Parameter | Symbol | μPD442002 -DD85X | | μPD442002 -DD10X | | μPD442002 -DD12X | | Unit | Condition |
|---------------------------------|------------------|---------------------|------|---------------------|------|---------------------|------|------|-------------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | t _{WC} | 85 | | 100 | | 120 | | ns | |
| /CS to end of write | t _{CW} | 70 | | 80 | | 100 | | ns | |
| /LB, /UB to end of write | t _{BW} | 70 | | 80 | | 100 | | ns | |
| Address valid to end of write | t _{AW} | 70 | | 80 | | 100 | | ns | |
| Address setup time | t _{AS} | 0 | | 0 | | 0 | | ns | |
| Write pulse width | t _{WP} | 55 | | 60 | | 85 | | ns | |
| Write recovery time | t _{WR} | 0 | | 0 | | 0 | | ns | |
| Data valid to end of write | t _{DW} | 35 | | 40 | | 60 | | ns | |
| Data hold time | t _{DH} | 0 | | 0 | | 0 | | ns | |
| /WE to output in high impedance | t _{WHZ} | | 30 | | 35 | | 40 | ns | Note |
| Output active from end of write | t _{OW} | 5 | | 5 | | 5 | | ns | |

Note The output load is 1TTL + 5 pF.

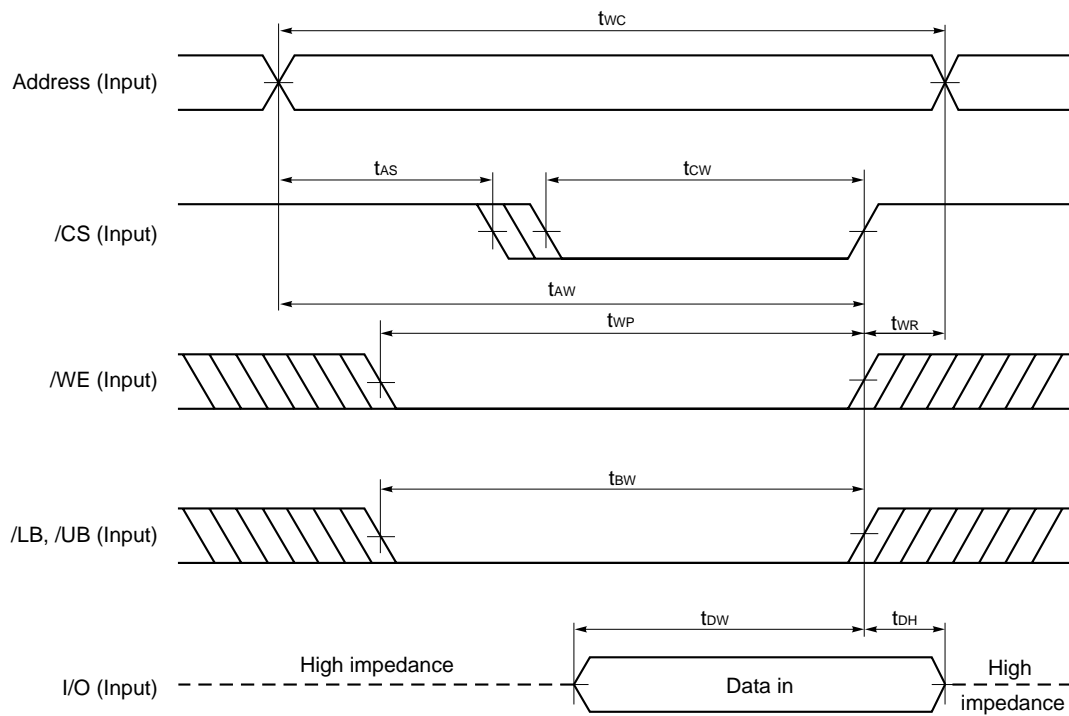
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins \overline{CS} , \overline{WE} should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

- Remarks**
1. Write operation is done during the overlap time of a low level \overline{CS} , a low level \overline{WE} and a low level \overline{LB} (or low level \overline{UB}).
 2. If \overline{CS} changes to low level at the same time or after the change of \overline{WE} to low level, the I/O pins will remain high impedance state.
 3. When \overline{WE} is at low level, the I/O pins are always high impedance. When \overline{WE} is at high level, read operation is executed. Therefore \overline{OE} should be at high level to make the I/O pins high impedance.

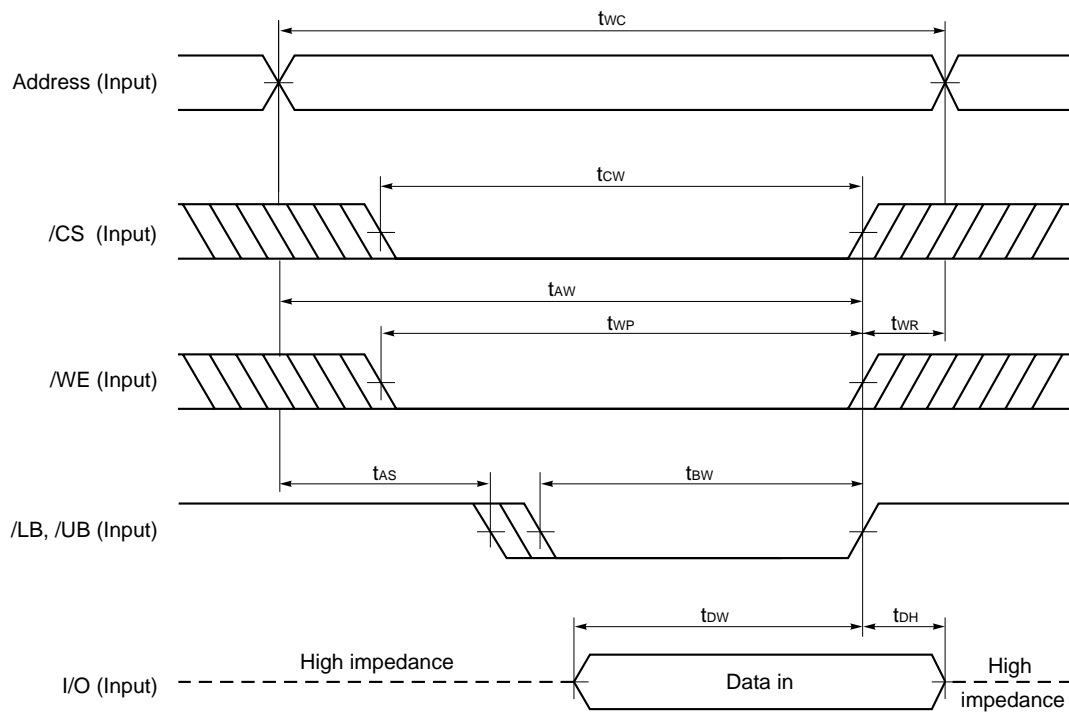
Write Cycle Timing Chart 2 (/CS Controlled)



- Cautions**
1. During address transition, at least one of pins /CS, /WE should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Write Cycle Timing Chart 3 (/LB, /UB Controlled)



- Cautions**
1. During address transition, at least one of pins /CS, /WE should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

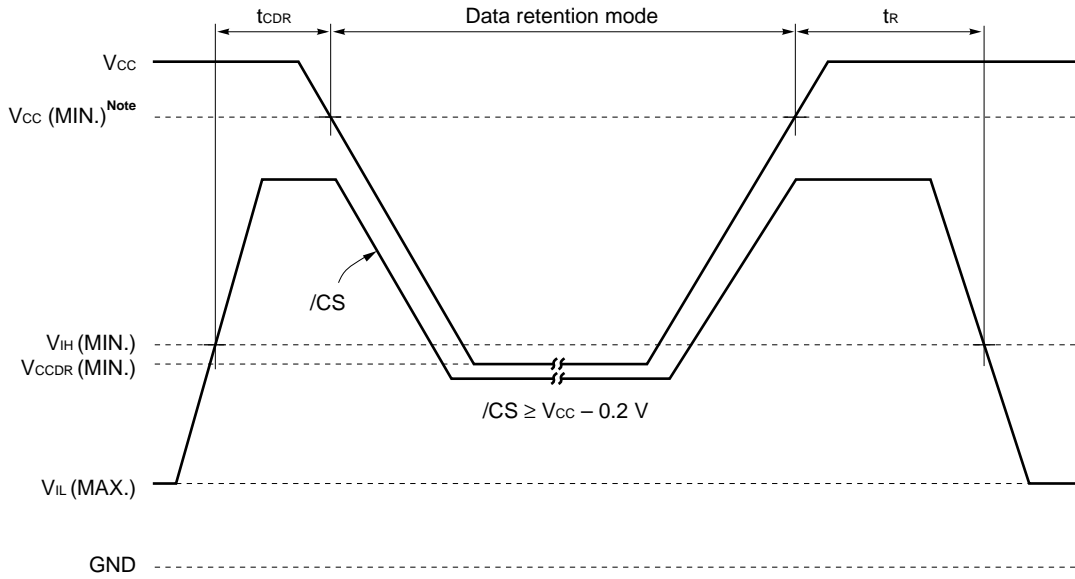
Low V_{CC} Data Retention Characteristics (T_A = -25 to +85°C)

| Parameter | Symbol | Test Condition | μPD442002 -BBxxX | | | μPD442002 -BCxxX | | | μPD442002 -DDxxX | | | Unit |
|---|--|--|---------------------------------|------|------|---------------------------------|------|------|---------------------------------|------|------|------|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Data retention supply voltage | V _{CCDR1} V _{CCDR2} | /CS ≥ V _{CC} - 0.2 V /LB = /UB ≥ V _{CC} - 0.2 V, /CS ≤ 0.2 V | 1.0 | | 3.6 | 1.0 | | 3.6 | 1.0 | | 2.2 | V |
| Data retention supply current | I _{CCDR1} I _{CCDR2} | V _{CC} = 1.2 V, /CS ≥ V _{CC} - 0.2 V V _{CC} = 1.2 V, /LB = /UB ≥ V _{CC} - 0.2 V, /CS ≤ 0.2 V | | 0.15 | 2 | | 0.15 | 2 | | 0.15 | 2 | μA |
| Chip deselection to data retention mode | t _{CDR} | | 0 | | | 0 | | | 0 | | | ns |
| Operation recovery time | t _R | | t _{RC} ^{Note} | | | t _{RC} ^{Note} | | | t _{RC} ^{Note} | | | ns |

Note t_{RC} : Read cycle time

Data Retention Timing Chart

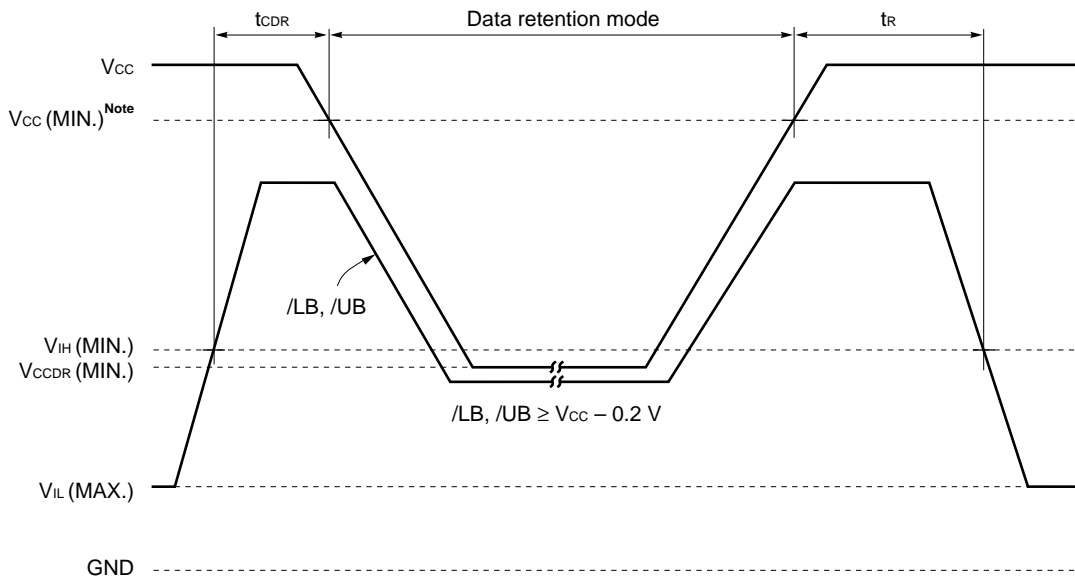
(1) /CS Controlled



Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling $/CS$, the other pins (Address, I/O, $/WE$, $/OE$, $/LB$, $/UB$) can be in high impedance state.

(2) /LB, /UB Controlled

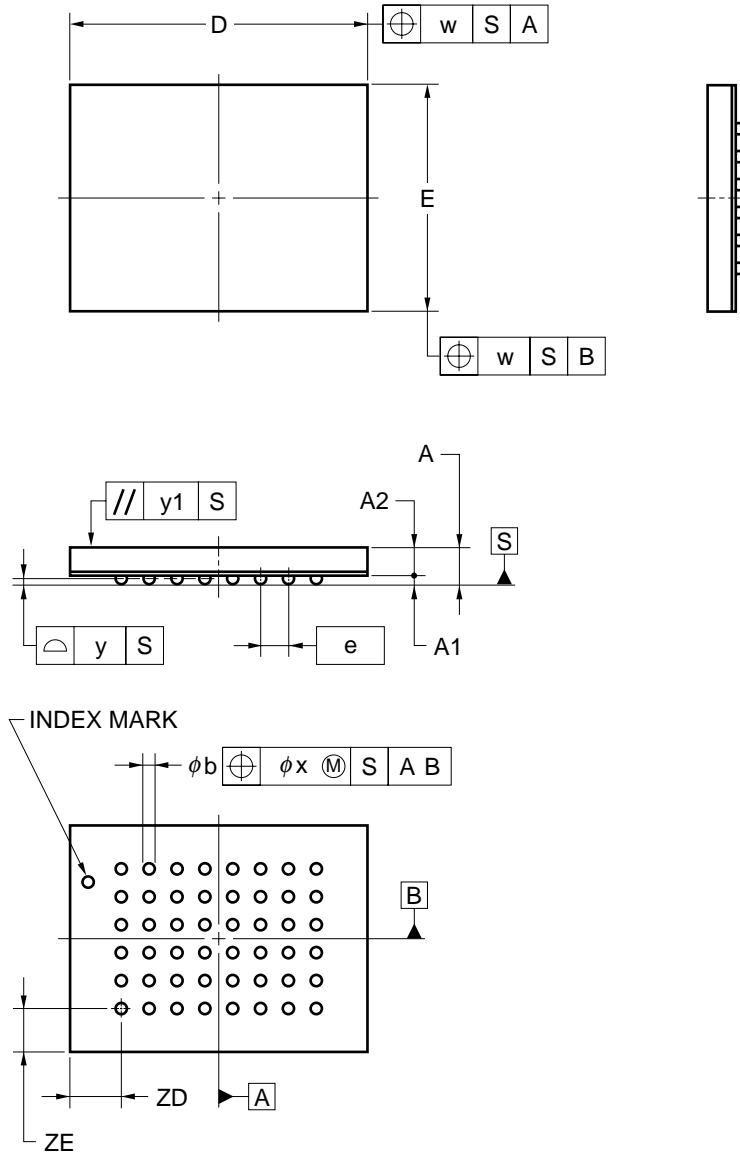


Note BB version : 2.7 V, BC version : 2.2 V, DD version : 1.8 V

Remark On the data retention mode by controlling $/LB$ and $/UB$, the input level of $/CS$ must be $\geq V_{CC} - 0.2 V$ or $\leq 0.2 V$. The other pins (Address, I/O, $/WE$, $/OE$) can be in high impedance state.

Package Drawing

48-PIN TAPE FBGA (6x8)



| ITEM | MILLIMETERS |
|------|-------------|
| D | 8.0±0.1 |
| E | 6.0±0.1 |
| w | 0.2 |
| e | 0.75 |
| A | 0.96±0.10 |
| A1 | 0.25±0.05 |
| A2 | 0.71 |
| b | 0.35±0.05 |
| x | 0.08 |
| y | 0.1 |
| y1 | 0.1 |
| ZD | 1.375 |
| ZE | 1.125 |

P48F9-75-BC1-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD442002-X.

Types of Surface Mount Device

μ PD442002F9-BBxxX-BC1 : 48-pin TAPE FBGA (6x8)

μ PD442002F9-BCxxX-BC1 : 48-pin TAPE FBGA (6x8)

μ PD442002F9-DDxxX-BC1 : 48-pin TAPE FBGA (6x8)

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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