



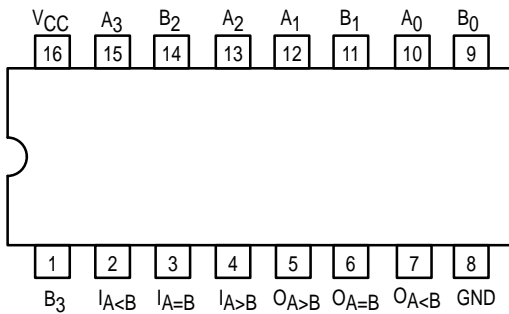
4-BIT MAGNITUDE COMPARATOR

The SN54/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0 – A_3 , B_0 – B_3); A_3 , B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}$, $O_{A<B}$, and $O_{A=B}$ Outputs Available

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

A_0 – A_3 , B_0 – B_3	Parallel Inputs
$I_{A=B}$	A = B Expander Inputs
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs
$O_{A>B}$	A Greater Than B Output (Note b)
$O_{A<B}$	B Greater Than A Output (Note b)
$O_{A=B}$	A Equal to B Output (Note b)

LOADING (Note a)

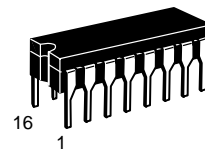
	HIGH	LOW
Parallel Inputs	1.5 U.L.	0.75 U.L.
A = B Expander Inputs	1.5 U.L.	0.75 U.L.
A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

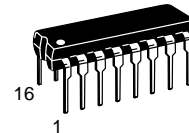
- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS85

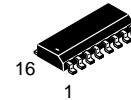
4-BIT MAGNITUDE COMPARATOR LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

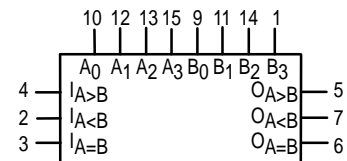


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

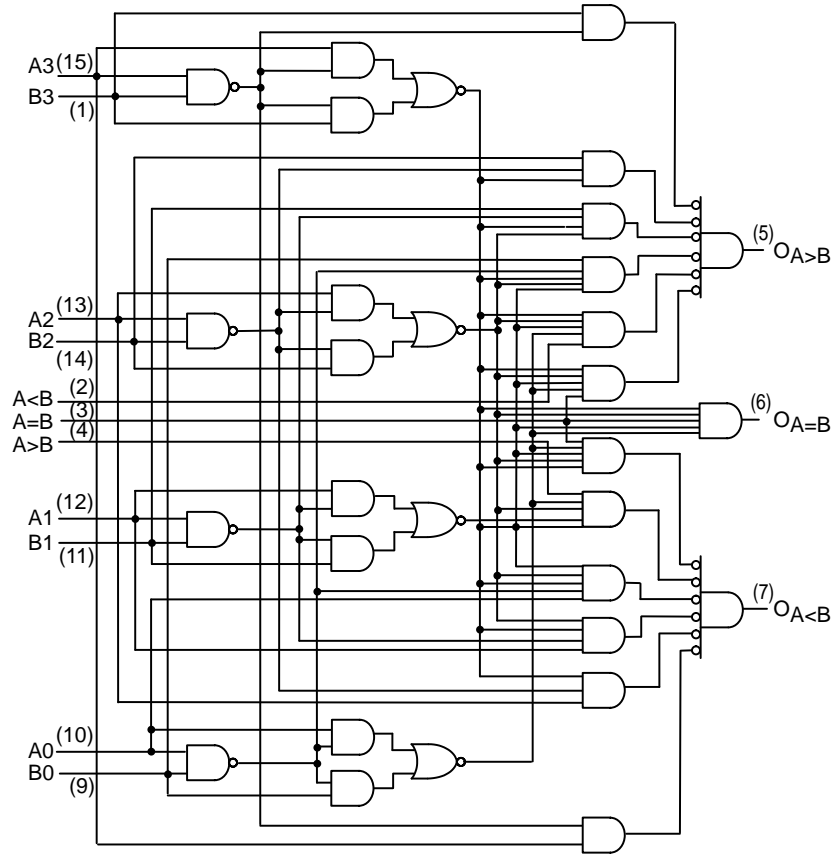
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

SN54/74LS85

LOGIC DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADE INPUTS			OUTPUTS		
A ₃ B ₃	A ₂ B ₂	A ₁ B ₁	A ₀ B ₀	I _{A>B}	I _{A<B}	I _{A=B}	O _{A>B}	O _{A<B}	O _{A=B}
A ₃ >B ₃	X	X	X	X	X	X	H	L	L
A ₃ <B ₃	X	X	X	X	X	X	L	H	L
A ₃ =B ₃	A ₂ >B ₂	X	X	X	X	X	H	L	L
A ₃ =B ₃	A ₂ <B ₂	X	X	X	X	X	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ >B ₁	X	X	X	X	H	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ <B ₁	X	X	X	X	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ >B ₀	X	X	X	H	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ <B ₀	X	X	X	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	H	L	L	H	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	L	H	L	L	H	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	X	X	H	L	L	H
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	H	H	L	L	L	L
A ₃ =B ₃	A ₂ =B ₂	A ₁ =B ₁	A ₀ =B ₀	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN54/74LS85

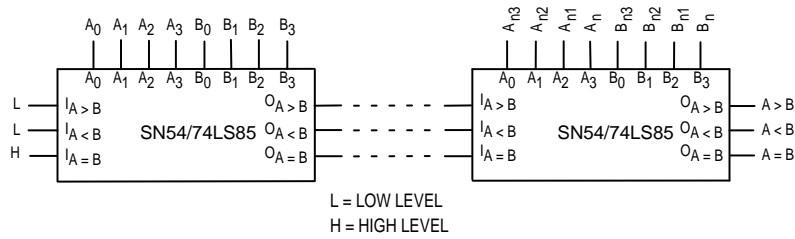


Figure 1. Comparing Two n-Bit Words

APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table 1.

Table 1

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2-6
25-120 Bits	8-31

NOTE:
The SN54/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A₀-A₃ and B₀-B₃ inputs of another SN54/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4.

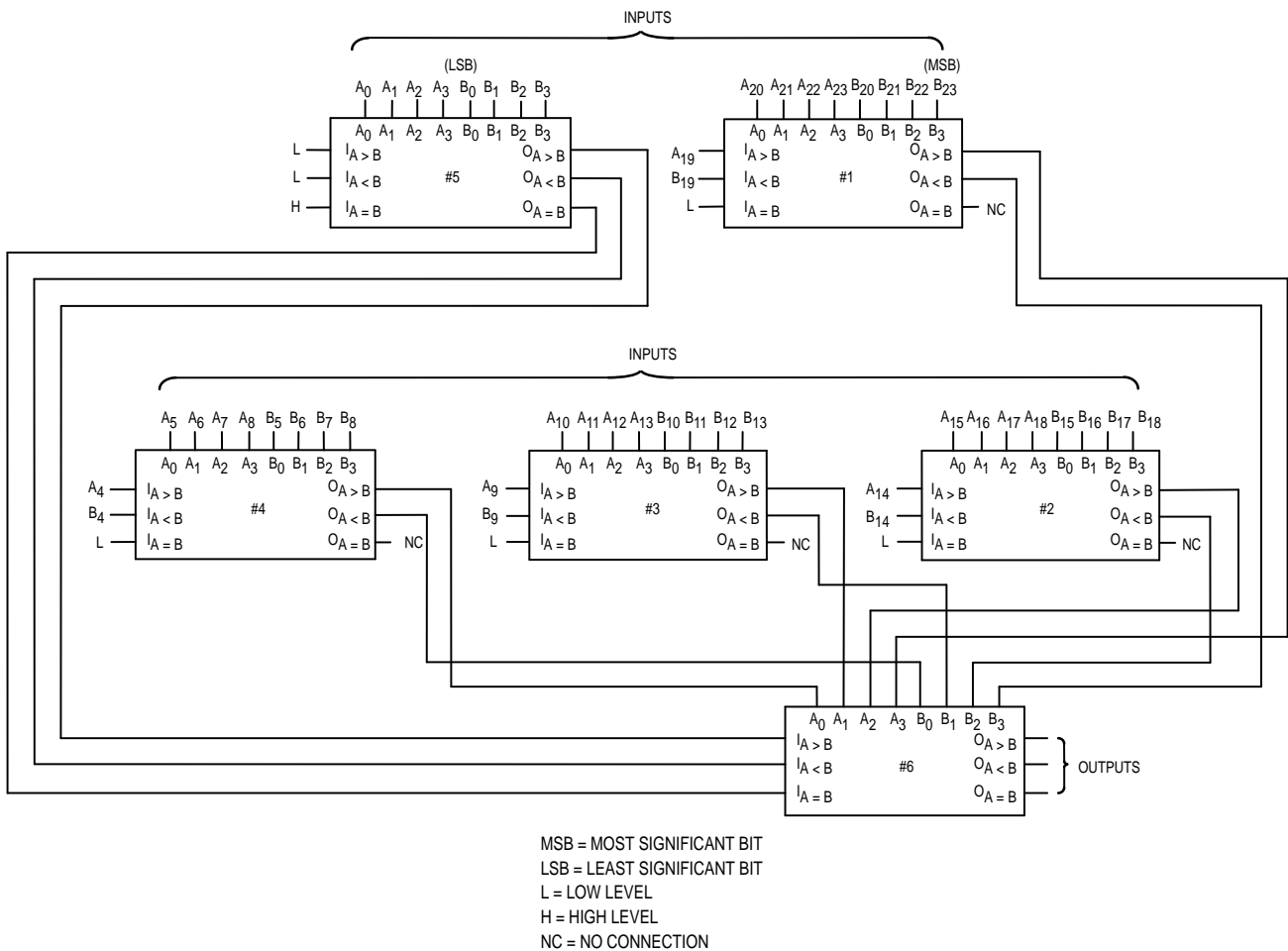


Figure 2. Comparison of Two 24-Bit Words

SN54/74LS85

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V_{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$	
V_{OH}	Output HIGH Voltage	54	2.5	3.5	V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table	
		74	2.7	3.5	V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC} \text{ MIN}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	
I_{IH}	Input HIGH Current A < B, A > B Other Inputs			20 60	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$	
	A < B, A > B Other Inputs			0.1 0.3	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$	
I_{IL}	Input LOW Current A < B, A > B Other Inputs			-0.4 -1.2	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$	
I_{OS}	Output Short Circuit Current (Note 1)	-20		-100	mA	$V_{CC} = \text{MAX}$	
I_{CC}	Power Supply Current			20	mA	$V_{CC} = \text{MAX}$	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0 \text{ V}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Any A or B to A < B, A > B		24 20	36 30	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{PLH} t_{PHL}	Any A or B to A = B		27 23	45 45	ns	
t_{PLH} t_{PHL}	A < B or A = B to A > B		14 11	22 17	ns	
t_{PLH} t_{PHL}	A = B to A = B		13 13	20 26	ns	
t_{PLH} t_{PHL}	A > B or A = B to A < B		14 11	22 17	ns	

AC WAVEFORMS

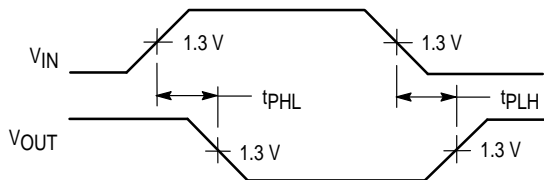


Figure 3

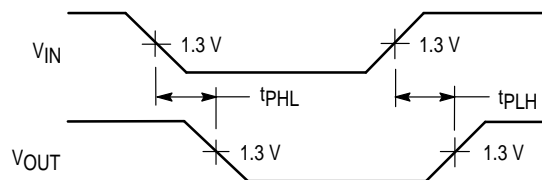


Figure 4