

## *Advance Information* **Low Voltage 1:18 Clock Distribution Chip**

The MPC940 is a 1:18 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVTTTL/LVCMOS compatible input. The 18 outputs are LVCMOS or LVTTTL compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 150ps, the MPC940 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a larger number of outputs, please consult the MPC941 data sheet.

- LVPECL or LVCMOS/LVTTTL Clock Input
- 150ps Maximum Targeted Output-to-Output Skew
- Drives Up to 36 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- 32-Lead TQFP Packaging
- 3.3V V<sub>CC</sub> Supply Voltage

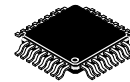
With a low output impedance ( $\approx 20\Omega$ ), in both the HIGH and LOW logic states, the output buffers of the MPC940 are ideal for driving series terminated transmission lines. More specifically, each of the 18 MPC940 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC940 has an effective fanout of 1:36 in applications where each line drives a single load. With this level of fanout, the MPC940 provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the MPC940 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS/LVTTTL input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS\_CLK\_Sel pin will select the TTL level clock input.

The MPC940 is fully 3.3V compatible. The 32-lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

**MPC940**

**LOW VOLTAGE  
1:18 CLOCK  
DISTRIBUTION CHIP**



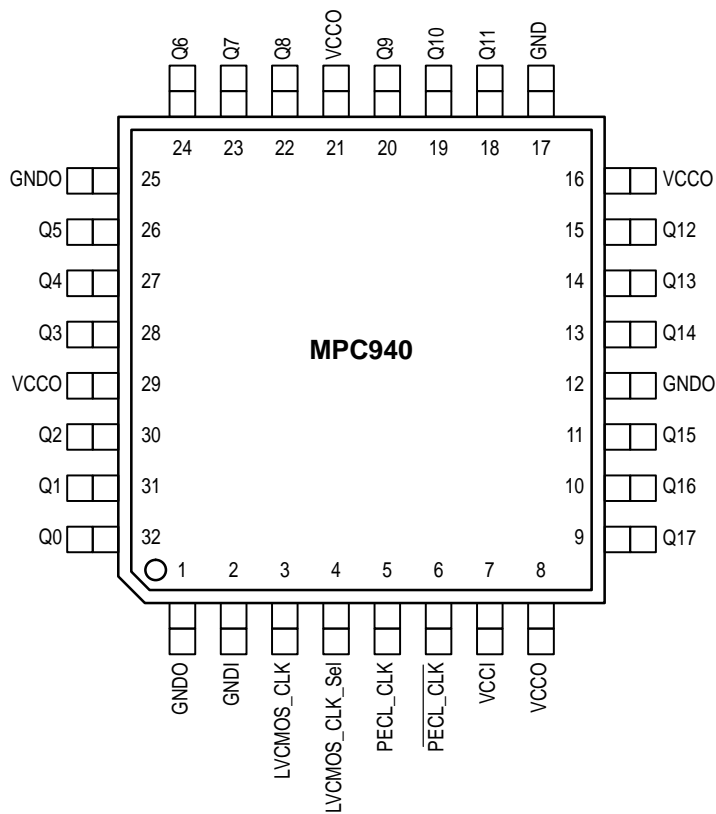
**FA SUFFIX**  
32-LEAD TQFP PACKAGE  
CASE 873A-02



LOGIC DIAGRAM



Pinout: 32-Lead TQFP (Top View)



FUNCTION TABLE

LVC MOS_CLK_Sel	Input
0	PECL_CLK
1	LVC MOS_CLK

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	−0.3	3.6	V
V <sub>I</sub>	Input Voltage	−0.3	V <sub>DD</sub> + 0.3	V
I <sub>IN</sub>	Input Current		±20	mA
T <sub>Stor</sub>	Storage Temperature Range	−40	125	°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**DC CHARACTERISTICS** (T<sub>A</sub> = 0° to 70°C, V<sub>CC</sub> = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V <sub>IH</sub>	Input HIGH Voltage PECL_CLK Other	2.135 2.0		2.42 3.60	V	
V <sub>IL</sub>	Input LOW Voltage PECL_CLK Other	1.49		1.825 0.8	V	
V <sub>PP</sub>	Peak-to-Peak Input Voltage PECL_CLK	300		1000	mV	
V <sub>CMR</sub>	Common Mode Range PECL_CLK	V <sub>CC</sub> −2.0		V <sub>CC</sub> −0.6	V	
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	I <sub>OH</sub> = −16mA, Note 1.
V <sub>OL</sub>	Output LOW Voltage			0.5	V	I <sub>OH</sub> = 16mA, Note 1.
I <sub>IN</sub>	Input Current			±100	μA	
C <sub>IN</sub>	Input Capacitance			4	pF	
C <sub>pd</sub>	Power Dissipation Capacitance		8		pF	Per Output
I <sub>CC</sub>	Maximum Quiescent Supply Current I <sub>CC</sub> L I <sub>CC</sub> H		70 140		mA	

1. The MPC940 outputs can drive series or parallel terminated 50Ω (or 50Ω to V<sub>CC</sub>/2) transmission lines on the incident edge.

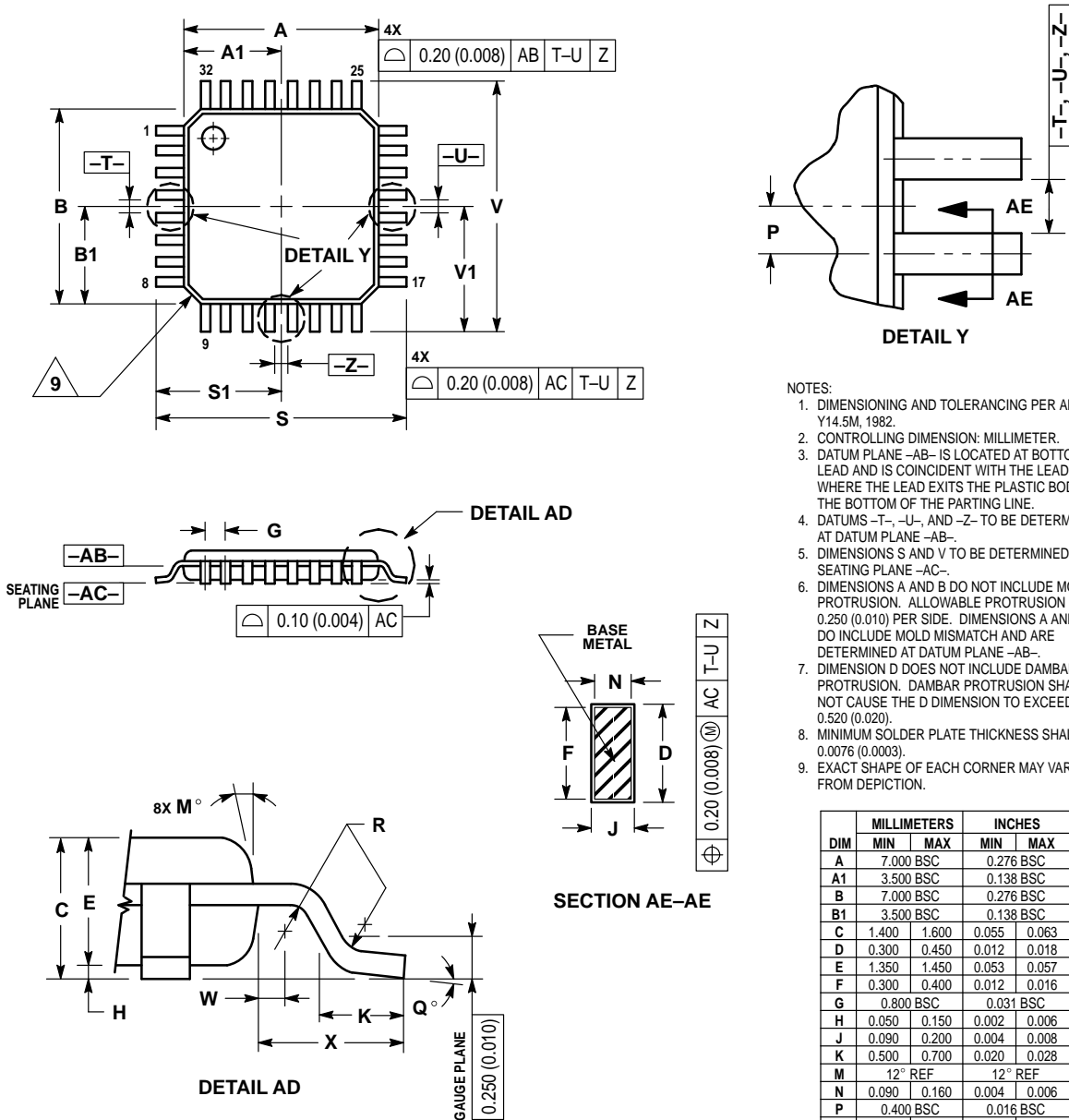
**AC CHARACTERISTICS** (T<sub>A</sub> = 0° to 70°C, V<sub>CC</sub> = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F <sub>max</sub>	Maximum Input Frequency		250		MHz	Note 1.
t <sub>pd</sub>	Propagation Delay PECL_CLK to Q TTL_CLK to Q		1.7 2.0		ns	Note 1.
t <sub>sk(o)</sub>	Output-to-Output Skew			150	ps	Note 1.
t <sub>sk(pr)</sub>	Part-to-Part Skew PECL_CLK to Q TTL_CLK to Q		800 800		ps	Notes 2., 3.
t <sub>pwo</sub>	Output Pulse Width	45		55	p%	Note 1., Measured at V <sub>CC</sub> /2
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time	0.20		1.0	ns	0.8V to 2.0V


1. Driving 50Ω transmission lines
2. Part-to-part skew at a given temperature and voltage
3. Final specification limits will be determined from matrix lot material. 800ps is the "best estimate" based on initial material and experience with previous products.

OUTLINE DIMENSIONS

FA SUFFIX  
TQFP PACKAGE  
CASE 873A-02  
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
  4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
  5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
  6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
  7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
  8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
  9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

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51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

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