Advance Information

Low Voltage PLL Clock Driver

MPC932

LOW VOLTAGE
PLL CLOCK DRIVER

FA SUFFIX
TQFP PACKAGE
CASE 873A-02

The MPC932 is a 3.3V compatible PLL based clock driver device targetted for zero delay applications. The device provides 6 outputs for driving clock loads plus a single dedicated PLL feedback clock output. The dedicated feedback output gives the user six choices of input multiplcation factors: x1, x1.25, x1.5, x2, x2.5 and x3.

- 6 Low Skew Clock Outputs
- 1 Dedicated PLL Feedback Output
- Individual Output Enable Control
- Fully Integrated PLL
- Output Frequency Up TO 120MHz
- 32–lead TQFP Packaging
- 3.3V VCC
- ±100ps Cycle–Cycle Jitter

The MPC932 provides individual output enable control. The enables are synchronized to the internal clock such that upon assertion the shut down signals will hold the clocks LOW without generating a runt pulse on the outputs. The shut down pins provide a means of powering down certain portions of a system or a means of disabling outputs when the full compliment are not required for a specific design. The shut down pins will disable the outputs when driven LOW. A common shut down pin is provided to disable all of the outputs (except the feedback output) with a single control signal.

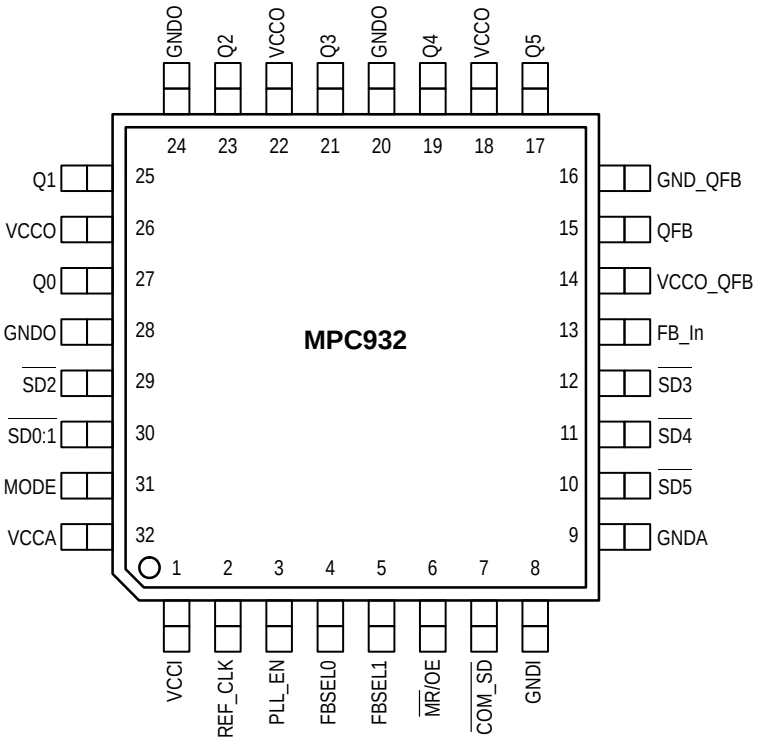
Two feedback select pins are provided to select the multiplication factor of the PLL. The MPC932 provides six multiplication factors: x1, x1.25, x1.5, x2, x2.5 and x3. In the x1.25 and x2.5 modes, the QFB output will not provide a 50% duty cycle. The phase detector of the MPC932 only monitors rising edges of its feedback signals, thus for this function a 50% duty cycle is not required. As the QFB signal can also be used to drive other clocks in a system it is important the user understand that the duty cycle will not be 50%. In the x1 and x1.5 modes the QFB output will produce 50% duty cycle signals.

The MPC932 provides two pins for use in system test and debug operations. The $\overline{\text{MR}}$/OE input will force all of the outputs into a high impedance state to allow for back driving the outputs during system test. In addition the PLL_EN pin allows the user to bypass the PLL and drive the outputs directly through the Ref_CLK input. Note the Ref_CLK signal will be routed through the dividers so that it will take several transitions on the Ref_CLK input to create a transition on the outputs.

The MPC932 is fully 3.3V compatible and requires no external loop filter components. All of the inputs are LVCMOS/LVTTL compatible and the outputs produce rail–to–rail 3.3V swings. For series terminated applications each output can drive two series terminated 50Ω transmission lines. For parallel terminated lines the device can drive terminations of 50Ω into VCC/2. The device is packaged in a 32–lead TQFP package to provide the optimum combination of performance, board density and cost.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Pinout: 32-Lead TQFP Package (Top View)

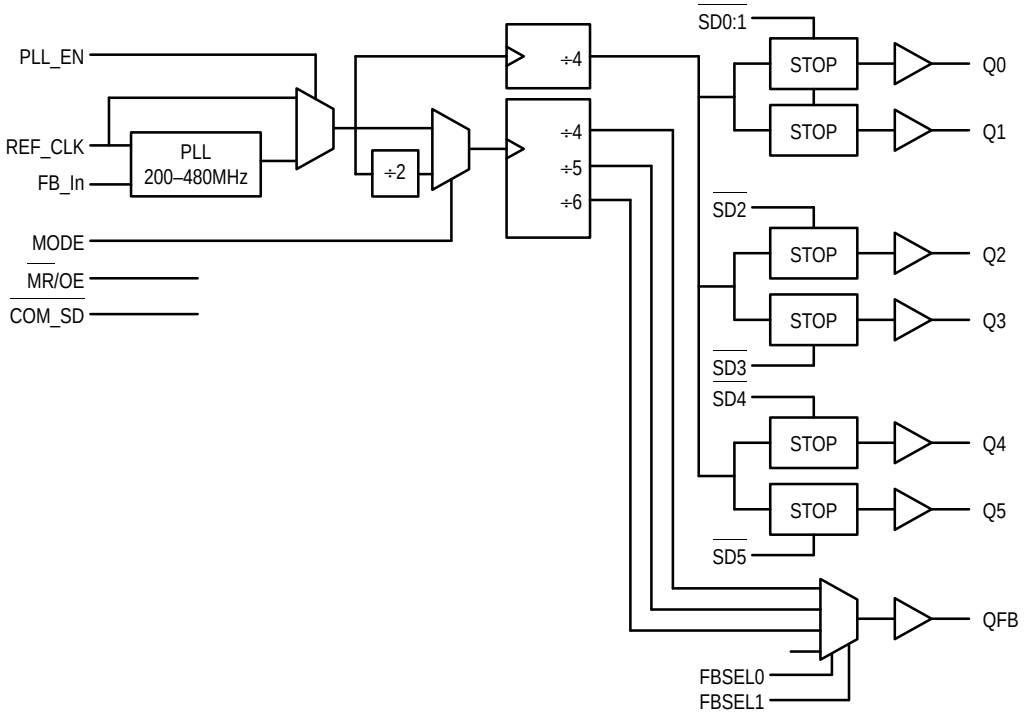


FUNCTION TABLES

$\overline{SDn}$, $\overline{COM\_SD}$	Qn
0	Held LOW
1	Enabled
PLL_En	**PLL Status**
0	Test Mode
1	PLL Enabled
$\overline{MR/OE}$	**PLL Status**
0	Disabled
1	Enabled

MODE	FBSEL1	FBSEL0	Qn	QFB
0	0	0	VCO/4	VCO/8
0	0	1	VCO/4	VCO/10
0	1	0	VCO/4	VCO/12
0	1	1	NA	NA
1	0	0	VCO/4	VCO/4
1	0	1	VCO/4	VCO/5
1	1	0	VCO/4	VCO/6
1	1	1	NA	NA

LOGIC DIAGRAM



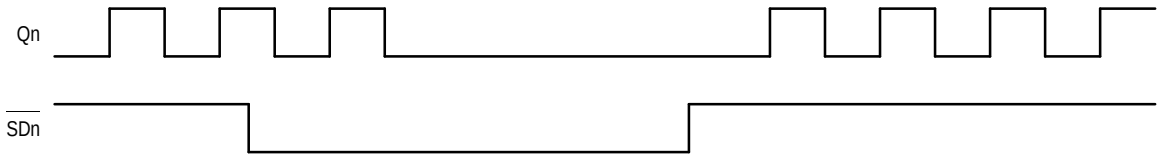


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
t_r, t_f	TCLK Input Rise/Falls		3.0	ns	
f_{ref}	Reference Input Frequency	Note 1.	Note 1.	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

1. Maximum and Maximum input reference frequency is limited by the VCO lock range and the feedback divider.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		3.6	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA (Note 2.)
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA (Note 2.)
I_{IN}	Input Current			±120	µA	Note 3.
I_{CC}	Maximum Core Supply Current			100	mA	
I_{CCPLL}	Maximum PLL Supply Current		15	20	mA	
C_{IN}				4	pF	
C_{pd}			25		pF	Per Output

2. The MPC932 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
3. Inputs have pull–up/pull–down resistors which affect input current.

MPC932 AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	Note 6.		Note 6.	MHz	
t_{os}	Output-to-Output Skew		200	300	ps	Note 4.
f_{VCO}	VCO Lock Range	200		480	MHz	
f_{max}	Maximum Output Frequency (÷4) (÷5) (÷6)			120 96 80	MHz	
t_{pd}	Reference to EXT_FB Average Delay TCLK PECL_CLK	X – 150	X	X + 150	ps	f_{ref} = 50MHz; Note 7.
t_{pw}	Output Duty Cycle (Note 4.)	$t_{CYCLE}/2$ –750	$t_{CYCLE}/2$ ±500	$t_{CYCLE}/2$ +750	ps	
t_r, t_f	Output Rise/Fall Time (Note 4.)	0.1		1.0	ns	0.8 to 2.0V
t_{PLZ}, t_{PHZ}	Output Disable Time	2.0		8.0	ns	50Ω to $V_{CC}/2$
t_{PZL}	Output Enable Time	2.0		10	ns	50Ω to $V_{CC}/2$
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		±100		ps	Note 5.
t_{lock}	Maximum PLL Lock Time			10	ms	

4. Measured with 50Ω to $V_{CC}/2$ termination.
5. See Applications Info section for more jitter information.
6. Input reference frequency is bounded by VCO lock range and feedback divide selection.
7. t_{pd} measurement uses the averaging feature of the oscilliscope to remove the jitter component.

APPLICATIONS INFORMATION

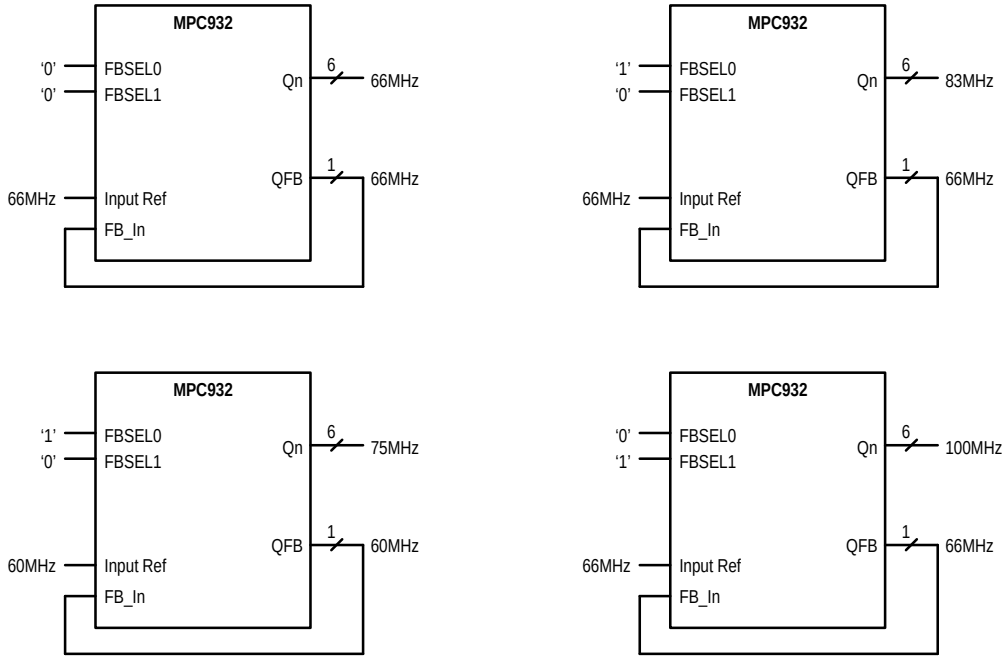


Figure 2. MPC932 Potential Configurations
(Mode = 1)

Power Supply Filtering

The MPC932 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC932 provides separate power supplies for the output buffers (V_{CCO}) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC932.

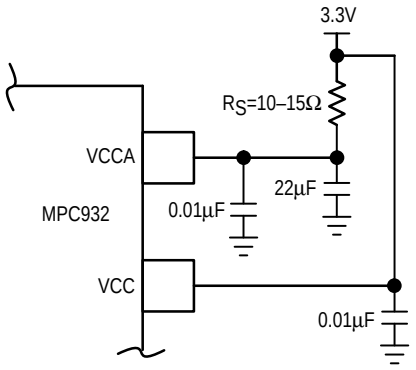


Figure 3. Power Supply Filter

Figure 3 illustrates a typical power supply filter scheme. The MPC932 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC932. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC932 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC932 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC932 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC932 clock driver is effectively doubled due to its capability to drive multiple lines.

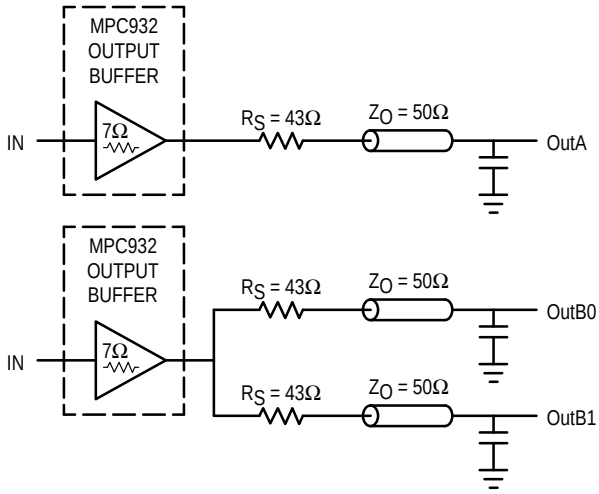


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC932 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC932. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the

line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / (Rs + Ro +Zo))

Zo = 50Ω || 50Ω
Rs = 43Ω || 43Ω
Ro = 7Ω

VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)
= 1.40V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

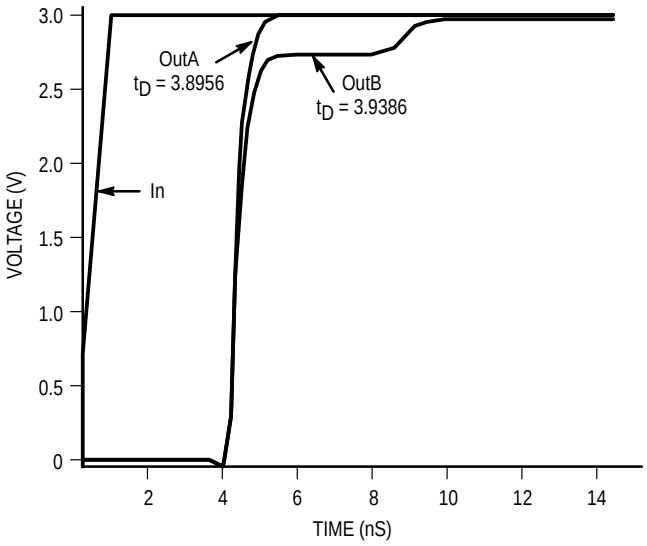
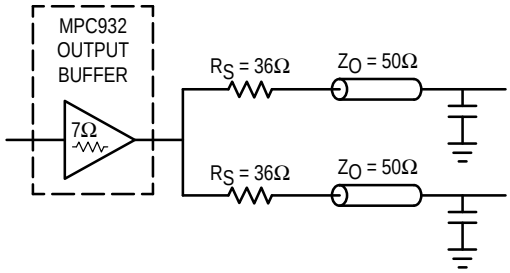


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



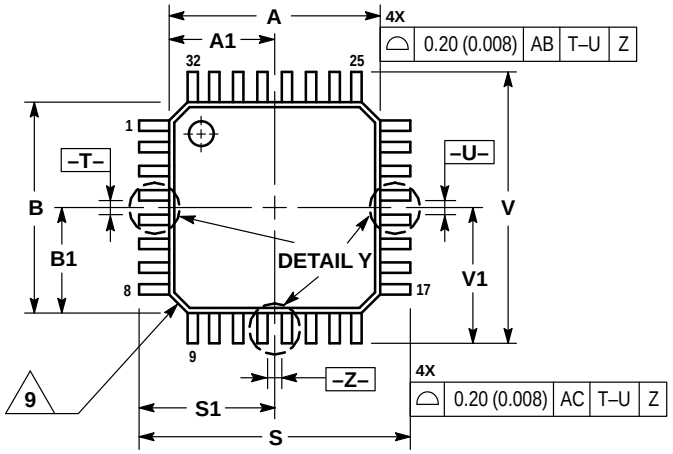
7Ω + 36Ω || 36Ω = 50Ω || 50Ω
25Ω = 25Ω

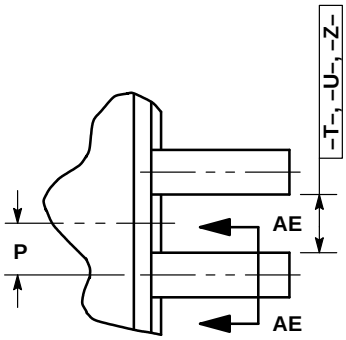
Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

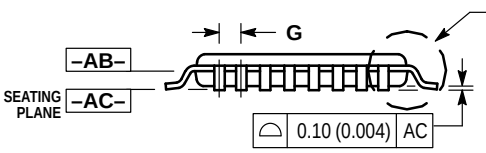
OUTLINE DIMENSIONS

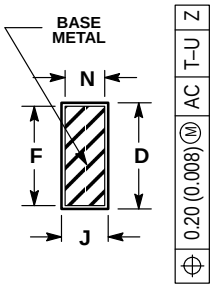
FA SUFFIX
TQFP PACKAGE
CASE 873A-02
ISSUE A



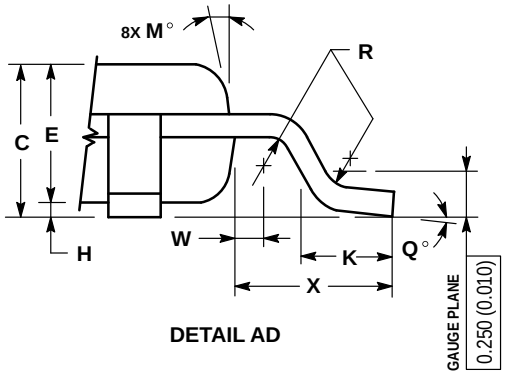


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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