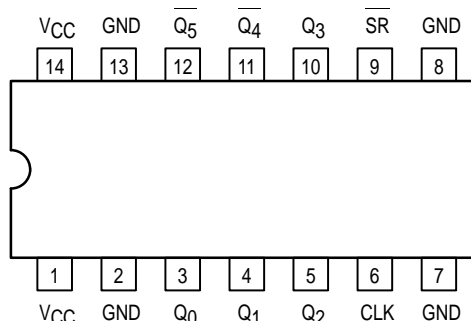


Low Skew CMOS Clock Driver With Reset

The MC88914 is a high-speed, low power, hex divide-by-two D-type flip-flop with matched propagation delays, an internal power-on-reset, and external synchronous reset. With TTL compatible buffered clock and external reset inputs that are common to all flip-flops, the MC88914 is ideal for use in high-frequency systems as a clock driver, providing multiple outputs that are synchronous.

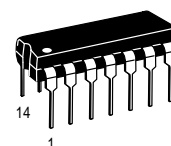
- Power-on-Reset and External Synchronous Reset
- TTL Compatible Positive Edge-Triggered Clock
- Matched Outputs for Synchronous Applications
- Outputs Source/Sink 24mA
- Part-to-Part Skew of Less Than 3.0ns
- Guaranteed Rise and Fall Times for a Given Capacitive Load

Pinout: 14-Lead Plastic (Top View)

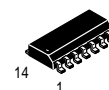


MC88914

**LOW SKEW CMOS
CLOCK DRIVER
WITH RESET**

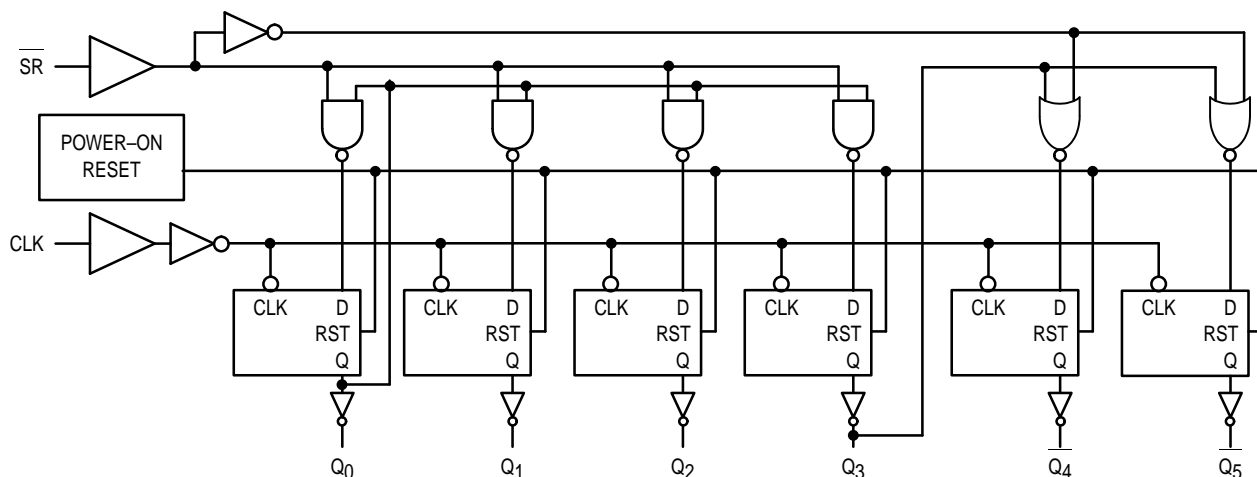


N SUFFIX
PLASTIC PACKAGE
CASE 646-06



D SUFFIX
PLASTIC PACKAGE
CASE 751A-03

LOGIC DIAGRAM



NOTE: This diagram is provided only for understanding of logic operation and should **not** be used to estimate propagation delays



DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter		Unit	Condition
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$, $T_A = 25^\circ C$
I_{CCT}	Maximum Additional I_{CC} /Input	1.5	mA	$V_{IN} = V_{CC} - 2.1V$ $V_{CC} = 5.5V$, $T_A = \text{Worst Case}$

DC CHARACTERISTICS

Symbol	Parameter	V _{CC}	T _A = +25°C		T _A = −40 to +85°C	Unit	Conditions
			Typ	Guaranteed Max			
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V _{OH}	Minimum High Level	4.5	4.49	4.4	4.4	V	I _{OUT} = −50μA
		5.5	5.49	5.4	5.4		
		4.5		3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = −24mA −24mA
		5.5		4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50μA
		5.5	0.001	0.1	0.1		
		4.5		0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} I _{OH} = 24mA 24mA
		5.5		0.36	0.44		
I _{IN}	Maximum Input	5.5		±0.1	±0.1	μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} −2.1V
I _{OLD}	Minimum Dynamic Output Current**	5.5			75	mA	V _{OLD} = 1.65V
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85V

* All outputs loaded; thresholds on inputs associated with output under test.

** Maximum test duration 20ms, one output at a time.

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ C$ $C_L = 50$ pF		$T_A = -40$ to $+85^\circ C$ $C_L = 50$ pF		Unit
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle)	5.0	110		110		MHz
t_{PLH} , t_{PHL}	Propagation Delay CLK to Q_n , Q_n	5.0	4.0	9.0	4.0	11	ns
t_{PV}	Propagation Delay Variation CLK to Q_n , Q_n (see Note 1)	5.0		3.0		3.0	ns
t_{PS}	Propagation Delay Skew (Q_n , Q_n) $ t_{PHL} \text{ Actual} - t_{PLH} \text{ Actual} $	5.0		1.0		1.0	ns
t_{OS}	Output-to-Output Skew (Q_n , Q_n) $ t_{p Q_n} - t_{p Q_m} $ (see Note 2)	5.0		1.0		1.0	ns
t_{rise} t_{fall}	Rise/Fall Time for Q_n , Q_n ($0.2 \times V_{CC}$ to $0.8 \times V_{CC}$)	5.0		3.0		4.0	ns

- For a given set of conditions (i.e., capacitive load, temperature and V_{CC}) the variation from device to device is guaranteed to be less than or equal to the maximum.
- Where $t_{p Q_n}$ and $t_{p Q_m}$ are the actual propagation delays (any combination of HIGH or LOW) for any two separate outputs from a given high transition of CLK.

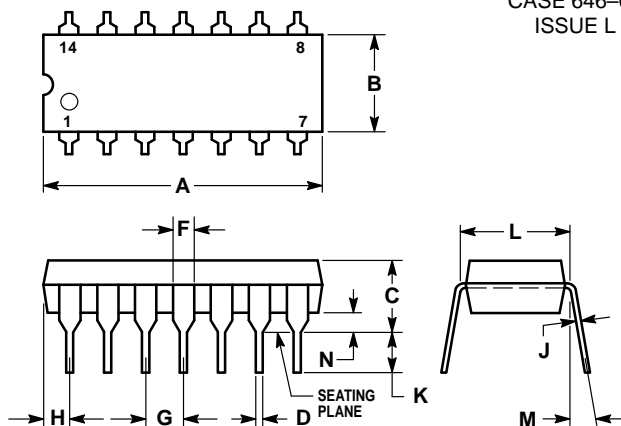
AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ C$ $C_L = 50$ pF		$T_A = -40$ to $+85^\circ C$ $C_L = 50$ pF		Unit
			Min	Max	Min	Max	
t_W	CLK Pulse Width (HIGH to LOW)	5.0	3.0		3.0		ns
t_{SU}	Minimum Setup Time, HIGH or LOW SRB to Clock	5.0	3.5		3.5		ns
t_{HD}	Minimum Hold Time, HIGH or LOW SRB to Clock	5.0	1.0		1.0		ns

CAPACITANCE

Symbol	Parameter	Typ	Unit	Condition
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30	pF	$V_{CC} = 5.0V$

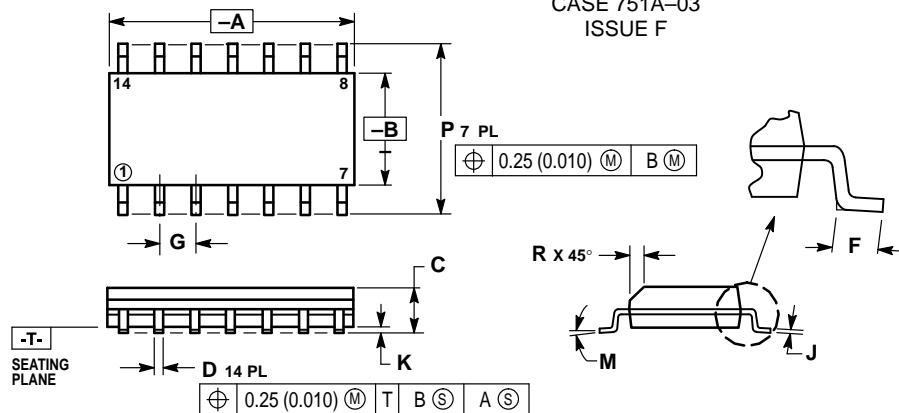
OUTLINE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 646-06
ISSUE L


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A-03
ISSUE F


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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How to reach us:

USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

MFAX: RMFA00@email.sps.mot.com -TOUCHTONE (602) 244-6609
INTERNET: http://Design-NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

