

## Dual Up Counters

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range

### MAXIMUM RATINGS\* (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

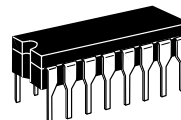
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

### TRUTH TABLE

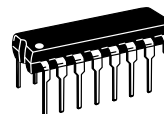
Clock	Enable	Reset	Action
↗	1	0	Increment Counter
0	↘	0	Increment Counter
↘	X	0	No Change
X	↗	0	No Change
↗	0	0	No Change
1	↘	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

## MC14518B MC14520B



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



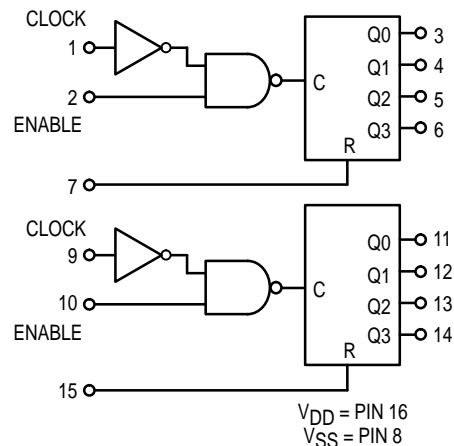
**DW SUFFIX**  
SOIC  
CASE 751G

### ORDERING INFORMATION

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBDW SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

### BLOCK DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
			10	7.0	—	7.0	5.50	—	7.0	—	
			15	11	—	11	8.25	—	11	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mA <sub>dc</sub>	
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mA <sub>dc</sub>	
		10	1.6	—	1.3	2.25	—	0.9	—		
15	4.2	—	3.4	8.8	—	2.4	—	—			
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μA <sub>dc</sub>	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μA <sub>dc</sub>	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.6 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.2 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (1.7 μA/kHz) f + I <sub>DD</sub>							μA <sub>dc</sub>	
10											
15											

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

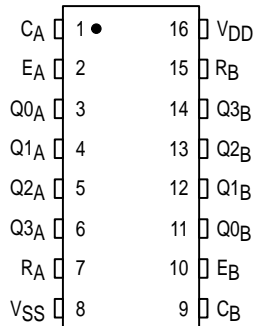
\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.002.

**PIN ASSIGNMENT**

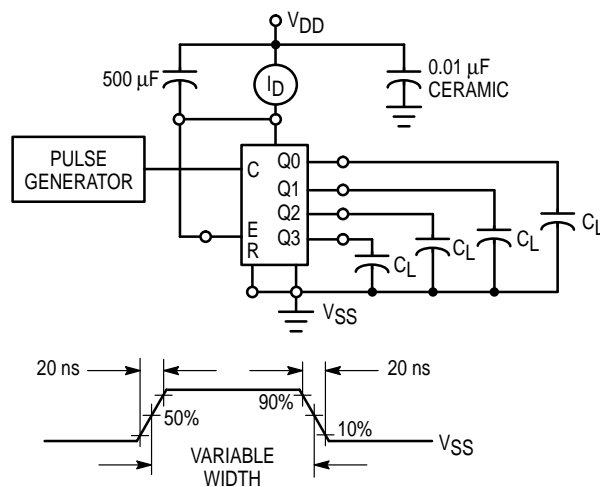


**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$	All Types			Unit
			Min	Typ #	Max	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q/Enable to Q $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	280 115 80	560 230 160	ns
Reset to Q $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 95 \text{ ns}$	$t_{PHL}$	5.0 10 15	— — —	330 130 90	650 230 170	ns
Clock Pulse Width	$t_{w(H)}, t_{w(L)}$	5.0 10 15	200 100 70	100 50 35	— — —	ns
Clock Pulse Frequency	$f_{cl}$	5.0 10 15	— — —	2.5 6.0 8.0	1.5 3.0 4.0	MHz
Clock or Enable Rise and Fall Time	$t_{THL}, t_{TLH}$	5.0 10 15	— — —	— — —	15 5 4	$\mu\text{s}$
Enable Pulse Width	$t_{WH(E)}$	5.0 10 15	440 200 140	220 100 70	— — —	ns
Reset Pulse Width	$t_{WH(R)}$	5.0 10 15	280 120 90	125 55 40	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	-5 15 20	-45 -15 -5	— — —	ns

\* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



**Figure 1. Power Dissipation Test Circuit and Waveform**

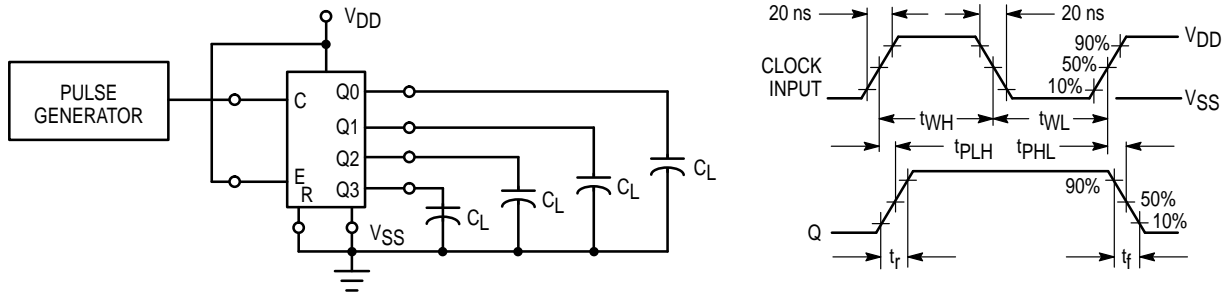


Figure 2. Switching Time Test Circuit and Waveforms

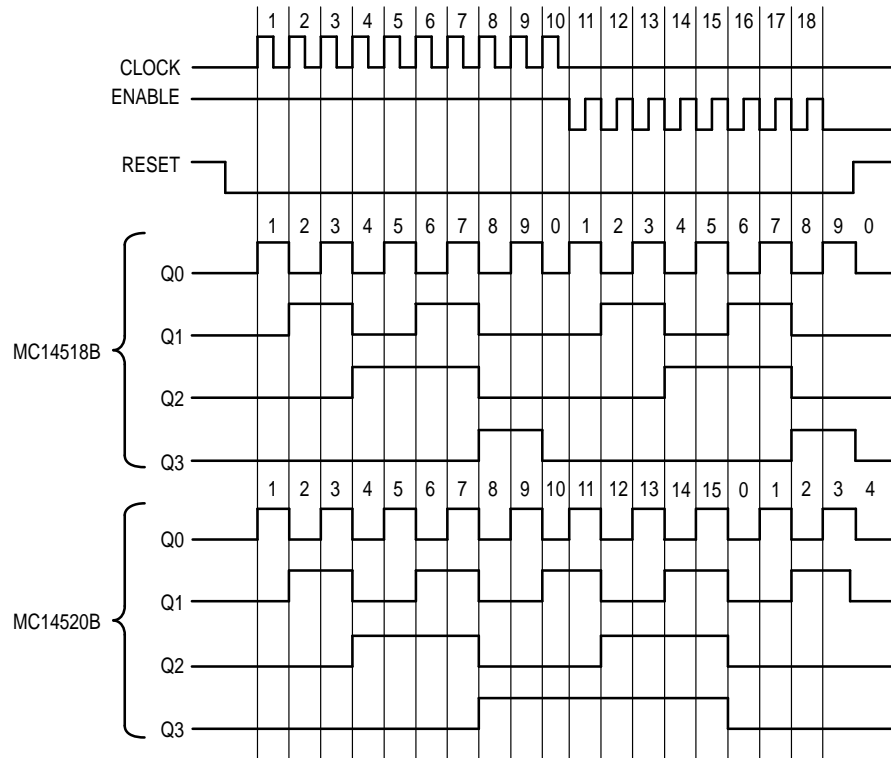
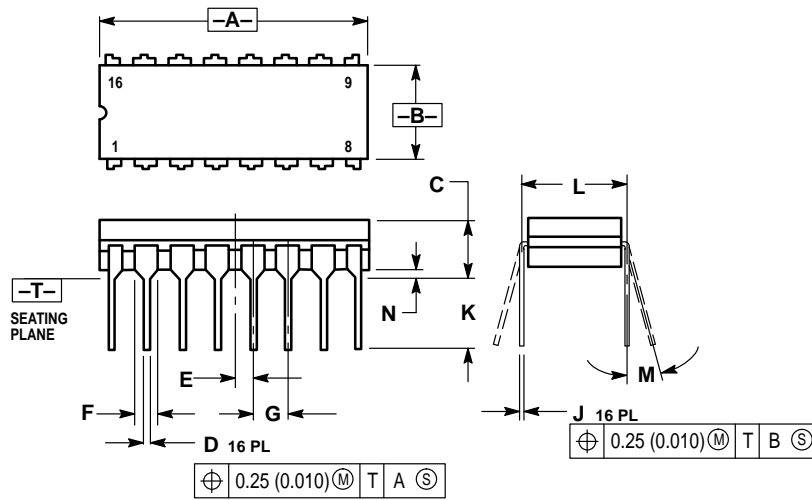


Figure 3. Timing Diagram



## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

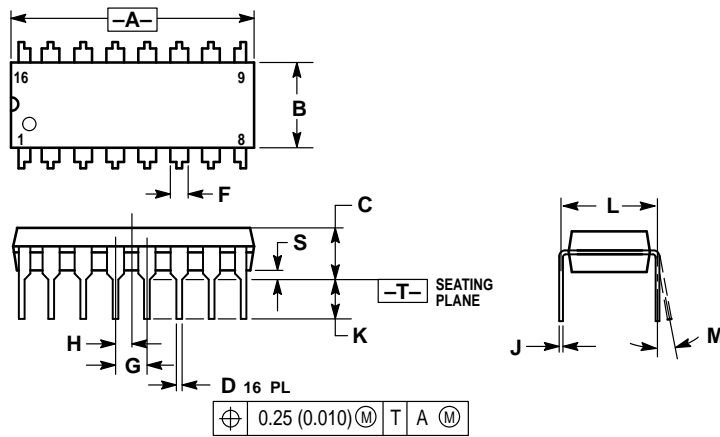


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



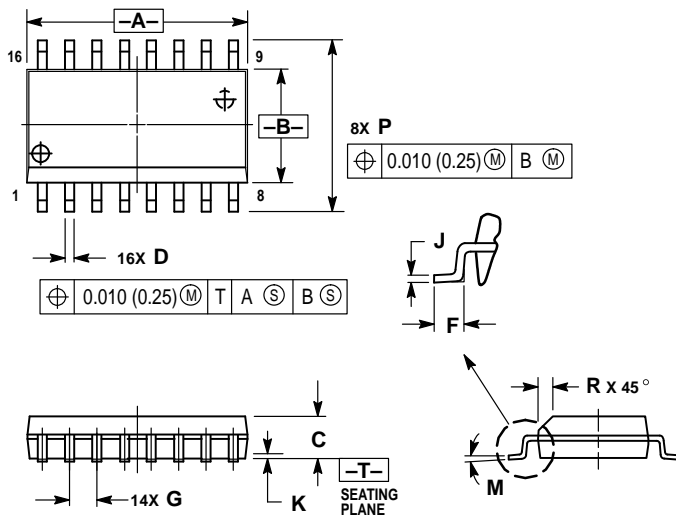
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-02 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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