

MC14020B

14-Bit Binary Counter

The MC14020B 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

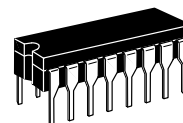
Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	- 0.5 to + 18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	- 0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

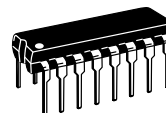
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

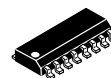
Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

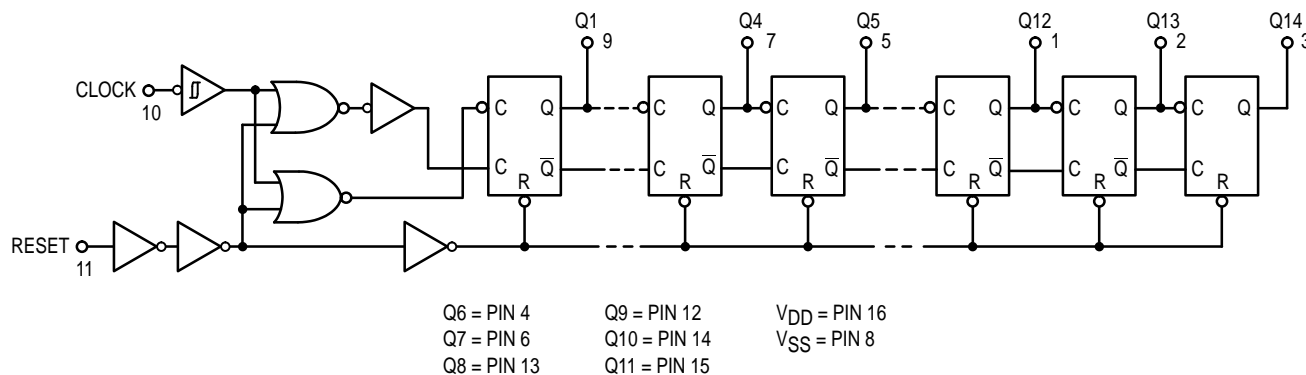
T_A = - 55° to 125°C for all packages.

TRUTH TABLE

Clock	Reset	Output State
⌋	0	No Change
⌋	0	Advance to Next State
X	1	All Outputs are Low

X = Don't Care

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit		
			Min	Max	Min	Typ #	Max	Min	Max			
Output Voltage V _{in} = V _{DD} or 0	"0" Level V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc		
		10	—	0.05	—	0	0.05	—	0.05			
		15	—	0.05	—	0	0.05	—	0.05			
	"1" Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—	Vdc
			10	9.95	—	9.95	10	—	9.95		—	
			15	14.95	—	14.95	15	—	14.95		—	
Input Voltage	"0" Level V _{IL} (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc		
		10	—	3.0	—	4.50	3.0	—	3.0			
		15	—	4.0	—	6.75	4.0	—	4.0			
	"1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5		—	Vdc
			10	7.0	—	7.0	5.50	—	7.0		—	
			15	11	—	11	8.25	—	11		—	
Output Drive Current	Source (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc	
			5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—		
			10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—		
			15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—		
	Sink (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
			10	1.6	—	1.3	2.25	—	0.9	—		
15	4.2	—	3.4	8.8	—	2.4	—	—				
Input Current	I _{in}	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc		
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF		
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc		
		10	—	10	—	0.010	10	—	300			
		15	—	20	—	0.015	20	—	600			
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.42 μA/kHz)f + I _{DD} I _T = (0.85 μA/kHz)f + I _{DD} I _T = (1.43 μA/kHz)f + I _{DD}							μAdc		

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

Q12	[1 ●]	16]	V _{DD}
Q13	[2]	15]	Q11
Q14	[3]	14]	Q10
Q6	[4]	13]	Q8
Q5	[5]	12]	Q9
Q7	[6]	11]	R
Q4	[7]	10]	C
V _{SS}	[8]	9]	Q1

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V _{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q1 t_{PHL} , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 175 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	t_{PLH} , t_{PHL}	5.0 10 15	— — —	260 115 80	520 230 160	ns
Clock to Q14 t_{PHL} , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 1735 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 772 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 535 \text{ ns}$		5.0 10 15	— — —	1820 805 560	3900 1725 1200	ns
Propagation Delay Time Reset to Q _n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 285 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$	t_{PHL}	5.0 10 15	— — —	370 155 115	740 310 230	ns
Clock Pulse Width	t_{WH}	5.0 10 15	500 165 125	140 55 38	— — —	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.0 6.0 8.0	1.0 3.0 4.0	MHz
Clock Rise and Fall Time	t_{TLH} , t_{THL}	5.0 10 15	No Limit			—
Reset Pulse Width	t_{WL}	5.0 10 15	3000 550 420	320 120 80	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	130 50 30	65 25 15	— — —	ns

* The formulas given are for the typical characteristics only at 25°C.

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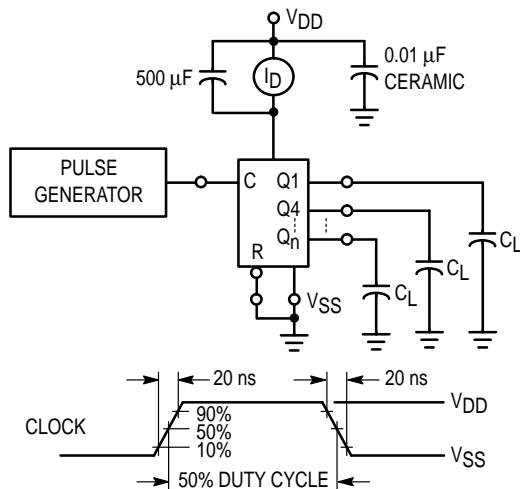


Figure 1. Power Dissipation Test Circuit and Waveform

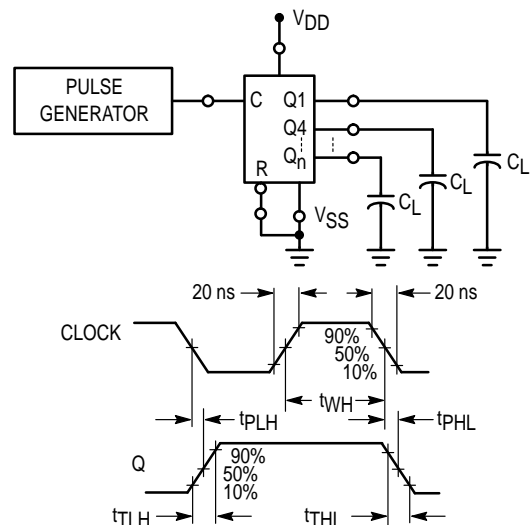


Figure 2. Switching Time Test Circuit and Waveforms

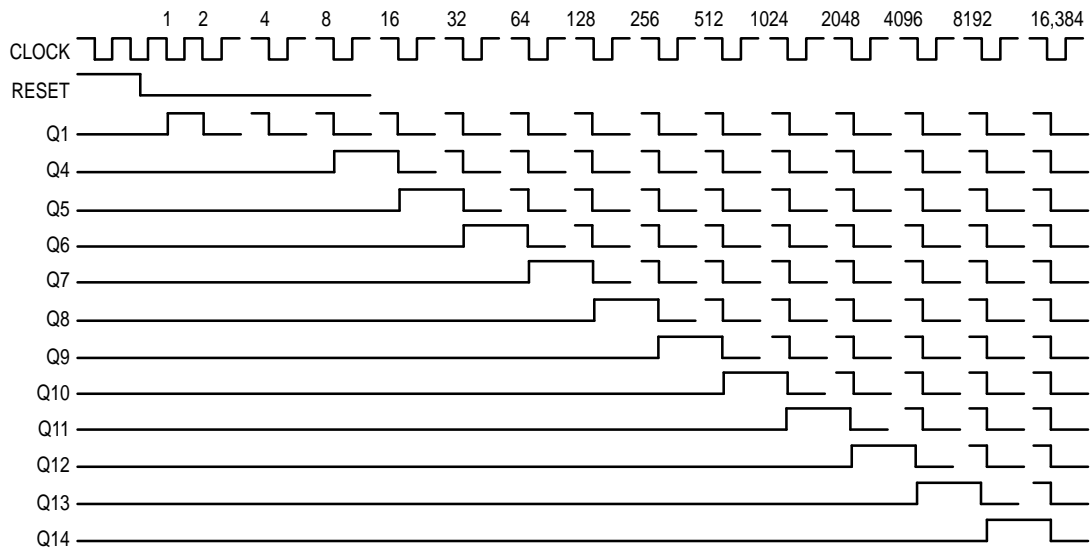
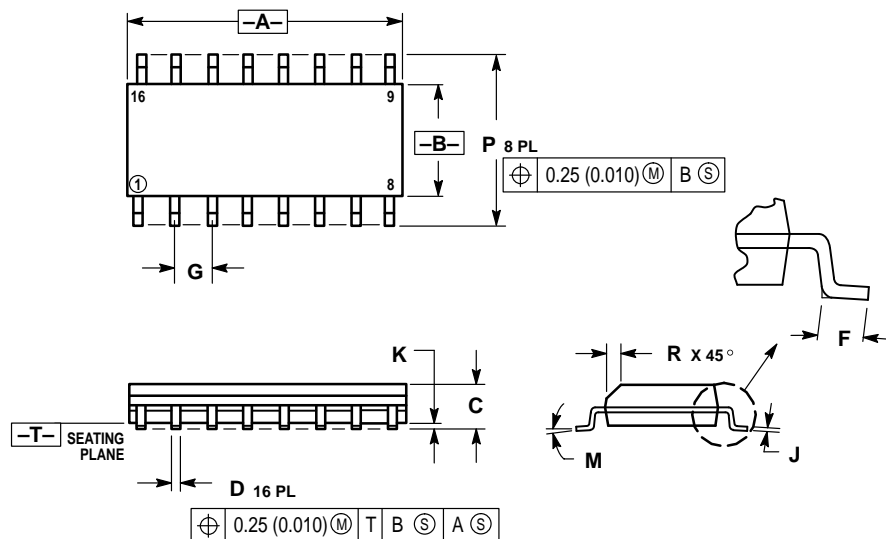


Figure 3. Timing Diagram

OUTLINE DIMENSIONS

D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14020B/D

