MOTOROLA

# MC12052A

# 1.1 GHz Super Low Power Dual Modulus Prescaler

The MC12052A is a super low power dual modulus prescaler used in phase–locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 2.7 mW at a minimum supply voltage of 2.7 V.

The MC12052A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- The MC12052 is Pin and Functionally Compatible with the MC12022
- Low Power 1.0 mA Typical
- 2.0 mA Maximum, –40 to 85°C, $V_{CC}$ = 2.7 to 5.5 Vdc
- Short Setup Time ($t_{set}$) 16 ns Maximum @ 1.1 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc

MOSAIC V is a trademark of Motorola

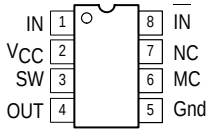
**MECL PLL COMPONENTS**
**÷64/65, ÷128/129 LOW POWER DUAL MODULUS PRESCALER**

**SEMICONDUCTOR TECHNICAL DATA**


**D SUFFIX**
PLASTIC PACKAGE
CASE 751
(SO–8)


**SD SUFFIX**
PLASTIC PACKAGE
CASE 940
(SSOP–8)

**PIN CONNECTIONS**




(Top View)

**FUNCTIONAL TABLE**

| SW | MC | Divide Ratio |
|---|---|---|
| H | H | 64 |
| H | L | 65 |
| L | H | 128 |
| L | L | 129 |

**NOTES:** 1. SW: H = $V_{CC}$, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to $V_{CC}$, L = GND to 0.8 V.

**MAXIMUM RATINGS**

| Characteristic | Symbol | Range | Unit |
|---|---|---|---|
| Power Supply Voltage, Pin 2 | $V_{CC}$ | –0.5 to 7.0 | Vdc |
| Operating Temperature Range | $T_A$ | –40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | –65 to 150 | °C |
| Modulus Control Input, Pin 6 | MC | –0.5 to 6.5 | Vdc |

**ORDERING INFORMATION**

| Device | Operating Temp Range | Package |
|---|---|---|
| MC12052AD | $T_A$ = – 40° to +85°C | SO–8 |
| MC12052ASD | | SSOP–8 |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 2.7 to 5.5 VDC, $T_A$ = –40 to 85°C, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Toggle Frequency (Sine Wave Input) | $f_t$ | 0.1 | 1.4 | 1.1 | GHz |
| Supply Current (Pin 2) | $I_{CC}$ | – | 1.0 | 2.0 | mA |
| Modulus Control Input High (MC) | $V_{IH1}$ | 2.0 | – | $V_{CC}$ + 0.5 V | V |
| Modulus Control Input Low (MC) | $V_{IL1}$ | Gnd | – | 0.8 | V |
| Divide Ratio Control Input High (SW) | $V_{IH2}$ | $V_{CC}$ – 0.5 V | $V_{CC}$ | $V_{CC}$ + 0.5 V | VDC |
| Divide Ratio Control Input Low (SW) | $V_{IL2}$ | Open | Open | Open | – |
| Output Voltage Swing (Note 2)<br>($C_L$ = 8.0 pF, $R_L$ = 3.3 kΩ) | $V_{out}$ | 0.8 | 1.1 | – | $V_{PP}$ |
| Modulus Setup Time MC to Out @ 1100 MHz | $t_{set}$ | – | 11 | 16 | ns |
| Input Voltage Sensitivity 250–1100 MHz<br>100–250 MHz | $V_{in}$ | 100<br>400 | –<br>– | 1000<br>1000 | $mV_{PP}$ |
| Output Current (Note 1)<br>$V_{CC}$ = 2.7 V, $C_L$ = 8.0 pF, $R_L$ = 3.3 kΩ<br>$V_{CC}$ = 5.0 V, $C_L$ = 8.0 pF, $R_L$ = 7.2 kΩ | $I_O$ | <br>–<br>– | <br>0.5<br>0.5 | <br>3.0<br>3.0 | mA |

**NOTES: 1.** Divide ratio of ÷64/65 @ 1.1 GHz
2. Valid over voltage range 2.7 to 5.5 V; $R_L$ = 3.3 kΩ @ $V_{CC}$ = 2.7 V; $R_L$ = 7.2 kΩ @ $V_{CC}$ = 5.0 V

**Figure 1. Logic Diagram (MC12052A)**

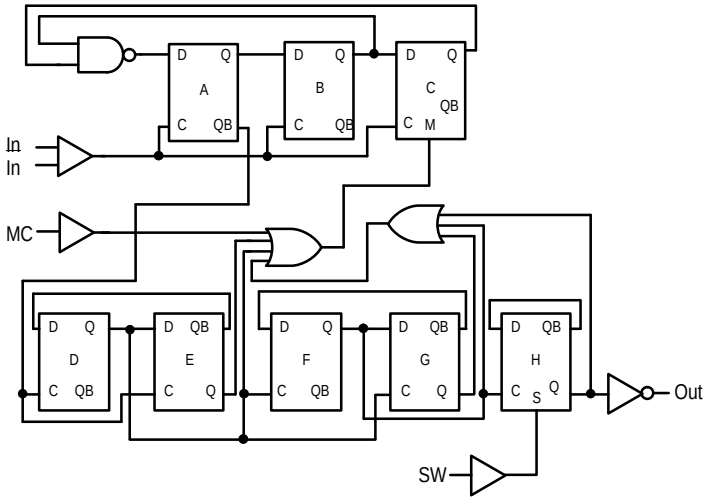
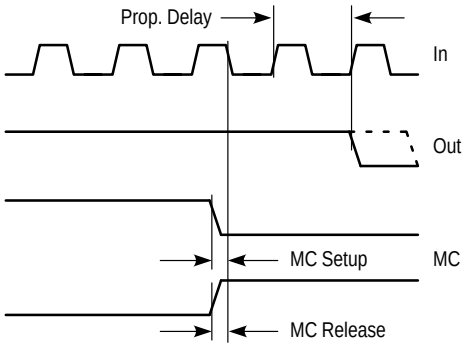
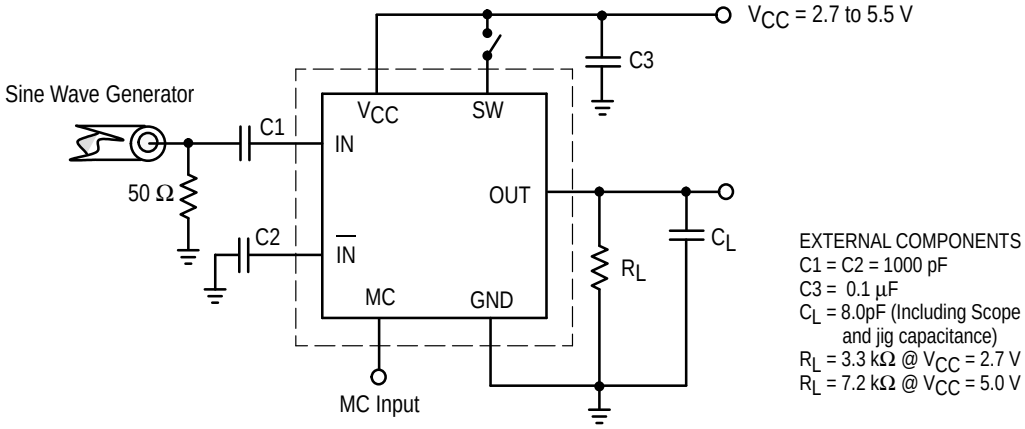



**Figure 2. Modulus Setup Time**



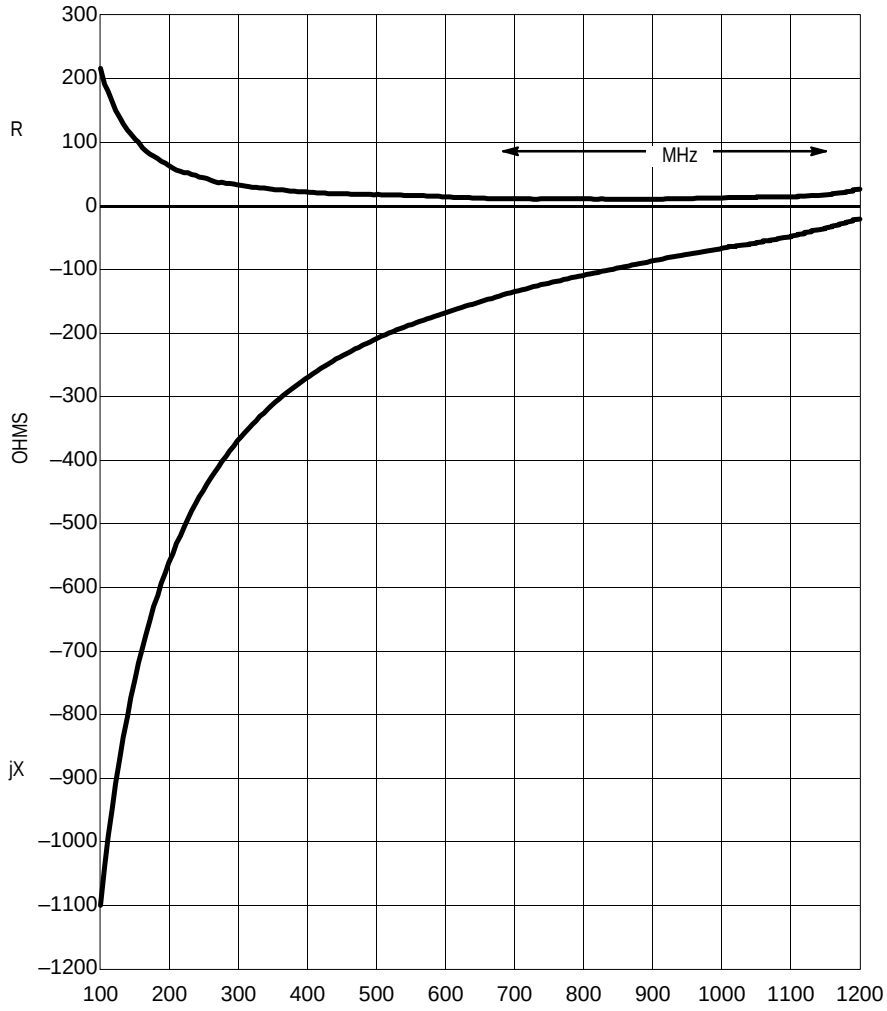

Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

**Figure 3. AC Test Circuit**



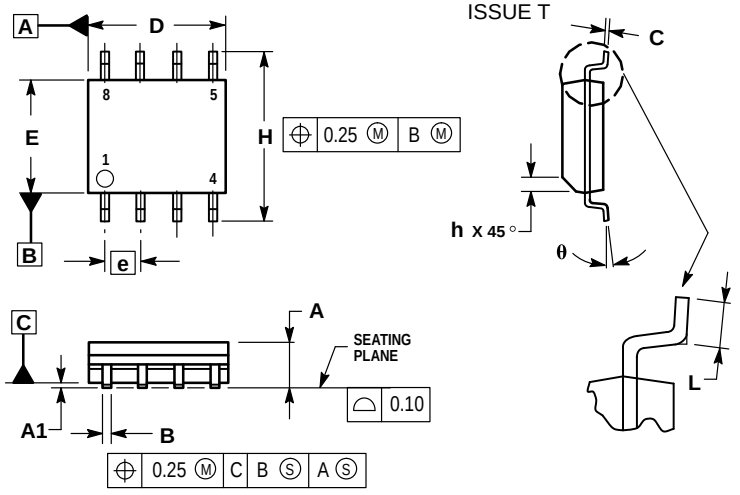

EXTERNAL COMPONENTS
C1 = C2 = 1000 pF
C3 = 0.1 µF
$C_L$ = 8.0pF (Including Scope and jig capacitance)
$R_L$ = 3.3 kΩ @ $V_{CC}$ = 2.7 V
$R_L$ = 7.2 kΩ @ $V_{CC}$ = 5.0 V

**Figure 4. Typical Input Impedance versus Input Frequency**



## OUTLINE DIMENSIONS

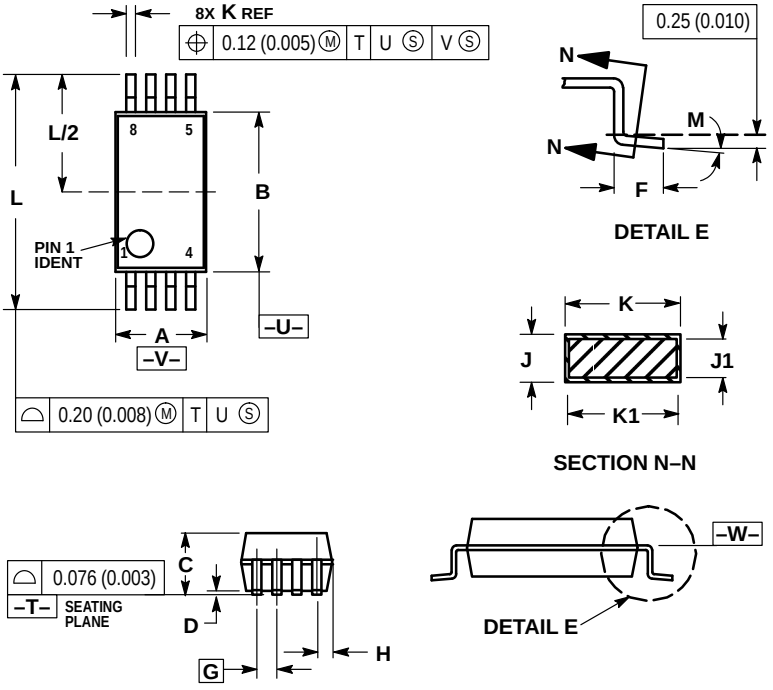
**D SUFFIX**
PLASTIC PACKAGE
CASE 751–06
(SO–8)
ISSUE T




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.25 |
| θ | 0° | 7° |

**SD SUFFIX**
PLASTIC PACKAGE
CASE 940–03
(SSOP–8)
ISSUE B




NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.87 | 3.13 | 0.113 | 0.123 |
| B | 5.20 | 5.38 | 0.205 | 0.212 |
| C | 1.73 | 1.99 | 0.068 | 0.078 |
| D | 0.05 | 0.21 | 0.002 | 0.008 |
| F | 0.63 | 0.95 | 0.024 | 0.037 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.44 | 0.60 | 0.017 | 0.023 |
| J | 0.09 | 0.20 | 0.003 | 0.008 |
| J1 | 0.09 | 0.16 | 0.003 | 0.006 |
| K | 0.25 | 0.38 | 0.010 | 0.015 |
| K1 | 0.25 | 0.33 | 0.010 | 0.013 |
| L | 7.65 | 7.90 | 0.301 | 0.311 |
| M | 0° | 8° | 0° | 8° |

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