M66290AGP/FP

Ver.1.0 Oct. 27, 2000

USB DEVICE CONTROLLER

DESCRIPTION

The M66290A is a general purpose USB (Universal Serial Bus) device controller compatible with the USB specification version 1.1 and corresponds to full speed transfer. Built-in transceiver circuits meet all transfer type which is defined in USB.

M66290A has FIFO of 3k Bytes for data transfer and can set 6 endpoints (maximum).

Each endpoint can be set programmable of its transfer condition, so can correspond to each device class transfer system of USB.

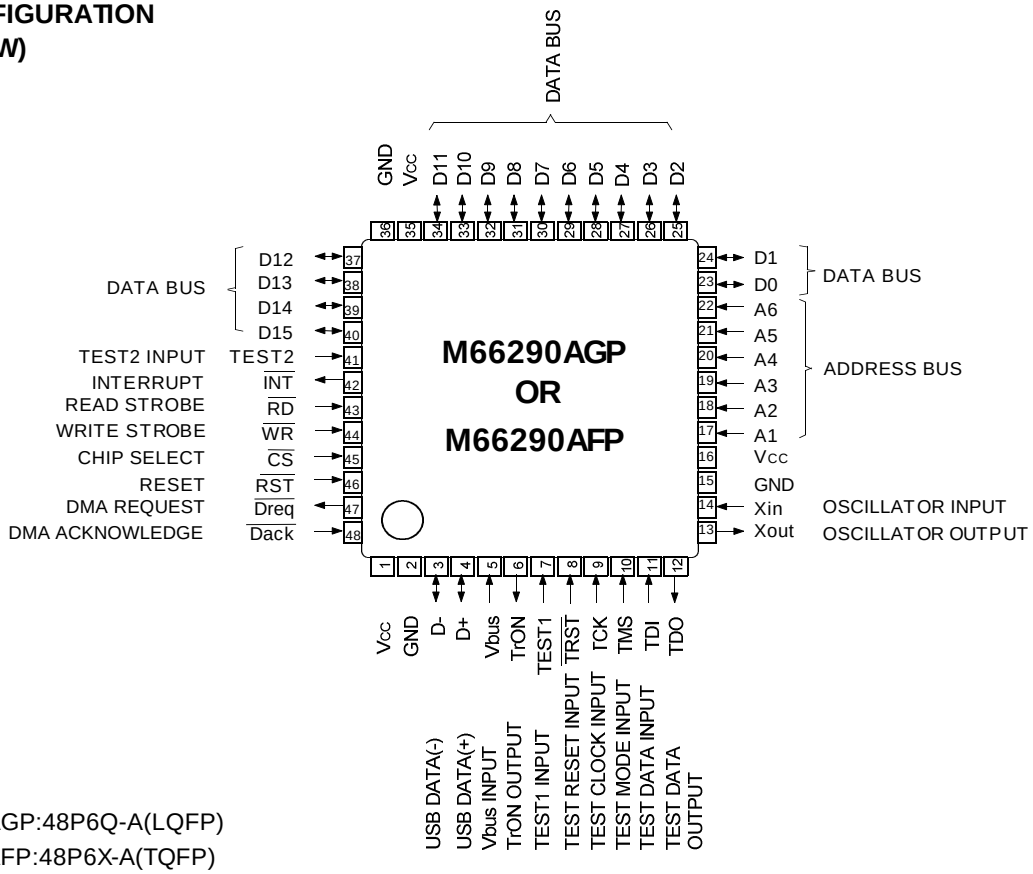
FEATURES

- USB specification 1.1 compliant
- Built-in USB transceiver circuit
- Supports Full Speed (12 Mbps) transmission
- Supports all four USB transfer type :
  - Control transfer
  - Bulk transfer
  - Isochronous transfer
  - Interrupt transfer
- Built-in FIFO (3 KBytes) for Endpoint
- Up to 6 endpoint (EP0 to EP5) selectable
- Data transfer condition selectable for each Endpoints (EP1 to EP5)
  - Data transfer type (Bulk, Isochronous and Interrupt)
  - Transfer direction (IN/OUT)
  - Buffer size of FIFO (maximum 1024 Bytes)
  - Double (Toggle) buffer configuration
  - Continuous transfer mode (Buffering up to 1 KByteX2)
  - Max packet size
- Supports 4 input clock frequencies
  - Input clock : 6/12/24/48 MHz
  - Built-in PLL which has an oscillation buffer and outputs at 48 MHz
- Supports both 8-bit and 16-bit DMA transfers
- 16-bit CPU bus interface
- 3.3V single power source
- Built-in JTAG

APPLICATION

- Printer , Scanner , DSC , DVC
- PC camera , Multimedia speaker , Terminal adapter etc.
- Support all PC peripheral using Full Speed USB

PIN CONFIGURATION (TOP VIEW)

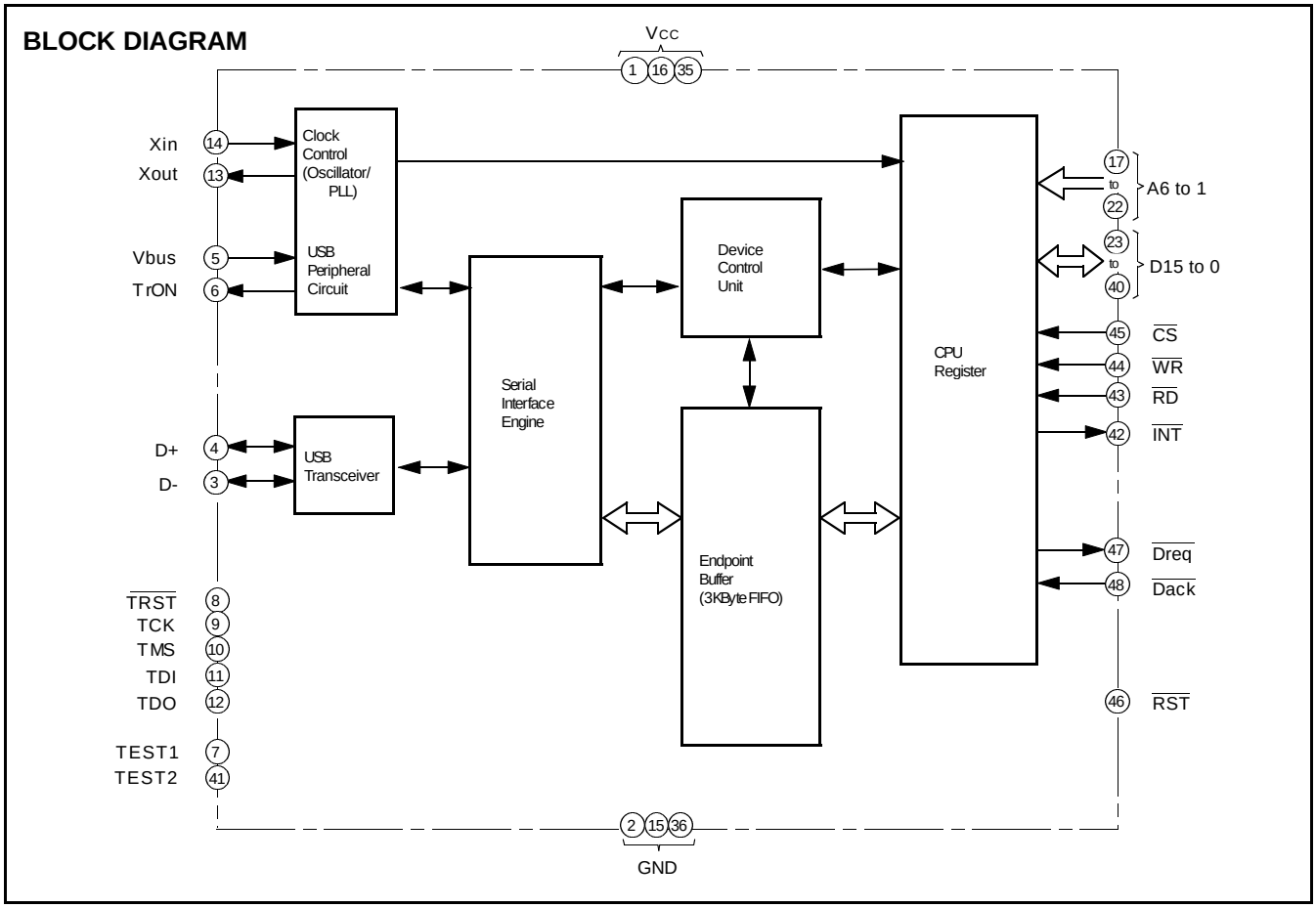


Outline

M66290AGP:48P6Q-A(LQFP)

M66290AFP:48P6X-A(TQFP)

BLOCK DIAGRAM



BLOCK DESCRIPTIONS

The M66290A contains USB transceiver, oscillation circuit, PLL, serial interface engine, endpoint buffer, device control unit, and CPU register.

USB Transceiver
USB Transceiver is consisted of differential driver and differential receiver.
And is compatible with USB specification version 1.1 and corresponds to Full Speed Transfer mode.

Serial Interface Engine (SIE)
SIE handles protocol layer as follows.

- Extract a USB 12MHz clock
- Serial-Parallel data conversion
- SYNC detection
- NRZI encode and decode
- Bit stuffing and destuffing
- CRC generator and checker

Device Control Unit (DCU)
DCU controls the device state sequence, control transfer sequence, and so on.

Endpoint Buffer
This is a FIFO buffer for transmit and receive between endpoints.
Except for EP0 for control transfer, five endpoints (EP1 to EP5) can be set.

CPU Register
This is an interface block with CPU.

Oscillator/PLL
This block oscillates the internal operation clock source of 48MHz.
External clock of 6/12/24/48MHz can be input.

USB peripheral circuit
Detect the connection and the shutdown of USB by the Vbus input.
Connect the Vbus of USB bus to or the 5V power supply to Vbus input.
Connect the TrON output to D+ pull-up resistor of 1.5kohm. ON/OFF of the pull-up resistor is controlled by the register.

PIN DESCRIPTIONS

Item	Pin name	Input/	Function	Number of
CPU interface	D15 to D0	Input/ Output	DATA BUS Data bus to access the register from the system	16
	A6 to A1	Input	ADDRESS BUS Address bus to access the register from the system	6
	$\overline{CS}$	Input	CHIP SELECT "L" level enables to communicate with M66290A	1
	$\overline{WR}$	Input	WRITE STROBE Input data is written into the register by the positive edge	1
	$\overline{RD}$	Input	READ STROBE Register data can be read when "L" level	1
	$\overline{INT}$	Output	INTERRUPT "L" level requests interrupt to system	1
DMA interface	$\overline{Dreq}$	Output	DMA REQUEST DMA transfer request to endpoint FIFO	1
	$\overline{Dack}$	Input	DMA ACKNOWLEDGE FIFO access by DMA transfer is available in "L" level	1
USB interface	D+	Input/ Output	USB DATA(+) D+ of USB. Connect the external resistor serially.	1
	D-	Input/ Output	USB DATA(-) D- of USB. Connect the external resistor serially.	1
	Vbus	Input	Vbus INPUT (Built-in pull down resistor) Connect to the Vbus of USB bus or to the 5V power supply. Connection or shutdown of the Vbus can be detected.	1
	TrON	Output	TrON OUTPUT Connect to the D+ pull-up resistor of 1.5kohm. ON/OFF control of the pull-up resistor is available.	1
JTAG interface	$\overline{TRST}$	Input	TEST RESET INPUT (Built-in pull up resistor) Reset input of JTAG. Even if the JTAG is not used, JTAG circuit must be initialized. Input "L" level to initialize like the $\overline{RST}$ input.	1
	TMS	Input	TEST MODE INPUT (Built-in pull up resistor) Mode set input to JTAG. If JTAG is not used, keep "H" level or open.	1
	TCK	Input	TEST CLOCK INPUT (Built-in pull down resistor) Clock input to JTAG. If JTAG is not used, keep "L" level or open.	1
	TDI	Input	TEST DATA INPUT (Built-in pull up resistor) Data input to JTAG. If JTAG is not used, keep "H" level or open.	1
	TDO	Output	TEST DATA OUTPUT Data output from JTAG. If the JTAG is not used, keep open.	1
Others	$\overline{RST}$	Input	RESET "L" level initializes the register or the counter of M66290A.	1
	Xin	Input	OSCILLATOR INPUT Generate an internal clock. Input or output of internal clock oscillator. When use as a crystal oscillator, connect a crystal between Xin and Xout. If an external clock is used, input it to Xin, and Xout must be opened.	1
	Xout	Output	OSCILLATOR OUTPUT	1
	TEST1	Input	TEST1 INPUT (Built-in pull down resistor) Input for the test. Keep "L" level or open.	1
	TEST2	Input	TEST2 INPUT (Built-in pull down resistor) Input for the test. Keep "L" level or open.	1
	Vcc	-	Power supply pin	3
	GND	-	Ground	3

USB DATA TRANSFER DESCRIPTIONS

M66290A is a USB device controller correspond to all the four types of transfer (control, bulk, isochronous, and interrupt transfer), which is compatible to USB specification 1.1.

M66290A acts USB functions as below automatically.
(1) Bit stuffing/destuffing
(2) CRC generate/check
(3) NRZI encode/decode
(4) Packet handling
(5) USB address check
(6) Bus error handling

Therefore, when CPU transact the operations as follows, USB transfer is realized.
(1) Response to the control transfer request
(2) Permission of store and transmission of the transmit data into the endpoint buffer.
(Or read of the received data from the endpoint buffer)
(3) Stall handling
(4) Suspend/resume handling

Below are the descriptions about the data transfer.

Data receive

In data receive, there are differences of its function between setup transaction and out transaction.

In setup transaction, when received device request from host, 8Byte request is always stored into four resistors.
When request data is received correctly,sends back ACK packet to host and at the same time, occurs interrupt to CPU and urge CPU to read request.

In out transaction, after M66290A received OUT token packet, host transmits data packet.
If packet of maximum packet size or short packet is stored into the endpoint FIFO of M66290A, and moreover, error is not occurred in that transfer, M66290A transmits ACK packet to host and informs CPU that the data was received by occurring buffer ready interrupt.
If USB protocol error is occurred in the host data which received via USB bus, or if the endpoint FIFO is full, M66290A does not transmit ACK packet to host. Host knows that the error occurred because the ACK packet does not come, and take a step such as data resend.

Data transmit

When the data of endpoint FIFO, which corresponds to transmit request by IN token packet, is ready, M66290A transmit the corresponded data packet to USB bus.
If the ACK packet come from the host for the transmitted data packet, a transaction completed and the endpoint FIFO becomes empty and urge CPU to write the next transmit data by buffer ready interrupt.

If the transmit data, which correspond to transmit request by IN token packet, is not exist in the endpoint FIFO, M66290A transmit NAK packet to host when received IN token packet from host and occurs interrupt and request CPU to write transmit data.
When M66290A received IN token packet again from host, M66290A transmits the data which is written.
If error is not occurred in that transfer, host transmit ACK packet and if M66290A received it normally, a transaction completed.
If USB protocol error is occurred in the data which is transmitted via USB bus, host does not transmit ACK packet, so M66290A watch and wait until receive IN token packet, with keeping the data to be transmitted.

CONTROL REGISTER TABLE

Below is the table of registers of M66290A.
Bit width of all register is 16bits.
In reset item, "H/W" shows the reset status by external $\overline{RST}$ input, "S/W" shows reset status by USBE register, and "USB" shows the reset status by receiving USB reset.
" - " shows that the previous status is kept.
Write into reserved address is inhibited.

Address	Name	R/W			
			H/W	S/W	USB
00h	USB Operation Enable Register	R/W	0000h	-	-
02h	Remote Wake-up Register	R/W	0000h	0000h	-
04h	Sequence Bit Clear Register	R/W	0000h	0000h	-
06h	Reserved				
08h	USB Address Register	R	0000h	0000h	0000h
0Ah	IsochronousStatus Register	R/W (note 2)	0000h	0000h	-
0Ch to 0Eh	Reserved				
10h	Interrupt Enable Register0	R/W	0000h	0000h	-
12h	Interrupt Enable Register1	R/W	0000h	0000h	-
14h	Interrupt Enable Register2	R/W	0000h	0000h	-
16h	Interrupt Enable Register3	R/W	0000h	0000h	-
18h	Interrupt Status Register0	R/W (note 2)	0000h	0000h	Note 2
1Ah	Interrupt Status Register1	R	0000h	0000h	-
1Ch	Interrupt Status Register2	R/W	0000h	0000h	-
1Eh	Interrupt Status Register3	R/W	0000h	0000h	-
20h	Request Register	R	0000h	-	-
22h	Value Register	R	0000h	-	-
24h	Index Register	R	0000h	-	-
26h	Length Register	R	0000h	-	-
28h	Control Transfer Control Register	R/W	0000h	-	-
2Ah	EP0 Packet Size Register	R/W	0008h	-	-
2Ch	Auto-response Control Register	R/W	0000h	-	-
2Eh	Reserved				
30h	EP0 FIFO Selection Register	R/W	0000h	-	-
32h	EP0_FIFO Control Register	R/W (note 2)	0800h	-	-
34h	EP0 FIFO Data Register	R/W	xxxx	-	-
36h	EP0 Continuous transmit Data Length	R/W	0000h	-	-
38h to 3Eh	Reserved				
40h	CPU FIFO Selection Register	R/W	0000h	-	-
42h	CPU FIFO Control Register	R/W (note 2)	0800h	-	-
44h	CPU FIFO Data Register	R/W	xxxx	-	-
46h	Reserved				
48h	DMA FIFO Selection Register	R/W	0000h	-	-
4Ah	DMA FIFO Control Register	R/W (note 2)	0800h	-	-
4Ch	DMA FIFO Data Register	R/W	xxxx	-	-
4Eh to 5Eh	Reserved				
60h	EP1 Configuration Register0	R/W	0000h	-	-
62h	EP1 Configuration Register1	R/W	0040h	-	-
64h	EP2 Configuration Register0	R/W	0000h	-	-
66h	EP2 Configuration Register1	R/W	0040h	-	-
68h	EP3 Configuration Register0	R/W	0000h	-	-
6Ah	EP3 Configuration Register1	R/W	0040h	-	-
6Ch	EP4 Configuration Register0	R/W	0000h	-	-
6Eh	EP4 Configuration Register1	R/W	0040h	-	-
70h	EP5 Configuration Register0	R/W	0000h	-	-

note 1 : Detail description is mentioned later.
note 2 : Some are read only.

Functional and register descriptions

We explain about Function and register constitution of M66290A dividing into four items as follows.

(1) System control
(2) Interrupts
(3) Control transfer/enumeration
(4) Endpoints and FIFO control

(1) System control

CLOCK

Clock of 48MHz is needed for internal operations of M66290A.

Built in PLL enables to input external clock of 6/12/24/48MHz. Selection of it is realized by the XTAL of "USB Operation Enable Register".

When use external clock of 48MHz, PLL is not needed, so set to PLL operation disable.

Built in oscillation circuit enables to supply clock by self oscillation.

To set the "USB Operation Enable Register", it can be set the device to standby state. Oscillation is halted (clock input halted) by XCKE, PLL operation is halted by PLLC, and clock supply to USB block is halted by SCKE.

To prevent unstable behavior by unstable clock, clock supply to USB block must be obeyed the process, that is, enables clock input by XCKE, wait until oscillation stabilized, start PLL by PLLC, wait until oscillation stabilized (less than 1ms), and start clock supply to USB block by SCKE.

RESET

S/W reset by the register set (USBE), different from the hardware reset, keeps the value of register of USB operation enable register, FIFO relational register, control transfer relational register,endpoint setting register, and so on.

And in USB reset (when more than 2.5us of SE0 state is continued on D+, D- terminal), the value of register is kept except for "Interrupt Status Register 0" and "USB_Address Register"

As to details of reset state, see each item of register.

D+ pull-up resistor control function

To set the register, external TrON output is controlled and can control the ON/OFF of pull-up resistor (1.5kohm) on USB D+ line.

Remote wakeup function

When device is in suspended state, outputs remote wakeup signal and can cancel suspended state to receive resume from USB.

Remote wakeup function is only effective in Suspended state in which device state shifts from Configured state, so don't use to other device state.

And when use this function, device state shifts to Address state after outputs remote wakeup signal, so it is needed to set up again the device state to Configured state. Change of set up of device state can be done in S/W control mode.

Remote wakeup signal is a signal to set USB bus to idle state after output K-state of 10ms length.

If this remote wakeup function is set up immediately after detected suspend, USB bus idle state is kept for 2ms and then shifts to K state output. (Because USB bus idle state must be kept for 5ms minimum until transmit of remote wakeup signal, on the other hand after detect suspend, USB idle state is continued for 3ms)

Sequence toggle bit clear function

In each endpoint of EP0 to EP5, data PID can be reset independently and also can appoint PID of DATA0.

By this function, management of sequence toggle bit in transfer after reset PID, is done by H/W automatically.

Error information in isochronous transfer

In isochronous transfer there is not retry function of transmit/receive, because the handshake from receiver to transmitter is not returned not to disturb the time equivalent data transfer.

M66290A has enough information function which enables firmware to manage incorrect transfer in case of transfer error occurred in isochronous transfer.

Information which M66290A can inform is, over run error, under run error, received data error (CRC error, bit stuffing error), and frame number.

Software control mode

In software control mode, it is available to set up (write) from CPU as follows, USB_Address register (USB_Addr), device state register (DVSQ), control transfer stage register (CTSQ).

Normally, use this mode with OFF.

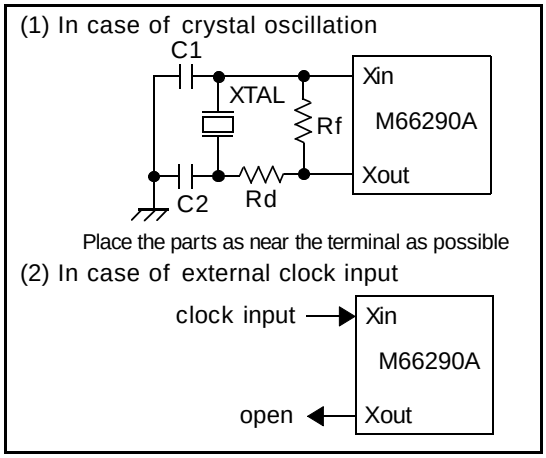


Figure 1. Xin and Xout connections

(1-1) USB Operation Enable Register (Address : 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
XCKE	PLLC	XTAL[1:0]		SCKE	USBPC	Tr_on[1:0]								SCTR	USBE

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	XCKE	Oscillator enable	0 : Oscillator disable (clock input disable) 1 : Oscillator enable (clock input enable)	W/R	0	-	-
14	PLLC	PLL control	0 : PLL disable 1 : PLL enable When use external clock of 48MHz, set to PLL disable.	W/R	0	-	-
13, 12	XTAL[1:0]	Crystal select	00 : 1/1 division (external 48MHz input) 10 : 1/2 division (external 24MHz input) 01 : 1/4 division (external 12MHz input) 11 : 1/8 division (external 6MHz input)	W/R	00	-	-
11	SCKE	Internal clock enable	0 : Internal clock (sck) disable 1 : Internal clock (sck) enable	W/R	0	-	-
10	USBPC	USB transceiver power control	0 : USB transceiver disable 1 : USB transceiver enable In suspend state, resume signal can be received even if USB transceiver disabled.	W/R	0	-	-
9, 8	Tr_on [1:0]	Tr_on output control	X0 : TrON port ="Hi-Z" 01 : TrON port ="L" 11 : TrON port ="H" This fields selects TrON output state, and it is effective when external Vbus input is "H" level (5V). If external Vbus input is "L", these bits can be set but TrON output does not operate.	W/R	00	-	-
7 to 2	Reserved		Write/Read "0"				
1	SCTR	Software control mode	0 : Normal Operation 1 : Software Control Mode Operation	W/R	0	-	-
0	USBE	USB module enable	0 : USB module disable (S/W Reset) 1 : USB module enable	W/R	0	-	-

(1-2) Remote Wake-up Register (Address : 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															WKUP

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 1	Reserved		Write/Read "0"				
0	WKUP	Remote wake-up	When CPU write "1" to WKUP for remote wake-up, M66290A outputs K-State for 10ms, and return to Bus Idle-State. (Remote wake-up signal) This bit returns to "0" automatically after suspend is canceled. If "1" is written into this bit after detected suspend, bus idle state is kept for 2ms and after then shifts to K state output.	W/R	0	0	-

(1-3) Sequence Bit Clear Register (Address : 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										SQCLR[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	SQCLR [5:0]	Sequence toggle bit clear	When write "1" into the bit which is correspond to the number of endpoint, sequence toggle bit of that endpoint is cleared and appoint the DATA0 by the data PID of next transmission. Write "1" into the bit after set the response PID of the endpoint, which clears sequence toggle bit, to NAK("00") . Transfers After the transfer appointed, sequence toggle bit is controlled by H/W. In USB reset, Sequence toggle bit of each endpoint is not cleared. If "0" is written into this bit, flag is not changed. Read data of this bit is always "0".	W/R	00h	00h	-

(1-4)USB Address Register (Address : 08h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									USB_Addr[6:0]						

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 7	Reserved		Write/Read "0"				
6 to 0	USB_ Addr [6:0]	USB_Address register	USB address which is assigned by host is stored. After stored the address, transaction is done only to the token packet which is transmitted to this address. (If S/W control mode is set, write operation is available)	R	00h	00h	00h

(1-5) Isochronous Status Register (Address : 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OVRN	CRCE			FMOD	FRNM[10:0]										

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	OVRN	Over run error	In isochronous transfers (OUT/IN), when over-run or under-run is occurred to the endpoint buffer, this flag is set at the timing of the receive end of the OUT/IN token packet. Over run is occurred when delayed to read the received data from the endpoint buffer, and means that could not received. Over run is occurred when the direction of transmission is OUT. Also the received data has CRC or bit stuffing error, this flag is set. Under run is occurred when delayed to write the transmit data into the endpoint buffer, and means that could not transmitted. Under-run is occurred when the direction of transmission is IN. When a state above is occurred, endpoint buffer notready interrupt is occurred. When "0" is written, status flag is cleared. When "1" is written, flag is not changed.	W/R	0	0	-
14	CRCE	Receive data error	In isochronous transfers(OUT), if the received data has CRC or bit stuffing error, this flag is set at the timing of the end of transaction. When a state above is occurred, endpoint buffer notready interrupt is occurred. When "0" is written, status flag is cleared. When "1" is written, flag is not changed.	W/R	0	0	-
13 to 12	Reserved		Write/Read "0"				
11	FMOD	Frame number mode	Select the renewal timing of the flame number to be stored to FRNM[10:0]. 0 : Renew the flame number when SOF is received . 1 : In isochronous transfer, renew the flame number at the timing of the end of transaction.	W/R	0	0	-
10 to 0	FRNM [10:0]	Frame number	Stores the flame number. The timing to renew the stored flame number is selectable by set FMOD.	R	000h	000h	-

(2) Interrupts

There are eight factors of interrupt to CPU.
When interrupt occurred, the factor can be known to refer to "Interrupt Status Register 0" and "Interrupt Status Register 1".
These interrupts can be set of its enable/disable independently to set "Interrupt Enable Register 0" and "Interrupt Enable Register 1".
If disable is set, interrupt is not occurred but interrupt status flag is set.
Each factor of interrupt is shown in the table below, and also describes below the interrupt conditions and how to deal with the interrupt.

Vbus (connect/shut down) interrupt (VBUS)

Interrupt occurs when Vbus input state is changed (both "L" to "H" and "H" to "L").
To know Vbus input state, confirm the Vbus bit of interrupt status register 0. Confirmation of Vbus bit must be done after enabled internal clock operation.
This interrupt can be occurred even if the internal clock(sck) is halted. To clear the status flag, enables the internal clock(sck) in operation and then write "0".
If the internal clock(sck) is halted, status flag can not be cleared.
This interrupt is useful to detect connect/shut-down of USB for prepareration/close of USB transfers.

Resume detect interrupt (RESM)

If device state is in suspended state and resume interrupt enable flag is set, interrupt occurs when USB bus state is changed ("J" to "K" or "SE0").
This interrupt can be occurred even if the internal clock(sck) is halted. To clear the status flag, set the internal clock(sck) in operation and then write "0". If the internal clock(sck) is halted, status flag can not be cleared.

SOF detect interrupt (SOFR)

Interrupt occurs when detect SOF.

Device state transition interrupt (DVST)

M66290A manages the device state by H/W.
It manages Powered, Default, Address, Configured, and Suspended state. Device state can be known to refer to "Interrupt Status Register 0".
As to device state shift, see the item of "Device state shift" in "(3) Control transfer/emulation" in the latter part.
Device state transition interrupt occurs when device state shifted. The number of factors is four, that is, USB bus reset detect, suspend detect, execution of "Set Address", and execution of "Set Configuration".
USB reset is detected when SE0 state over 2.5us is continued on D+, D- terminal.
Suspend is detected when idle state over 3ms is continued on D+, D- terminal.

Summary of interrupts

Status bit	Name	Abstract of interrupt factor	Relational status bit
VBUS	Vbus interrupt (connec/shut-down detect)	Change of the Vbus input (both "L" to "H" and "H" to "L")	Vbus
RESM	Resume detect interrupt	Resume signal received in suspended	—
SOFR	SOF detect interrupt	Received SOF	—
DVST	device state transition interrupt	Shift of device state	DVSQ[2:0]
CTRT	Control transfer stage transition interrupt	Stage shift of control transfer	CTSQ[2:0]
BEMP	Endpoint buffer empty/size-over interrupt	In each endpoint, when data transmit of all buffer is ended and buffer is empty, or in OUT transfer, received packet which exceeds max packet size.	EPB_EMP_OVR[5:0]
INTN	Endpoint buffer not ready interrupt	When buffer is in not ready state (SIE cannot read and write) to IN/OUT token of each endpoint.	EPB_NRDY[5:0]
INTR	Endpoint buffer ready interrupt	When buffer of each endpoint became ready (read enable/write enable)	EPB_RDY[5:0]

Each of "Set Address" and "Set Configuration" execution detects the device state shift by analyzing the device request in control transfer.
Each of these four factors can be set of its interrupt to enable or disable by setting the corresponded bit of interrupt enable register 0.
For example by using this interrupt, when USB bus reset is detected, a step to USB bus is available and when suspend is detected, a step to shift device to low power consumption.

Control transfer stage transition interrupt (CTRT)

M66290A manages the sequence of control transfer by H/W.
Each stage of control transfer, such as setup stage, data stage, and status stage can be known to refer to the "Interrupt Status Register 0".
Control transfer stage transition interrupt is occurred when the control transfer stage is shifted.
There are five factors, that is, setup stage end, control write transfer stage shift, control read transfer stage shift, control transfer end, and control transfer sequence error.
Except for setup stage, Each of these four factors can be set of its interrupt to enable or disable by setting the corresponded bit of interrupt enable register 0.
As to control transfer sequence error which can be recognized by H/W, refer to "Control transfer stage shift" in the item of "(3) Control transfer/enumeration" in the latter part.

Endpoint buffer empty/size-over interrupt (BEMP)

Interrupt factor is different by transfer direction of endpoint.

1. In case of transfer direction is IN
   In each endpoint, interrupt occurs when transmission ended of all data which is stored in the buffer.
   By this interrupt, when endpoint is set to double buffer, end of data transmission of all data of the buffer can be known.
   And also can know the end of data transmission of control read transfer in endpoint 0 (EP0).
2. In case of transfer direction is OUT
   In each endpoint, interrupt occurs in data packet receive when received packet which exceeds the maximum packet size.
   By refer to EPB_EMP_OVR[5:0] of interrupt status register, it can be known which endpoint occurred the interrupt.

Endpoint buffer not ready interrupt (INTN)

When the buffer is in not ready state to IN/OUT token of each endpoint, interrupt occurs at the timing of token packet receive end.
By refer to EPB_NRDY[5:0] of interrupt status register 1, it can be known which endpoint occurred the interrupt.

If endpoint is set to isochronous transfer, when over-run/ under-run error is occurred, interrupt occurs at the timing of token packet receive end.
And if it is set to isochronous (OUT), if received data has
error such as CRC error, interrupt occurs at the timing of transaction end.
The variety of error in isochronous transfer is known to refer "Isochronous Status Register".

Endpoint buffer ready interrupt (INTR)

Interrupt occurs when the buffer of each endpoint became ready (read/write is available).
It can be known which endpoint occurred the interrupt to refer EPB_RDY[5:0] of interrupt status register 1.
According to the endpoint and its access mode, the factor of interrupt is different as follows.

1. In case of EP0
   Interrupt occurs when receive (OUT) buffer of endpoint 0 became ready.
   If it is set to control write continuous receive mode, when continuous receive of 255 bytes ended or when received short packet, interrupt occurs.
   Interrupt is not occurred even if the transmit buffer became ready.
2. In case of EP1 to EP5, when CPU access
   Interrupt occurs when the buffer of each endpoint became ready.
3. In case of EP1 to EP5, when DMA access
   If the transfer direction is set to OUT, interrupt occurs when received short data packet and then ended DMA transfer.
   Interrupt is not occurred if the transfer direction is set to IN.

Figure 2. shows the examples of interrupt output timing

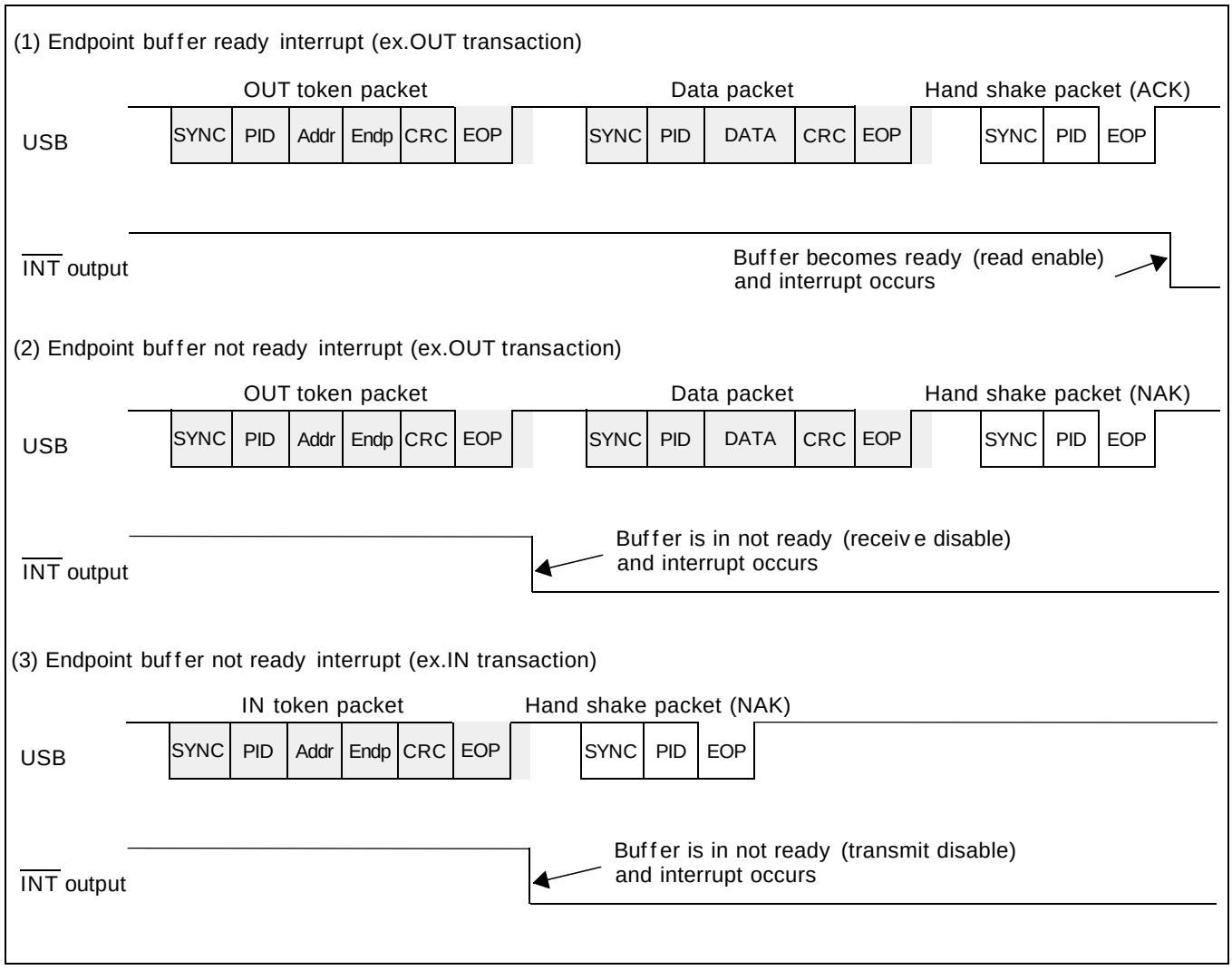


Figure 2. Examples of interrupt output timing

(2-1) Interrupt Enable Register 0 (Address : 10h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	INTNE	INTRE	URST	SADR	SCFG	SUSP	WDST	RDST	CMPL	SERR

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	VBSE	Vbus interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
14	RSME	Resume interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
13	SOFE	SOF interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
12	DVSE	Device state interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
11	CTRE	Control transfer interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
10	BEMPE	Endpoint5-0 buffer empty/size error interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
9	INTNE	Endpoint5-0 buffer not ready interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
8	INTRE	Endpoint5-0 buffer ready interrupt enable	0 : Disable 1 : Enable	W/R	0	0	-
7	URST	USB reset detect	If this bit is "1", then the DVST flag is set when detected USB reset.	W/R	0	0	-
6	SADR	Set Address execute	If this bit is "1", then the DVST flag is set after executed SetAddress.	W/R	0	0	-
5	SCFG	Set Configration execute	If this bit is "1", then the DVST flag is set after executed SetConfigration.	W/R	0	0	-
4	SUSP	Suspend detect	If this bit is "1", then the DVST flag is set when detected suspend.	W/R	0	0	-
3	WDST	Control write transfer status stage	If this bit is "1", then the CTRT flag is set when shifted to status stage in control write transfer.	W/R	0	0	-
2	RDST	Control read transfer status stage	If this bit is "1", then the CTRT flag is set when shifted to status stage in control read transfer.	W/R	0	0	-
1	CMPL	Control transfer complete	If this bit is "1", then the CTRT flag is set when control transfer completed (when the status stage completed normally).	W/R	0	0	-
0	SERR	Control transfer sequence error	If this bit is "1" then the CTRT flag is set when error occurred in the sequence of control transfer.	W/R	0	0	-

(2-2) Interrupt Enable Register 1(Address : 12h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										EPB_RE[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	EPB_RE [5:0]	Endpoint5-0 buffer ready interrupt enable	0 : Disable 1 : Enable The number of endpoint is correspond to each bit one by one.	W/R	00h	00h	-

(2-3) Interrupt Enable Register 2 (Address : 14h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										EPB_NRE[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	EPB_NRE [5:0]	Endpoint5-0 buffer not ready interrupt enable	0 : Disable 1 : Enable The number of endpoint is correspond to each bit one by one.	W/R	00h	00h	-

(2-4) Interrupt Enable Register 3 (Address : 16h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										EPB_EMPE[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	EPB_ EMPE [5:0]	Endpoint5-0 buffer empty/size error interrupt enable	0 : Disable 1 : Enable The number of endpoint is correspond to each bit one by one.	W/R	00h	00h	-

(2-5) Interrupt Status Register 0 (Address : 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VBUS	RESM	SOFR	DVST	CTRT	BEMP	INTN	INTR	Vbus	DVSQ[2:0]			VALID	CTSQ[2:0]		

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	VBUS	Vbus interrupt	This bit changes to "1" when Vbus input changed both "0" to "1" and "1" to "0". As to the Vbus input state, confirm to see the bit of Vbus input port. This bit is set even if the internal clock (sck) is in halt state. If "0" is written after enabled internal clock as operation, status flag is cleared. But if internal clock is in halt state, flag is not cleared. If "1" is written, flag is not changed.	W/R	0	0	-
14	RESM	Resume detect interrupt	This bit changes to "1" when USB bus state changed("J" to "K" or "SE0") under the condition that resume interrupt enable flag is set. This bit is set even if the internal clock (sck) is in halt state. If "0" is written after enabled internal clock as operation, status flag is cleared. But if internal clock is in halt state, flag is not cleared. If "1" is written, flag is not changed.	W/R	0	0	-
13	SOFR	SOF detect interrupt	This bit changes to "1" when detected SOF. If "0" is written, status flag is cleared. If "1" is written, flag is not changed.	W/R	0	0	-
12	DVST	Device state transition interrupt	This bit changes to "1" when device state shifted. There are four factors, that is, USB reset detect, suspend detect, "Set Address" execution, and "Set Configuration" execution. These four factors can be masked by the corresponded bit of "Interrupt Enable Register0" . If "0" is written, status flag is cleared. If "1" is written, flag is not changed.	W/R	0	0	1
11	CTRT	Control transfer stage transition interrupt	This bit changes to "1" when the stage of control transfer is shifted. There are five factors, that is, setup stage end, control write transfer status stage shift, control read transfer status stage shift, control transfer end, and control transfer sequence error. Four factors, except for setup stage end, can be masked by the corresponded bit of the "Interrupt Enable Register0". If "0" is written, status flag is cleared. If "1" is written, flag is not changed.	W/R	0	0	-
10	BEMP	Endpoint5-0 buffer empty/size error interrupt	The factor is different by the direction of the transfer of each endpoint. In each endpoint, this bit changes to "1" when the transmission of all stored data is completed (direction:IN) and when received the packet which is exceeded to maximum packet size (direction:OUT). The endpoint which occurs the interrupt can be checked to see the EPB_EMP_OVR[5:0]. This flag is cleared to clear the status flag of EPB_EMP_OVR[5:0].	R	0	0	-

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
9	INTN	Endpoint5-0 buffer not ready interrupt enable	This bit changes to "1" at the timing of token packet receive end when buffer respond NAK, of its not ready state, to IN/OUT token of each endpoint. The endpoint which occurred the interrupt is checked to see EPB_NRDY[5:0]. This flag is cleared to clear the status flag of EPB_NRDY[5:0].	R	0	0	-
8	INTR	Endpoint5-0 buffer ready interrupt enable	This bit changes to "1" when the buffer of each endpoint became ready (read/write enable). The endpoint which occurred the interrupt is checked to see EPB_RDY[5:0]. This flag is cleared to clear the status flag of EPB_RDY[5:0].	R	0	0	-
7	Vbus	Vbus input port	Input data from external Vbus is stored. 0: Vbus input port is "L" 1: Vbus input port is "H" External Vbus input data is latched by the positive edge of internal clock. Refer to this bit after enabled internal clock operation.	R	Ext.	Ext.	Ext.
6-4	DVSQ [2:0]	Device state	000: Powered State 001: Default State 010: Address State 011: Configured State 1xx: Suspended State Device state can be known. As to the device state shift, refer to Fig.5 in the later part. When detect USB reset, this becomes 001: Default state automatically. When detect suspend, this becomes 1xx: Suspended state automatically. Whatever the automatic response mode is, this becomes 010: Address state after executed Set_Address request, and becomes 011: Configured state after executed Set_Configuration request. (Write operation is available when S/W control mode is set)	R	000	000	001
3	VALID	Setup packet detect	This bit changes to "1" when received setup packet. This flag does not the factor of interrupt. When "0" is written, status flag is cleared . When "1" is written, flag is not changed .	W/R	0	0	-
2-0	CTSQ [2:0]	Control transfer Stage	000 : Idle or Setup stage 001 : Control read transfer data stage 010 : Control read transfer status stage 011 : Control write transfer data stage 100 : Control write transfer status stage 101 : Control write no data transfer status stage 110 : Control transfer sequence error 111 : Not assigned Can be seen the stage of control transfer. As to the stage shift of control transfer, refer to Fig.5 in the later part. (Write operation is available when S/W control mode is set)	R	000	000	-

(2-6) Interrupt Status Register 1 (Address : 1Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										EPB_RDY[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	EPB_RDY [5:0]	Endpoint5-0 buffer ready interrupt	When buffer becomes ready (read/write enabled) to each endpoint, the bit which corresponds to the number of endpoint changes to "1". The factor of the interrupt is different by the transfer condition of each endpoint. 1. As to EP0 This bit changes to "1" when receive buffer(OUT) became ready (read enabled) in control write transfer. If it is set to control write continuous receive mode or completed receiving of the data of 255Bytes or received short data packet, this bit changes to "1". This bit is not changed even if the transmission buffer(IN) became ready (write enabled) in control read transfer. The ready state of the transmission buffer(IN) can be known by the buffer empty interrupt. 2. As to EP1 to EP5, when CPU access This bit changes to "1" when each buffer of each endpoint became ready(read/write enabled). This bit also changes to "1" when set the direction of the transfer to IN in initialization. 3. As to EP1 to EP5, when DAM access If the direction of the transfer is set to OUT, this bit changes to "1" when received short data packet and then completed DMA transfer of received data. In this case, clear is only available to write the BCLR command. This bit is not changed if the direction of transfer is set to IN. Clearance of this flag is different by the transfer direction of endpoint. 1. If the transfer direction is OUT After set the number of the object endpoint to the "FIFO Selection Register", write BCLR command or read all data of the buffer, then flag is cleared. (When DMA access, clearance is only available to write BCLR command) 2. If the direction is IN After set the number of the object endpoint to the "FIFO Selection Register", write IVAL command or write data into the buffer of maximum packet size (buffer size, if in continuous transmission mode), then flag is cleared.	R	00h	00h	-

(2-7) Interrupt Status Register 2 (Address : 1Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										EPB_NRDY[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	EPB_ NRDY [5:0]	Endpoint5-0 buffer not ready interrupt	To IN/OUT token of each endpoint, if the set of response PID is not NAK("00") and if buffer is in not ready state (receive/transmit disabled), the bit which corresponds to the number of endpoint changes to "1". (If the endpoint is control transfer or bulk transfer or interrupt transfer, NAK response is executed) If the endpoint is set to isochronous transfer, M66290A does not execute NAK response, but when over-run or under-run of endpoint buffer occurred, this bit changes to "1" at the timing of token packet receive end. If it is set to isochronous (OUT), and if received data has error such as CRC, this bit changes to "1" at the timing of transaction end. When "0" is written, status flag is cleared. When "1" is written, flag is not changed.	W/R	00h	00h	-

(2-8) Interrupt Status Register 3 (Address : 1Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
										EPB_EMP_OVR[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 6	Reserved		Write/Read "0"				
5 to 0	EPB_EMP_OVR [5:0]	Endpoint5-0 buffer empty/size error interrupt	When factors below are occurred to each endpoint, the bit which corresponds to the number of endpoint, changes to "1". 1. If the transfer direction is IN In each endpoint, when transmission completed of all data which stored in buffer, c By this interrupt, if endpoint is set to double buffer, it can be known that transmission of all data of buffer is completed. And also by this interrupt, it can be known that transmission of EP0 is completed. 2. If the direction is OUT In each endpoint, when received data which exceeds the maximum packet size in data packet receive, the bit which corresponds to the number of endpoint changes to "1". When "0" is written, status flag is cleared. When "1" is written, status flag is not cleared.	W/R	00h	00h	-

(3) Control transfer / Enumeration

In control transfer, there are setup stage, data stage, and status stage.
M66290A manages stage and inform CPU the stage shift by interrupt. CPU do stage transact of control transfer according to the interrupt factor.

Setup stage

In setup stage, 8Bytes request (setup data) of setup transaction data packet which transferred from host is stored into four registers automatically (Request, Value, Index, and Length register).
Except for device state shift request (Set Address and Set Configuration) which can cope with by the automatic response control function, analysis (decode) and execution of contents of request must be done by CPU. By executing the request, it proceeds to data stage or to status stage.

Data stage

Data stage executes IN transaction or OUT transaction according to the contents of request. If it is control write transfer, data stage is OUT transaction and CPU prepares for data receive at the timing of interrupt in setup stage and reads the received data from endpoint FIFO when data receive ended.

If it is control read transfer, data stage is IN transaction and CPU prepares for data transmit (write into endpoint FIFO) at the timing of interrupt in setup stage.
M66290A is equipped with control transfer continuous transmit and receive function. After ended data stage, it proceeds to status stage.

Status stage

Status stage executes receive/transmit of Null data (data length 0), in both control write and control read transfer. Receive/transmit of Null data is possible to set control transfer complete enable bit (CCPL) after ended setup stage.
Control transfer complete enable bit is reset when received setup packet.

Control transfer executes data transfer using EP0. To both control read and control write, buffer size of EP0 can be set by a unit of 64Bytes by "Control Transfer Control Register".
Access to EP0_FIFO data register must be done by CPU access. DMA transfer can not be set.

Figure 3. shows the abstract of enumeration operations.

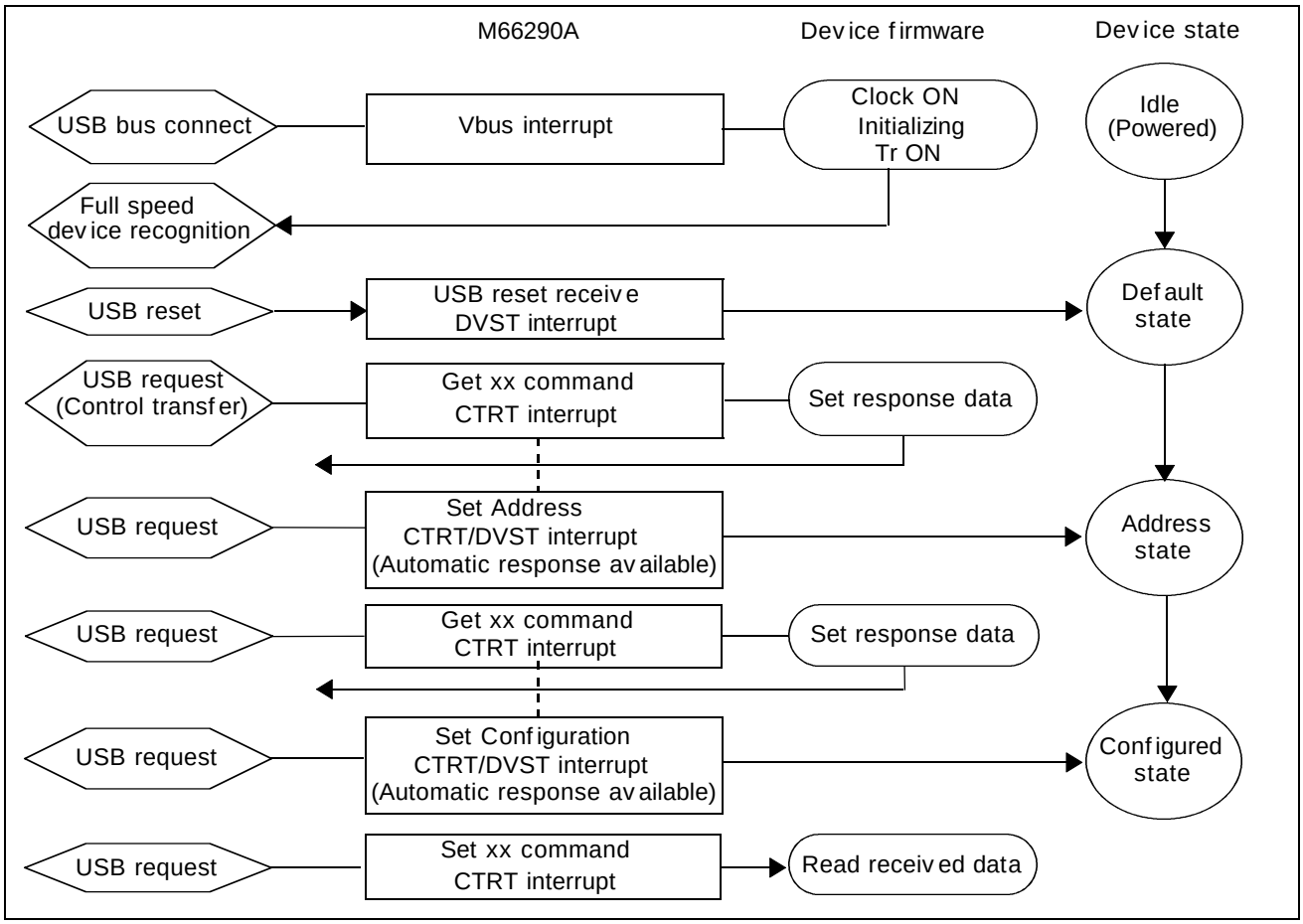


Figure 3. Abstract of enumeration operations

Auto-response control function

M66290A has auto-response function to device state transition request (Set Address and Set Configuration)in control transfer.
By the set of "Auto-response Control Register", auto-response mode to Set Address and to Set Configuration can be set individually.
If the auto-response mode is set, device state transition request can be ended without occurring interrupt.

Continuous transfer function

M66290A has continuous transfer function to transmit/receive continuously of requested data which extend plural of transaction.
If continuous transfer mode is set, it can transfer the transmit which data length is set to "EP0 Continuous Transmit Data Length Register", without occurring interrupt.
Control read buffer can be set up to 256Bytes at a unit of 64Bytes. Control write buffer can receive continuously up to 255Bytes, so secure the area of 256Bytes.

Abstract of control transfer operations

Figure 4. shows examples of abstraction of control transfer operations.

Transfer direction of packet : Host to M66290A M66290A to Host

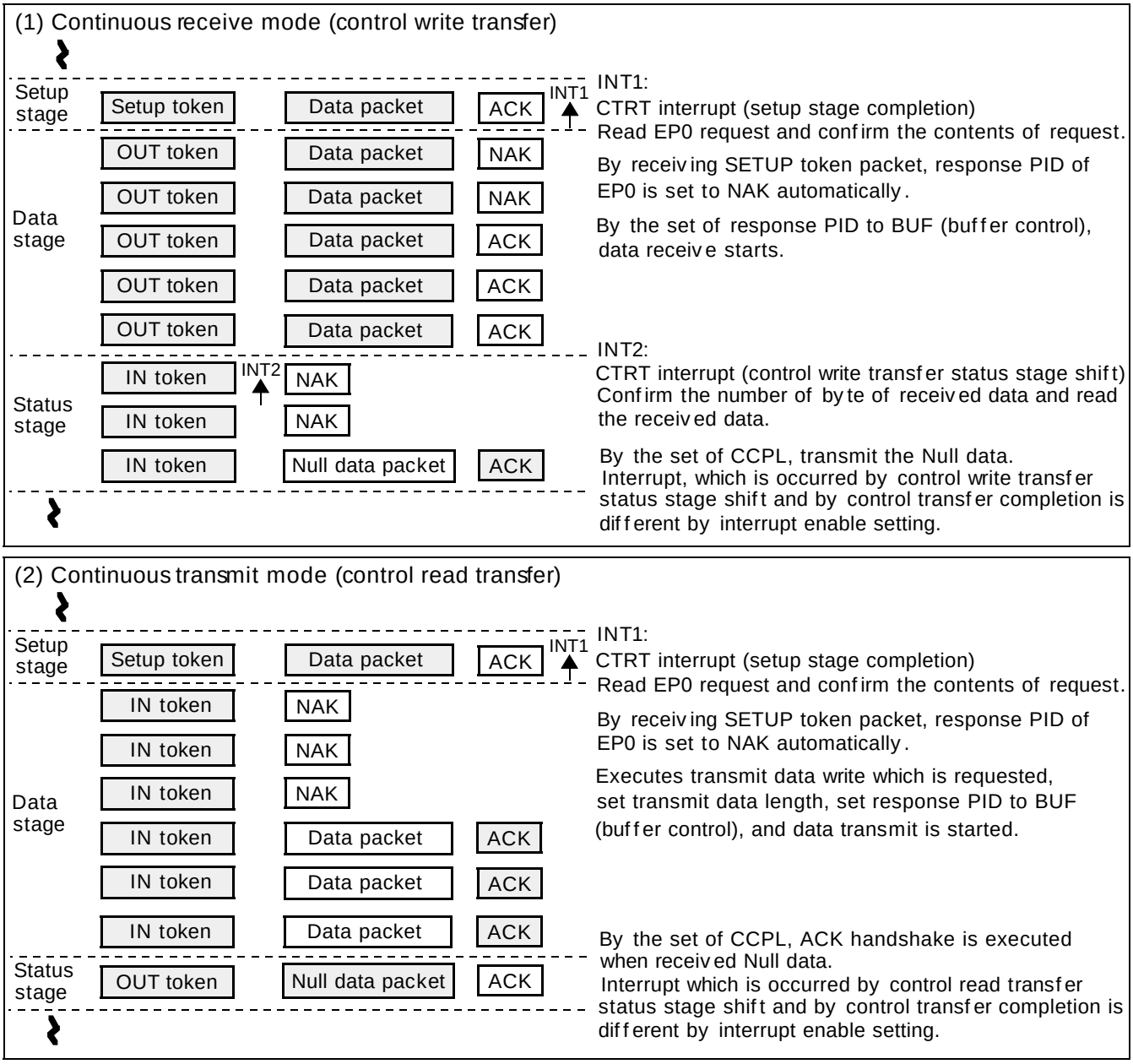


Figure 4. Examples of abstract of control transfer operations

Device state transition

M66290A manages device state by H/W.
It manages Powered, Default, Address, Configured, and Suspended state of USB device state.
To Set_Address and Set_Configuration request in auto-response mode, transfer can be completed without occurring interrupt to CPU.
To Set_Address request, auto-response is executed to Set_Address request (DeviceAddess=01h to 7Fh) which device state is in Default state, and to other state and to Set_Address request which DeviceAddess is not equal to 01h to 7Fh, auto-response is not executed.
To Set_Configuration request, auto-response is executed to Set_Configuration request (ConfigurationValue is not equal to 0) which device state is in Address state and to Set_Configuration request (ConfigurationValue=0) which device state is in Configured state.
To other state and to Set_Configuration request which is different of its ConfigurationValue from the value above, auto-response is not executed.

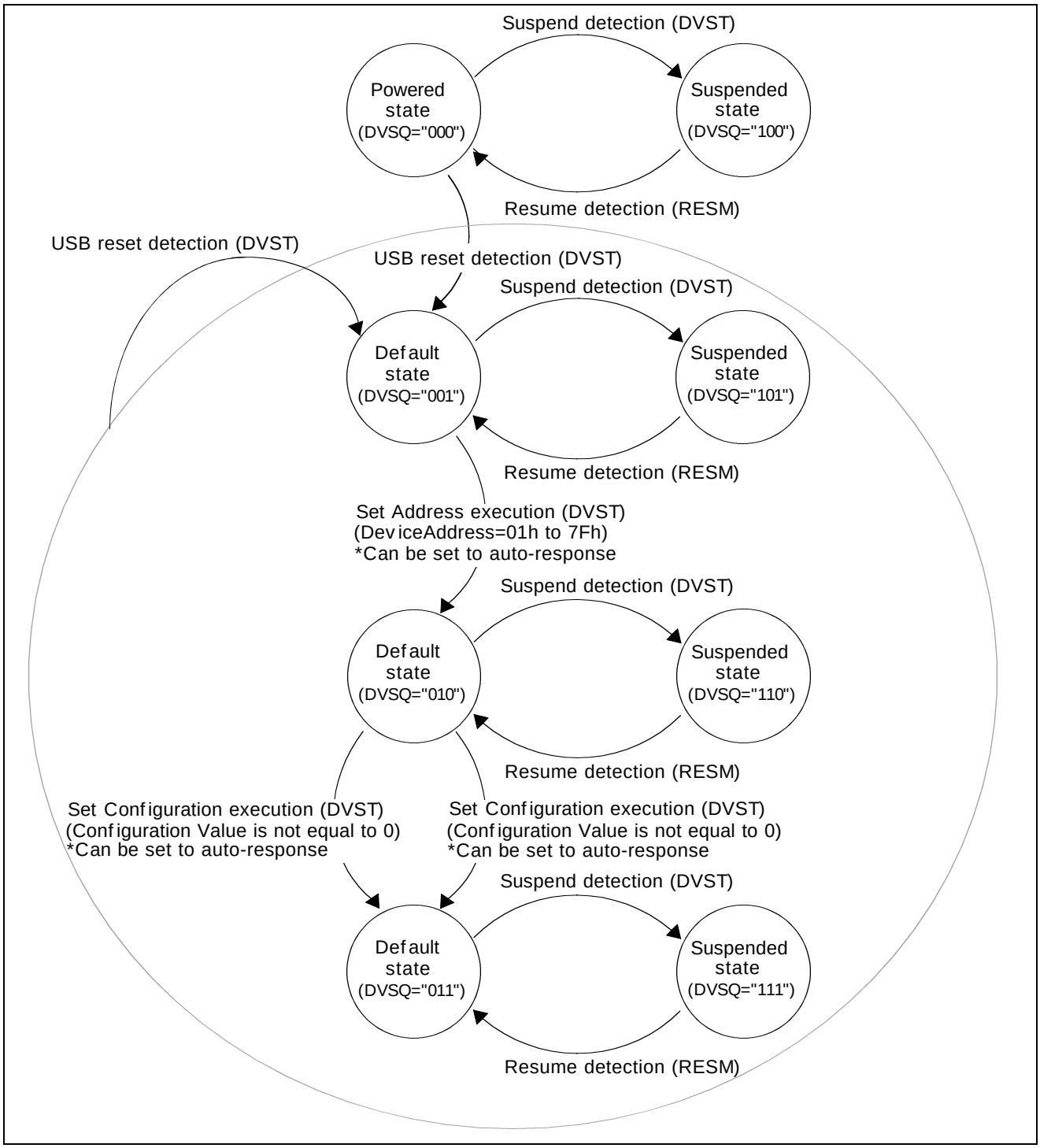


Figure 5. Device state shift

Control transfer stage transition

M66290A manages control transfer sequence by H/W. There are setup stage, data stage, and status stage in control transfer stage, as shown in figure 6. And when stage shifts, CTRT interrupt occurs.
There are five factors in CTRT interrupt, that is, setup stage end, control write transfer status stage shift, control read transfer status stage shift, control transfer end, and control transfer sequence error. And there are seven errors as follows in control transfer sequence error which can be detected by H/W.
If H/W detected control transfer sequence error, response PID is set to STALL("1x") automatically.

1. IN token packet receive in control write data stage (In token packet receive which did not do ACK handshake once to OUT token packet in data stage)
2. OUT token packet receive in control write status stage
3. OUT token packet receive in control read data stage. (OUT token packet receive which did not do data transfer once to IN token packet in data stage).
4. IN token packet receive in control read status stage.
5. Data packet receive except for Null data in control read status stage.
6. OUT token packet receive in control write no data status stage.
7. Data receive which exceeds maximum packet size.

   In control write data stage, it can not be recognized as sequence error when received data packet which exceeds request wLength value.

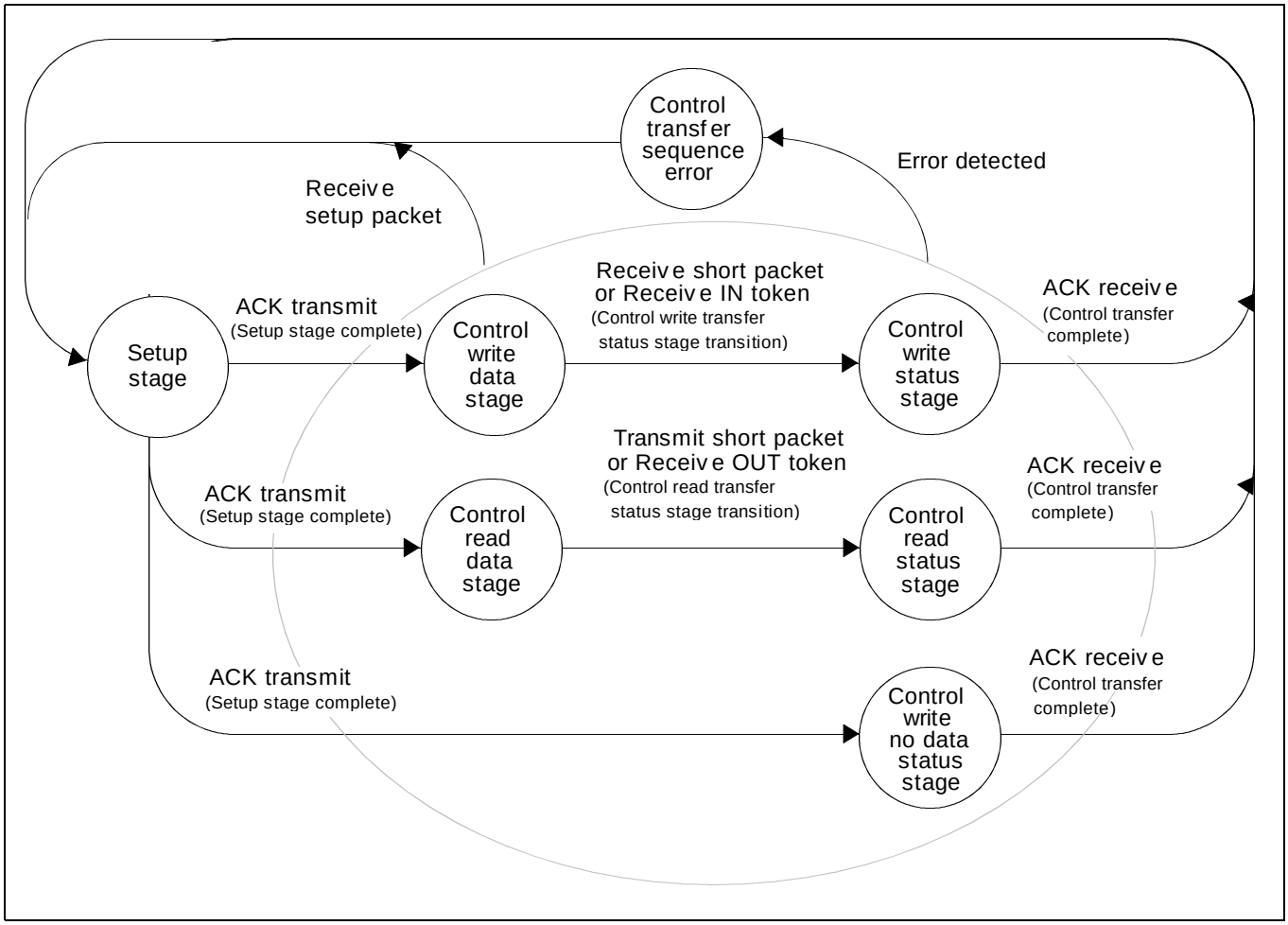


Figure 6. Stage shift of control transfer

(3-1) Request Register (Address : 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bRequest[7:0]								bmRequestType[7:0]							

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 8	bRequest [7:0]	Request register	This fields provides bRequest of the last setup packet received.	R	00h	00h	-
7 to 0	bmRequest Type [7:0]	RequestType register	This fields provides bmRequest of the last setup packet received.	R	00h	00h	-

(3-2) Value Register (Address : 22h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
wValue[15:0]															

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 0	wValue [15:0]	Value register	This fields provides wValue of the last setup packet received.	R	0000h	-	-

(3-3) Index Register (Address : 24h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
wIndex[15:0]															

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 0	wIndex [15:0]	Index register	This fields provides wIndex of the last setup packet received.	R	0000h	-	-

(3-4) Length Register (Address : 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
wLength															

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 0	wLength [15:0]	Length register	This fields provides wLength of the last setup packet received.	R	0000h	-	-

(3-5) Control Transfer Control Register (Address : 28h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CTRR		Ctr_Rd_Buf_Nmb[5:0]						CTRW		Ctr_Wr_Buf_Nmb[5:0]					

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	CTRR	Control read transfer continuous transmit mode	Control read transfer continuous transmit mode is set when "1" is written in this bit.	W/R	0	-	-
14	Reserved		Write/Read "0"				
13 to 8	Ctr_Rd_ Buf_Nmb [5:0]	Control read buffer start number	Appoint the start number of the buffer which is used in control read transfer by a unit of 64bytes. The buffer is available from #00h to #2Fh. When control read continuous transmit mode is set, it can transmit continuously up to 255Bytes, so keep the area of the buffer of 256Bytes (4 blocks).	W/R	00h	-	-
7	CTRW	Control write transfer continuous receive mode	When "1" is written, control write transfer continuous receive mode is set.	W/R	0	-	-
6	Reserved		Write/Read "0"				
5 to 0	Ctr_Wr_ Buf_Nmb [5:0]	Control write buffer start number	Appoint the start number of the buffer which is used in control write transfer by a unit of 64bytes. The buffer is available from #00h to #2Fh. When control write continuous receive mode is set, it can receive continuously up to 255bytes, so keep the area of buffer of 256bytes (4 blocks).	W/R	00h	-	-

(3-6) EP0 Packet Size Register (Address : 2Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
									EP0_MXPS[6:0]						

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 7	Reserved		Write/Read "0"				
6 to 0	EP0_MXPS [6:0]	Max Packet size	Set the maximum value of data (byte) which transmit or receive in a packet transfer. Set the value of wMaxPacketSize in request. This bit must be set after set the response PID to NAK("00").	W/R	08h	-	-

(3-7) Auto-response Control Register (Address : 2Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														ASCN	ATAD

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 2	Reserved		Write/Read "0"				
1	ASCN	Set_Configuration Auto-response mode	When "1" is written into this bit, auto-response mode of Set_Configuration request is set. To the Set_Configuration request in auto-response mode, transfer can be completed without occurring interrupt to CPU. (Set of CCPL is not needed) Auto-response is done to the Set_Configuration request (ConfigurationValue is not equal to 0) in Address device state and to the Set_Configuration request (ConfigurationValue is equal to 0) in Configured state. To the other state and to the Set_Configuration request which ConfigurationVale is different from the value above, auto-response is not done.	W/R	0	-	-
0	ASTD	Set_Address Auto-response mode	When "1" is written into this bit, automatic response mode of Set_Address request is set. To the Set_Address request in automatic response mode, transfer can be completed without occurring the interrupt to CPU. (Set of CCPL is not needed) Automatic response is done to the Set_Address request (DeviceAddress is equal to 01h to 7Fh) which device state is Default state. To the other state and to the Set_Address request which DeviceAddress is not equal to 01h to 7Fh, automatic response is not done.	W/R	0	-	-

(3-8) EP0_FIFO Selection Register (Address : 30h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RCNT					Octl										ISEL

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	RCNT	Read count mode	If this bit is "1", every time when read EP0_FIFO register,the value of ODLN register is counted down.	W/R	0	-	-
14 to 11	Reserved		Write/Read "0"				
10	Octl	FIFO access 8 bit mode	If this bit is set to "1", data register of FIFO turns to 8-bit mode and lower 8 bit[7:0] becomes enable when access the "FIFO Data Register" of endpoint. When transmit data of odd number byte, data must be written in 8-bit mode. When read in 8-bit mode, set to 8-bit mode before data receive.	W/R	0	-	-
9-1	Reserved		Write/Read "0"				
0	ISEL	Buffer select	0 : Control write (OUT) buffer select 1 : Control read (IN) buffer select	W/R	0	-	-

(3-9) EP0_FIFO Control Register (Address : 32h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EP0_PID[1:0]		IVAL	BCLR	E0req	CCPL			ODLN[7:0]							

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 14	EP0_PID [1:0]	Response PID	Setting the response PID. 00 : NAK Whatever the buffer state is,do NAK handshake. 01 : BUF Response PID is selected by the state of buffer and sequence toggle bit status. (One of ACK, NAK, and DATA0/DATA1) 1x : STALL Do STALL handshake 1. When received Setup packet, turns to "00"(=NAK) automatically. 2. When received request (Set_Address, etc.) which is set to automatic response, turns to "01"(=ACK) automatically after completed the Setup transaction. 3. If sequence error occurred in control transfer,or received data in control write transfer which exceed maximum packet size, this turns to "1x'(=STALL) automatically.	W/R	00	-	-
13	IVAL	In buffer status	If the control read buffer is selected, this becomes IN buffer effective state flag. When set to "1", it becomes to transmit data set state (SIE read enabled). If data is written which exceeds to the maximum byte of maximum packet size (MXPS), this bit is set to "1". When short packet transmit, set this bit to "1" after wrote transmit data. If the IVAL="1" and BCLR="1" is written at the same time, IN buffer effective state flag is set. (This is effective to transmit 0 length data) If the control readout) buffer is selected, it becomes OUT buffer effective state status. Status "1" shows that there is data which can be read. This bit shows the effective value when E0req bit is "0". If "1" is written, it is not changed. If "0" is written, flag is not changed.	W/R	0	-	-
12	BCLR	Buffer clear	If "1" is written into this bit When the selected endpoint is set to IN, IN buffer effective state flag and the data (byte) which is written are cleared. If IVAL="1" and BCLR="1" is written at the same time, data is cleared but IN buffer effective state flag is set.(This is effective to transmit 0 length data) When "1" is written into this bit, if the selected endpoint is set to OUT, OUT buffer effective state flag is cleared and read data is also cleared. When "0" is written, this bit is not changed.	W/R	0	-	-
11	E0req	EP0_FIFO ready	If this bit is "0", access to EP0_FIFO data register is enabled. And when this bit is "0", IVAL and ODLN bit shows the effective value. EP0_FIFO data register, when read or write, needs cycle time of 200ns (min). (Continuous access at 5MHz is available)	R	1	-	-

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
10	CCPL	Control transfer complete enable	To write "1" into this register, status stage of control transfer can be completed. If this bit is "1" and response PID is BUF("01"), Null data is transmitted in control write transfer, and do response ACK in control read transfer when received NULL data. If this bit is "0", do response NAK in status stage. This flag is reset to "0" when received setup packet.	W/R	0	-	-
9 to 8	Reserved		Write/Read "0"				
7 to 0	ODLN [7:0]	Control write receive data length	Received data length(byte) can be read from this register. If RCNT mode is set, every time when read EP0_FIFO data register, it is counted down by -1(8-bit mode) or by -2(16-bit mode). This bit shows effective value when E0req bit is "0".	R	00h	-	-

(3-10) EP0_FIFO Data Register (Address : 34h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EP0_FIFO[15:0]															

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 0	EP0_FIFO [15:0]	EP0_FIFO data	When read, this becomes to receive data FIFO register. If it is set to 8-bit mode, lower 8 bit[7:0] is valid. When write, this becomes to transmit data FIFO register. If it is set to 8-bit mode, lower 8 bit[7:0] is valid. Both for read and write, cycle time of 200ns (min) is needed. (Continuous access at 5MHz is available) Read when IN buffer is selected or write when OUT buffer is selected is inhibited.	W/R	xxxx	-	-

(3-11) EP0 Continuous transmit Data Length (Address : 36h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								SDLN[7:0]							

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
14-8	Reserved		Write/Read "0"				
7 to 0	SDLN [7:0]	Control read continuous transmit data length	Set the control read continuous transmit data length (byte). It can be set up to FFh (255bytes). In control read continuous transmit mode, write FIFO data (transmit data) after set this register. This is available in control read continuous transmit mode.	W/R	00h	-	-

(4) Endpoint and FIFO control

Except for EP0 for control transfer, M66290A can set five endpoints as EP1 to EP5.
Each of these five endpoints (EP1 to EP5) can be set to bulk, interrupt, and isochronous transfer. And yet, another constitution can configurated independently.
Below are the constitutions to be realized.
Built-in FIFO for endpoint buffer is 3kBytes totally of its memory capacity. This FIFO of 3kBytes can divided into each endpoint of EP0 to EP5 and to each endpoint, can assign up to 1024Bytes (max) by a unit of 64Bytes.
Buffer size of each endpoint must be set to over the capacity which is set in maximum buffer size.
In the buffer size, which is set, bytes of maximum packet size is used for valid. (If set the buffer size to 128Bytes to the endpoint which maximum packet size is set to 64Bytes, 64Bytes are valid)
We show setting examples to each of these buffer of EP0 to EP5 below, and next explain about continuous transmit and receive function, FIFO control, DMA transfer, and double buffer.

Continuous transfer function

Continuous transfer function is to transmit/receive data which extend plural transaction without occurring interrupt to CPU.
For EP1 to EP5, this function is effective when transfer type is bulk transfer.
In each endpoint, when continuous transfer mode is set, it can transfer data up to the buffer size which is set to the endpoint without occurring interrupt to CPU.

Construction of endpoint (EP1 to EP5) FIFO

	Register	EP1 to EP5
Transfer type	EPi_TYP[1:0]	Can be set to Bulk, Interrupt, isochronous transfer.
Transfer direction	EPi_DIR	Can be set to IN/OUT
Double buffer (Toggle buffer)	EPi_DBLB	Can be set
Continuous transmit/receive	EPi_RWMD	Can be set (Effective in bulk transfer)
Buffer size	EPi_Buf_siz[3:0]	Can be set (Up to 1024bytes by a unit of 64bytes)
Response PID	EPi_PID[1:0]	Can be set to NAK, STALL, and BUF(buffer control).
DMA transfer	EPi_DMAE	Can be set
Receive data read and abandon mode	EPi_ACLR	Can be set
Max packet size	EPi_MXPS[9:0]	Can be set (0 to 1023bytes)

To use with double buffer constitution, 1kBytes x2 maximum of buffering is realized.
Continuous receive mode can receive data packet continuously up to the buffer size which is set, or until receives short packet. If the data to be received is data packet of max packet size, it can receive continuously up to the buffer size without occurring interrupt to CPU, and if the data is data packet (max packet size) which is less than buffer size, interrupt to CPU is not occurred.
In bulk transfer, when set max packet size as 64Bytes, buffer size as 1024Bytes, and FIFO constitution as double buffer, when received data of max packet size as 16 times (1024Bytes), it became buffer redried enable) and urge to CPU by interrupt to read received data. When received short packet, ends the continuous receive and buffer became redried enable).
Continuous transmit mode can transmit data packet continuously up to buffer size which is set. Short packet transmit can be done to set IVAL flag. And it is needed to set IVAL flag to transmit a multiple data of maximum packet size which is less than buffer size.
By set Null data transmit addition mode, when write a multiple data of max packet size into buffer and transmit, Null data can be transmitted automatically after the last packet is transmitted .

Examples of endpoint FIFO setting

FIFO number	Memory address	Endpoint setting
00h to 03h	000h to 0FFh	EP0:Control write transfer Buffer size:256Bytes Control write continuous receive mode(CTRW) FIFO area:256Bytes(4 blocks)
04h to 07h	100h to 1FFh	EP0:Control read transfer Buffer size:256Bytes Control read continuous transmit mode(CTRR) FIFO area:256Bytes(4 blocks)
08h	200h to 23Fh	EP2:Interrupt transfer(IN) Buffer size:64Bytes FIFO area:64Bytes(1 block)
09h	240h to 27Fh	EP4:Interrupt transfer(OUT) Buffer size:64Bytes FIFO area:64Bytes(1 block)
0Ah to 0Bh	280h to 2FFh	EP3:Bulk transfer(IN) Buffer size:64Bytes Double buffer constitution(DBLB) FIFO area:128Bytes(2 blocks)
0Ch to 0Fh	300h to 3FFh	Not used:256Bytes(4 blocks)
10h to 2Fh	400h to BFFh	EP1:Bulk transfer(OUT) Buffer size:1024Bytes Double buffer constitution(DBLB) Continuous receive mode(RWMD) FIFO area:2kBytes(32 blocks)

FIFO control

Access to endpoint buffer of EP0 to EP5 is done by three FIFO data registers. One is only for EP0 and Others are common to EP1 to EP5. Common data registers are divided into two, because accessing is different, that is for CPU access and for DMA transfer. Which endpoint of EP1 to EP5 to be accessed can be selected to set each FIFO selection register.

Endpoint	Accessing	Register name
EP0	CPU access	EP0_FIFO data register
EP1 to EP5	CPU access	CPU_FIFO data register
	DMA transfer	DMA_FIFO data register

Each of three FIFO registers has functions as follows. And these functions can be used to set "Each FIFO Selection/Control Register".

Short packet transmission function
(IVAL : IN buffer status bit)

Transmit/receive buffer clear function
(BCLR : Buffer clear bit)

Null data (data length 0) transmit function
(IVAL & BCLR)

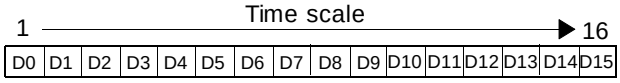
Data length (8/16 bit) set function
(Octl : Register 8bit mode bit)

Received data length count down function
(RCNT : Read count mode bit)
*: There is none for DMA transfer

Access to CPU_FIFO data register when interrupt occurred, to know the endpoint which requested access, access the "Interrupt Status Register 0/1" and by checking the interrupt status flag and know the endpoint which requested access, and then set endpoint to be accessed by "CPU_FIFO Selection Register".
If there is no change of endpoint setting, it is not needed to set again the CPU access endpoint appointment bit.

Data transfer procedure

Data which is set to endpoint FIFO, is sent to USB bus by LSB first. When store the received data from USB bus to endpoint FIFO, it is as the same as above.



(Data send procedure to USB bus)

DMA transfer

To endpoint of EP1 to EP5, 16bits width or 8bit width of DMA
transfer is available.
Each endpoint of EP1 to EP5 can be set to CPU access mode or DMA access mode by set of "EPx Configuration Register 1" mentioned later.

DMA transfer is realized to hand shake with external DMAC and Dreq, Dack signal. Dreq is asserted when endpoint buffer, which is set to DMA transfer mode, became ready. The means of Buffer ready state is, if the endpoint transfer
direction is set to Out (recive data from host) buffer ready means that in read enable state, if the endpoint transfer direction is set to IN(transmit data to host) buffer ready means that in write enable state. Setting the transfer direction can be done by "EPi Configuration Register 0" to each endpoint.

When Dack comes from external DMAC after asserted Dreq, Dreq is negated.
In DMA transfer, Dack is dealt equivalently with CS signal and DMA_FIFO address appointment.
Appoint read or write operation by RD or WR signal.
This DMA transfer can be used only for single transfer, which
transfers one word (16bit or 8bit) by one time Dreq start.

In DMA transfer, as same as the CPU access, occurs endpoint buffer not ready interrupt and endpoint buffer empty interrupt according to endpoint buffer state. But as to endpoint buffer ready interrupt, it is not same as the CPU access as follows.

In DMA transfer, endpoint buffer ready interrupt is not occurred if the transfer direction is IN.
If the transfer direction is OUT, interrupt is occurred when received short data packet and ended data transfer of all data which received in DMA transfer.
Occurring of endpoint buffer ready interrupt and to refer DMA_DTLN, it can be known that short data packet was received.
DMA_DTLN shows the number of byte of short data packet,
or in the continuous receive mode it shows the number of byte
of received data before short data packet receive.

Double buffer operations

The endpoint FIFO of EP1 to EP5 can be set to double buffer constitution.
So a double of transfer data of its buffer size, which is set, can be stored.

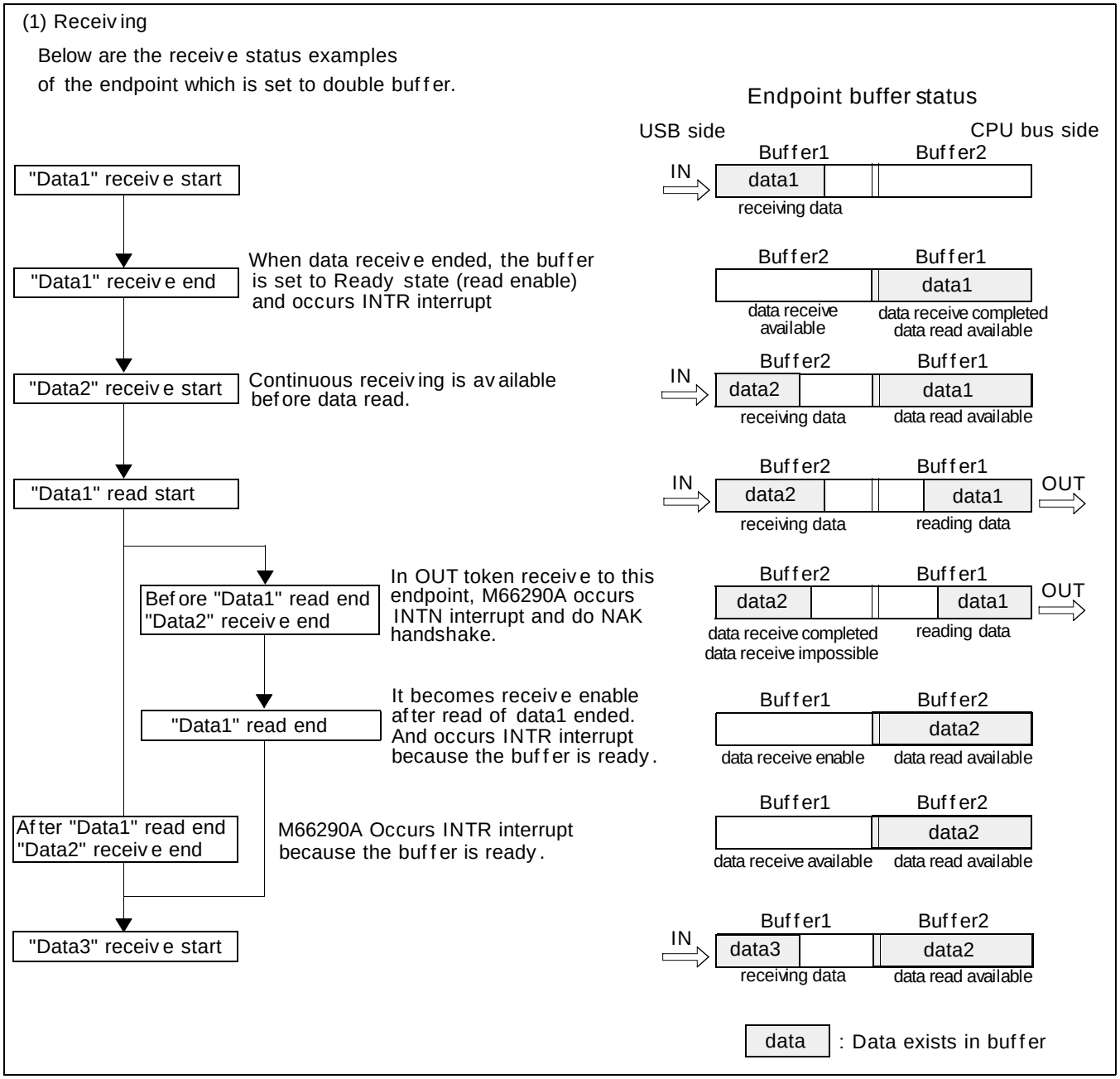


Figure 7. Double buffer activities-1

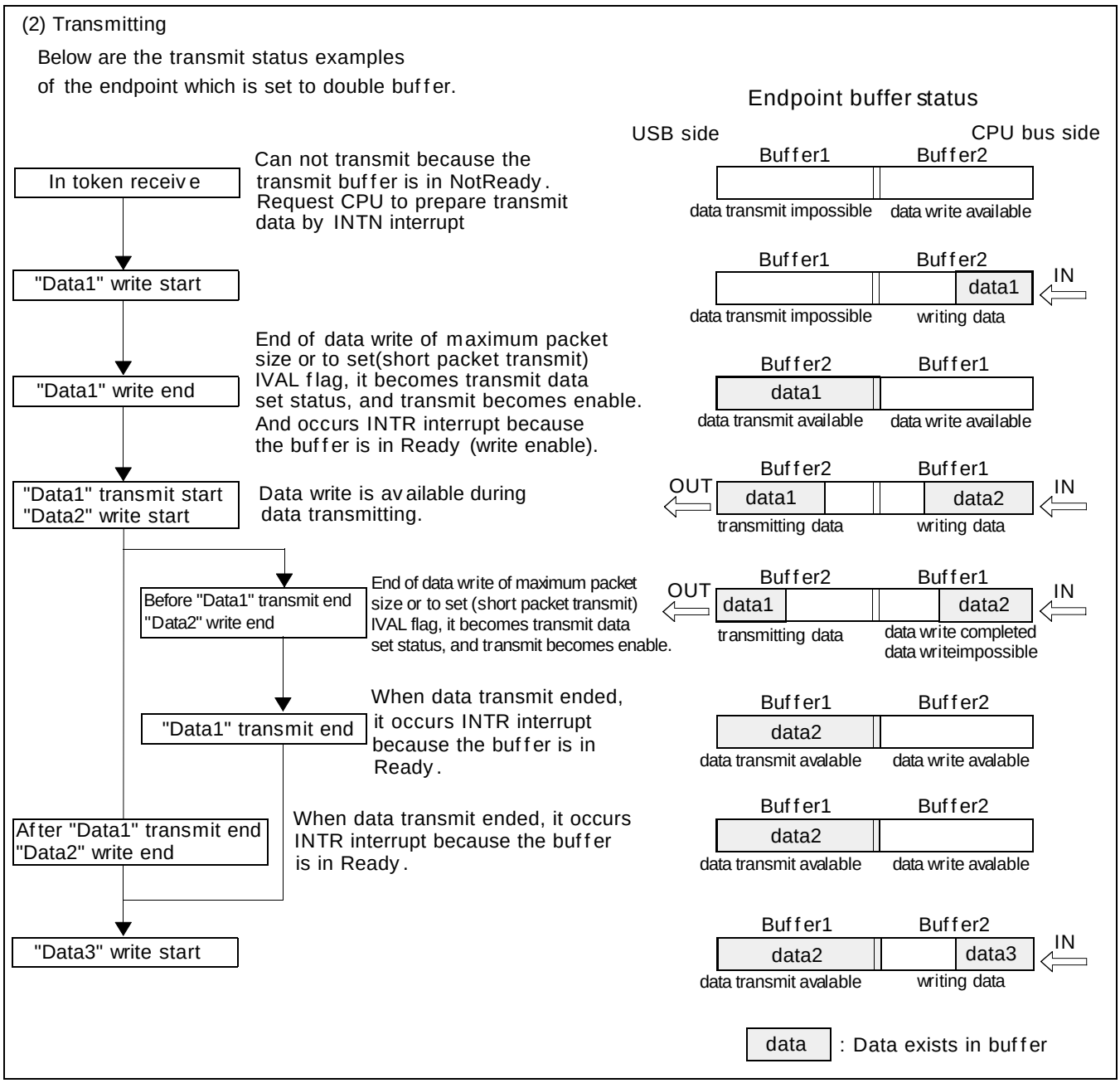


Figure 8. Double buffer activities-2

(4-1) CPU_FIFO Selection Register (Address : 40h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RCNT												CPU_EP[3:0]			

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	RCNT	Read count mode	If this bit is "1", every time when read CPU_FIFO register, CPU_DTLN register value is counted down.	W/R	0	-	-
14 to 4	Reserved		Write/Read "0"				
3 to 0	CPU_EP [3:0]	CPU access endpoint	Appoint the CPU access endpoint. "0001"=EP1,"0010"=EP2,"0011"=EP3, "0100"=EP4,"0101"=EP5 EP0 can not be appointed. Don't change the setting in writing (IN) or in reading (OUT). Change of the setting of the endpoint of direction IN must be done after confirmed that IVAL="0" and Creq="0", or IVAL="1" and Creq="1". Change of the setting of the endpoint of direction OUT must be done after confirmed that IVAL="1" and Creq="0", or IVAL="0" and Creq="1".	W/R	0000	-	-

(4-2) CPU_FIFO Control Register (Address : 42h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		IVAL	BCLR	Creq	CPU_DTLN[10:0]										

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15, 14	Reserved		Write/Read "0"				
13	IVAL	IN buffer status	If the selected endpoint is set to IN, this becomes IN buffer effective state flag. When set to "1", it becomes transmit data set state. (SIE is available to read) When the data (byte) which exceeds to the maximum packet size (MXPS) is written, this bit is set to "1". In short packet transmit, set this bit to "1" after wrote the transmit data. If IVAL="1" and BCLR="1" is written at the same time, the effective state flag is set. (This is effective to transmit 0 length data) If the selected endpoint is set to OUT, it becomes to OUT buffer effective state status. Status "1" shows that there is data which is available to read. When Creq bit is "0", this bit shows effective value. This bit is not changed when "1" is written. Flag is not changed when "0" is written.	W/R	0	-	-

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
12	BCLR	Buffer clear	If the selected endpoint is set to IN, when "1" is written into this bit, the IN buffer effective state flag and the data (byte) which is written are cleared. If IVAL="1" and BCLR="1" is written at the same time, data is cleared but the IN buffer effective state flag is set. (This is effective to transmit 0 length data) If the selected endpoint is set to OUT, when "1" is written into this bit, the OUT buffer effective state flag and the read data (byte) are cleared. If it is set to double buffer, the state of write/read enable buffer for CPU is cleared. To set the EPi_ACLR, USB bus buffer is cleared. This bit is not changed when "0" is written.	W/R	0	-	-
11	Creq	CPU_FIFO ready	If this bit is "0", access to CPU_FIFO data register is available. And if this bit is "0", the bit of IVAL and CPU_DTLN bit shows the effective value. When read or write to CPU_FIFO register, 200ns (min) of cycle time is needed. (Continuous access at 5MHz is available) If the access end point is changed, 200ns (min) of recovery time is needed.	R	1	-	-
10 to 0	CPU_DTLN[10:0]	CPU_FIFO receive data length	When read this register, receive data length (byte) appears. When RCNT mode is set, every time when read CPU_FIFO register, it is counted down by -1 (8-bit mode) or by -2 (16-bit mode). If RCNT mode is not set, this register turns to 000h after all of received data is read. This bit shows effective value when Creq bit is "0".	R	000h	-	-

(4-3) CPU_FIFO Data Register (Address : 44h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CPU_FIFO[15:0]															

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 0	CPU_FIFO [15:0]	CPU_FIFO data	If the selected endpoint is set to OUT, this becomes to receive data FIFO register. If the selected endpoint is set to IN, this becomes to transmit data FIFO register. If the selected endpoint is set to 8-bit mode, lower 8 bit [7:0] is valid. When read or write, 200ns (min) of cycle time is needed. (Continuous access at 5MHz is available) Read operation when direction IN is appointed or write operation when direction OUT is appointed, write operation is inhibited.	W/R	xxxx	-	-

(4-4) DMA_FIFO Selection Register (Address : 48h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MODE							DMAEN					DMA_EP[3:0]			

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15	MODE	DMA operation mode	Set the operation mode of DMA transfer. 0 : High speed transfer mode 1 : One word transfer mode In high speed transfer mode, when endpoint buffer is in read/write enable in the state that DMA transfer enable, Dreq is asserted. In one word transfer mode, when endpoint buffer is in read/write enable in the state that DMA transfer enable and Dack="H", Dreq is asserted. In both mode, Dreq detects Dack="L" and is negated.	W/R	0	-	-
14 to 9	Reserved		Write/Read "0"				
8	DMAEN	DMA transfer enable	If this bit is "1", endpoint buffer which is appointed by DMA_EP[3:0] is enable to write or when read is enable, Dreq is asserted. If "0" is written in DMA transferring, DMA transfer is forced to end.	W/R	0	-	-
7 to 4	Reserved		Write/Read "0"				
3 to 0	DMA_EP [3:0]	DMA transfer endpoint	Appoint the endpoint for DMA transfer. "0001"=EP1,"0010"=EP2,"0011"=EP3, "0100"=EP4,"0101"=EP5 EP0 can not be appointed. Don't change the setting during write (IN) or read (OUT). Change of the setting of the endpoint of direction IN must be done after confirmed that IVAL="0" and Dreq="0", or IVAL="1" and Dreq="1". Change of the setting of the endpoint of direction OUT must be done after confirmed that IVAL="0" and Dreq="1".	W/R	0000	-	-

(4-5) DMA_FIFO Control Register (Address : 4Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		IVAL	BCLR	Dreq	DMA_DTLN[10:0]										

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15, 14	Reserved		Write/Read "0"				
13	IVAL	IN buffer status	If the selected endpoint is set to IN, this becomes IN buffer effective state flag. When set to "1", it becomes transmit data set state. (SIE is available to read) When the data (byte) which exceeds to the maximum packet size (MXPS) is written, this bit is set to "1". In short packet transmit, set this bit to "1" after wrote the transmit data. If IVAL="1" and BCLR="1" is written at the same time, the IN buffer effective state flag is set to "1". (This is effective to transmit 0 length data) If the selected endpoint is set to OUT, it becomes to OUT buffer effective state status. Status "1" shows that there is data which is available to read. When Creq bit is "0", the value of this bit is effective. This bit is not changed when "1" is written. Flag is not changed when "0" is written.	W/R	0	-	-
12	BCLR	Buffer clear	If "1" is written into this bit when the selected endpoint is set to IN, IN buffer effective state flag and the data (byte) which is written are cleared. If the IVAL="1" and BCLR="1" is written at the same time, the data is cleared but the IN buffer effective state flag is set.(This is effective to transmit 0 length data) If "1" is written into this bit when the selected endpoint is set to OUT, OUT buffer effective state flag and the read data (byte) are cleared. If it is set to double buffer, the state of buffer which can be read or write for CPU bus is cleared. To set the EPi_ACLR, USB bus buffer is cleared. This bit is not changed when "0" is written.	W/R	0	-	-

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
11	Dreq	DMA_FIFO ready	If this bit is "0", then access is available to DMA_FIFO register. And if this bit is "0", then the bit of IVAL and DMA_DTLN is valid. This bit is used as DMA request signal (Dreq).	R	1	-	-
10 to 0	DMA_DTLN[10:0]	DMA_FIFO receive data length	When read this register, receive data length (byte) is appears. This bit is valid when Dreq bit is "0".	R	000h	-	-

(4-6) DMA_FIFO Data Register (Address : 4Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DMA_FIFO[15:0]															

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 0	DMA_FIFO[15:0]	DMA_FIFO data	If the selected endpoint is set to OUT, this becomes to receive data FIFO register. If the selected endpoint is set to IN, this becomes to transmit data FIFO register. If the selected endpoint is set to 8-bit mode, lower 8 bit [7:0] are valid. Read operation when the endpoint appointed direction IN, or write operation when the endpoint appointed direction OUT, is inhibited.	W/R	xxxx	-	-

(4-7) EPi Configuration Register 0 (i=1 to 5)

(Address : EP1=60h, EP2=64h, EP3=68h, EP4=6Ch, EP5=70h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EPi_TYP[1:0]		DIR	ITMD	EPi_Buf_siz[3:0]				DBLB	RWMD	EPi_Buf_Nmb[5:0]					

The EPi configuration register 0 must be set in a state of response PID is NAK("00").

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15 to 14	EPi_TYP [1:0]	Transfer type	To set the transfer type of endpoint. 00 : not Configured 01 : bulk transfer 10 : interrupt transfer 11 : isochronous transfer	W/R	00	-	-
13	EPi_DIR	Transfer direction	To set the transfer direction of endpoint 0 : OUT (receive data from host) 1 : IN (transmit data to host) When changed the state of transfer direction, clear (EPi_ACLR) the endpoint buffer.	W/R	0	-	-
12	EPi_ITMD	Interrupt toggle mode	To set the sequence toggle bit mode of interrupt transfer. 0 : Alternation data toggle bit mode (Only toggled when transfer completed with no problem) 1 : Continuous toggle bit mode (Whatever the hand shake exists or the types are, it toggles every time when data packet is transmitted) This is effective when endpoint is set to interrupt(IN) transfer.	W/R	0	-	-
11 to 8	EPi_Buf_ siz[3:0]	Buffer size	Set endpoint buffer size at a unit of 64Bytes. "0000"=64Bytes, "0001"=128Bytes, ..., "1110"=960Bytes, "1111"=1024Bytes	W/R	0000	-	-
7	EPi_DBLB	Double buffer mode	Set the constitution of endpoint buffer. 0 : Single buffer mode 1 : Double buffer mode In double buffer mode, double of the buffer size is taken as the endpoint buffer.	W/R	0	-	-
6	EPi_ RWMD	Continuous transfer mode (only for Bulk transfer)	If "1" is written into this bit, continuous transfer mode of endpoint is set. When the direction of endpoint is set to OUT, then it is set to continuous receive mode. And when the direction of endpoint is set to IN, then it is set to continuous transmit mode. Continuous receive mode can receive data packet up to the buffer size which is set, or can receive continuously before receives short packet. Continuous transmit mode can transmit data packet up to the buffer size which is set, and transmission of short packet can be done by set the IVAL flag. In data packet (max packet size) receive which is less than buffer size, interrupt to CPU does not occur. Continuous transfer mode is effective only in bulk transfer.	W/R	0	-	-
5 to 0	EPi_Buf_ Nmb[5:0]	Buffer start number	Appoint the first number of the buffer of a unit of 64Bytes. Buffer exists from #00h to #2Fh. Buffer size(double of the buffer size in double buffer mode), which is appointed from the first, is secured for endpoint buffer. Set that plural of endpoint do not occupy the same buffer area.	W/R	00h	-	-

(4-8) EPi Configuration Register 1 (i=1 to 5)

(Address : EP1=62h, EP2=66h, EP3=6Ah, EP4=6Eh, EP5=72h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EPi_PID[1:0]		DMAMD	NULMD	ACLR	Octl	EPi_MXPS[9:0]									

The EPi configuration register 1 must be set in a state of response PID is NAK("00").

Bit	Bit Name	Name	Function	W/R	Reset		
					H/W	S/W	USB
15, 14	EPi_ PID [1:0]	Response PID	Set response PID. 00 : NAK Whatever the buffer state is, do NAK handshake. 01 : BUF Response PID is selected according to the state of buffer and sequence toggle bit. (In bulk/interrupt transfer, one of ACK, NAK, DATA0, and DATA1) 1x : STALL Do STALL handshake. If the transfer direction of selected endpoint is OUT, when received data which exceeded maximum packet size (MXPS), it becomes "1x" (=STALL) automatically.	W/R	00	-	-
13	EPi_ DMAMD	DMA transfer mode	Set the access mode to endpoint buffer. 0 : CPU access mode 1 : DMA transfer mode	W/R	0	-	-
12	EPi_ NULMD	Null data addition transmit mode	To set this bit as "1", Null data addition transmit mode is set . In the endpoint which is set to continuous transmit mode, when write a multiple data of maximum packet size into buffer and transmit, Null data is transmitted automatically after transmitted the last packet. This setting is effective when continuous transmit mode is set.	W/R	0	-	-
11	EPi_ ACLR	OUT buffer automatic clear mode	When the selected endpoint is set to OUT and if this bit is set to "1", OUT buffer effective flag and read data (number of byte) is cleared. In this state(OUT buffer does not become effective state), SIE side writes data from host into OUT buffer but CPU side does not read. When set this bit to "1", whatever the transfer direction is, endpoint buffer (all buffer of single/double buffer) are cleared. When clear the endpoint buffer, set this bit to "1" and then set again to "0".	W/R	0	-	-
10	EPi_Octl	FIFO access 8 bit mode	When this bit is set to "1", FIFO data register becomes 8-bit mode and when accessed "FIFO Data Register" of endpoint, lower 8bit[7:0] becomes effective. When transmit odd number of byte, it is needed to write in 8-bit mode. When read in 8-bit mode, set to 8-bit mode before data receive.	W/R	0	-	-
9 to 0	EPi_ MXPS [9:0]	Max Packet size	Set the maximum data size (Byte) to transmit/receive in one packet transfer. Set the value of wMaxPacketSize in request.	W/R	040h	-	-

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	-0.3 to +4.2	V
V_I	Input voltage	-0.3 to V_{CC}+0.3	V
V_O	Output voltage	-0.3 to V_{CC}+0.3	V
I_O	Output current	±20	mA
P_d	Power dissipation	400	mW
T_{stg}	Storage temperature	-55 to +150	C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		3.0	3.3	3.6	V
GND	Supply voltage			0		V
V_I	Input voltage		0		V_{CC}	V
$V_{I(Vbus)}$	Input voltage (Only for Vbus Input)		0		5.25	V
V_O	Output voltage		0		V_{CC}	V
T_{opr}	Operating temperature		0	+25	+70	℃
t_r, t_f	Input rise, fall time	Normal input			500	ns
		Schmidt trigger input			5	ms

ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Condition		Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	"H" input voltage	Xin	V_{CC} = 3.6V		2.52		3.6	V
V_{IL}	"L" input voltage		V_{CC} = 3.0V		0		0.9	V
V_{T+}	Threshold voltage in positive direction	Note 1	V_{CC} = 3.3V		1.4		2.4	V
V_{T-}	Threshold voltage in negative direction				0.5		1.65	V
V_{OH}	"H" output voltage	Xout	V_{CC} = 3.0V	I_{OH} = -50uA	2.6			V
V_{OL}	"L" output voltage			I_{OL} = 50uA			0.4	V
V_{OH}	"H" output voltage	Note 2	V_{CC} = 3.0V	I_{OH} = -2mA	2.6			V
V_{OL}	"L" output voltage			I_{OL} = 2mA			0.4	V
V_{OH}	"H" output voltage	Note 3	V_{CC} = 3.0V	I_{OH} = -4mA	2.6			V
V_{OL}	"L" output voltage			I_{OL} = 4mA			0.4	V
I_{IH}	"H" input current		V_{CC} = 3.6V	V_I = V_{CC}			10	uA
I_{IL}	"L" input current			V_I = GND			-10	uA
I_{OZH}	"H" output current in off status	D15-0 ,TDO	V_{CC} = 3.6V	V_O = V_{CC}			10	uA
I_{OZL}	"L" output current in off status			V_O = GND			-10	uA
R_{dv}	Pull down resistance	Note 4				100		kΩ
R_{dt}	Pull down resistance	Note 5				50		kΩ
R_u	Pull up resistance	Note 6				50		kΩ
$I_{CC(A)}$	Average supply current in operation mode		f(Xin)=48MHz,V_{CC} = 3.6V USB transmit state			40	55	mA
$I_{CC(S)}$	Supply current in static mode		Oscillator disable,PLL disable, USB transceiver enable, TrON=H/L output VI=Vcc or GND fixed,Vcc = 3.6V			2	4	mA
			Oscillator disable,PLL disable, USB transceiver disable, TrON=H/L output VI=Vcc or GND fixed,Vcc = 3.6V Suspend state			30	200	uA
			Oscillator disable,PLL disable, USB transceiver disable, TrON=H/L output VI=Vcc or GND fixed,Vcc = 3.6V H/W reset state			10	100	uA

Notes 1: All input and bidirection pins except for Xin (except for USB buffer)

2: $\overline{INT}$,$\overline{Dreq}$,TDO output pins

3: D15-0 input /output pins

4: Vbus input pins

5: TEST1,TEST2,TCK input pins

6: $\overline{TRST}$,TMS,TDI input pins

ELECTRICAL CHARACTERISTICS (USB)

(1) DC CHARACTERISTICS

Symbol	Parameter	Test condition		Limits			Unit
				Min.	Typ.	Max.	
V_{DI}	Differential Input Sensitivity	| (D+)-(D-) |		0.2			V
V_{CM}	Differential Common Mode Range			0.8		2.5	V
V_{SE}	Single Ended Receiver Threshold			0.8		2.0	V
V_{OL}	"L" Output voltage	V_{CC} = 3.0V	RL of 1.5KΩ to 3.6V			0.3	V
V_{OH}	"H" Output voltage		RL of 15KΩ to GND	2.8		3.6	V
I_{OZL}	"L" output current in off status	V_{CC} = 3.6V	V_O =0V	-10		10	mA
I_{OZH}	"H" output current in off status		V_O =3.6V	-10		10	mA
$R_{o(Pch)}$	Output resistance	V_{CC} = 3.3V	V_O =0V	4	7	15	Ω
$R_{o(Nch)}$	Output resistance		V_O =3.3V	4	7	15	Ω

(2) AC CHARACTERISTICS

Symbol	Parameter	Test condition		Limits			Unit
				Min.	Typ.	Max.	
t_r	Rise transition time	10% to 90% of the data signal	$C_{L=50pF}$	4		20	ns
t_f	Fall transition time	10% to 90% of the data signal	$C_{L=50pF}$	4		20	ns
TRFM	Rise/fall time matching	t_r/t_f		90		110	%
V_{CRS}	Output signal crossover voltage	$C_{L=50pF}$		1.3		2.0	V

SWITCHING CHARACTERISTICS

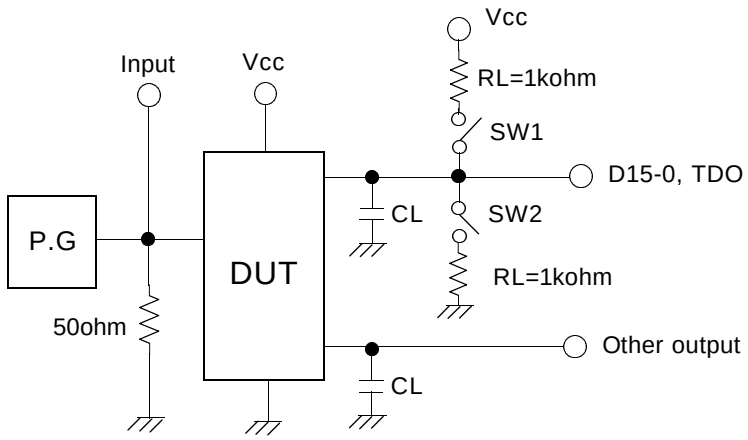
Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
ta(A)	Address access time	CL=50pF			30	ns
ta(CTRL)	Control access time				30	ns
tv(CTRL)	Data valid time after control		0			ns
ten(CTRL)	Data output enable time after control		0		20	ns
tdis(CTRL)	Data output disable time after control		0		20	ns
td(Dack-	Dreq disable propagation time				60	ns
td(WR-INT)	INT disable propagation time				60	ns
twh(INT)	INT "H" pulse width		320			ns
twh(Dreq)	Dreq "H" pulse width		60			ns
td(CTRL-Dreq)	Dreq output enable time after control		60			ns
td(Dackh-Dreq)	Dreq output enable time after Dack		20			ns
td(TCK-TDOV)	TDO output enable time after TCK				30	ns
td(TCK-TDOX)	TDO output disable time after TCK				30	ns

TIMING REQUIREMENTS

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
tsu(A)	Address setup time		30			ns
th(A)	Address hold time		0			ns
tw(CTRL)	Control pulse width		30			ns
trec(CTRL)	Control recovery time		30			ns
tsu(D)	Data setup time		20			ns
th(D)	Data hold time		0			ns
tw(cycle)	FIFO access cycle time		200			ns
tw(RST)	RESET pulse width		100			ns
tst(RST)	Control start time after RESET		100			ns
tc(TCK)	TCK cycle time		100			ns
tw(TCKH)	TCK "H" pulse width		40			ns
tw(TCKL)	TCK "L" pulse width		40			ns
tsu(TDI-TCK)	TDI,TMS setup time		20			ns
th(TDI-TCK)	TDI,TMS setup time		20			ns
tw(TRST)	TRST "L" pulse width		100			ns
td(CTRL-Dack)	TRST "L" pulse width				83	ns

Measurement circuit

1. Terminals except for USB buffer block

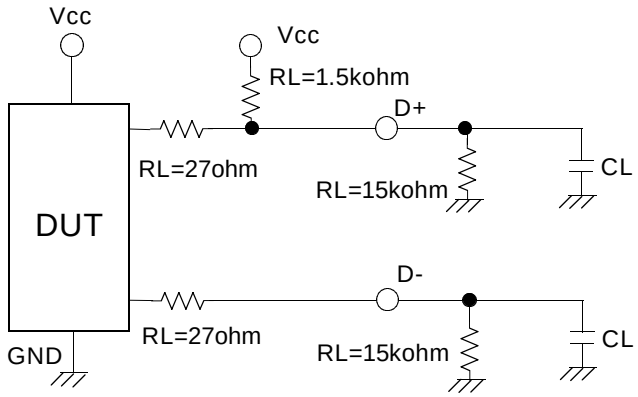


Item	SW1	SW2
tdis(CTRL(LZ))	close	open
tdis(CTRL(HZ))	open	close
ta(CTRL(ZL))	close	open
ta(CTRL(ZH))	open	close

(1) Input pulse level : 0 to 3.3V
Input pulse rise/fall time : tr=tf=3ns
Input timing voltage : 1.65V
Output timing voltage : Vcc/2
(tdis(LZ) is measured at 10% of output,
tdis(HZ) is measured at 90% of output)

(2) Capacitance CL includes stray capacitance and probe capacitance.

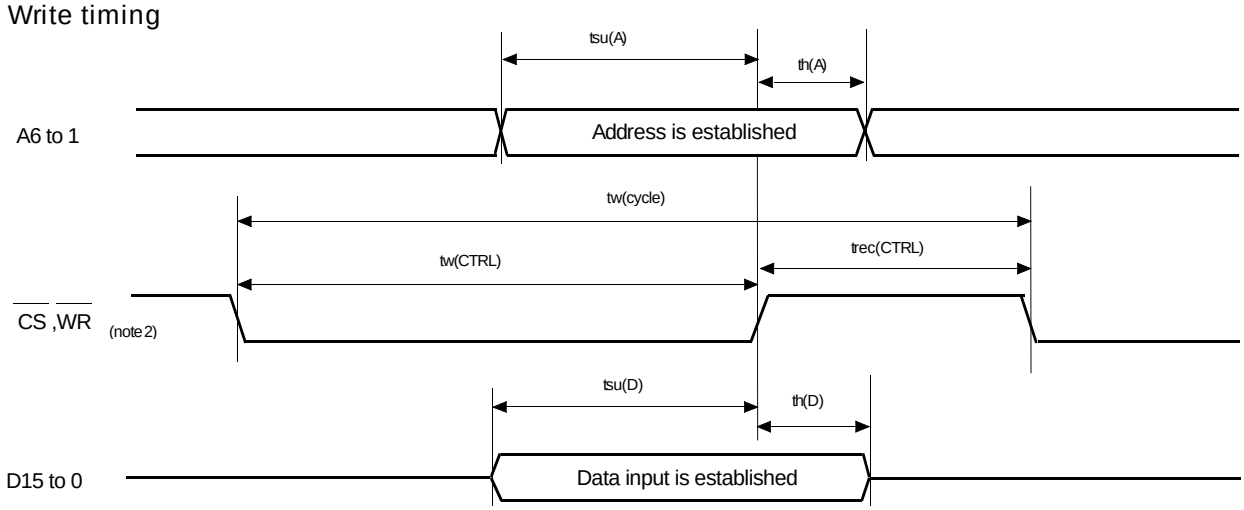
2. USB buffer block



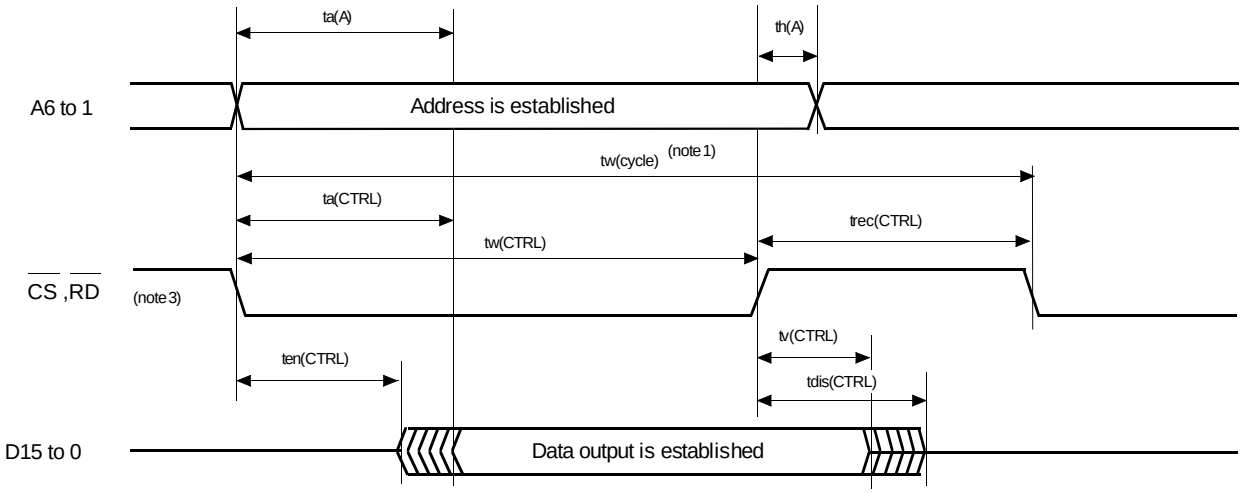
(1) tr, tf is measured from 10% to 90% of output.
(2) Capacitance CL includes stray capacitance and probe capacitance.

TIMING DIAGRAM

(1) Write timing



(2) Read timing



note 1 : tw(cycle) is needed when access FIFO.

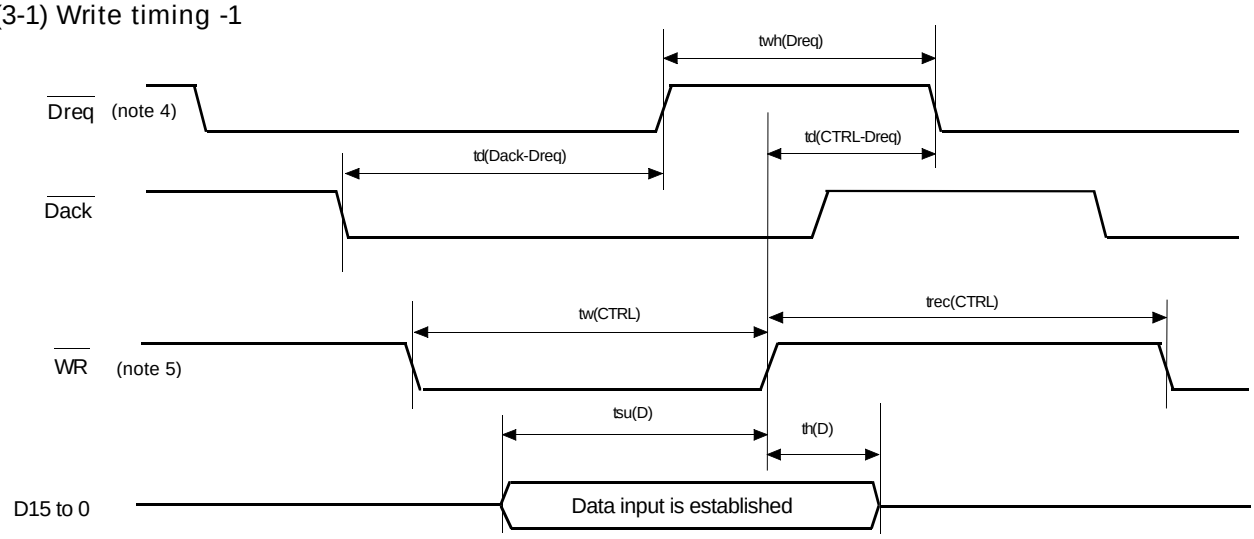
note 2 : Write is done in the overlap period when $\overline{CS}$ and $\overline{WR}$ is active "L".
Spec from the positive edge is valid from the fastest inactive signal.
Spec of pulse width is valid of the overlap period of active "L".

note 3 : Read is done in the overlap period of $\overline{CS}$ and $\overline{RD}$ is active "L"
Spec from the negative edge is valid from the latest signal.
Spec from the positive edge is valid form the fastest inactive signal.
Spec of pulse width is valid during active "L" overlap period.

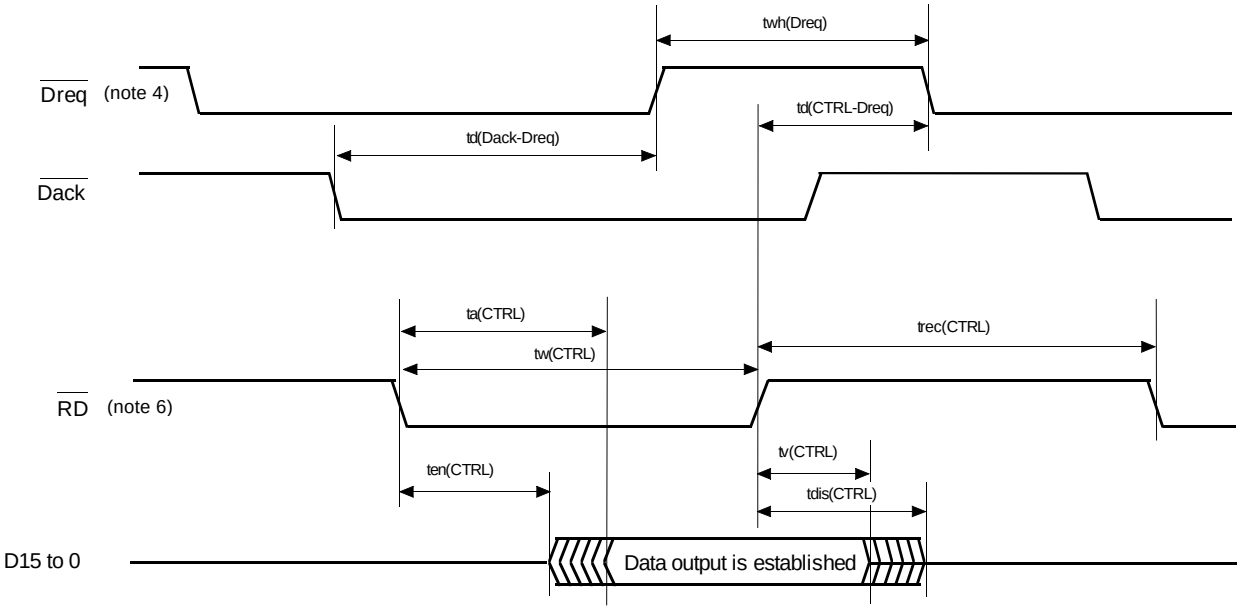
(3) DMA Transfer Timing -1

In case of Full speed transfer mode (DMA operation mode register : MODE=0)

(3-1) Write timing -1



(3-2) Read timing -1

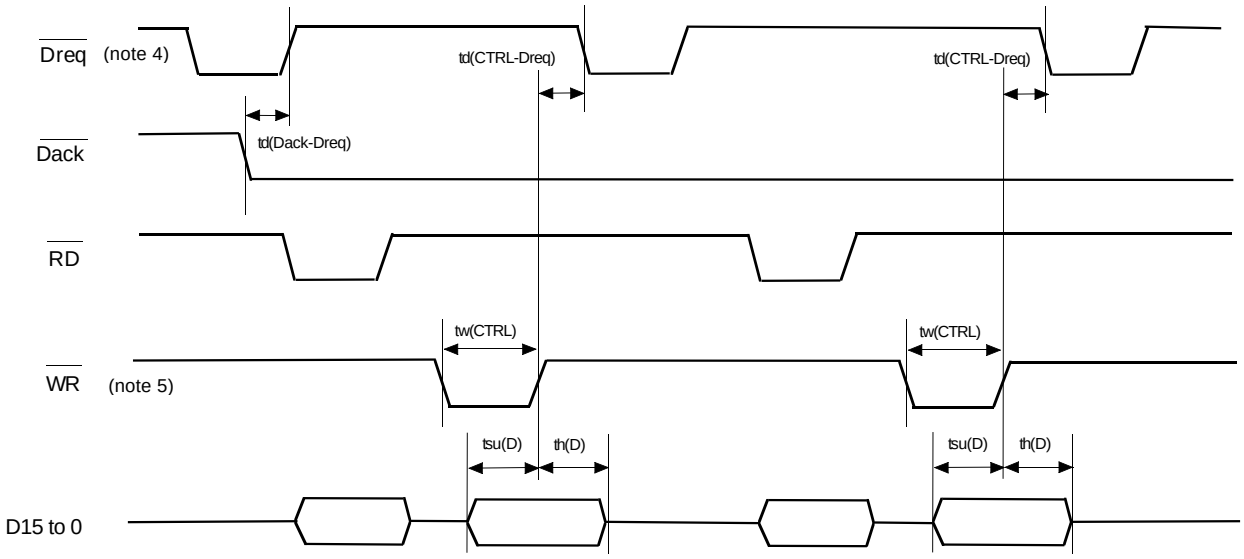


note 4 : Inactive condition of $\overline{Dreq}$ is $\overline{Dack}$="L"
And when next DMA transfer exists, spec when $\overline{Dreq}$ turns to active is valid the latest one of twh(Dreq) or td(CTRL-Dreq).

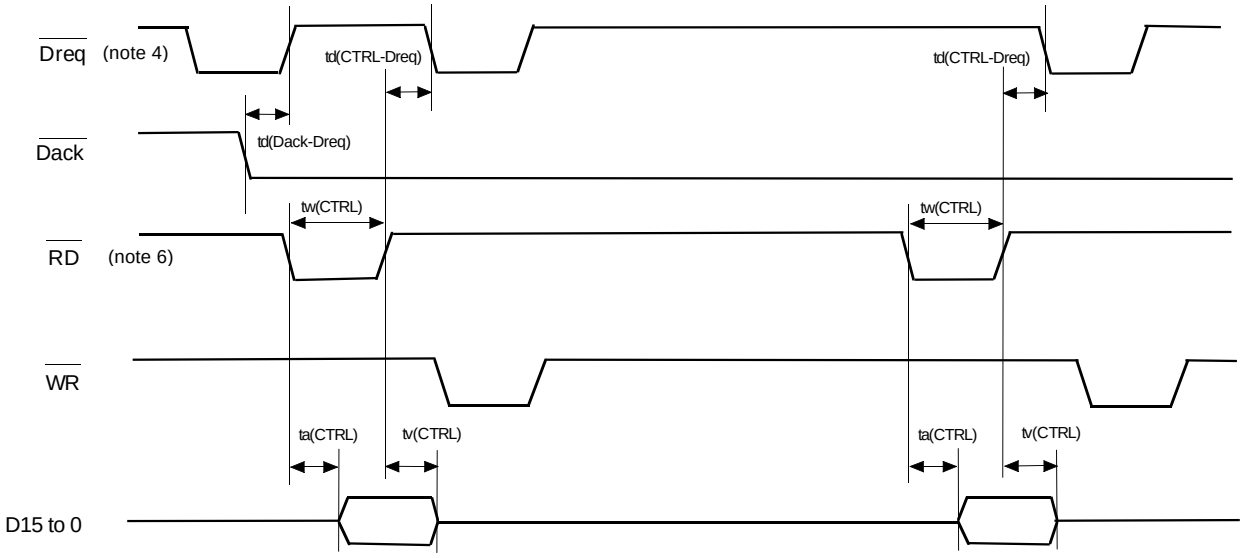
note 5 : Write is done in the overlap period when $\overline{Dack}$ and $\overline{WR}$ is active "L".
Spec from the positive edge is valid from the fastest inactive signal.
Spec of pulse width is valid of the overlap period of active "L".

note 6 : Read is done in the overlap period of $\overline{Dack}$ and $\overline{RD}$ is active "L"
Spec from the negative edge is valid from the latest signal.
Spec from the positive edge is valid form the fastest inactive signal.
Spec of pulse width is valid during active "L" overlap period.

(3-3) Write timing -2



(3-4) Read timing -2



note 4 : Inactive condition of $\overline{\text{Dreq}}$ is $\overline{\text{Dack}}$="L"
And when next DMA transfer exists, spec when $\overline{\text{Dreq}}$ turns to active is valid the latest one of twh(Dreq) or td(CTRL-Dreq).

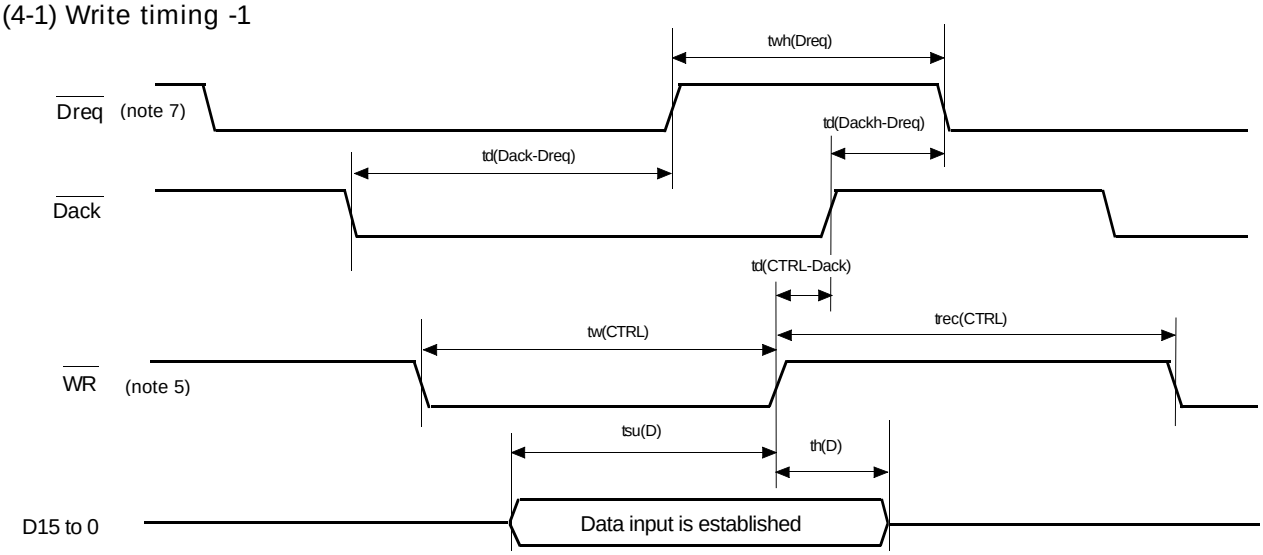
note 5 : Write is done in the overlap period when $\overline{\text{Dack}}$ and $\overline{\text{WR}}$ is active "L".
Spec from the positive edge is valid from the fastest inactive signal.
Spec of pulse width is valid of the overlap period of active "L".

note 6 : Read is done in the overlap period of $\overline{\text{Dack}}$ and $\overline{\text{RD}}$ is active "L"
Spec from the negative edge is valid from the latest signal.
Spec from the positive edge is valid form the fastest inactive signal.
Spec of pulse width is valid during active "L" overlap period.

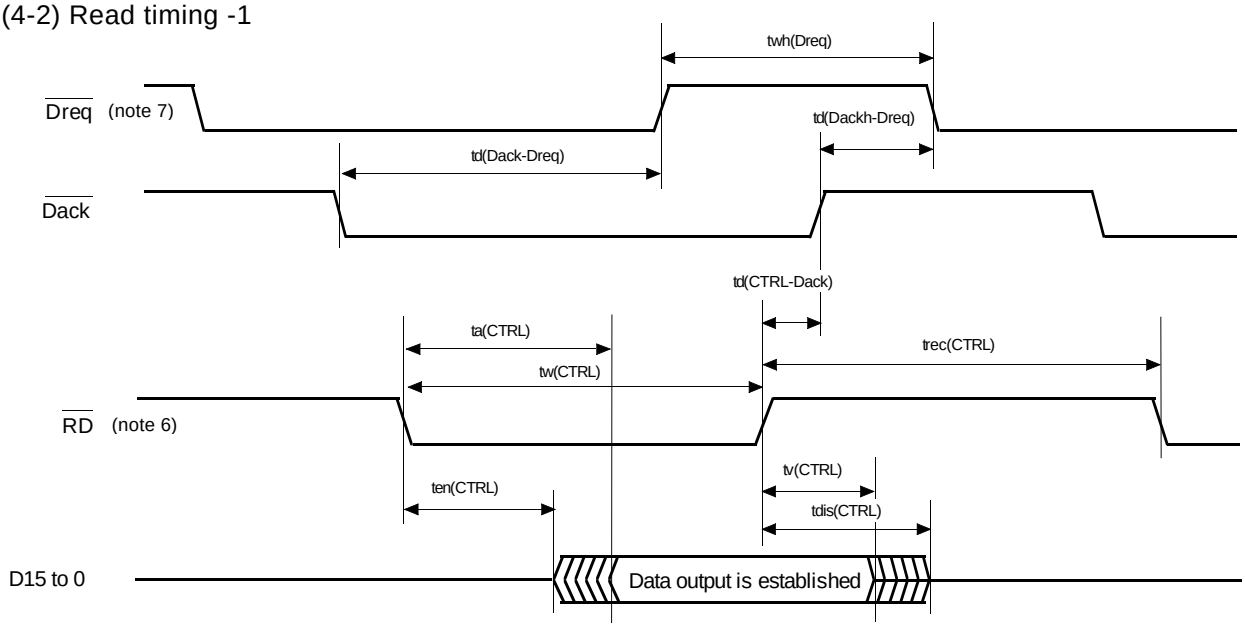
(4) DMA Transfer Timing -2

In case of one word transfer mode (DMA operation mode register : MODE=1)

(4-1) Write timing -1



(4-2) Read timing -1

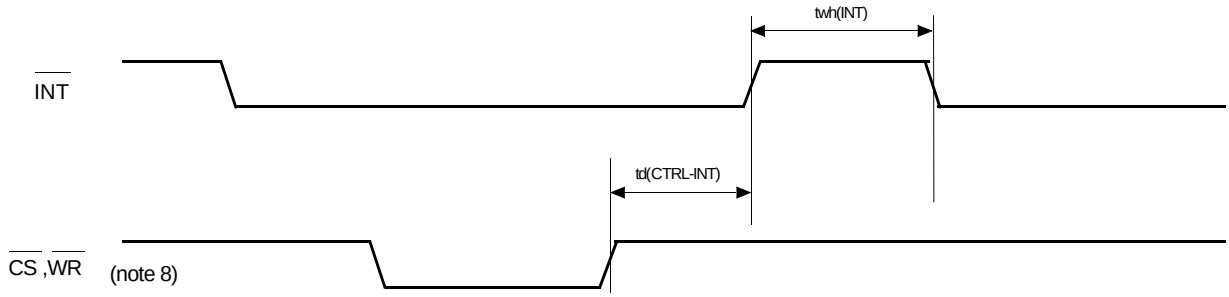


note 7 : Inactive condition of $\overline{Dreq}$ is $\overline{Dack}$="L"
And when next DMA transfer exists, spec when $\overline{Dreq}$ turns to active is valid the latest one of twh(Dreq) or td(Dackh-Dreq).

note 5 : Write is done in the overlap period when $\overline{Dack}$ and $\overline{WR}$ is active "L".
Spec from the positive edge is valid from the fastest inactive signal.
Spec of pulse width is valid of the overlap period of active "L".

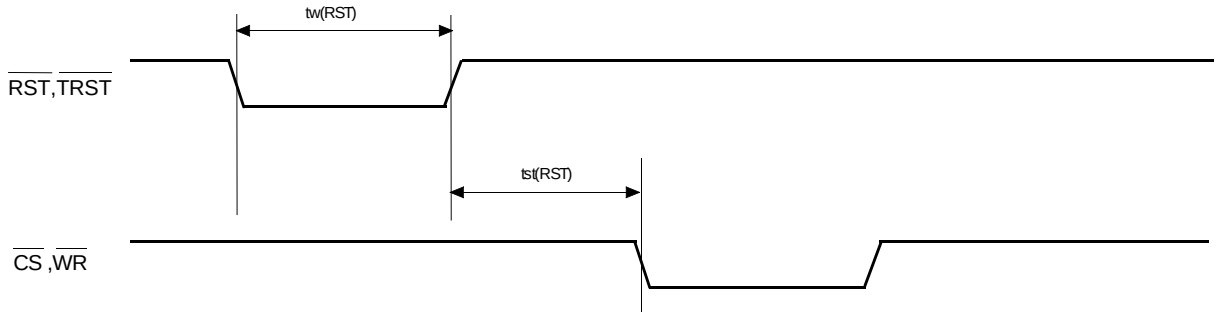
note 6 : Read is done in the overlap period of $\overline{Dack}$ and $\overline{RD}$ is active "L"
Spec from the negative edge is valid from the latest signal.
Spec from the positive edge is valid form the fastest inactive signal.
Spec of pulse width is valid during active "L" overlap period.

(5) Interrupt timing

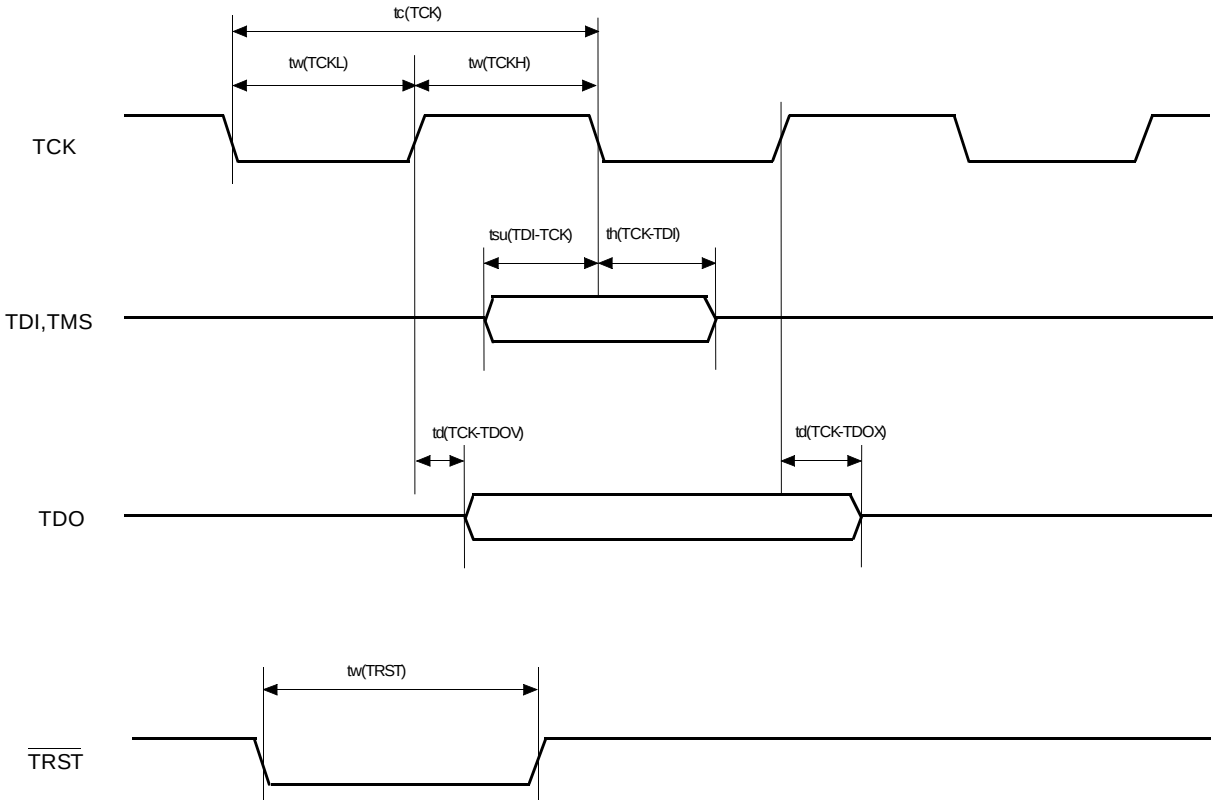


note 8 : Write is done in the overlap period when $\overline{CS}$ and $\overline{WR}$ is active "L".
Spec from the positive edge is valid from the fastest inactive signal.

(6) Reset timing



(7) JTAG timing



Abstraction of JTAG

M66290A has JTAG (Joint Test Action Group) interface which meets IEEE 1149.1 test access port spec.
This JTAG interface can be used for input/output path (boundary scan path) for boundary scan test.
Further information as to JTAG test access port, refer to "IEEE Std. 1149.1a-1993".

Pin descriptions

Pin description which relates to JTAG interface of M66290A are as follows.

Test clock input (TCK)

Clock input into test circuit.

Test data input (TDI)

Synchronous serial input to input test command code and test data. Data is sampled by the positive edge of TCK.

Test data output (TDO)

Synchronous serial output to output test command code and test data. Output data changes by the negative edge of TCK and is output only in the state of Shift-IR or Shift-DR. In other state,keeps "Z".

Test mode input (TMS)

Test mode select input to control status shift of test circuit. This is sampled by the positive edge of TCK.

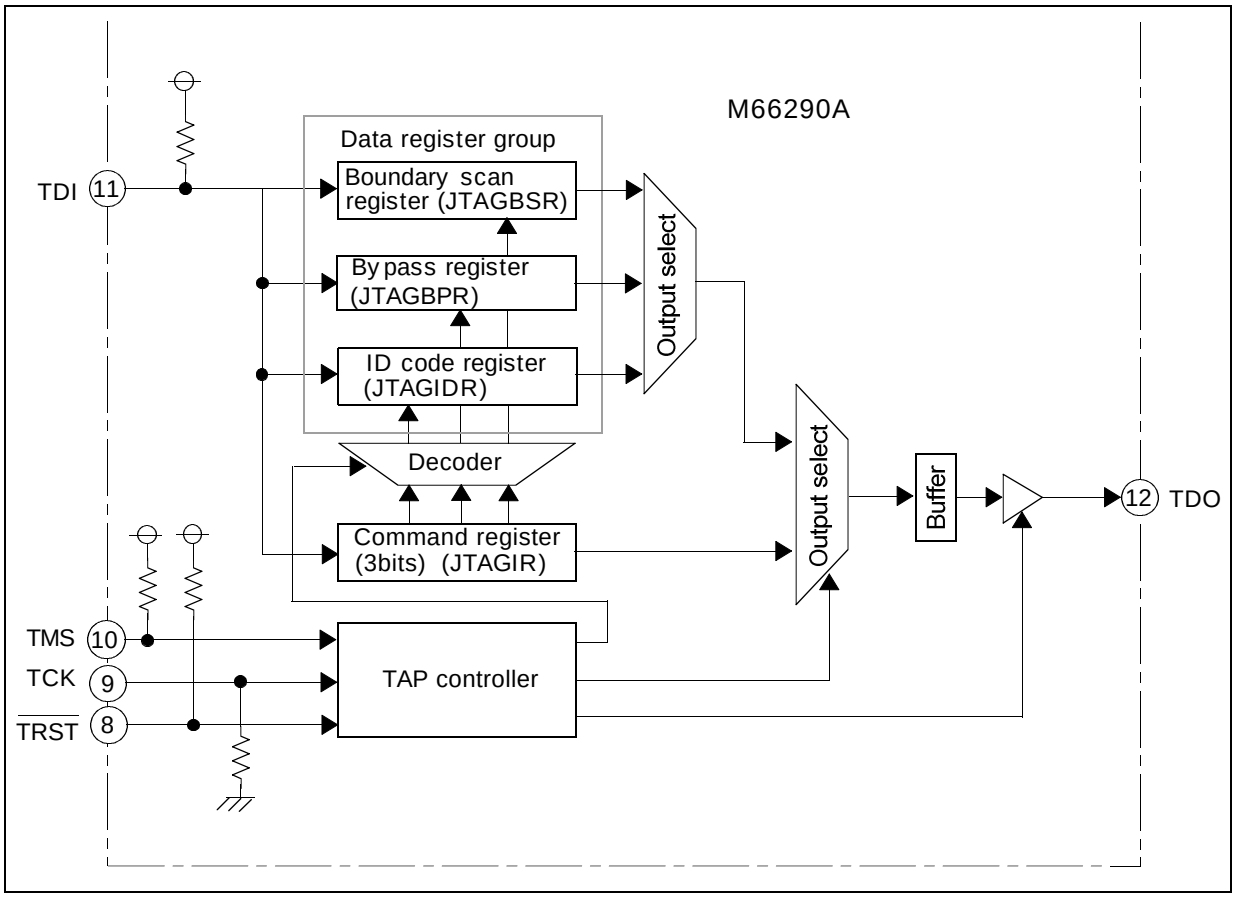
Test reset input ($\overline{\text{TRST}}$)

"L" active test reset input to initialize the test circuit asynchronously. To assure this reset function, keep TMS input as "H" when this signal changes from "L" to "H".

JTAG circuit constitution

JTAG circuit of M66290A is constituted by the blocks as follows.

(1) Command register which keeps command code which is fetched through the boundary scan path.
(2) Data register group which is accessed through the boundary scan pass.
(3) Test access port (TAP) controller to control the status shift of JTAG block.
(4) Control logic for input select, output select, and so.



Abstract of JTAG operations

There are four basic access to command register and to data register. And the access is executed based on the status shift of TAP controller.
TAP controller is shifted of its status by the TMS input and make a control signal which is needed to each state.

Capture operation

Result of the boundary scan test or the fixed data which is defined to each register, is sampled. For operation, load the input data into shift register stage.

Shift operation

Through the boundary scan path, access from external is done. M66290A set the data from external and at the same time, output the data which is sampled by capture operation.
For register operation, right shift is executed among shift register stage of each bit.

Update operation

In shift operation, drive the data which is set by external. For register operation, transfer the value which is set to shift register stage, to parallel output stage.

JTAG interface shifts the internal state according to TMS input, and do two kinds of operations as follows. Both are basically
executed in turn of "Capture -> Shift -> Update".

IR path sequence

Set the command code into command register and when path sequence comes, select the data register which is the object of the operation.

DR path sequence

To selected data register, refer or set the data.

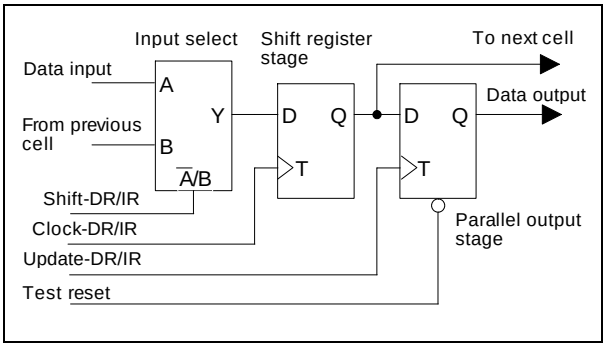


Figure. Basic construction of JTAG related register

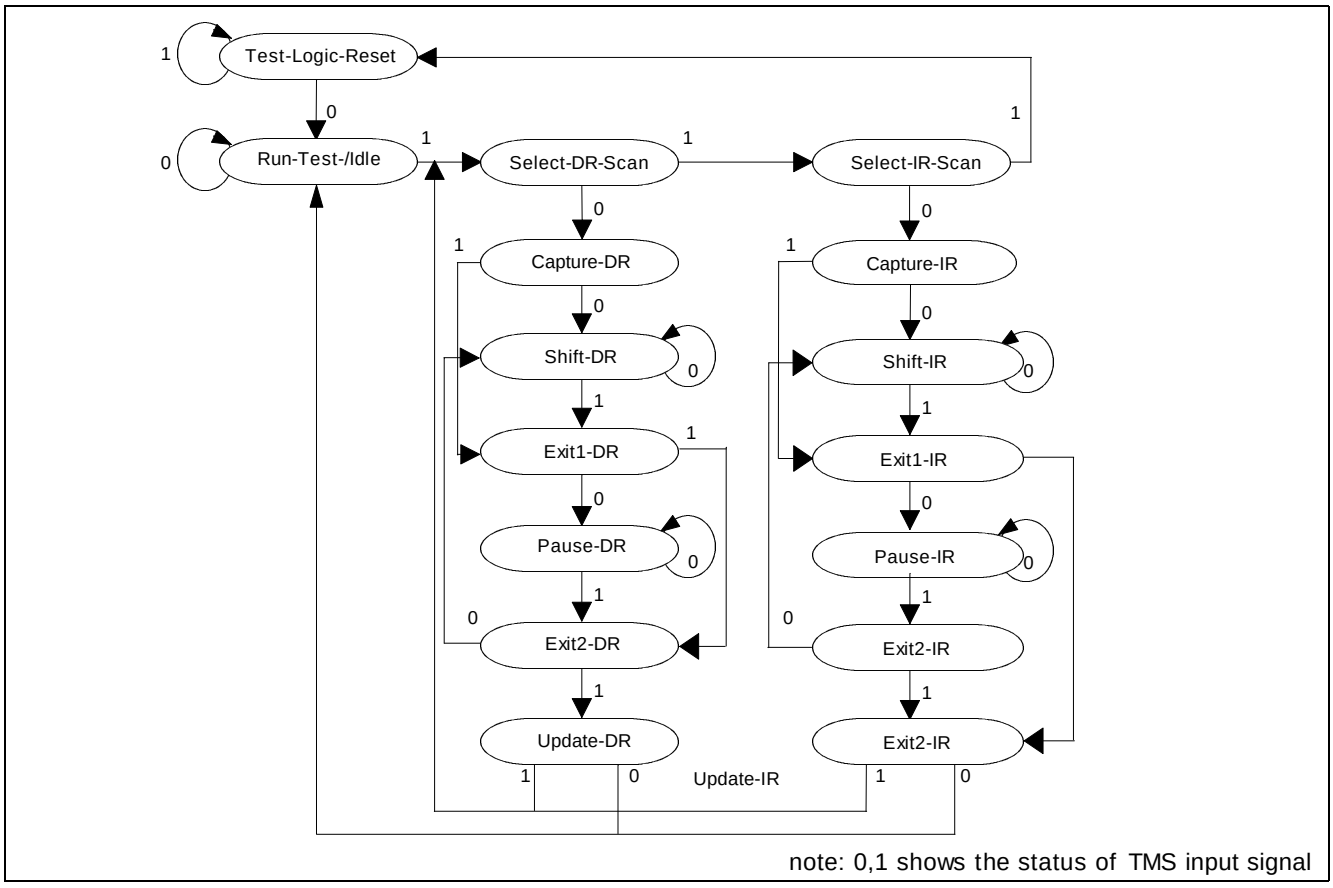


Figure. Status shift of TAP controller

JTAG registers

Command registers

Command register is constituted by 3 bits register which keeps command code, and is set in the IR path sequence. Data register, which is selected in the following path sequence, is determined by the command which is set into the command register. Initial value in test reset is IDCODE command. Until the command code is set from external, IDCODE register is kept selecting as the data register.

M66290A supports three commands (EXTEST, SAMPLE/PRELOAD, and BYPASS) which are established as essential by IEEE 1149.1 and the device recognize register access command (IDCODE).
Below are the commands and the related code.

EXTEST (Command code : b'000)

Executes outside circuit connection test and on board connection test. Reads the TDI input into the "Boundary Scan Register" and outputs the contents of "Boundary Scan Register" from TDO.

IDCODE (Command code : b'001)

Selects the "IDCODE Register" and outputs the device and company discrimination data from TDO.

SAMPLE/PRELOAD (Command code : b'010)

Samples the circuit status in operation and outputs it from TDO, and at the same time, inputs the data from TDI which will be use in the next boundary scan test and set into the "Boundary Scan Register" previously.

BYPASS (Command code : b'111)

Selects the "BYPASS Register" and executes the refer and the set of the data.

Don't set the command code except for above.

Data registers

(1) Boundary scan register (JTAGBSR)

This is for boundary scan test and is assigned to each terminal of M66290A which is related to JTAG.
Boundary scan register is connected between TDI and TDO terminal, and is selected when "EXTEST Command" is ordered. This register captures the status of input terminal or the output value from internal logic circuit in the state of Capture-DR. In the state of Shift-DR, input the data for boundary scan test parallely outputting the sampled value. And set terminal function (IN/OUT of bidirectional terminal or direction of 3-state output) and output value.
As to the JTAG related terminal and the structure of boundary scan, refer to BSDL specially.

(2) BYPASS register (JTAGBPR)

BYPASS register is one bit register to bypass the boundary scan path when M66290A is not the object in boundary scan test. BYPASS register is connected between TDI and TDO terminal, and is selected when "BTPASS command" is ordered. In the state of Capture-DR, "0" is loaded.

(4) IDCODE register (JTAGIDR)

IDCODE register is a register of 32bits to discriminate the device and the company, and keeps information as follows.
IDCODE register is connected between TDI and TDO terminal,
and is selected when "IDCODE Command" is ordered.
IDCODE data is loaded in Capture-DR state and is output from TDO in Shift-DR state.

1. Version information (4bits) : b'0000
2. Part number (16bits) : b'0001 1000 1001 0010 (Binary code of "6290")
3. Company ID (11bits) : b'000 0001 1100 (JEDEC code of MITSUBISHI)
4. LSB (1bit) : b'1 (Fixed)