

Preliminary

Note : This is not a final specification.

Some of information in this document are subject to changes.

Mitsubishi Semiconductor<Digital IC>
M65580MAP-XXXFP
 Digital Video/Chroma/Deflection+MCU

Description

The M65580MAP-XXXFP are semiconductor integrated circuits designed with CMOS silicon gate technology for NTSC television system, include 8bit MCU(M37272MA core) with a closed caption decoder and circuits needed for TV baseband signals(Video and Chroma) processor and Deflection in a chip. PCB area and EMI noise can be reduced by one chip and 80QFP, and internal connection of OSD signals. And it can realize a adjustment free system by built-in MCU and get a high performance adaptive YC separation by 1 line memory. The above technology makes its performance more stable and better.

Feature

- Y/C processor : 8bit Input, 10bit Output digital processing
- Deflection processor : optimized system by conventional analog and digital mixed solution
- ADC&DAC : 8bit high speed video ADC & 10bit high speed video DAC

[MCU Block]

MCU(single microcomputer) in this IC has almost same function and performance as M37272MA-XXXSP/FP in mass-production. And it is operated by simple instruction in the same memory space as that of built-in ROM, RAM, I/O.

It has a OSD, data slicer, and I²C-BUS interface. So it is very useful for a channel selection system for NTSC TV with a closed caption decoder.

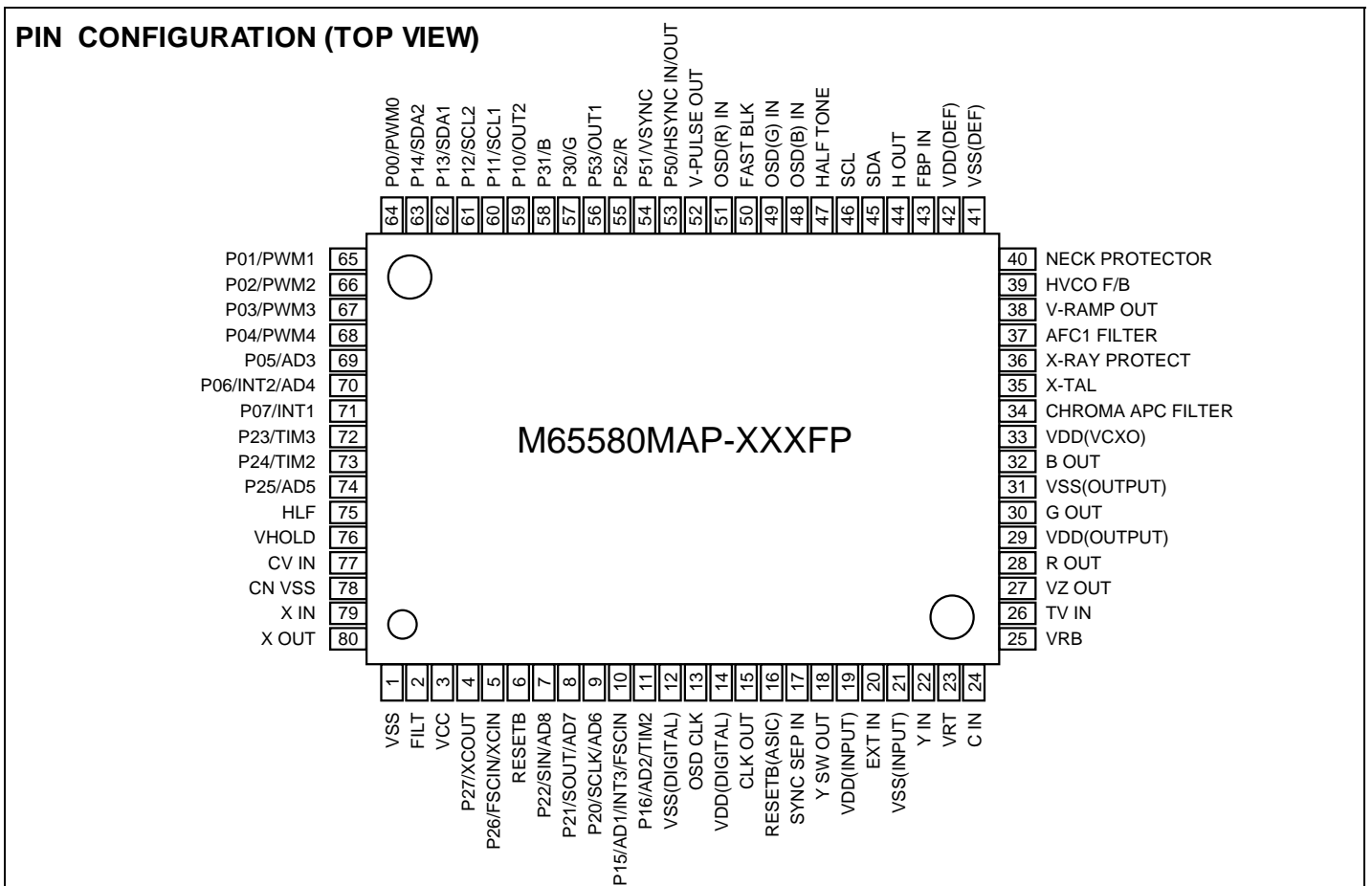
[ASIC Block]

ASIC block consists of the following blocks.

- (1) Analog frontend block ; Analog SW(2 CVBS(TV&EXT) inputs, Y/C signals to one signal, 2 channels 8 bit high speed video ADCs, and ACC amplifiers
- (2) Video and Chroma block ; A high performance 2 line adaptive YC separation by 1 line memory, Video blocks including sharpness, YNR, a high performance blackstretch circuits, Chroma decoder, and RGB matrix including OSD mixing circuit.
- (3) Deflection block ; A high performance sync separation by analog and digital mixed solution
- (4) Analog backend block ; 3 channels 10 bit high speed video DACs for Cutoff & Drive, and Mute circuit.

Application

NTSC TV with a closed caption decoder



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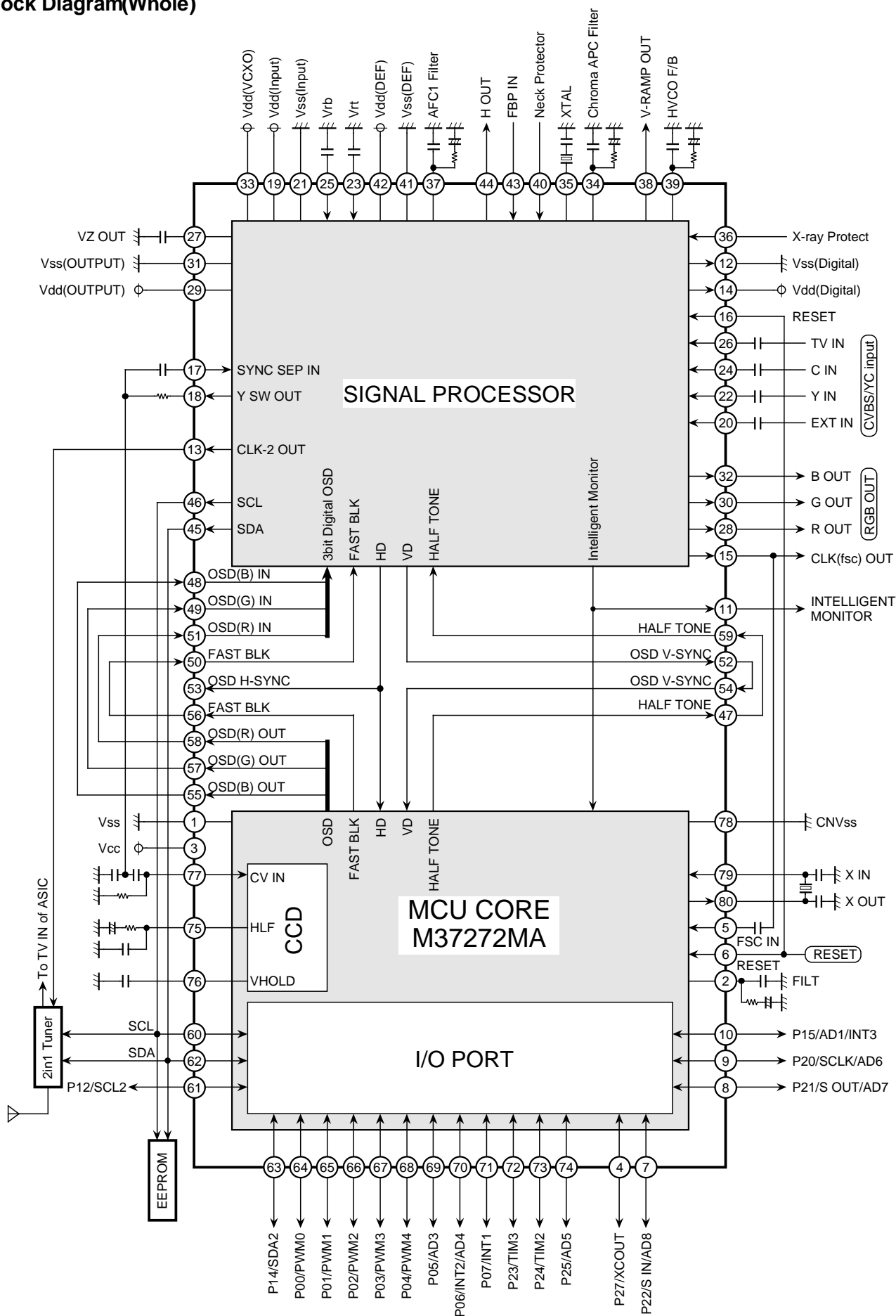
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Mitsubishi Semiconductor<Digital IC>

M65580MAP-XXXFP

Digital Video/Chroma/Deflection+MCU

Block Diagram(Whole)



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Absolute maximum ratings

| Symbol | Parameter | Conditions | Ratings | Unit |
|----------------------------|---|--|------------------------------|--------|
| V _{DD} (MCU) | Supply voltage (MCU) | All voltage are based on V _{SS} . Output transistors are cut off. | -0.3 to 6.0 | V |
| V _{DD} (ASIC5V) | Supply voltage (ASIC5V) | | -0.3 to 6.0 | V |
| V _{DD} (ASIC3.3V) | Supply voltage (ASIC3.3V) | | -0.3 to 4.0 | V |
| V _I (MCU) | Input Voltage (MCU) | | -0.3 to V _{CC} +0.3 | V |
| V _O (MCU) | Output Voltage (MCU) | | -0.3 to V _{CC} +0.3 | V |
| I _{OH} (MCU) | Circuit current (MCU) | | 0 to 1 (See note 1) | mA |
| I _{OL1} (MCU) | Circuit current (P00-P07, P10, P15, P16, P20-P27, P30, P31, P52, P53) | | 0 to 2 (See note 2) | mA |
| I _{OL2} (MCU) | Circuit current (P11-P14) | | 0 to 6 (See note 2) | mA |
| V _{ID} (ASIC) | Digital input voltage | | -0.3 to V _{CC} +0.3 | V |
| I _{OUT} (ASIC) | Analog output current | | -30 | mA |
| P _d | Power dissipation | | 1460 | mW |
| K _t | Thermal derating | | 14.6 | mW/ °C |
| T _{opr} | Operating temperature | | -20 to 65 | °C |
| T _{stg} | Storage temperature | | -40 to 125 | °C |

Recommended operating condition

(T_a=-20 to 65 °C, unless otherwise noted)

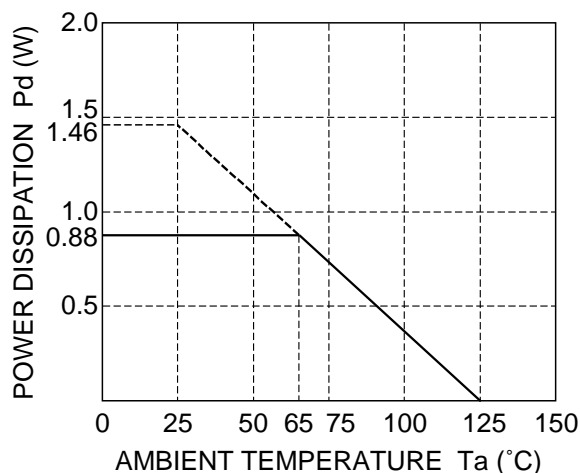
| Symbol | Parameter | Limits | | | Unit |
|---------------------------|---|--------------------|------|--------------------|------|
| | | Min. | Typ. | Max. | |
| V _{DD} (MCU) | Supply voltage (MCU) (See note 3) | 4.75 | 5.0 | 5.25 | V |
| V _{DD} (Digital) | Supply voltage (Digital) | 4.75 | 5.0 | 5.25 | V |
| V _{DD} (Input) | Supply voltage (Input) | 3.13 | 3.3 | 3.47 | V |
| V _{DD} (Output) | Supply voltage (Output) | 3.13 | 3.3 | 3.47 | V |
| V _{DD} (VCXO) | Supply voltage (VCXO) | 4.75 | 5.0 | 5.25 | V |
| V _{DD} (DEF) | Supply voltage (DEF) | 4.75 | 5.0 | 5.25 | V |
| | | | | | |
| V _{IH1} (MCU) | High Input voltage P00-P07, P10-P16, P20-P27, P50, P51, RESETB, X _{IN} | 0.8V _{CC} | | V _{CC} | V |
| V _{IH2} (MCU) | High Input voltage SCL1, SCL2, SDA1, SDA2 (When using I ² C-Bus) | 0.7V _{CC} | | V _{CC} | V |
| V _{IH3} (ASIC) | High Input voltage RESETB, FBP IN, HALF TONE, OSD(R/G/B) IN, FAST BLK | 0.8V _{CC} | | V _{CC} | V |
| V _{IL1} (MCU) | Low Input voltage P00-P07, P10-P16, P20-P27 | 0 | | 0.4V _{CC} | V |
| V _{IL2} (MCU) | Low Input voltage SCL1, SCL2, SDA1, SDA2 (When using I ² C-Bus) | 0 | | 0.3V _{CC} | V |
| V _{IL3} (MCU) | Low Input voltage (See note 4) P50, P51, RESETB, X _{IN} , TIM2, TIM3, INT1, INT2, INT3, S _{IN} , SCLK | 0 | | 0.2V _{CC} | V |
| V _{IL4} (ASIC) | Low Input voltage RESETB, FBP IN, HALF TONE, OSD(R/G/B) IN, FAST BLK | 0 | | 0.2V _{CC} | V |
| I _{OH} (MCU) | High average output current (See note 1) P10-P16, P20-P27, P30, P31, P52, P53 | | | 1 | mA |

| Symbol | Parameter | Limits | | | Unit |
|---------------|--|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| IOL1 (MCU) | Low average output current (See note 2) P00-P07, P10, P15, P16, P20-P27, P30, P31, P52, P53 | | | 2 | mA |
| IOL2 (MCU) | Low average output current (See note 2) P11-P14 | | | 6 | mA |
| f(XIN) (MCU) | Oscillation frequency (for CPU operation) XIN (See note 5) | 7.9 | 8.0 | 8.1 | MHz |
| f(XCIN) (MCU) | Oscillation frequency (for sub-clock operation) XCIN | 29 | 32 | 35 | kHz |
| FSCIN (MCU) | Oscillation frequency (for OSD standard clock) FSCIN | — | 3.58 | — | MHz |
| fhs1 (MCU) | Input frequency TIM2, TIM3, INT1, INT2, INT3 | | | 100 | kHz |
| fhs2 (MCU) | Input frequency SCLK | | | 1 | MHz |
| fhs3 (MCU) | Input frequency SCL1, SCL2 | | | 400 | kHz |
| VI (MCU) | Input amplitude video signal CVIN | 1.5 | 2.0 | 2.5 | V |

- Note**
- 1: The total current that flows out the MCU must be 20mA or less.
 - 2: The total input current to MCU (IOL1+IOL2) must be 30mA or less.
 - 3: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8MHz.
 - 4: Pin name in each parameter is described pin names.
 - (1) Dedicated pins: dedicated pin name.
 - (2) Double-/Triple-function ports.
 When the same limits: I/O port name.
 When the limits of function except ports are different from I/O port limits; function pin name.
 - 5: P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer pins.
 P11-P14 have the hysteresis when these pins are used as multi-master I²C-Bus interface ports.
 P20-P22 have the hysteresis when these pins are used as serial I/O pins.

Thermal derating

THERMAL DERATING (MAXIMUM RATING)



[MCU Block(M37272MA)]

Description

MCU(single microcomputers) in this IC has almost same function and performance as M37272MA-XXXSP/FP in mass-production. And it is operated by simple instruction in the same memory space as that of built-in ROM, RAM, I/O. It has a OSD, data slicer, and I²C-BUS interface, so it is very useful for a channel selection system for NTSC TV with a closed caption decoder.

Features

- Number of basic instructions ----- 71
- Memory size
 - ROM ----- 40Kbytes
 - RAM ----- 1152bytes
(ROM correction memory:64bytes included)
- minimum instruction execution time ----- 0.5μs
(at 8 MHz oscillation frequency)
- Power source voltage ----- 5V±10%
- Subroutine nesting ----- 128 levels(max.)
- Interrupts ----- 17bytes 16vector
- 8-bit timers ----- 6
- Programmable I/O ports(Ports P0,P1,P2) ----- 23
- Input ports(Ports P50,P51) ----- 2
- Output ports(Ports P30,P31,P52,P53) ----- 4
- Serial I/O ----- 8-bit x 1channel
- Multi-master I²C-BUS interface ----- 1(2 systems)
- A-D comparator (7-bit resolution) ----- 8 channels
- PWM output circuit ----- 8-bit x 5
- ROM correction function ----- 32 bytes x 2
- Power dissipation ----- 165mW
(at Vcc=5.5V, 8MHz oscillation frequency, OSD on, and Data slicer on)
- Closed caption data slicer
- OSD function
 - Display characters ----- 32 characters x 2 lines(possible to display 3 lines or more by software)
 - Kinds of characters 254 kinds
 - Character display area CC mode : 16x26 dots
OSD mode : 16x20 dots
 - Kinds of character sizes CC mode : 1 kind
OSD mode : 8 kinds
 - Kinds of character colors 8 colors(R,G,B) (coloring unit: a character)
 - Kinds of background colors CC mode : 1 kind(black)
OSD mode : 8 kinds(possible to select color in character unit)
 - Display position horizontal : 128 levels Vertical : 512 levels
 - Attribute CC mode : smooth italic, underline, flash, automatic solid space
OSD mode : border(black)
 - Kinds of raster colors 8 kinds
 - Smooth roll-up
 - Window function

[ASIC Block]

Description

CVBS(TV/EXT) signals or Y/C signals input to this IC are converted to 8 bit digital signal by 2 channels high speed video ADCs. These signals are input to digital section to obtain high performance R/G/B signals. First, CVBS signals are separated to high quality Y/C signals by 2 dimensional adaptive YC separation circuit, and then Y/C signals are converted to R-Y&B-Y signals by digital chroma decoder, after that, to R/G/B signals by RGB matrix circuit. These signals are mixed with OSD signals come from MCU block, are converted to analog R/G/B signals by 3 channel 10 bit high speed video DACs. In deflection block, to get a better Horizontal & Vertical signals, a conventional analog solution by analog CMOS technology is used.

ASIC block consists of the followings blocks.

- (1) Analog frontend block ; Analog SW(2 CVBS(TV&EXT) inputs, Y/C signals to one signal), 2 channels 8 bit high speed video ADCs , and ACC amplifiers
- (2) Video and Chroma block ; A high performance 2 line adaptive YC separation by 1 line memory, Video blocks including sharpness, YNR, a high performance blackstretch circuits, Chroma decoder, and RGB matrix including OSD mixing circuit.
- (3) Deflection block ; A high performance sync separation by analog and digital mixed solution
- (4) Analog backend block ; 3 channels 10 bit high speed video DACs for Cutoff & Drive, and Mute circuit.

Features

[Video/Chroma Block]

- Built-in 1 Video SW for TV/EXT signal input
- 2 additional pins for S(Y/C) input
- YUV input signal available (T.B.D)
- 2 channel 8 bit Video ADCs for CVBS(TV&EXT) or Y/C signal inputs
- Built-in adaptive 2 line comb filter(2DYCS) => Few dot crawl&crosscolor, and clear color transition
- Built-in a high performance Blackstretch => Dynamic & detailed picture
- Digital Luminance delay circuit => stable Y/C timing adjustment
- Built-in VCXO circuit(4fsc)
- High resolution R/G/B output => Built-in 10bit high speed Video DACs
- Internal connection of 8 color digital OSD (R/G/B, F.B, H.T)
- Reference CLK output for tuner (fsc or 4MHz)
- Built-in YNR (about fsc±1MHz)
- Gamma correction(for R/G/B signals)

[Deflection Block]

- Analog(conventional) sync separation => Better performance by abundant experience
- Double AFC Circuit => Stable Horizontal scanning
- Built-in Horizontal reference Oscillator => No ceramic resonator and Adjustment free
- HD and VD pulse by Countdown => Stable HD&VD
- Built-in digital Vramp generator

[List of main I²C bus controllable Items]

- Chip : Power-down mode
- Analog Input Stage : CVBS/Y&C Input SW
- Luminance Processing : Sharpness, Blackstretch
- Chroma Processing : Color, Tint, Killer level
- RGB Matrix : ACL, OSD Input Level, Contrast, Brightness
- Analog Output Stage : Drive adj.(R/G/B), Cutoff adj.(R/G/B)
- Deflection Block : H-Phase, V-size, V-shift, V-Linearity

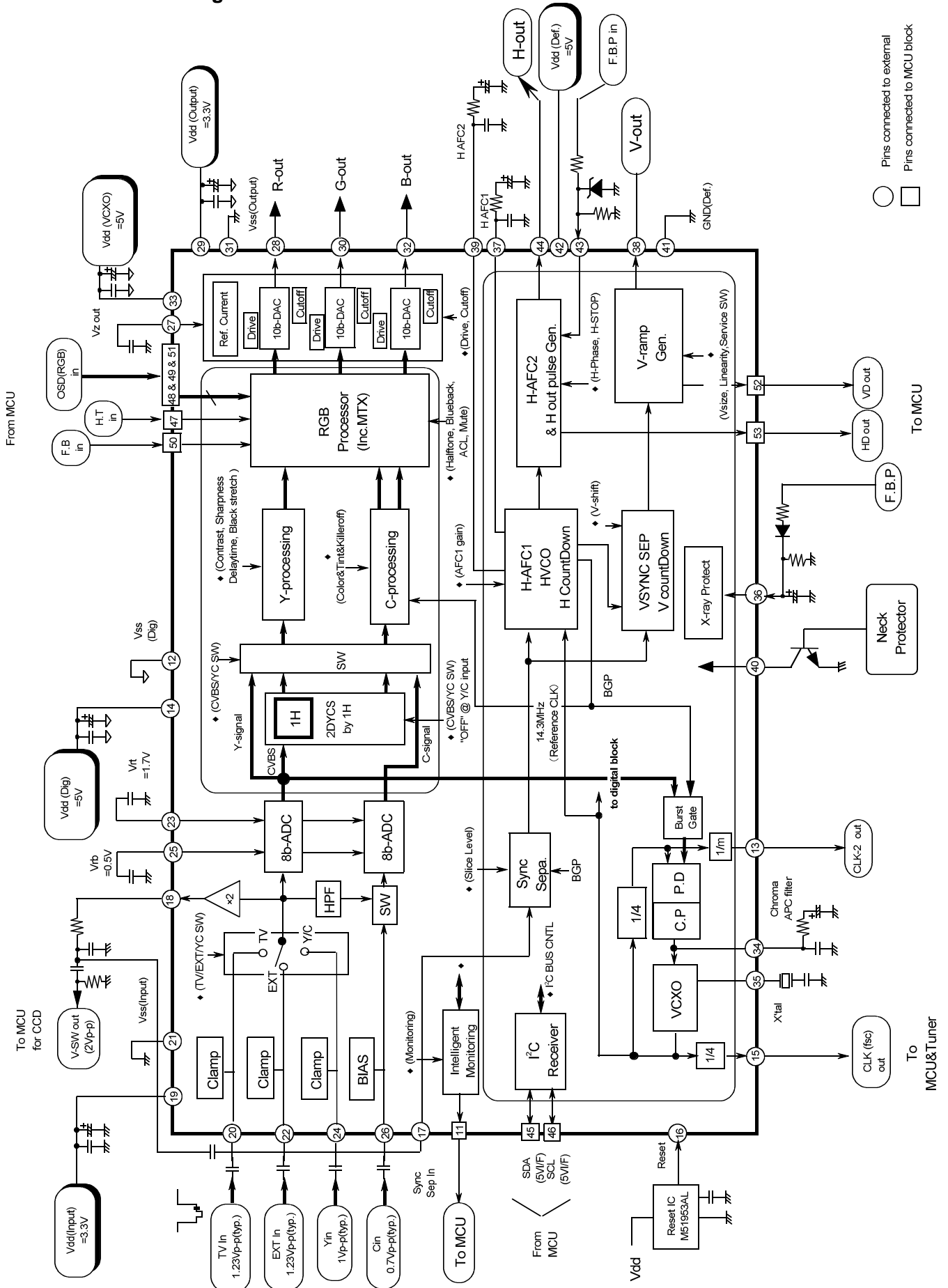
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ASIC Block Detailed Diagram



Function and Outline of ASIC Block

Chip

- Power down mode : 3 modes [PD0 & PD1 & PD2]
- Service SW : stop of Vertical(Vramp) output (For cutoff adjustment)

Analog Block

- Input stage => CVBS&Y/C input signals
 - Input level (CVBS) : 1.23Vp-p (173IRE) @max. / 1.0Vp-p @typ.
 - Input level (Y/C) : Y:1.00Vp-p (140IRE) @typ./ C:0.7Vp-p @typ.
- Output stage => RGB output signals
 - Output level : 0.7 Vp-p (typ.)
 - Drive(R&G&B) : -3 to +4 dB by 7bit (White Balance)
 - Cutoff(R&G&B) : 0.5 V by 9bit (Start lighting point)

Digital Block

- 2DYCS
 - Adaptive YC separation by using of 1H line memory and original algorithm
- Luminance processing
 - Contrast : 0 to 200 LSB by 7bit
 - Brightness : -20 to 20 LSB by 8bit (Pedestal DC level)
 - Sharpness : 0 to 3 dB by 5bit (by 0, 70, 140, 210ns)
 - Delay adjustment : 0 to 210 ns by 2bit(70ns step) to Chroma signal
 - Blackstretch : 3 selectable stretch point
 - [Stretch areas (0 to 25/30/40IRE), Through areas (25/30/40IRE ~)]
 - 4 selectable blackstretch curves (1/4, 2/4, 3/4, 4/4)
- Chroma processing
 - Tint : -45 to 45 degree by 7bit => about 0.7 degree
 - : Variable demodulator (R-Y) axis
 - (-22.5 to +22.5 degree by 6bit => about 0.7 degree)
 - Color : 0 to 200 % by 7bit
- RGB matrix
 - : Matrix(R-Y signal) ratio selectable (12/8, 13/8, 14/8)
 - ACL : Automatic Contrast Limiter by MCU port(ADC) and I²C bus
 - EXT/RGB : clip to 7LSB @ data < 0Fh
 - BlueBack : ON/OFF selectable
 - Mute : ON/OFF of R/G/B output
 - Neck Protector : R/G/B output to zero(no signal)

Deflection Block

- Horizontal Output
 - AFC2 phase : +5 to -5 μ s by 5bit
 - Hold => Shut down : fh@Hold-down : in about 16.5KHz => fh@Shutdown : H-STOP
 - AFC1 gain : Normal/High selectable for VTR skew
- Vertical Output
 - V position : 0 to 16 H by 3 bit => 2H unit(connected with BLK)
 - V size : 1.4 to 2.6 V by 7bit
 - Linearity : 0 to 30 % by 7bit

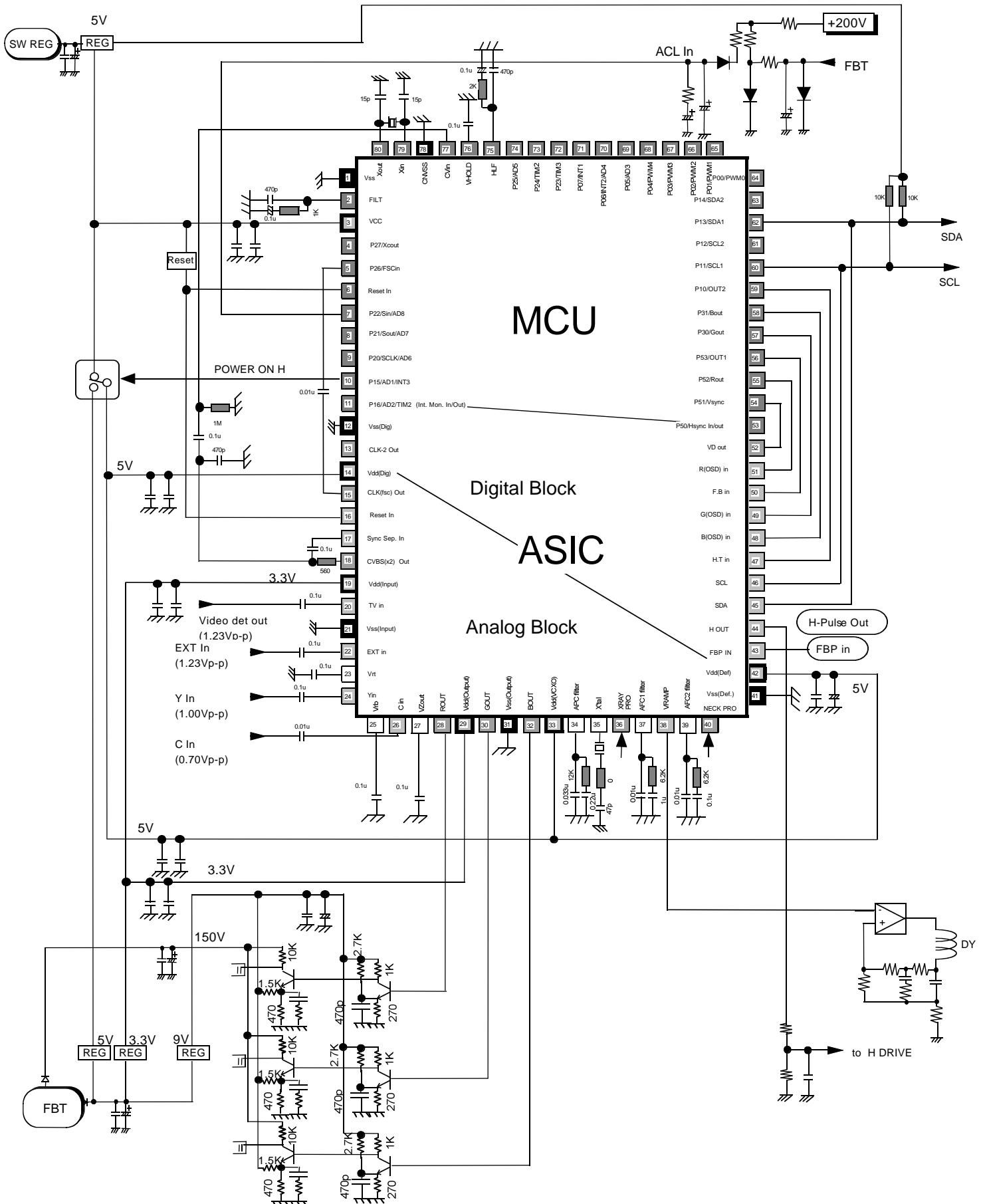
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Application Examples



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Electrical characteristics

(Ta=25°C, Vdd=5.0V, 3.3V)

| Symbol | Parameter | Input signal | | Test point | Limits | | | Unit | Remarks |
|------------|---------------------|--------------|----|----------------|--------|------|------|------|---|
| | | Pins | SG | | Min. | Typ. | Max. | | |
| ICC | Standard conditions | | | | | | | | |
| ICC50 | 5.0V supply current | - | - | 3,14, 33,42 | 102 | 116 | 130 | mA | Supply of MCU, Digital, VCXO and Deflection |
| ICC33 | 3.3V supply current | - | - | 18, 29 | 47 | 56 | 65 | mA | Supply of A/D and D/A |

| | | | | | | | | | |
|-------------------|--|----|------|--------------|-----|-----|-----|------------------|--|
| VIDEO | Standard conditions of video character | - | - | - | - | - | - | - | |
| 2AGTV | Video SW output level (TV input) | 26 | SG.A | 18 | 1.5 | 1.7 | 1.9 | V _{pp} | |
| 2AGEV | Video SW output level (External input) | 20 | SG.A | 18 | 1.5 | 1.7 | 1.9 | V _{pp} | |
| V _{typ} | Video standard output | 26 | SG.A | 28,30, 32 | 590 | 740 | 890 | mV _{pp} | |
| FBY | Video frequency characteristics | 26 | SG.B | 28,30, 32 | -3 | 0 | 3 | dB | f=5MHz |
| Y/C1 | Y/C separation function 1 | 26 | SG.E | 28,30, 32 | - | -30 | -20 | dB | feb=fec=fsc |
| Y/C2 | Y/C separation function 2 | 26 | SG.E | 28,30, 32 | -3 | 0 | 3 | dB | feb=fsc, fec=fsc±1/2f _H |
| Y/C3 | Y/C separation function 3 | 26 | SG.E | 28,30, 32 | - | -30 | -20 | dB | feb=fsc, fec=fsc±f _H |
| YDL0 | Y total delay time | 26 | SG.A | 28,30, 32 | 2.4 | 3.0 | 3.6 | μsec | |
| YDL1 | Y delay time 1 | 26 | SG.A | 28,30, 32 | 50 | 70 | 90 | nsec | YDL1=measure – YDL0 |
| YDL2 | Y delay time 2 | 26 | SG.A | 28,30, 32 | 50 | 70 | 90 | nsec | YDL2=measure – YDL1 |
| YDL3 | Y delay time 3 | 26 | SG.A | 28,30, 32 | 50 | 70 | 90 | nsec | YDL3=measure – YDL2 |
| GT _{nor} | Video tone control characteristic 1 | 26 | SG.B | 28,30, 32 | 640 | 800 | 960 | mV | f=2.5MHz |
| GT _{max} | Video tone control characteristic 2 | 26 | SG.B | 28,30, 32 | 1 | 2.5 | 4 | dB | f=2.5MHz |
| GT _{min} | Video tone control characteristic 3 | 26 | SG.B | 28,30, 32 | -7 | -4 | -1 | dB | f=2.5MHz |
| BLS | Black stretch characteristic | 26 | SG.D | 28,30, 32 | 20 | 50 | 80 | mV | V _y =0.18V, 45H=80h(BLS ON) / 00h(BLS OFF) |
| HT | Half Tone function | 26 | SG.A | 28,30, 32 | -9 | -6 | -3 | dB | |

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| Symbol | Parameter | Input signal | | Test point | Limits | | | Unit | Remarks |
|--------|--|--------------|------|------------|--------|-------|-------|------|---|
| | | Pins | SG | | Min. | Typ. | Max. | | |
| CHROMA | Standard condition of chroma parameter | - | - | - | - | - | - | - | 5DH=03h |
| CnorR | Chroma standard output (R-Y) | 26 | SG.E | 28 | 155 | 180 | 205 | mV | feb=fec+50kHz |
| CnorB | Chroma standard output (B-Y) | 26 | SG.E | 32 | 275 | 310 | 345 | mV | feb=fec+50kHz |
| ACC1 | ACC characteristic 1 | 26 | SG.E | 28 | -3 | 0 | 3 | dB | Vec, Vec : +6dB of typical input level |
| ACC2 | ACC characteristic 2 | 26 | SG.E | 28 | -3 | 0 | 3 | dB | Vec, Vec : -20dB of typical input level |
| VikN | Killer operation input level | 26 | SG.E | 28 | -40 | -35 | -30 | dB | Vec, Vec : variable |
| KillP | Color residual at Killer on | 26 | SG.E | 28 | - | -40 | -28 | dB | Vec = 0mV |
| APCU | APC pull-in range (upper) | 26 | SG.E | 28 | 400 | - | - | Hz | feb=fec : variable |
| APCL | APC pull-in range (lower) | 26 | SG.E | 28 | - | - | -400 | Hz | feb=fec : variable |
| DEMR | Demodulated output ratio | 26 | SG.E | 28,32 | 0.47 | 0.57 | 0.67 | - | feb=fec+50kHz |
| DEMP | Demodulation phase angle | 26 | SG.F | 28,32 | 85 | 90 | 95 | deg | |
| Ccon 1 | Color control characteristic 1 | 26 | SG.E | 28 | 160 | 200 | 240 | % | feb=fec+50kHz |
| Ccon 2 | Color control characteristic 2 | 26 | SG.E | 28 | - | 0 | 10 | % | feb=fec+50kHz |
| TC1 | TINT control characteristic 1 | 26 | SG.F | 28,32 | 30 | 45 | 60 | deg | |
| TC2 | TINT control characteristic 2 | 26 | SG.F | 28,32 | -60 | -45 | -30 | deg | |
| Fclk | CLK output frequency | 26 | SG.C | 15 | 3.578 | 3.579 | 3.580 | MHz | |
| Vclk | CLK output amplitude | 26 | SG.C | 15 | 350 | 500 | 650 | mVpp | |

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| Symbol | Parameter | Input signal | | Test point | Limits | | | Unit | Remarks |
|------------|--|--------------|------|------------|--------|------|------|------------------|-------------------------------------|
| | | Pins | SG | | Min. | Typ. | Max. | | |
| RGB | Standard condition of RGB parameter | - | - | - | - | - | - | - | |
| VPED | Output Pedestal voltage | 26 | SG.D | 28,30,32 | 2.7 | 3.0 | 3.3 | V | V _y = 0.0V |
| MTXRB | Matrix ratio R/B | 26 | SG.H | 28,32 | 0.74 | 0.92 | 1.10 | - | |
| MTXGB | Matrix ratio G/B | 26 | SG.H | 30,32 | 0.24 | 0.33 | 0.42 | - | |
| GYmax | Contrast control characteristic 1 | 26 | SG.D | 28,30,32 | 160 | 200 | 240 | % | V _y =0.286V |
| GYmin | Contrast control characteristic 2 | 26 | SG.D | 28,30,32 | - | 0 | 10 | % | V _y =0.286V |
| GYEclip | Contrast control characteristic 5 | 48,49,51 | SG.G | 28,30,32 | 250 | 300 | 350 | mV | |
| Lum max | Brightness control characteristic 2 | 26 | SG.D | 28,30,32 | 100 | 150 | 200 | mV | |
| Lum min | Brightness control characteristic 3 | 26 | SG.D | 28,30,32 | -200 | -150 | -100 | mV | V _y =0.286V |
| D(R)1 | R Drive control characteristic 1 | 26 | SG.D | 28 | 1.5 | 3.5 | 5.5 | dB | V _y =0.286V |
| D(G)1 | G Drive control characteristic 1 | 26 | SG.D | 30 | 1.5 | 3.5 | 5.5 | dB | V _y =0.286V |
| D(B)1 | B Drive control characteristic 1 | 26 | SG.D | 32 | 1.5 | 3.5 | 5.5 | dB | V _y =0.286V |
| D(R)2 | R Drive control characteristic 2 | 26 | SG.D | 28 | -4.6 | -2.6 | -0.6 | dB | V _y =0.286V |
| D(G)2 | G Drive control characteristic 2 | 26 | SG.D | 30 | -4.6 | -2.6 | -0.6 | dB | V _y =0.286V |
| D(B)2 | B Drive control characteristic 2 | 26 | SG.D | 32 | -4.6 | -2.6 | -0.6 | dB | V _y =0.286V |
| C(R)1 | R Cut off control characteristic 1 | 26 | SG.D | 28 | 210 | 260 | 310 | mV | V _y =0.286V |
| C(G)1 | G Cut off control characteristic 1 | 26 | SG.D | 30 | 210 | 260 | 310 | mV | V _y =0.286V |
| C(B)1 | B Cut off control characteristic 1 | 26 | SG.D | 32 | 210 | 260 | 310 | mV | V _y =0.286V |
| C(R)2 | R Cut off control characteristic 2 | 26 | SG.D | 28 | -310 | -260 | -210 | mV | V _y =0.286V |
| C(G)2 | G Cut off control characteristic 2 | 26 | SG.D | 30 | -310 | -260 | -210 | mV | V _y =0.286V |
| C(B)2 | B Cut off control characteristic 2 | 26 | SG.D | 32 | -310 | -260 | -210 | mV | V _y =0.286V |
| OSD(R) | OSD (R) output level | 51 | SG.G | 28 | 500 | 600 | 700 | mV _{pp} | |
| OSD(G) | OSD (G) output level | 49 | SG.G | 30 | 500 | 600 | 700 | mV _{pp} | |
| OSD(B) | OSD (B) output level | 48 | SG.G | 32 | 500 | 600 | 700 | mV _{pp} | |
| SOSD1 | OSD speed characteristic 1 | 48,49,51 | SG.G | 28,30,32 | - | 100 | 200 | nsec | |
| SOSD2 | OSD speed characteristic 2 | 48,49,51 | SG.G | 28,30,32 | - | 100 | 200 | nsec | |
| OFF(R) | Offset voltage between R and OSD(R) | - | - | - | -50 | 0 | 50 | mV | Difference at pedestal level |
| OFF(G) | Offset voltage between G and OSD(G) | - | - | - | -50 | 0 | 50 | mV | Difference at pedestal level |
| OFF(B) | Offset voltage between B and OSD(B) | - | - | - | -50 | 0 | 50 | mV | Difference at pedestal level |
| NECK | Neck protector function threshold voltage | 26 | SG.A | 40 | 1.0 | 1.3 | 1.6 | V | while monitoring at pins 28, 30, 32 |

Preliminary

Note : This is not a final specification.

Some of information in this document are subject to changes.

Mitsubishi Semiconductor<Digital IC>
M65580MAP-XXXFP
Digital Video/Chroma/Deflection+MCU

| Symbol | Parameter | Input signal | | Test point | Limits | | | Unit | Remarks |
|--------|--|--------------|------|------------|--------|-------|-------|-----------------|--|
| | | Pins | SG | | Min. | Typ. | Max. | | |
| DEF | Standard condition of deflection parameter | - | - | - | - | - | - | - | |
| fH1 | Horizontal free-running frequency 1 | - | - | 44 | 15.53 | 15.73 | 15.93 | kHz | |
| fH2 | Horizontal free-running frequency 2 | - | - | 44 | 13.72 | 14.32 | 14.92 | kHz | |
| fH3 | Horizontal free-running frequency 3 | - | - | 44 | 17.25 | 17.85 | 18.45 | kHz | |
| FPHU | Horizontal pull-in range (upper) | 17 | SG.I | 44 | 250 | 500 | - | Hz | Vary frequency of input signal. |
| FPHL | Horizontal pull-in range (lower) | 17 | SG.I | 44 | - | -500 | -250 | Hz | Vary frequency of input signal. |
| HPV | Horizontal pulse amplitude | 26 | SG.A | 44 | 4.0 | 4.5 | 5.0 | V | |
| HPTW | Horizontal pulse width | 26 | SG.A | 44 | 19.3 | 22.3 | 25.3 | μsec | |
| HPD | Horizontal pulse duty cycle | 26 | SG.A | 44 | 30 | 35 | 40 | % | |
| HPT1 | Horizontal pulse timing 1 | 26 | SG.A | 44 | 8.7 | 10.7 | 12.7 | μsec | |
| HPT2 | Horizontal pulse timing 2 | 26 | SG.A | 44 | 2.2 | 4.2 | 6.2 | μsec | |
| HPT3 | Horizontal pulse timing variable range | 26 | SG.A | 44 | 4.5 | 6.5 | 8.5 | μsec | HPT2 – HPT1 |
| HDOWN | Hold down function threshold voltage | 26 | SG.A | 36 | 3.0 | 3.1 | 3.2 | V | while monitoring at pin 44 |
| SDOWN | Shut down function threshold voltage | 26 | SG.A | 36 | 3.3 | 3.5 | 3.7 | V | while monitoring at pin 44 |
| fV | Vertical free-running frequency | - | - | 38 | 55 | 60 | 65 | Hz | |
| SVC | Service mode function | - | - | 38 | 2.5 | 2.8 | 3.1 | V | |
| FPVU | Vertical pull-in frequency (upper) | 17 | SG.J | 38 | - | - | 63 | Hz | Vary frequency of input signal. |
| FPVL | Vertical pull-in frequency (lower) | 17 | SG.J | 38 | 57 | - | - | Hz | Vary frequency of input signal. |
| VRsi 1 | Vertical ramp size | 26 | SG.A | 38 | 2.1 | 2.5 | 2.9 | V _{pp} | |
| VRsc 1 | Vertical ramp size control range 1 | 26 | SG.A | 38 | 20 | 27 | 35 | % | |
| VRsc 2 | Vertical ramp size control range 2 | 26 | SG.A | 38 | -35 | -27 | -20 | % | |
| VLin 1 | Vertical ramp Linearity control range 1 | 26 | SG.A | 38 | -5 | 0 | 5 | % | |
| VLin 2 | Vertical ramp Linearity control range 2 | 26 | SG.A | 38 | 19 | 24 | 29 | % | |
| VRpo 1 | Vertical ramp position control range 1 | 26 | SG.A | 38 | 0 | 50 | 200 | μsec | |
| VRpo 2 | Vertical ramp position control range 2 | 26 | SG.A | 38 | 790 | 940 | 1090 | μsec | (Measured value) – (V _{rpo 1}) |
| VW | Vertical pulse width | 26 | SG.A | 52 | 0.35 | 0.53 | 0.65 | msec | |
| VBLKW | Vertical blanking width | 26 | SG.A | 28,30,32 | 1.52 | 1.64 | 1.76 | msec | |
| WVSS | Minimum vertical sync detection width | 26 | SG.A | 11 | 13 | 18 | 23 | μsec | |

Electrical characteristics (MCU part)

(V_{CC}=5V±10%, V_{SS} = 0V, f(X_{IN})=8MHz, T_a=-20°C to 65°C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit | Test circuit | | |
|-----------------------------------|--|---|--|---|------|------|--------------|-----|----|
| | | | Min. | Typ. | Max. | | | | |
| I _{CC} | Power source current | V _{CC} = 5.5 V, f(X _{IN}) = 8 MHz | OSD OFF Data slicer OFF | 15 | 30 | mA | 1 | | |
| | | | OSD ON | 30 | 45 | | | | |
| | | System operation | V _{CC} = 5.5 V, f(X _{IN}) = 0, f(X _{CIN}) = 32 kHz, OSD OFF, Data slicer OFF, Low-power dissipation mode set (CM5 = "0", CM6 = "1") | | 60 | 200 | | μA | |
| | | | Wait mode | V _{CC} = 5.5 V, f(X _{IN}) = 8 MHz | | 2 | | 4 | mA |
| | | | | V _{CC} = 5.5 V, f(X _{IN}) = 0, f(X _{CIN}) = 32 kHz, Low-power dissipation mode set (CM5 = "0", CM6 = "1") | | 25 | | 100 | μA |
| | V _{CC} = 5.5 V, f(X _{IN}) = 0, f(X _{CIN}) = 0 | | 1 | 10 | | | | | |
| V _{OH} | HIGH output voltage P10–P16, P20–P27, P30, P31, P52, P53 | V _{CC} = 4.5 V I _{OH} = -0.5 mA | 2.4 | | | V | 2 | | |
| V _{OL} | LOW output voltage P00–P07, P10, P15, P16, P20–P27, P30, P31, P52, P53 | V _{CC} = 4.5 V I _{OL} = 0.5 mA | | | 0.4 | V | | | |
| | LOW output voltage P11–P14 | V _{CC} = 4.5 V | | | 0.4 | | | | |
| | | | | | 0.6 | | | | |
| V _{T+} – V _{T-} | Hysteresis (See note 1) RESET, P50–P51, INT1, INT2, INT3, TIM2, TIM3, SIN, SCLK, SCL1, SCL2, SDA1, SDA2 | V _{CC} = 5.0 V | | 0.5 | 1.3 | V | 3 | | |
| I _{IZH} | HIGH input leak current P00–P07, P10–P16, P20–P27, P50, P51, RESET | V _{CC} = 5.5 V V _I = 5.5 V | | | 5 | μA | 4 | | |
| I _{IZL} | LOW input leak current P00–P07, P10–P16, P20–P27, P50, P51, RESET | V _{CC} = 5.5 V V _I = 0 V | | | 5 | μA | 4 | | |
| R _{BS} | I ² C-BUS • BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2) | V _{CC} = 4.5 V | | | 130 | Ω | 5 | | |

Notes 1: P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P11–P14 have the hysteresis when these pins are used as multi-master I²C-BUS interface ports. P20–P22 have the hysteresis when these pins are used as serial I/O pins.

2: Connect 0.1μF or more capacitor externally between the power source pins V_{CC}–V_{SS} so as to reduce power source noise.

Also connect 0.1μF or more capacitor externally between the pins V_{CC}–CNV_{SS}.

3: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.

4: Pin names in each parameter is described as below.

(1) Dedicated pin: dedicated pin names.

(2) Double-/triple-function ports

- When the same limits: I/O port name.

- When the limits of functions except ports are different from I/O port limits: function pin name.

Preliminary

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Mitsubishi Semiconductor<Digital IC>
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I²C Bus Table

SLAVE ADDRESS= BAH(WRITE), BBH(READ)

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
|----|----|----|----|----|----|----|-----|
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1/0 |

WRITE TABLE(input bytes)

| SUB ADDRESS | | DATA | | | | | | | | INITIAL |
|-------------|----------|-------------------------|------------------|-------------------------|-------------------------------|------------------------------|----------------|------------------|-----|---------|
| HEX | BIN | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 00H | 00000000 | (not assigned) | | | | Power Down Mode | | H Stop | | 02H |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| 01H | 00000001 | X-ray Enable | YUV input | Y/C input | EXT input | TV input | Y/C through | (for evaluation) | | 08H |
| | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| 02H | 00000010 | Ped Clamp | (not assigned) | | VRT Voltage | | Sync-tip Clamp | | | 08H |
| | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| 04H | 00001000 | Sharpness Delay (Front) | | | Sharpness Gain (Front) | | | | | A0H |
| | | V1 | V0 | V1 | V0 | V0 | V0 | V0 | V0 | |
| 05H | 00001001 | Sharpness Delay (Rear) | | | Sharpness Gain (Rear) | | | | | A0H |
| | | V1 | V0 | V1 | V0 | V0 | V0 | V0 | V0 | |
| 06H | 00001100 | (not assigned) | Y DL Time Adj. | | YNR SW | YNR Limiter Level | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 07H | 00001101 | (not assigned) | | Sharpness Limiter Level | | | | | | 15H |
| | | V0 | V0 | V0 | V1 | V0 | V1 | V0 | V1 | |
| 08H | 00001000 | (not assigned) | Tint Control | | | | | | 29H | |
| | | V0 | V0 | V1 | V0 | V1 | V0 | V0 | V1 | |
| 09H | 00001001 | (not assigned) | Color Control | | | | | | 28H | |
| | | V0 | V0 | V1 | V0 | V1 | V0 | V0 | V0 | |
| 0AH | 00001010 | (not assigned) | Contrast Control | | | | | | 3BH | |
| | | V0 | V0 | V1 | V1 | V1 | V0 | V1 | V1 | |
| 0BH | 00001011 | Half Tone | | OSD Level (R) | | | | | | 1EH |
| | | V0 | V0 | V0 | V1 | V1 | V1 | V1 | V0 | |
| 0CH | 00001100 | RGB Matrix Ratio | | OSD Level (G) | | | | | | 5EH |
| | | V1 | V0 | V0 | V1 | V1 | V1 | V1 | V0 | |
| 0DH | 00001101 | OSD Comp | | OSD Level (B) | | | | | | 0EH |
| | | V0 | V0 | V0 | V1 | V1 | V1 | V1 | V0 | |
| 0EH | 00001110 | Brightness Control | | | | | | | | 80H |
| | | V1 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 0FH | 00001111 | (not assigned) | H Free | AFC1 Gain | H Phase Control | | | | | 08H |
| | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| 10H | 00010000 | (not assigned) | | (for evaluation) | 2D Y/C | (for evaluation) | | | | 00H |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 11H | 00010001 | (not assigned) | Black Stre. SW | (for evaluation) | | | | | | 40H |
| | | V0 | V1 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 12H | 00010010 | RGB Mute | (inhibited) | | | Gamma Control | | | | 80H |
| | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 13H | 00010011 | Service SW | V-Shift | | (inhibited) | Hold Down Level | | | | 10H |
| | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| 14H | 00010100 | V-Blanking Stop | | V-Ramp Size | | | | | | 40H |
| | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 15H | 00010101 | V-Ramp Invert | | V-Ramp Linearity | | | | | | FFH |
| | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 16H | 00010110 | Cut Off (R) | | | | | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 17H | 00010111 | CutOff(R) MSB | | | Drive (R) | | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 18H | 00011000 | Cut Off (G) | | | | | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 19H | 00011001 | CutOff(G) MSB | | | Drive (G) | | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 1AH | 00011010 | Cut Off (B) | | | | | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 1BH | 00011011 | CutOff(B) MSB | | | Drive (B) | | | | | 00H |
| | | V0 | V0 | V0 | V0 | V0 | V0 | V0 | V0 | |
| 1CH | 00011100 | (not assigned) | | | | Intelligent Monitor (Analog) | | | | 00H |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 1DH | 00011101 | (not assigned) | | I/M(D) Enable | Intelligent Monitor (Digital) | | | | 00H | |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 51H | 01010001 | H VCO Adjust | | | | | | | | 00H |
| | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

NOTE: V0 / V1 ==> V- LATCH BIT

READ TABLE(output bytes)

| SUB ADDRESS | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|------------|----------------|----------|-----|----------------|--------|--------|--------|
| 60H | 01100000 | KILLER | H COINCI | V COINCI | B_W | IIC_STILL | MV_180 | DET_NZ | K_MONI |
| 61H | 01100001 | B2 ROM | | | | | | | |
| 62H | 01100010 | B2 ROM MSB | (not assigned) | | | | | C Gain | |
| 63H | 01100011 | BLKDETV | | | | (not assigned) | | | |

Preliminary

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Mitsubishi Semiconductor<Digital IC>
M65580MAP-XXXFP
Digital Video/Chroma/Deflection+MCU

Bus function

WRITE

| FUNCTION | BIT | SUB ADD | DATA | DISCRIPTION | INITIAL | NOTE |
|-------------------------------|-----|---------|-------|--|----------|---------|
| H STOP | 1 | 00H | D0 | Horizontal output switch (0: H OUT, 1: H STOP) | 0 | |
| Power Down | 2 | 00H | D1-D2 | Power down mode control (0: normal, 1: PD0, 2: PD1, 3: PD2) | 01 | |
| Input Video SW | 4 | 01H | D3-D6 | Video SW Selector (1: TV, 2: EXT, 4: Y/C input, 9: YUV input) | 0001 | |
| X-ray Enable | 1 | 01H | D7 | X-ray protect function switch (0: X-ray Protect OFF, 1: X-ray Protect ON) | 0 | |
| Y/C through | 1 | 01H | D2 | Y/C separation input switch (0: Y/C Sep ON, 1: Y/C Sep. through) | 0 | |
| Sync-tip Clamp | 3 | 02H | D0-D2 | Sync-tip clamp switch (0: Clamp ON, 1: TV clamp OFF, 2: EXT clamp OFF, 4: Y clamp OFF) | 000 | |
| Ped Clamp | 1 | 02H | D7 | Pedestal clamp switch (0: Pedestal clamp OFF, 1: Pedestal clamp ON) | 0 | |
| VRT Voltage | 2 | 02H | D3-D4 | Reference voltage adjustment for A/D | 01 | |
| Sharpness Gain (Front) | 6 | 04H | D0-D5 | Over-shoot gain control by 6bit | 100000 | V Latch |
| Sharpness Delay (Front) | 2 | 04H | D6-D7 | Over-shoot width control (0: 0ns, 1: 70ns, 2: 140ns 3: 210ns) | 10 | V Latch |
| Sharpness Gain (Rear) | 6 | 05H | D0-D5 | Pre-shoot gain control by 6bit | 100000 | V Latch |
| Sharpness Delay (Rear) | 2 | 05H | D6-D7 | Pre-shoot width control (0: 0ns, 1: 70ns, 2: 140ns 3: 210ns) | 10 | V Latch |
| YNR SW | 7 | 06H | D4 | YNR control switch (0: YNR OFF, 1: YNR ON) | 0 | V Latch |
| YNR Limiter Level | 1 | 06H | D0-D3 | YNR limiter level control | 0000 | V Latch |
| Y DL Time Adj. | 2 | 06H | D5-D6 | Delay time adjustment of luminance signal (0: 0ns, 1: 70ns, 2: 140ns 3: 210ns) | 00 | V Latch |
| Sharpness Limiter Level | 6 | 07H | D0-D5 | Maximum level control of sharpness | 010101 | V Latch |
| Tint Control | 7 | 08H | D0-D6 | Tint Control by 7bit | 0101001 | V Latch |
| Color Control | 7 | 09H | D0-D6 | Color Saturation control by 7bit | 0101000 | V Latch |
| Contrast Control | 7 | 0AH | D0-D6 | Contrast control by 7bit | 0111011 | V Latch |
| OSD Level (R) | 6 | 0BH | D0-D5 | Digital OSD (R) level adjustment by 6bit | 011110 | V Latch |
| Half Tone | 2 | 0BH | D6-D7 | Setting of Half Tone mode | 00 | V Latch |
| OSD Level (G) | 6 | 0CH | D0-D5 | Digital OSD (G) level adjustment by 6bit | 011110 | V Latch |
| RGB Matrix Ratio | 2 | 0CH | D6-D7 | RGB Matrix ratio control | 10 | V Latch |
| OSD Level (B) | 6 | 0DH | D0-D5 | Digital OSD (B) level adjustment by 6bit | 011110 | V Latch |
| OSD Comp | 2 | 0DH | D6-D7 | Digital OSD threshold voltage control of input signal | 00 | V Latch |
| Brightness Control | 8 | 0EH | D0-D7 | Brightness control by 8bit | 10000000 | V Latch |
| AFC2 H Phase | 5 | 0FH | D0-D4 | Horizontal phase adjustment by 5bit | 01000 | |
| AFC1 Gain | 1 | 0FH | D5 | Horizontal AFC gain switch (0: Low, 1: High) | 0 | |
| H-free | 1 | 0FH | D6 | Horizontal forced free-running mode switch (0: OFF, 1: Forced Free-running) | 0 | |
| 2D Y/C | 1 | 10H | D4 | Y/C separation mode switch (0: Y/C Sep ON, 1: Y/C Sep. through) | 0 | |
| Black Stretch SW | 1 | 11H | D6 | Black Stretch function ON/OFF switch (0: OFF, 1: ON) | 0 | |
| Gamma Control | 1 | 12H | D0-D3 | RGB gamma threshold control (0: Gamma OFF) | 0000 | |
| RGB Mute | 1 | 12H | D7 | RGB signal mute ON/OFF switch (0: Mute 1: RGB output) | 1 | |
| Hold Down Level | 3 | 13H | D0-D2 | Hold Down level adjustment by 3bit | 000 | |
| V Shift | 3 | 13H | D4-D6 | V RAMP start timing adjustment 2Line/Step | 001 | |
| Service SW | 1 | 13H | D3 | Service mode switch (0: Vertical output ON, 1: Vertical output OFF) | 0 | |
| V-Ramp Size | 7 | 14H | D0-D6 | V-Ramp amplitude adjustment by 7bit | 1000000 | |
| Test | 1 | 14H | D7 | No use for customer (Test mode) | 0 | |
| V-Ramp Linearity | 7 | 15H | D0-D6 | V-Ramp linearity adjustment by 7bit | 1111111 | |
| V-Ramp Invert | 1 | 15H | D7 | V-Ramp polarity switch | 1 | |
| Cut Off(R) | 9 | 16H | D0-D7 | R OUT pedestal level adjustment by 9bit | 00000000 | V Latch |
| | | 17H | D7 | | 0 | |
| Drive(R) | 7 | 17H | D0-D6 | R OUT amplitude adjustment by 7bit | 0000000 | V Latch |
| Cut Off(G) | 9 | 18H | D0-D7 | G OUT pedestal level adjustment by 9bit | 00000000 | V Latch |
| | | 19H | D7 | | 0 | |
| Drive(G) | 7 | 19H | D0-D6 | G OUT amplitude adjustment by 7bit | 0000000 | V Latch |
| Cut Off(B) | 9 | 1AH | D0-D7 | B OUT pedestal level adjustment by 9bit | 00000000 | V Latch |
| | | 1BH | D7 | | 0 | |
| Drive(B) | 7 | 1BH | D0-D6 | B OUT amplitude adjustment by 7bit | 0000000 | V Latch |
| Intelligent Monitor (Analog) | 4 | 1CH | D0-D3 | Intelligent Monitor (Analog) mode selector | 0000 | |
| Intelligent Monitor (Digital) | 5 | 1DH | D0-D4 | Intelligent Monitor (Digital) mode selector | 00000 | |
| Intelligent Monitor(D) Enable | 1 | 1DH | D5 | Intelligent Monitor (Digital) function switch (0: OFF, 1: ON) | 0 | |
| H VCO Adj. | 8 | 51H | D0-D7 | H VCO free-running frequency adjustment by 8bit | 00000000 | |

Read

| | | | | |
|-----------|---|-----|-------|--|
| K_MONI | 1 | 60H | D0 | C-processor Killer det. output (1: C-pro Killer ON) |
| DET_NZ | 1 | 60H | D1 | Noise Killer det. output (1: Noise Killer ON) |
| MV_180 | 1 | 60H | D2 | Reversed Burst signal (all reversed) det. output (1: Reversed Burst) |
| IIC_STILL | 1 | 60H | D3 | VCR Still mode det. output (1: Still mode) |
| B_W | 1 | 60H | D4 | PLL Killer (Chroma) det. output (1: PLL Killer ON) |
| V COINCI | 1 | 60H | D5 | Vertical Coincidence det. output (1: V Coincident) |
| H COINCI | 1 | 60H | D6 | Horizontal Coincidence det. output (1: H Coincident) |
| KILLER | 1 | 60H | D7 | Color/Killer condition (1: color output, 0: Killer (color off)) |
| B2ROM | 9 | 61H | D0-D7 | B2ROM output |
| | | 62H | D7 | |
| C Gain | 2 | 62H | D0-D1 | ACC amplifier status |
| BLKDETV | 4 | 63H | D4-D7 | Black det. output of Black Stretch circuit |

Preliminary

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Mitsubishi Semiconductor<Digital IC>

M65580MAP-XXXFP

Digital Video/Chroma/Deflection+MCU

M65580MAP I²C bus Standard data

| Sub address | data | Sub address | data | Sub address | data |
|-------------|------|-------------|------|-------------|------|
| 00h | 00 | 30h | 20 | 50h | 00 |
| 01h | 08 | 31h | 05 | 51h | 00 |
| 02h | 08 | 32h | 04 | 52h | 00 |
| 03h | 21 | 33h | 81 | 53h | 35 |
| 04h | C0 | 34h | 8D | 54h | 22 |
| 05h | C0 | 35h | 63 | 55h | 94 |
| 06h | 00 | 36h | 79 | 56h | 14 |
| 07h | 15 | 37h | 50 | 57h | A6 |
| 08h | 40 | 38h | 55 | 58h | 00 |
| 09h | 40 | 39h | 25 | 59h | A6 |
| 0Ah | 40 | 3Ah | 21 | 5Ah | 00 |
| 0Bh | 1E | 3Bh | 19 | 5Bh | 00 |
| 0Ch | 9E | 3Ch | B3 | 5Ch | 00 |
| 0Dh | 1E | 3Dh | 0F | 5Dh | 80 |
| 0Eh | 80 | 3Eh | 06 | | |
| 0Fh | 10 | 3Fh | 08 | | |
| 10h | 10 | 40h | 00 | | |
| 11h | 4A | 41h | 01 | | |
| 12h | 8D | 42h | C0 | | |
| 13h | 00 | 43h | 04 | | |
| 14h | 40 | 44h | 64 | | |
| 15h | 40 | 45h | 3D | | |
| 16h | 00 | 46h | 15 | | |
| 17h | C0 | 47h | 00 | | |
| 18h | 00 | 48h | 83 | | |
| 19h | C0 | 49h | 00 | | |
| 1Ah | 00 | 4Ah | A0 | | |
| 1Bh | C0 | 4Bh | 00 | | |
| 1Ch | 00 | 4Ch | 15 | | |
| 1Dh | 00 | 4Dh | 01 | | |
| | | 4Eh | 6E | | |
| | | 4Fh | 38 | | |

Preliminary

Note : This is not a final specification.


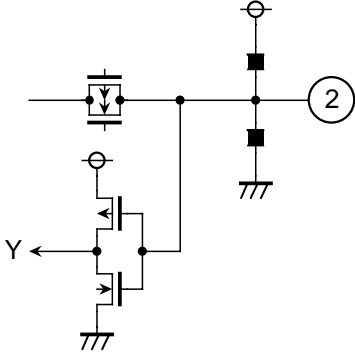

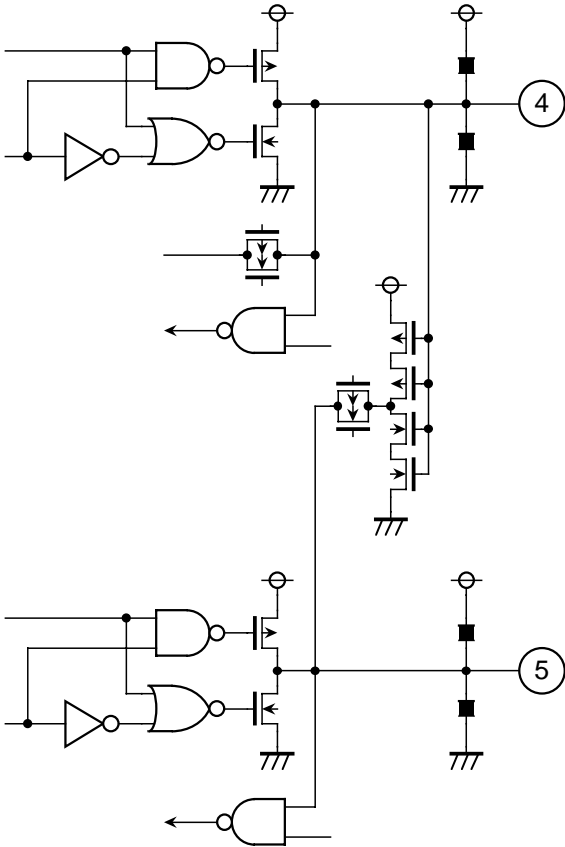
Some of information in this document are subject to changes.

Mitsubishi Semiconductor<Digital IC>

M65580MAP-XXXFP

Digital Video/Chroma/Deflection+MCU

DESCRIPTION OF PIN

| Pin No. | Name | Peripheral circuit of pins | Note |
|---------|---------------------------------|--|--|
| 1 | Vss (MCU) |  | Power source for MCU. 0V |
| 2 | FILT |  | |
| 3 | Vcc (MCU) |  | Power source for MCU. 5.0V ± 5% |
| 4 5 | P27/XCOUT P26/FSCIN/ XCIN |  | |

Preliminary

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| Pin No. | Name | Peripheral circuit of pins | Note |
|-------------------|---|----------------------------|--|
| 6 | RESETB | | CMOS INPUT (Impedance > 100kΩ) VOL = 0V : Reset state VOH = 5V : Release from Reset state |
| 7 8 9 10 | P22/SIN/AD8 P21/SOUT/AD8 P20/SCLK/AD6 P15/AD1/ INT3/FSCIN | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |
| 11 | P16/AD2/TIM2 | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) Intelligent monitor output (Analog/Digital) |
| 12 | Vss (Digital) | | 0V |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|---------|---------------|----------------------------|---|
| 13 | OSD CLK | | CMOS IN/OUT 1 (Impedance > 100kΩ (input)) (Impedance < 100Ω (output)) |
| 14 | Vdd (Digital) | | Power source for Digital block. 5.0V ± 5% |
| 15 | CLK OUT | | Impedance ≈ 400Ω |
| 16 | RESET | | CMOS INPUT (Impedance > 100kΩ) V _{IL} = 0V : Reset state V _{IH} = 5V : Release from Reset state |
| 17 | C.Sync IN | | Sync Sep. input Impedance = N.A. DC 2.5V |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|----------------|-------------------------------------|----------------------------|---|
| 18 | CVBS OUT | | Impedance \approx 150 Ω DC : 0.55V (sync) AC : 1.75V _{p-p} (typ.) |
| 19 | Vdd (Input) | _____ | Power source for A/D etc. 3.3V \pm 5% |
| 20 22 26 | EXT(CVBS) IN Y IN TV(CVBS) IN | | Impedance=N.A. DC : 0.5V (sync) AC : 1.0V _{p-p} (typ.) |
| 21 | Vss (Input) | _____ | Power source for A/D etc. 0V |
| 23 25 | VRT VRB | | Impedance $>$ 50 Ω DC : 1.7V (VRT) 0.5V (VRB) |
| 24 | C IN | | Impedance \approx 7.5k Ω DC : 1.0V AC : 0.286V _{p-p} (burst) |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|----------------|-------------------------|----------------------------|---|
| 27 | VZ OUT | | Impedance \approx 400 Ω DC : 2.05V |
| 28 30 32 | R OUT G OUT B OUT | | Impedance \approx 1k Ω DC : 3V (blanking) |
| 29 | Vdd (Output) | _____ | Power source for D/A etc. 3.3V \pm 5% |
| 31 | Vss (Output) | _____ | Power source for D/A etc. 0V |
| 33 | Vdd (VCXO) | _____ | Power source for VCXO etc. 5.0V \pm 5% |
| 34 | APC Filter | | Impedance=N.A. (Additional filter on PCB board) DC 2.9V |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|---------|-----------------|----------------------------|---|
| 35 | X'tal | | Impedance \approx 1k Ω |
| 36 | X-ray Protector | | Impedance $>$ 100k Ω 0.0-3.0 : Normal 3.2-3.3 : Hold down 3.7-5.0 : Shut down |
| 37 | AFC1 Filter | | Impedance=N.A. (Additional filter on PCB board) DC 2.5V |
| 38 | V RAMP OUT | | Impedance \approx 400 Ω 2.5V _{p-p} (typ.) |
| 39 | HVCO F/B | | Impedance=N.A. (Additional filter on PCB board) DC 3.0V |
| 40 | Neck Protector | | Impedance \approx 5k Ω 0.0-1.0 : RGB off 1.6-3.0 : Normal 4.0-5.0 : Test mode |

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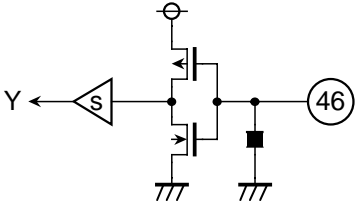
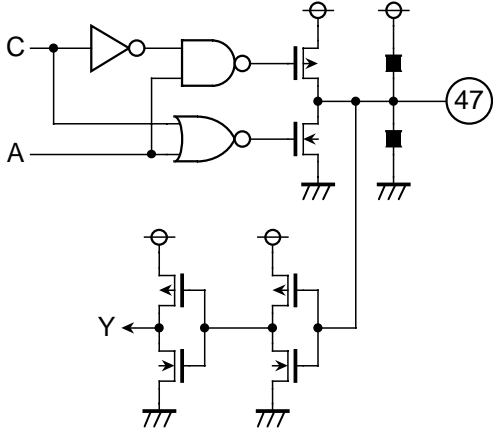
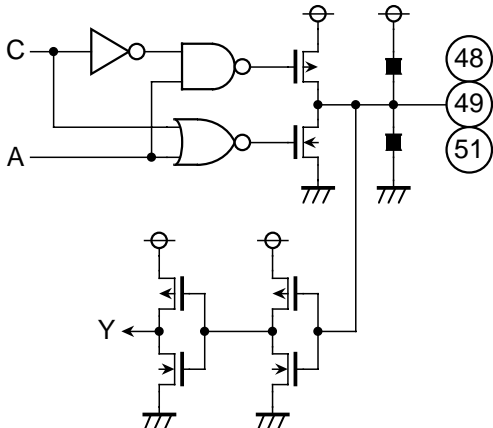
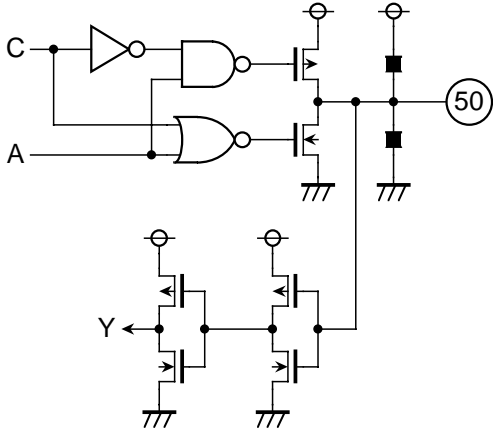
| Pin No. | Name | Peripheral circuit of pins | Note |
|---------|-----------|----------------------------|---|
| 41 | Vss (DEF) | | Power source for Deflection block. 0V |
| 42 | Vdd (DEF) | | Power source for Deflection block. 5.0V ± 5% |
| 43 | FBP IN | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) V _{IL} = 0V : RGB output V _{IH} = 5V : Blanking |
| 44 | H OUT | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) V _{OL} : 0V V _{OH} : 5V |
| 45 | SDA | | CMOS IN/OUT 2 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) V _{IL} : 0V V _{IH} : 5V |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|----------------|-------------------------------------|--|---|
| 46 | SCL |  | CMOS Schmitt IN (Impedance > 100kΩ) V _{IL} : 0V V _{IH} : 5V |
| 47 | Half Tone IN |  | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) V _{IL} = 0V : RGB output V _{IH} = 5V : Half tone on |
| 48 49 51 | OSD(B) IN OSD(G) IN OSD(R) IN |  | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) V _{IL} : 0V V _{IH} : 5V |
| 50 | Fast BLK IN |  | CMOS IN/OUT 1 Impedance > 100kΩ (input) Impedance < 100Ω (output) V _{IL} = 0V : RGB output V _{IH} = 5V : OSD output |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|----------------------------|---|----------------------------|---|
| 52 | V sync OUT | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) VOL : 0V VOH : 5V |
| 53 | H sync OUT | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) VOL : 0V VOH : 5V |
| 54 | P51/VSYNCR | | CMOS INPUT (Impedance > 100kΩ) |
| 55 56 57 58 59 | P52/R P53/OUT1 P30/G P31/B P10/OUT2 | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|----------------------------|--|----------------------------|---|
| 60 61 62 63 | P11/SCL1 P12/SCL2 P13/SDA1 P14/SDA2 | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |
| 64 65 66 67 68 | P00/PWM0 P01/PWM1 P02/PWM2 P03/PWM3 P04/PWM4 | | CMOS IN/OUT (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |
| 69 70 | P05/AD3 P06/INT2/AD4 | | CMOS IN/OUT (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |
| 71 | P07/INT1 | | CMOS IN/OUT (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |

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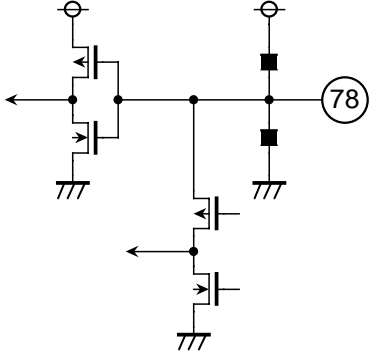
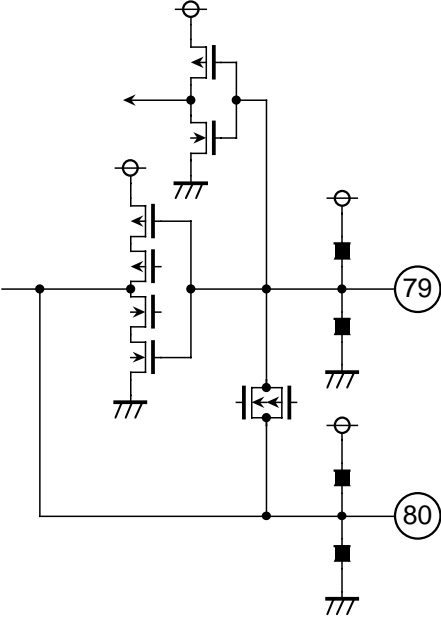
| Pin No. | Name | Peripheral circuit of pins | Note |
|----------|----------------------|----------------------------|--|
| 72 73 | P23/TIM3 P24/TIM2 | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance < 100Ω (output)) |
| 74 | P25/AD5 | | CMOS IN/OUT 1 (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |
| 75 | HLF | | Impedance = N.A. (Additional filter on PCB board) |
| 76 | VHOLD | | |
| 77 | CV IN | | |

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| Pin No. | Name | Peripheral circuit of pins | Note |
|----------|---------------|---|--|
| 78 | CN VSS |  | CMOS IN/OUT (Impedance > 100kΩ (input) Impedance ≈ 250Ω (output)) |
| 79 80 | X IN X OUT |  | |
| | | | |

MEMORY MAP

