M64898GP

PLL FREQUENCY SYNTHESIZER WITH DC-DC CONVERTER FOR PC

DESCRIPTION

The M64898GP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR /PC.

It contains the prescaler with operating up to1.3GHz,4 band drivers and DC-DC converter for Tuning voltage.

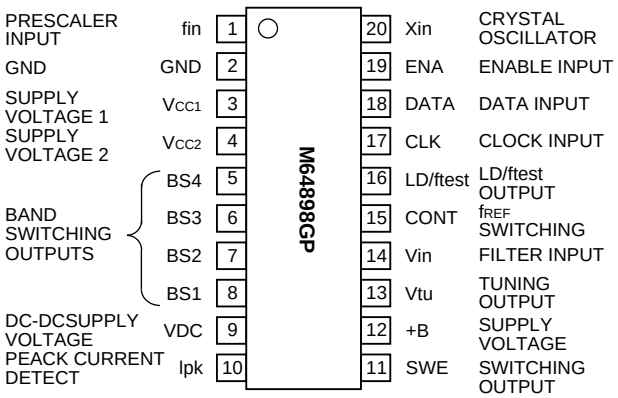
FEATURES

- Built-in DC-DC converter for Tuning voltage
- 4 integrated PNP band drivers (Io=30mA, Vsat=0.2V typ@V_{CC1} to 10V)
- Built-in prescaler with input amplifier (max=1.3GHz)
- PLL lock/unlock status display out put (Built-in pull up resistor)
- X'tal 4MHz is used to realize 3 type of tuning steps (Divider ratio 1/512, 1/640, 1/1024)
- Software compatible with M64892/M64893
- Automatick switching of tuning step according to the number of data bits (62.5kHz at 18bits , 32.25kHz at 19bits)
- Built-in Power on reset system
- Small Package(SSOP)

APPLICATION

PC, TV, VCR tuners

PIN CONFIGURATION (TOP VIEW)



Outline 20P2E-A

RECOMMENDED OPERATING CONDITION

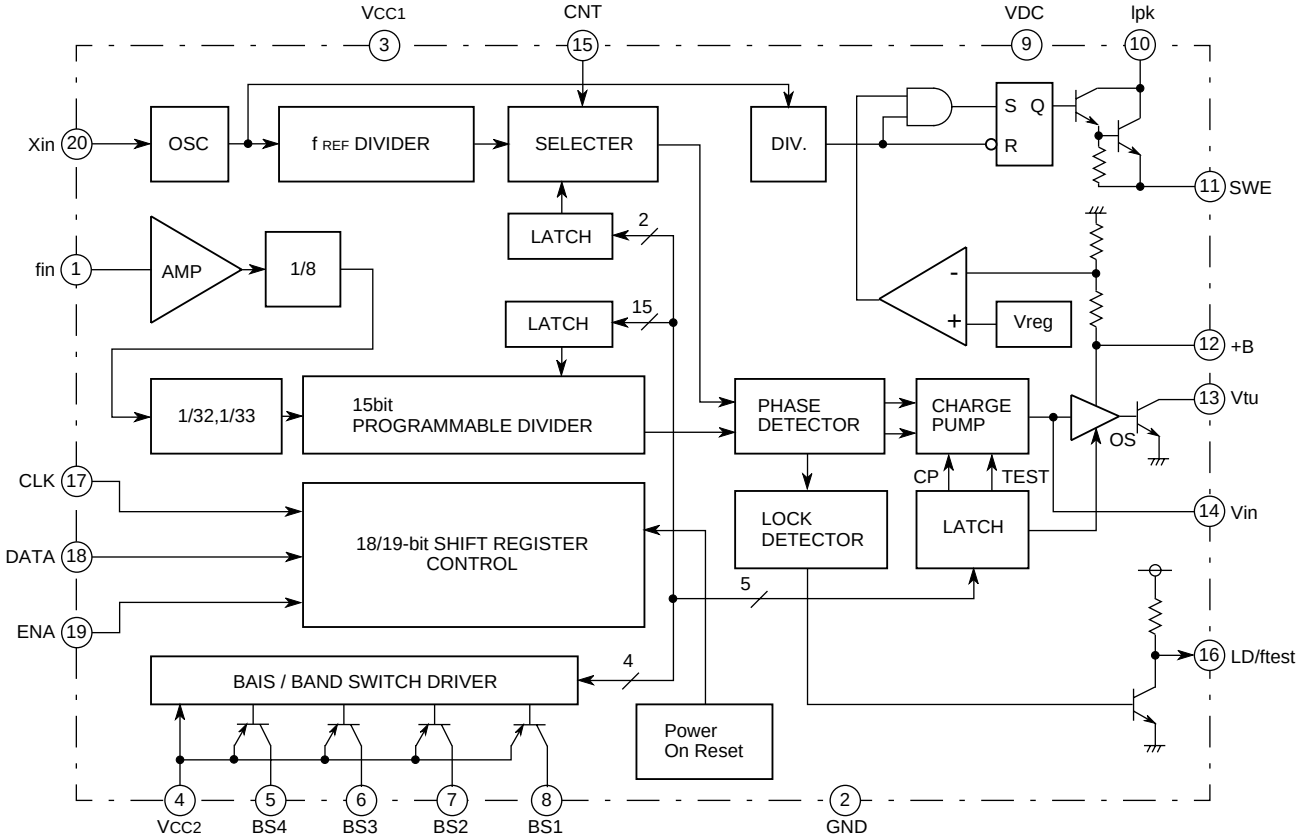
Supply voltage range.....V_{CC1}=4.5 to 5.5V

V_{CC2}=V_{CC1} to 10V

Rated supply voltage.....V_{CC1}=5V

V_{CC2}=V_{CC1}

BLOCK DIAGRAM



DESCRIPTION OF PIN

Pin No.	Symbol	Pin name	Function
1	f in	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	V_{CC1}	Power supply voltage 1	Power supply voltage terminal. 5.0V±0.5V
4	V_{CC2}	Power supply voltage 2	Power supply for band switching, V_{CC1} to 10V
5	BS4	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
6	BS3		
7	BS2		
8	BS1		
9	VDC	DC-DC power supply voltage	DC-DC power supply voltage terminal. 5.0V±0.5V
10	Ipk	Peack current detect	When potential difference with VDC terminal becomes more than 0.33V by current limiting detector of DC-DC converter, the listing rises with off.
11	SWE	Switching output	DC-DC converter oscillator output.
12	+B	Power supply voltage	Power supply voltage for turning voltage.
13	Vtu	Tuning output	This supplies the tuning voltage.
14	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (f_{REF}), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
15	LD/ftest	Lock detect /Test port	Lock detector output. When loop of phase locked loop locked it, it rises with "H" level in "L" level or unlock. In control byte data input, the programmabule freq. divider output and reference freq. output is selected by the test mode.
16	CONT	f_{REF} Switchi	Set up reference frequency divider ratio. In "L" level, set it up in 1/640(19Bit) in setting "opening" in 1/1024(19Bit) or 1/512 (18Bit).
17	CLOCK	Clock input	Data is read into the shift register when the clock signal falls.
18	DATA	Data input	Input for band SW and programmable freq. divider set up.
19	ENABLE	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the enable signal after the 18th signal of the clock signal falls or when the 19th pulse of the clock signal falls.
20	X in	This is connected to the crystal oscillator.	4.0MHz crystal oscillator is connected.

ABSOLUTE MAXIMUM RATINGS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1	Pin3	6.0	V
V_{CC2}	Supply voltage 2	Pin4	10.8	V
V_I	Input voltage	Not to exceed V_{CC1}	6.0	V
V_O	Output voltage	f_{REF} output	6.0	V
V_{BSOFF}	Voltage applied when the band output is OFF		10.8	V
I_{BSON}	Band output current	per 1 band output circuit	40.0	mA
t_{BSON}	ON the time when the band output is ON	40mA per 1 band output circuit 3circuits are pn at same time,	10	sec
P_d	Power dissipation	Ta=75°C	255	mW
T_{opr}	Operating temperature		-20 to +75	°C
T_{stg}	Storage temperature		-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1	Pin3	4.5 to 5.5	V
V_{CC2}	Supply voltage 2	Pin4	V_{CC1} to 10.0	V
f_{opr1}	Operating frequency (1)	Crystal oscillation circuit	4.0	V
f_{opr2}	Operating frequency (2)		80 to 1300	MHz
I_{BDL}	Band output current 5 to 8	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 30	mA

ELECTRICAL CHARACTERISTICS (Ta=-20°C to +75°C, unless otherwise noted, V_{CC1}=5.0V, V_{CC2}=9.0V)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	Input terminals	"H" input voltage	17 to 19		3.0	–	V_{CC1}+0.3	V
V_{IL1}		"L" input voltage	15		–	–	0.4	V
V_{IL2}		"L" input voltage	17 to 19		–	–	1.5	V
I_{IH}		"H" input current	17 to 19	V_{CC1}=5.5V, Vi=4.0V	–	–	10	µA
I_{IL1}		"L" input current	15	V_{CC1}=5.5V, Vi=0V	–	-50	-80	µA
I_{IL2}		"L" input current	17, 19	V_{CC1}=5.5V, Vi=0.5V	–	-6	-10	µA
I_{IL3}		"L" input current	18	V_{CC1}=5.5V, Vi=0.5V	–	-18	-30	µA
V_{OH}	Lock output	"H" output voltage	16	V_{CC1}=5.5V	5.0	–	–	V
V_{OL}		"L" output voltage	16	V_{CC1}=5.5V	–	0.3	0.5	V
V_{BS}	Band SW	Output voltage	5 to 8	V_{CC2}=9V, Io=-30mA	11.6	11.8	-	V
I_{olk1}		Leak current	5 to 8	V_{CC2}=9V, Band SW is OFF Vo=0V	–	–	-10	µA
V_{toH}	Tuning output	Output voltage "H"	13	+B=31V	30.5	–	–	V
V_{toL}		Output voltage "L"	13	+B=31V	–	0.2	0.4	V
I_{cpo}	Charge pump	"H" output current	14	V_{CC1}=5.0V, Vo=2.5V	–	±270	±370	µA
I_{cpLK}		Leak current	14	V_{CC1}=5.0V, Vo=2.5V	–	–	±50	nA
I_{CC1}	Supply current 1		3	V_{CC1}=5.5V	–	20	30	mA
I_{CC2A}	Supply current 2	4 circuits OFF	4	V_{CC2}=9V	–	–	0.3	mA
I_{CC2B}		1 circuits ON, Output open	4	V_{CC2}=9V	–	4.0	6.0	mA
I_{CC2C}		Output current 30mA	4	V_{CC2}=9V, Io=-30mA	–	34.0	36.0	mA
DC-DC Converter								
I_{CCdc}	Supply current (action)		9	V_{CC1}=5.5V	–	1.3	3.0	mA
V_{do}	Output voltage		12	V_{CC1}=5.5V	28	31	35	V
f_{OSC}	OSC frequency		11	V_{CC1}=5.5V	–	571	–	kHz
V_{ipk}	Current limit detect voltage		10	V_{CC1}=5.5V	–	330	–	mV

The typical values are at V_{CC1}=5.0V, V_{CC2}=9.0V, Ta=+25°C.

SWITCHING CHARACTERISTICS (Ta=-20°C to +75°C, unless otherwise noted, V_{CC1}=5.0V, V_{CC2}=9.0V)

Symbol	Parameter	Test pin	Test conditions		Limits			Unit
					Min.	Typ.	Max.	
f_{opr}	Prescaler operating frequency	1	V_{CC1}=4.5 to 5.5V Vin=Vinmin to Vinmax		80	–	1300	MHz
Vin	Operating input voltage	1	V_{CC1}=4.5 to 5.5V	80 to 100MHz	-24	–	4	dBm
				100 to 950MHz	-27	–	4	
				950 to 1300MHz	-15	–	4	
t_{PWC}	Clock pulse width	17	V_{CC1}=4.5 to 5.5V		1	–	–	µs
$t_{SU\ (D)}$	Data setup time	18	V_{CC1}=4.5 to 5.5V		2	–	–	µs
$t_{H\ (D)}$	Data hold time	18	V_{CC1}=4.5 to 5.5V		1	–	–	µs
$t_{SU\ (E)}$	Enable setup time	18	V_{CC1}=4.5 to 5.5V		3	–	–	µs
$t_{H\ (E)}$	Enable hold time	18	V_{CC1}=4.5 to 5.5V		3	–	–	µs
t_{INT}	Enable data interval time	19, 18	V_{CC1}=4.5 to 5.5V		1	–	–	µs
t_r	Rise time	17, 18, 19	V_{CC1}=4.5 to 5.5V		–	–	1	µs
t_f	Fall time	17, 18, 19	V_{CC1}=4.5 to 5.5V		–	–	1	µs
tBT	Next enable prohibit time	19	V_{CC1}=4.5 to 5.5V		5	–	–	µs
tBCL	Next clock prohibit time	17, 19	V_{CC1}=4.5 to 5.5V		5	–	–	µs

METHOD OF SETTING DATA

The programmable divider ratio uses 15bits. Setting up the band switching output uses 4bits.

The test mode data uses 8bits. The total bits used is 27bits. Data is read in when the enable signal is "H" and the clock signal falls.

The band switching data is read in at the 4th pulse of the clock signal. The programmable counter data is read into the latch by the fall of the enable signal after the 18th pulse of the clock signal or the fall of the 19th pulse of the clock signal. When the enable signal goes to "L" before the 18th pulse of the enable signal, only the band SW data is updated and other data is ignored.

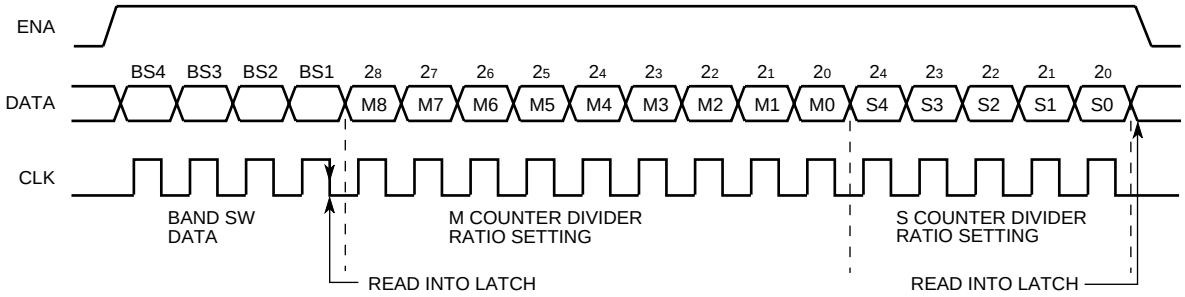
Automatic judgment facility comes being it, and, as for Shift resister, CONT terminal rises by 18/19 bits at the time of "L". At the time of data of 18 bits, M9 bit of Programable divider is done reset of, and it is established in reference frequency divider ratio 1/512.

At the time of 19 bits,reference frequency divider ratio is established in 1/1024.

When reference frequency divider ratio was established in 1/640 by 19 bits at the time of "opening" CONT terminal, and it became "L" before 19 pulse enable signal, only band SW data are renewed, and other data are ignored.

(1) Transfer of the 18th bit data (CONT terminal is "L")

Data is latched by the fall of the enable signal after the 18th clock signal. At this time, the divider of the 1/512 of the reference frequency is used.



(2) Transfer of the 19th bit data (CONT terminal is "L" or "open")

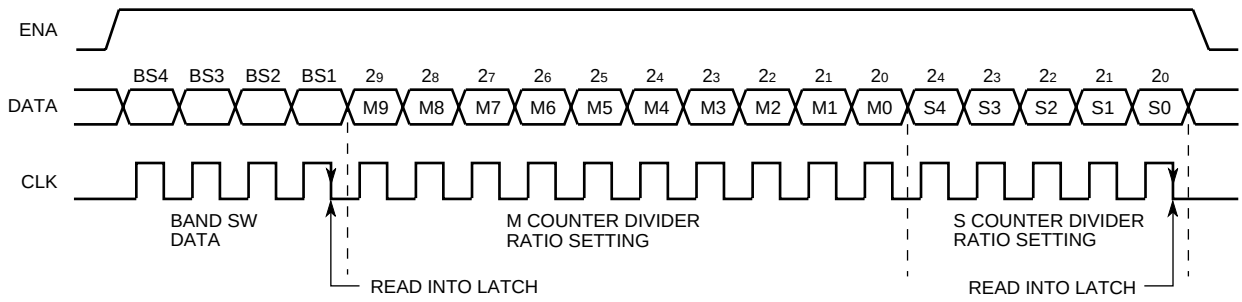
The data is latched at the 19th pulse of the clock signal.

Reference frequency divider ratio is established in 1/1024 in case of "L" CONT terminal at this time.

Reference frequency divider ratio is established in 1/640 in case of "opening" CONT terminal.

Invalid the clock signal after 19th pulse.

Notice) When CONT terminal is "L", to change reference frequency, set up as ENA in "L" after 19th pulse of clock signal by all means.



HOW TO SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER

(1) Transfer of the 18th bit data (CONT terminal is "L")

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

N=8 • (32M+S) M : 9 bit main counter divider

S : 5 bit swallow counter divider

The M and S counters are binary the possible ranges of divider are as follows.

32≤M≤511

0≤S≤31

Therefore, the range of divider N is 8,192 to 131,064.

The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO}=f_{REF}\times N$

$=7.8125\times 8\times(32M+S)$

$=62.5\times(32M+S)$ [kHz]

Therefore, the tuning frequency range is 64MHz to 1023.9375MHz.

(2) Transfer of the 19th bit data (CONT terminal is "L")

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

N=8 • (32M+S) M : 10 bit main counter divider

S : 5 bit swallow counter divider

The M and S counters are binary the possible ranges of divider are as follows.

32≤M≤1023

0≤S≤31

Therefore, the range of divider N is 8,192 to 262,136.

The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO}=f_{REF}\times N$

$=3.90625\times 8\times(32M+S)$

$=31.25\times(32M+S)$ [kHz]

Therefore, the tuning frequency range is 32MHz to 1023.96875 MHz.

(3) Transfer of the 19th bit data (CONT terminal is "open")

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

N=8 • (32M+S) M : 10 bit main counter divider

S : 5 bit swallow counter divider

The M and S counters are binary the possible ranges of divider are as follows.

32≤M≤1023

0≤S≤31

Therefore, the range of divider N is 8,192 to 262,136.

The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO}=f_{REF}\times N$

$=6.25\times 8\times(32M+S)$

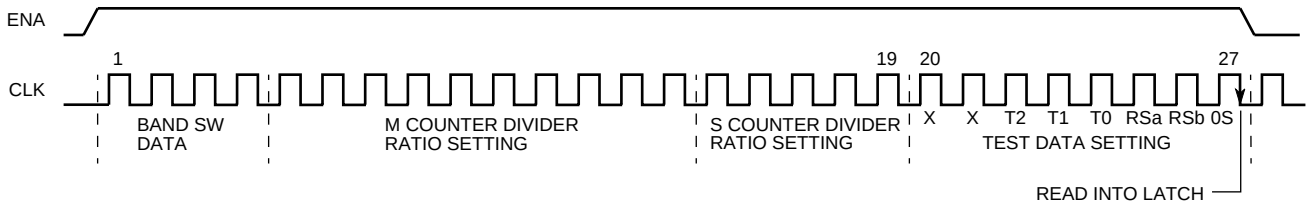
$=50.0\times(32M+S)$ [kHz]

But, the tuning frequency range is 51.2MHz to 1300MHz from the maxmum prescaler operating frequency.

TEST MODE DATA SET UP METHOD

The data for the test mode uses 20 to 27bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27 bit data



(2) Test Mode Bit Set Up

X :Random, 0 or 1.normal "0"

T0, T1,&T2 :Set up test modes

RSa, Rsa :Set the frequency divider of the reference frequency

OS :Set up the tuning amplifier

Setting up for the test mode

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	f_{REF}	Test mode
1	0	1	High impedance	f1/N	Test mode

Set up for the reference Frequency divider ratio

RSa	RSb	Divider ratio
1	1	1/512
0	1	1/1024
X	0	1/640

Set up the tuning amplifier

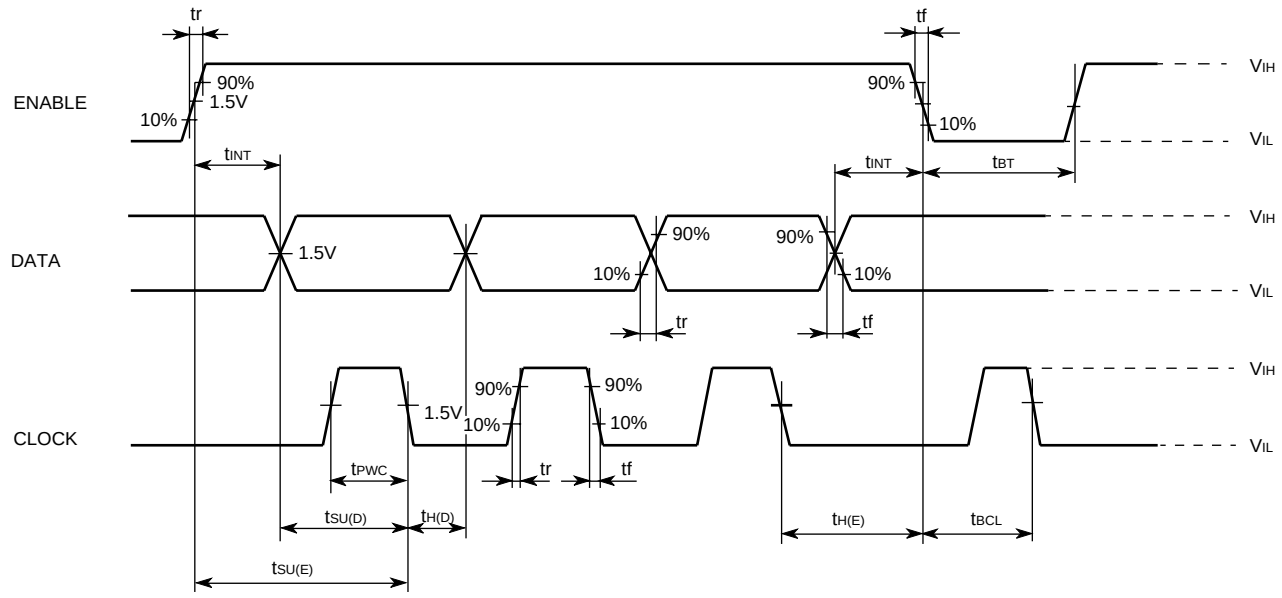
OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

Power on reset operation (Initial state the power is turned ON)

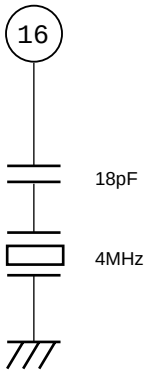
BS4 to BS1 : OFF
Charge pump : High impedance
Tuning amplifier : OFF
Charge pump current : 270µA ∗
Frequency divider ratio : 1/1024
Lock detect : H

∗ Charge pump current is replaced by 70µA when locks it by automatic change facility.

TIMING DIAGRAM



CRYSTAL OSCILLATOR CONNECTION DIAGRAM



Crystal oscillator characteristics
Actual resistance : less then 300Ω
Load capacitance : 20pF

APPLICATION EXAMPLE