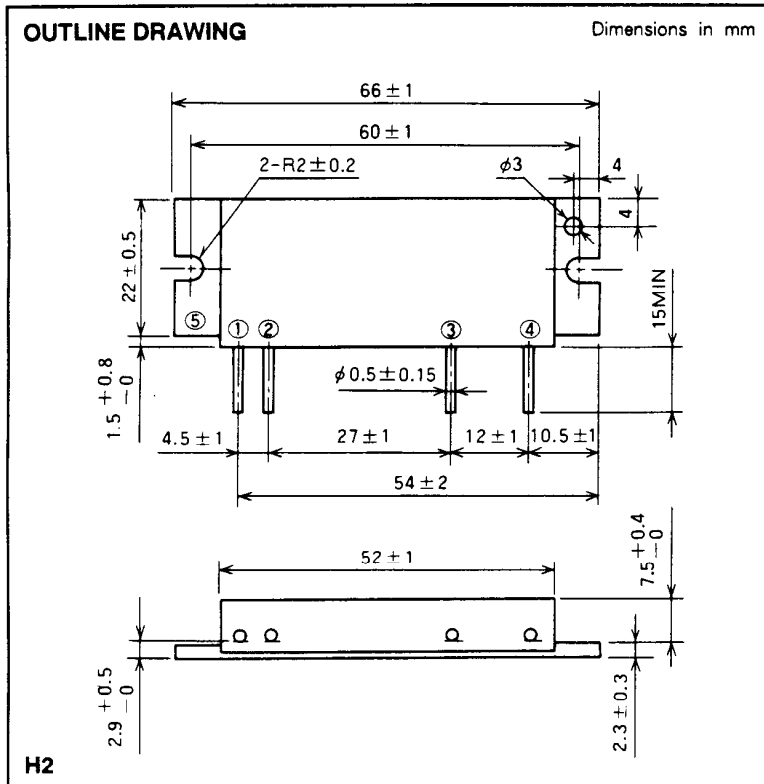
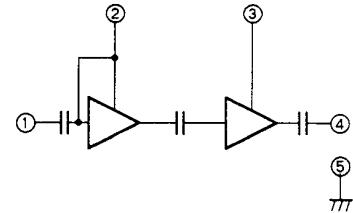


M57737

144-148MHz, 12.5V, 30W, FM MOBILE RADIO



BLOCK DIAGRAM



- PIN :
- ① Pin : RF INPUT
 - ② Vcc1 : 1st. DC SUPPLY
 - ③ Vcc2 : 2nd. DC SUPPLY
 - ④ Po : RF OUTPUT
 - ⑤ GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		17	V
Icc	Total current		7	A
Pin(max)	Input power	ZG = ZL = 50 Ω	0.4	W
Po(max)	Output power	ZG = ZL = 50 Ω	40	W
Tc(OP)	Operation case temperature		- 30 to 110	°C
Tstg	Storage temperature		- 40 to 110	°C

Note. Above parameters are guaranteed independently.

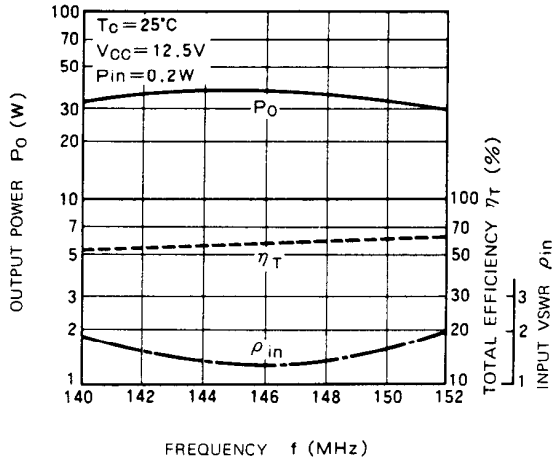
ELECTRICAL CHARACTERISTICS (Tc = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	Pin = 0.2W Vcc = 12.5V ZG = ZL = 50 Ω	144	148	MHz
Po	Output power		30		W
ηT	Total efficiency		45		%
2fo	2nd. harmonic			- 25	dBc
3fo	3rd. harmonic			- 30	dBc
ρin	Input VSWR			2.8	-
-	Load VSWR tolerance	Vcc = 15.2V, Po = 35W (Pin : controlled) Load VSWR=20:1 (All phase), 5sec. ZG = 50Ω	No degradation or destroy		-

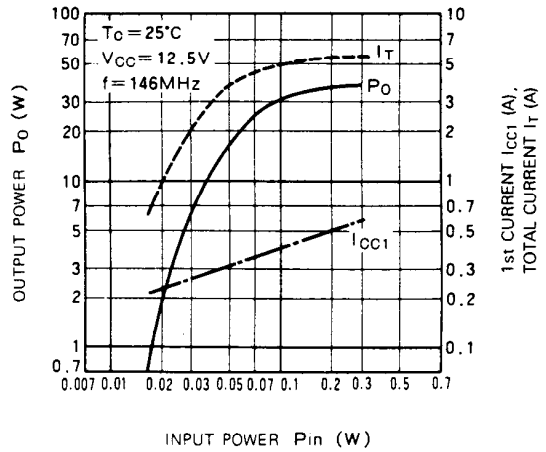
Note. Above parameters, ratings, limits and conditions are subject to change.

TYPICAL PERFORMANCE DATA

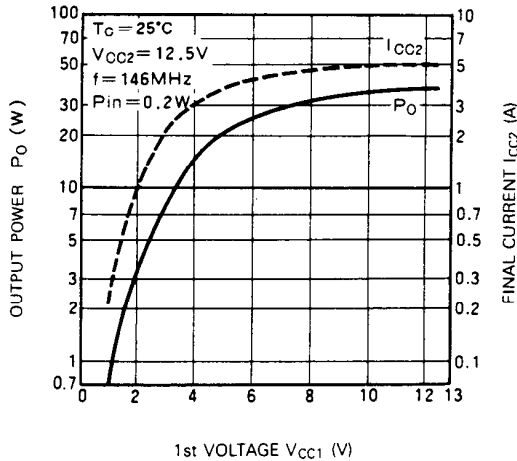
OUTPUT POWER, TOTAL EFFICIENCY, INPUT VSWR VS. FREQUENCY



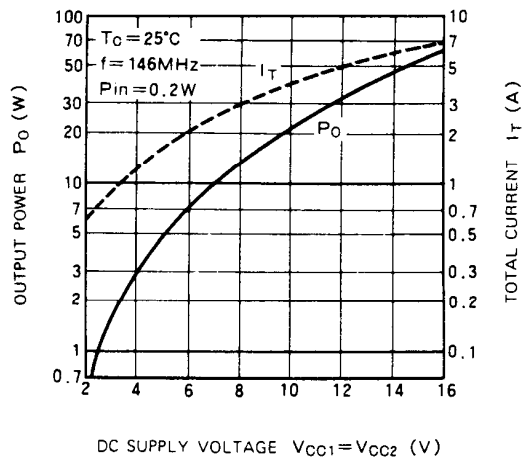
OUTPUT POWER, 1st CURRENT TOTAL CURRENT VS. INPUT POWER



OUTPUT POWER, FINAL CURRENT VS. 1st VOLTAGE

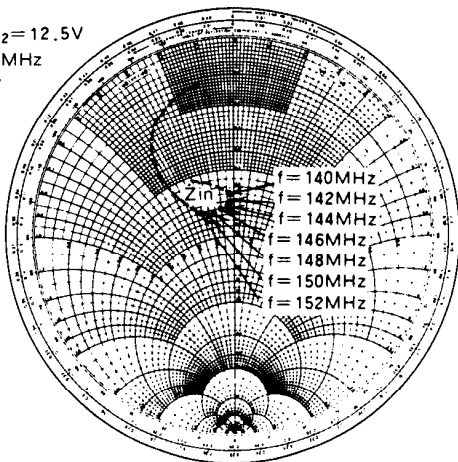


OUTPUT POWER, TOTAL CURRENT VS. DC SUPPLY VOLTAGE



INPUT IMPEDANCE VS. FREQUENCY

$T_c = 25^\circ\text{C}$
 $V_{CC1} = V_{CC2} = 12.5\text{V}$
 $f = 144\text{-}148\text{MHz}$
 $P_{in} = 0.2\text{W}$
 $Z_l = 50\ \Omega$



DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to following consideration when designing heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistance between junction and package of incorporated transistors.

a) First stage transistor

$$R_{th(j-c)1} = 8^{\circ}\text{C/W (Typ.)}$$

b) Second stage transistor

$$R_{th(j-c)2} = 2^{\circ}\text{C/W (Typ.)}$$

(2) Junction temperature of incorporated transistors at standard operation.

- Conditions for standard operation.

$P_o = 28\text{W}$, $V_{CC} = 12.5\text{V}$, $P_{in} = 0.2\text{W}$, $\eta_T = 45\%$ (minimum rating), $P_{O1}(\text{Note 1}) = 5\text{W}$, $I_T = 5.0\text{A}$ ($I_{T1}^{(2)} = 0.9\text{A}$, $I_{T2}^{(3)} = 4.1\text{A}$)

DES Note 1: Output power of the first stage transistor

Note 2: Circuit current of the first stage transistor

Note 3: Circuit current of the final stage transistor

- Junction temperature of the first stage transistor

$$\begin{aligned} T_{j1} &= (V_{CC} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_c^{(4)} \\ &= (12.5 \times 0.9 - 5 + 0.2) \times 8 + T_c \\ &= 52 + T_c \text{ (}^{\circ}\text{C)} \end{aligned}$$

Note 4: Package temperature of device

- Junction temperature of the final stage transistor

$$\begin{aligned} T_{j2} &= (V_{CC} \times I_{T2} - P_o + P_{O1}) \times R_{th(j-c)2} + T_c \\ &= (12.5 \times 4.1 - 28 + 5) \times 2 + T_c \\ &= 57 + T_c \text{ (}^{\circ}\text{C)} \end{aligned}$$

2. Heat sink design;

In thermal design of heat sink, try to keep the package temperature at the upper limit of the operating ambient temperature (normally $T_a = 60^{\circ}\text{C}$) and at the output power of 28W below 90°C .

The thermal resistance $R_{th(c-a)}^{(5)}$ of the heat sink to realize this:

$$\begin{aligned} R_{th(c-a)} &= \frac{T_c - T_a}{(P_o/\eta_T) - P_o + P_{in}} = \frac{90 - 60}{(28/0.45) - 28 + 0.2} \\ &= 0.87 \text{ (}^{\circ}\text{C/W)} \end{aligned}$$

Note 5: Inclusive of the contact thermal resistance between device and heat sink

Mounting the heat sink of the above thermal resistance on the device,

$$T_{j1} = 142^{\circ}\text{C}, T_{j2} = 147^{\circ}\text{C} \text{ at } T_a = 60^{\circ}\text{C}, T_c = 90^{\circ}\text{C}.$$

In the annual average of ambient temperature is 30°C ,

$$T_{j1} = 112^{\circ}\text{C}, T_{j2} = 118^{\circ}\text{C}$$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C , application under fully derated condition is ensured.