

FEATURES

- 5V and 3.3V power supplies required
- Also, supports LVPECL-to-PECL translation
- 500ps propagation delays
- Fully differential design
- Differential line receiver capability
- Application note
- Available in 20-pin SOIC package

DESCRIPTION

The SY100EL92 is a triple LVPECL-to-PECL or PECL-to-LVPECL translator. The device receives standard PECL signals and translates them to differential LVPECL output signals (or vice versa). SY100EL92 can also be used as a differential line receiver for PECL-to-PECL or LVPECL-to-LVPECL signals. However, please note that for the latter we will need two different power supplies. Please refer to Function Table for more details.

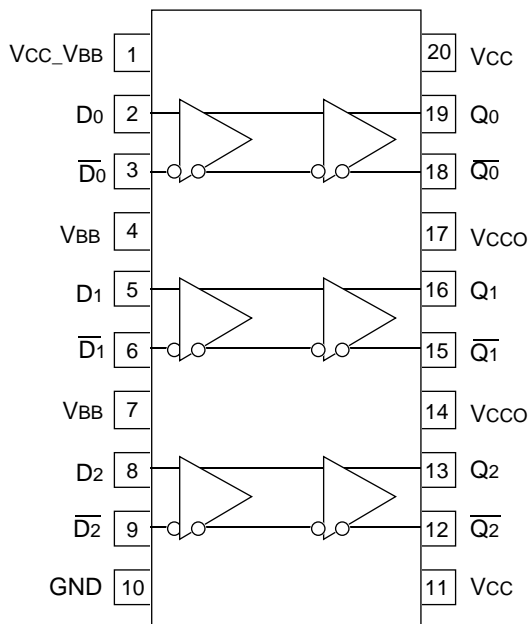
VBB outputs are provided for interfacing single ended input signals. If a single ended input is to be used, the VBB output should be connected to the \bar{D} input and the active signal will drive the D input. When used, the VBB should be bypassed to VCC via a 0.01 μ F capacitor. The VBB is designed to act as a switching reference for the SY100EL92 under single ended input conditions. As a result, the pin can only source/sink 0.5mA of current.

To accomplish the PECL-to-LVPECL level translation, the SY100EL92 requires three power rails. The VCC and VCC_VBB supply is to be connected to the standard PECL supply, the 3.3V supply is to be connected to the VCCO supply, and GND is connected to the system ground plane. Both the VCC and VCCO should be bypassed to ground with a 0.01 μ F capacitor.

To accomplish the LVPECL-to-PECL level translation, the SY100EL92 requires three power rails as well. The 5.0V supply is connected to the VCC and VCCO pins, 3.3V supply is connected to the VCC_VBB pin and GND is connected to the system ground plane. VCC_VBB is used to provide a proper VBB output level if a single ended input is used. For differential LVPECL input VCC_VBB can be either 3.3V or 5V.

Under open input conditions, the \bar{D} input will be biased at a VCC/2 voltage level and the D input will be pulled to GND. This condition will force the "Q" output low, ensuring stability.

PIN CONFIGURATION/BLOCK DIAGRAM



**SOIC
TOP VIEW**

FUNCTION TABLE

Function	Vcc	Vcco	Vcc_VBB
PECL-to-LVPECL	5.0V	3.3V	5.0V
LVPECL-to-PECL	5.0V	5.0V	3.3V
PECL-to-PECL	5.0V	5.0V	5.0V
LVPECL-to-LVPECL	5.0V	3.3V	3.3V

PIN NAMES

Pin	Function
Dn	PECL / LVPECL Inputs
Qn	PECL / LVPECL Outputs
VBB	PECL / LVPECL Reference Voltage Output
VCCO	Vcc for Output
VCC_VBB	Vcc for VBB Output
GND	Common Ground Rail
VCC	Vcc for Internal Circuitry

PECL INPUT DC ELECTRICAL CHARACTERISTICS

VCC_VBB = VCC = +4.5V to +5.5V; VCCO = +3.0V to +3.8V

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
VCC	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
VIH	Input HIGH Voltage ⁽¹⁾	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V
VIL	Input LOW Voltage ⁽¹⁾	3.190	—	3.515	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V
VPP	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I _{IL}	Input LOW Current	0.5 -600	— —	— —	0.5 -600	— —	— —	0.5 -600	— —	— —	0.5 -600	— —	— —	μA
V _{BB}	Output Reference ⁽¹⁾	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	V
I _{CC}	Power Supply Current	—	—	12	—	—	12	—	8.0	12	—	—	12	mA

NOTE:

1. These levels are for VCC_VBB = 5.0V. Level specifications will vary 1:1 with VCC_VBB.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

VCC_VBB = VCC = +4.5V to +5.5V; VCCO = +3.0V to +3.8V

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{CCO}	Power Supply Voltage	3.0	—	3.8	3.0	—	3.8	3.0	3.3	3.8	3.0	—	3.8	V
V _{OH}	Output HIGH Voltage ⁽¹⁾	2.215	—	2.420	2.275	—	2.420	2.275	2.350	2.420	2.275	—	2.420	V
V _{OL}	Output LOW Voltage ⁽¹⁾	1.470	—	1.745	1.490	—	1.680	1.490	1.600	1.680	1.490	—	1.680	V
I _{CCO}	Power Supply Current	—	—	20	—	—	20	—	15	20	—	—	21	mA

NOTE:

1. These levels are for V_{CCO} = 3.3V. Level specifications will vary 1:1 with V_{CCO}.

LVPECL INPUT DC ELECTRICAL CHARACTERISTICS

VCC_VBB = +3.0V to +3.8V⁽¹⁾; VCC = VCCO = +4.5V to +5.5V

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
VCC	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
VIH	Input HIGH Voltage ⁽²⁾	2.135	—	2.420	2.135	—	2.420	2.135	—	2.420	2.135	—	2.420	V
VIL	Input LOW Voltage ⁽²⁾	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	V
VPP	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	μA
I _{IL}	Input LOW Current	0.5 -600	— —	— —	0.5 -600	— —	— —	0.5 -600	— —	— —	0.5 -600	— —	— —	μA
V _{BB}	Output Reference ⁽²⁾	1.92	—	2.04	1.92	—	2.04	1.92	—	2.04	1.92	—	2.04	V
I _{CC}	Power Supply Current	—	—	12	—	—	12	—	8.0	12	—	—	12	mA

NOTES:

- VCC_VBB = 3.3V is only required for single-ended LVPECL input. For differential LVPECL input, VCC_VBB can be either 3.3V or 5V.
- These levels are for VCC_VBB = 3.3V. Level specifications will vary 1:1 with VCC_VBB.

PECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = +3.0V to +3.8V; V_{CC} = V_{CCO} = +4.5V to +5.5V

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{CCO}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V _{OH}	Output HIGH Voltage ⁽¹⁾	3.915	—	4.120	3.975	—	4.120	3.975	—	4.120	3.975	—	4.120	V
V _{OL}	Output LOW Voltage ⁽¹⁾	3.170	—	3.445	3.190	—	3.380	3.190	—	3.380	3.190	—	3.380	V
I _{CCO}	Power Supply Current	—	—	20	—	—	20	—	15	20	—	—	21	mA

NOTE:

1. These levels are for V_{CCO} = 5.0V. Level specifications will vary 1:1 with V_{CCO}.

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

Symbol	Parameter	T _A = -40°C			T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t _{PLH} t _{PHL}	Propagation Delay D to Q Diff. S.E.	430 410	520 540	630 710	430 410	520 540	630 710	430 410	520 540	630 710	430 410	520 540	630 710	ps
t _{skew}	Within-Device Skew Output-to-Output ⁽²⁾ Part-to-Part (Diff.) ⁽²⁾ Duty Cycle (Diff.) ⁽³⁾	— — —	20 20 25	100 200 —	— — —	20 20 25	100 200 —	— — —	20 20 25	100 200 —	— — —	20 20 25	100 200 —	ps
V _{PP}	Minimum Input Swing ⁽⁴⁾	150	—	—	150	—	—	150	—	—	150	—	—	mV
V _{CMR}	Common Mode Range ⁽⁵⁾ V _{PP} < 500mV V _{PP} ≥ 500mV	1.3 1.5	— —	V _{CC} -0.2 V _{CC} -0.2	1.2 1.4	— —	V _{CC} -0.2 V _{CC} -0.2	1.2 1.4	— —	V _{CC} -0.2 V _{CC} -0.2	1.2 1.4	— —	V _{CC} -0.2 V _{CC} -0.2	V
t _r t _f	Output Rise/Fall Times Q (20% to 80%)	320	—	580	320	—	580	320	—	580	320	—	580	ps

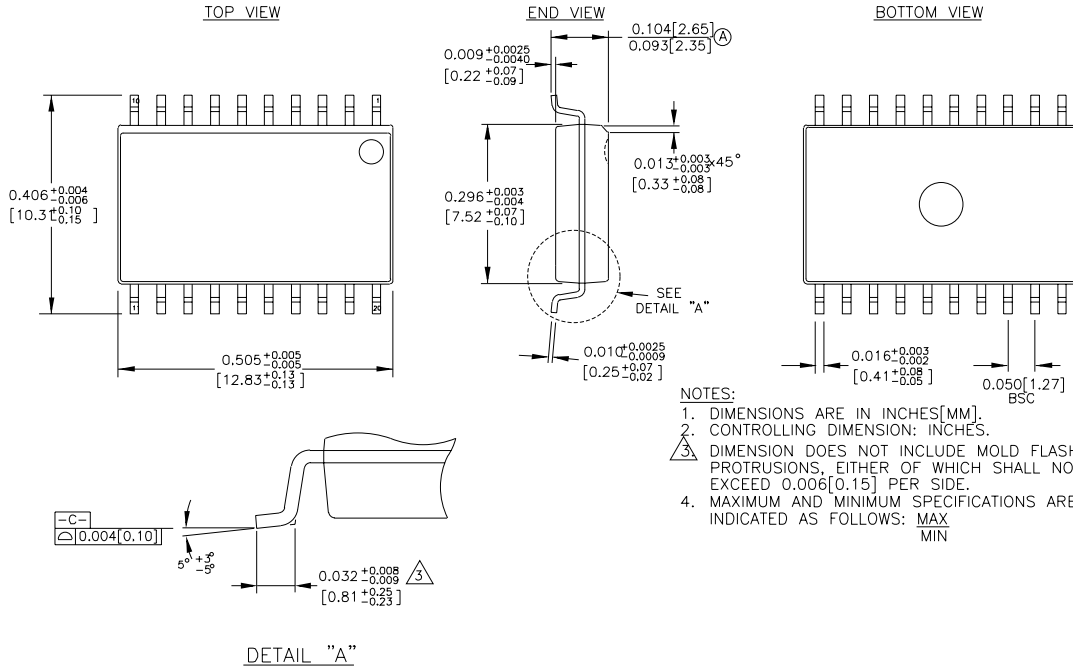
NOTES:

1. Power supply requirements applies as indicated in the DC electrical characteristics tables.
2. Skew is measured between outputs under identical transitions.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device Common Mode Range.
4. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ~40.
5. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100EL92ZC	Z20-1	Commercial
SY100EL92ZCTR	Z20-1	Commercial

20 LEAD SOIC .300" WIDE (Z20-1)



Rev. 03

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB <http://www.micrel.com>

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