TH8060

Voltage Regulator with integrated LIN Transceiver

Features

- LIN-Bus transceiver according to LIN specification 1.3
  - PNP-bipolar driver with slew rate control and wave shaping for good EME behaviour
  - BUS input voltage -24V to 30V (independently of V_{SUP})
  - Current limitation
  - Possibility of BUS wake up
  - Baud rate up to 20 kBaud
- Operating voltage V_{SUP} = 5.5 ... 18 V
- Very low standby current consumption < 110 µA in normal mode (< 50 µA in sleep mode)
- Linear low drop voltage regulator
  - Output voltage 5V± 1%
  - Output current max. 100mA
  - Output current limitation
  - Overtemperature shutdown
- Configurable reset time (15ms/100ms) and reset threshold voltage (3.15V / 4.65V)
- Low voltage detection at VSUP
- Wake-up by LIN BUS traffic and start-up capable independent of EN voltage level
- Universal comparator with an input voltage range –24V to 30V and digital output
- Load dump protected (40V)
- SOIC16 Package with 4 GND connection for better thermal dissipation

Ordering Information

Part No.	Temperature Range	Package
TH8060	J (-40 to 125 °C)	DF (SOIC16, 300mil)

General Description

The RELIN TH8060 consist a low drop voltage regulator 5V/100mA and a LIN Bus transceiver. The LIN-transceiver is suitable for LIN-Bus systems conform to “LIN-Protocol Specification” Rev.1.3.
The combination of voltage regulator and bus transceiver in combination with the monitoring functions make it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

The wide output current area and the configurable reset time and reset voltage works together with many different microcontrollers.

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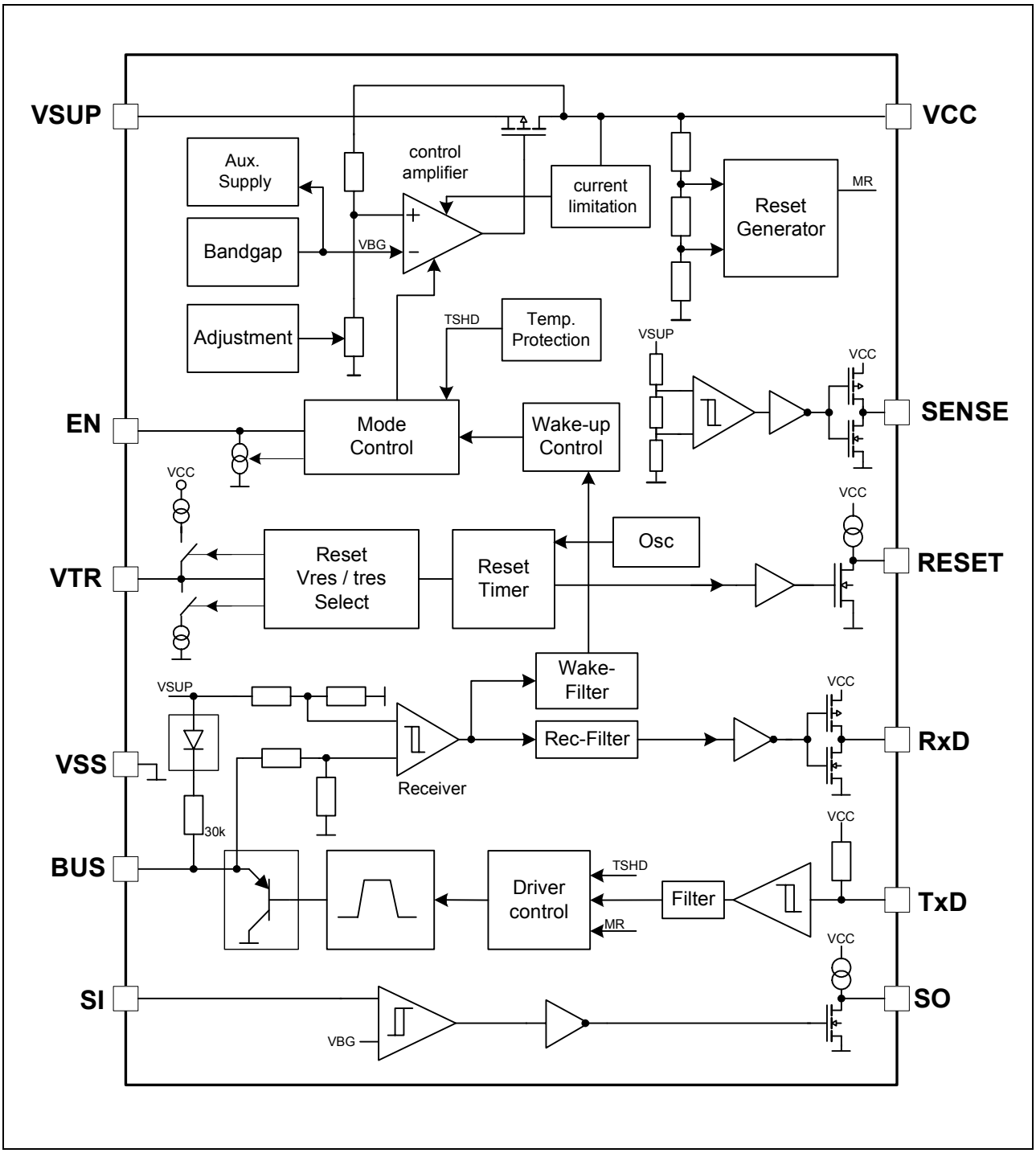


Figure 1- Block diagram

2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Correct operating of the device can't be guaranteed if any of these limits are exceeded.

2.1 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{SUP}	5.25	18	V
Output voltage	V_{CC}	4.95	5.05	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature [1]	T_{Jc}		+150	°C

2.2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at VSUP [1]	V_{SUP}		-1.0	18	V
		T ≤ 60 s	-	30	
		T ≤ 500 ms	-	40	
Input voltage at pin SI, BUS [1]	V_{BUS}		-24	30	V
		T ≤ 500 ms	-	40	
Difference VSUP-VCC	V_{SUP}-V_{CC}		-0.3	40	V
Input voltage at pin EN	V_{INEN}		-0.3	V_{SUP}+0.3	V
Input voltage at pin VTR, TxD, RxD, SO, RESET, SENSE	V_{IN}		-0.3	V_{CC}+0.3	V
Input current at pin EN, VTR, SO, TxD, RxD, RESET, SENSE	I_{IN}		-25	25	mA
Input current for short circuit of pin VSUP and VCC	I_{INSH}		-500	500	mA
ESD Capability on pin BUS	ESD_{BUSHB}	Human body Model, 100pF via 1.5kΩ	-2	2	kV
ESD Capability on all other pins	ESD_{HB}	Human body Model, 100pF via 1.5kΩ	-2	2	kV
Power dissipation	P_0		Internal limited [2]		
Thermal resistance from junction to ambient(SOIC16)	R_{THJA}			50	K/W
Junction temperature [3]	T_J			150	°C
Storage temperature	T_{STG}		-55	150	°C

[1] The current and voltage values are valid independent from each other.
[2] See chapter 4.3 Power Dissipation and operating range
[3] See chapter 3.9 Overtemperature Shut Down and 4.3 Power Dissipation and operating range

2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for V_{SUP} = 5.25...18V and T_{AMB} = -40...125°C. All voltages are referenced to ground (GND), positive currents are flow into the IC.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VSUP						
Operating voltage	V_{SUP}		5.25	12	18	V
Supply current, VCC „noload“ [3]	I_{Snl}	$V_{EN} = V_{SUP}$ = 12V, $V_{BUS} > V_{SUP}$-0.5V, Pins 8,10,11,14,15 and 16 open			110	µA
Supply current, „sleep mode“	I_{Ssleep}	V_{SUP} = 12V, V_{EN} = 0V, $V_{BUS} > V_{SUP}$-0.5V		35	50	µA
VCC						
Output voltage VCC	V_{CCn}	5.5V ≤ V_{SUP} ≤ 18V T_A = 25°C	4.95	5.0	5.05	V
	V_{CCt}	5.5V ≤ V_{SUP} ≤ 18V	4.90	5.0	5.10	V
	V_{CCh}	V_{SUP} > 18V	4.95	5.0	5.25	V
	V_{CCl}	3.3 V< V_{SUP}< 5.5 V	V_{SUP}-V_D		5.1	V
Drop-out voltage [4]	V_D	I_{VCC} = 25mA			150	mV
		I_{VCC} = 100mA			500	mV
Output current VCC	I_{VCC}	V_{SUP} ≥ 3.0V	100			mA
Current limitation VCC	I_{LVCC}	V_{SUP} > 0V			300	mA
Load capacity	C_{load}	1Ω ≤ ESR ≤ 7Ω	2			µF
Power-on-reset threshold on	V_{RES}	referred to V_{CC}, V_{SUP} > 4.6V	4.5	4.65	4.8	V
Power-on-reset threshold off	V_{POR}	VTR = High, VSUP > 0V	4.5	4,65	4.8	V
		VTR = Low, VSUP > 0V	3.0	3.15	3.3	
Enable Input EN						
Input voltage low	V_{ENL}		-0.3		1.6	V
Input voltage high	V_{ENH}		2.5		V_{SUP} +0.3	V
Hysteresis [1]	V_{ENHYS}		100			mV
Pull-down current EN	I_{pdEN}	$V_{EN} > V_{ENH}$	1.8	4.0	7.5	µA
		$V_{EN} < V_{ENL}$	70	100	130	µA
RESET Output						
Output voltage low	V_{OL}	I_{OUT} = 1 mA, V_{SUP} > 5.5 V			0.8	V
		10 kΩ RESET to VCC V_{CC} = 0.8 V			0.2	V
Pull-up current	I_{pu}		-500	-375	-250	µA

Static Characterirtics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SENSE Output						
VSUP - threshold low at SENSE	V_{SENL}		6.8			V
VSUP - threshold high an SENSE	V_{SENH}				7.8	V
Hysteresis SENSE	V_{SENHYS}		50			mV
Output voltage low	V_{OL}	I_{OUT} = 1mA			0.8	V
Output voltage high	V_{OH}	I_{OUT} = -1mA	V_{CC}-0.8			V
Comparator SI, SO						
Input Current SI	I_{INSI}	0V ≤ V_{SI} ≤ 18V	-20		20	µA
Input Current SI	$-I_{INSI}$	V_{SI} = -12V	-1			mA
Threshold low SI	V_{IL}		1.05	1.16		V
Threshold High SI	V_{IH}			1.21	1.4	V
Hysteresis	V_{HYS}		30			mV
Output voltage low at SO	V_{OL}	I_{OUT} = 1 mA, V_{SUP} > 5.5 V			0.8	V
		10 kΩ SO to VCC, V_{CC} = 0.8V			0.2	V
Pull-up current at SO	I_{pu}		-500	-375	-250	µA
VTR Input						
Threshold low	V_{TRL}		0.15	0.25		V_{CC}
Threshold high	V_{TRH}			0.75	0.85	V_{CC}
Output current low	I_{OL}	VCC > 3.3 V	160	230	300	µA
Output current high	I_{OH}		-300	-230	-160	µA

Static Characterirtics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LIN BUS Interface						
Receive threshold	V_{thr_rec}, V_{thr_dom}	7.3 V ≤ V_{SUP} ≤ 18 V	0.4* V_{SUP}		0.6* V_{SUP}	V
Center point of receive threshold $V_{thr\_cnt} = (V_{thr\_rec}+V_{thr\_dom})/2$	V_{thr_cnt}		0.475* V_{SUP}	0.5* V_{SUP}	0.525* V_{SUP}	
Hysteresis of receive threshold $V_{thr\_hys} = V_{thr\_rec}-V_{thr\_dom}$	V_{thr_hys}		0.12* V_{SUP}	0.135* V_{SUP}	0.15* V_{SUP}	
Input current BUS (recessive) [3]	I_{INBUSR}	7.3 ≤ V_{BUS} ≤ 18 V, V_{SUP}= V_{BUS} - 0.7V, TxD = High			20	µA
Input current BUS (recessive)	$-I_{INBUSR}$	V_{SUP}= 0V, V_{BUS} - 12V	-1			mA
Pull up resistor bus	R_{BUSpu}	V_{SUP}= 12V, V_{BUS} =0V, TxD = High	20	30	47	kΩ
Output voltage BUS (dominant) [3]	V_{BUSdom}	TxD = Low, I_{BUS} = 40mA			1.2	V
Output voltage BUS (recessive) [2] [3]	V_{BUSrec}	7.3 ≤ V_{SUP} ≤ 18 V, TxD = High	0.8*V_{SUP}			V
Current limitation BUS	I_{LIM}	V_{BUS} > 2.5V, TxD = 0V	40		120	mA
Input TxD						
Pull-up Strom TxD	Ipu		-500	-375	-250	µA
Input low level TxD	V_{IL}				0.25	V_{CC}
Input high level TxD	V_{IH}		0.75			V_{CC}
Output RxD						
Output voltage Low RxD	V_{OL}	I_{OUT} = 1 mA			0.8	V
Output voltage High RxD	V_{OH}	I_{OUT} = -1 mA	V_{CC} - 0.3			V
Thermal Protection						
Thermal shutdown [1]	$T_{jshutdown}$		150		170	°C
Thermal recovery [1]	T_{jrec}		126			°C

[1] No production test, guaranteed by qualification
[2] The recessive voltage at pin BUS don't should be less than 80% of voltage at KL30 $V_{BAT.}$ The voltage at V_{SUP} results with consideration of reverse diode V_{SUP} = V_{BAT} - 0,7V
[3] See chapter 2.6 Test Circuit for Dynamic and Static Characteristics
[4] The nominal V_{CC} voltage is measured at V_{SUP} =12V. If the V_{CC} voltage is 100mV below its nominal value then the voltage drop is $V_D = V_{SUP} – V_{CC}$.

2.4 Dynamic Characteristics

8V ≤ V_{SUP} ≤ 18V, -40°C ≤ T_A ≤ 125°C, unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RESET						
Reset time	t_{RES1}	R_{VTR} < 1 kΩ	70	100	140	ms
	t_{RES2}	R_{VTR} > 45 kΩ	10	15	20	
Reset rising time [1]	t_{rr}		3.0	6.5	10	µs
Propagation delay SI to SO	t_{dcomp}		4		11	µs
Debouncing time SENSE [1]	t_{deb_SEN}		10	17	25	µs
LIN BUS Interface						
Transmit propagation delay TxD -> BUS [2] [3]	t_{dr_TXD}, t_{df_TXD}	R_L/C_L at BUS 1kΩ/1nF 660Ω/6.8nF 500Ω/10nF			4	µs
Symmetry of propagation delay BUS -> RxD [2]	t_{dsym_TXD}	t_{dr_TXD} - t_{df_TXD}	-2		2	µs
Receiver propagation delay BUS -> RxD [2] [3]	t_{dr_RXD} t_{df_RXD}	$C_{L(RXD)}$ = 50pF			6	µs
Symmetry of propagation delay TxD -> BUS [2]	t_{dsym_RXD}	t_{dr_RXD} - t_{df_RXD}	-2		2	µs
Slew rate BUS rising edge [1]	dV/dT_{rise}	20% ≤ V_{BUS} ≤ 80% C_{BUS} = 100 pF	1.0	2.0	2.5	V/µs
Slew rate BUS falling edge [1]	dV/dT_{fall}	20% ≤ V_{BUS} ≤ 80% 100pF ≤ C_{BUS} ≤ 10nF	-2.5	-2.0	-1.0	V/µs
Slope time, transition from recessive to dominant [3] [4]	t_{sdom}	V_{SUP} = 8 V R_L= 500Ω / C_L=10nF			7.3	µs
Slope time, transition from dominant to recessive [3] [5]	t_{srec}	V_{SUP} = 8 V R_L= 500Ω / C_L=10nF			12	µs
Slope time symmetry	t_{ssym}	V_{SUP} = 8 V R_L= 500Ω / C_L=10nF T_{ssym} = t_{sdom} - t_{srec}	-7	0	1	µs
Slope time, transition from recessive to dominant [3] [4]	t_{sdom}	V_{SUP} = 18 V R_L= 500Ω / C_L=10nF			17.2	µs
Slope time, transition from dominant to recessive [3] [5]	t_{srec}	V_{SUP} = 18 V R_L= 500Ω / C_L=10nF			17.2	µs
Slope time symmetry	t_{ssym}	V_{SUP} = 18 V R_L= 500Ω / C_L=10nF T_{ssym} = t_{sdom} - t_{srec}	-5	0	5	µs
Debouncing time BUS	t_{deb_BUS}		1.5	2.8	4.0	µs
Wake-up time	t_{Wake_BUS}		25	60	120	µs

[1] No production test, guaranteed by qualification
[2] See chapter 2.5 Timing Diagrams timing diagram
[3] See chapter 2.6 Test Circuit for Dynamic and Static Characteristics
[4] t_{sdom} = ($t_{VBUS40\%}$ - $t_{VBUS95\%}$) / 0.55
[5] t_{sdom} = ($t_{VBUS60\%}$ - $t_{VBUS5\%}$) / 0.55

2.5 Timing Diagrams

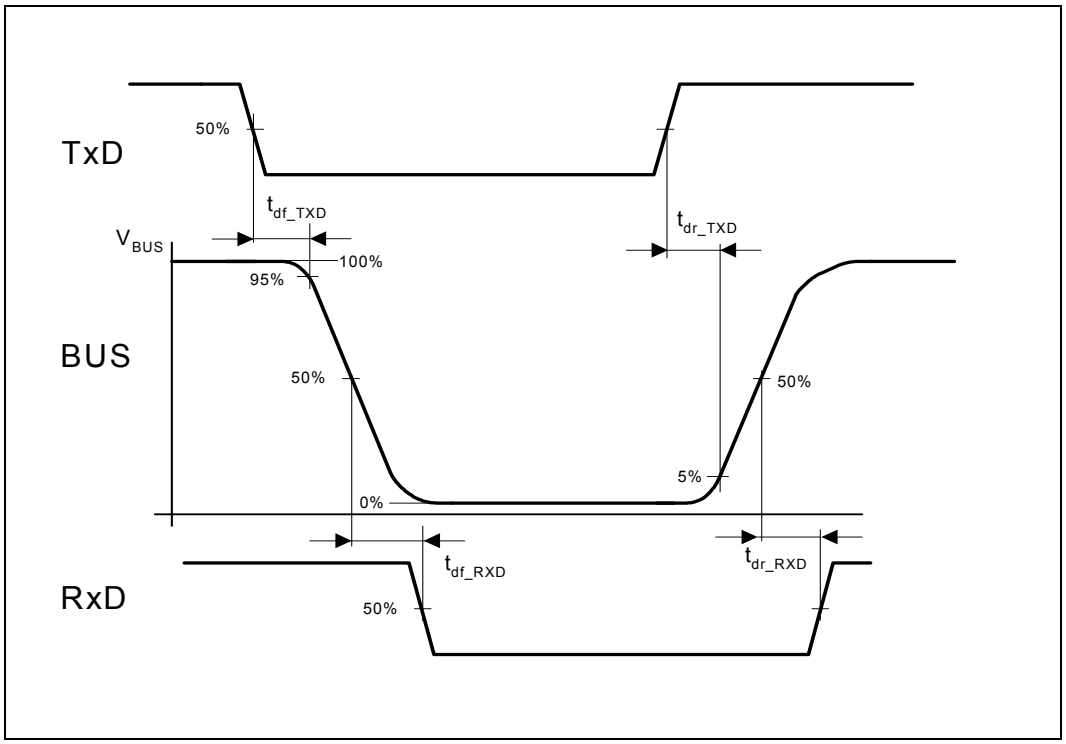


Figure 2 - Timing diagram for propagation delay

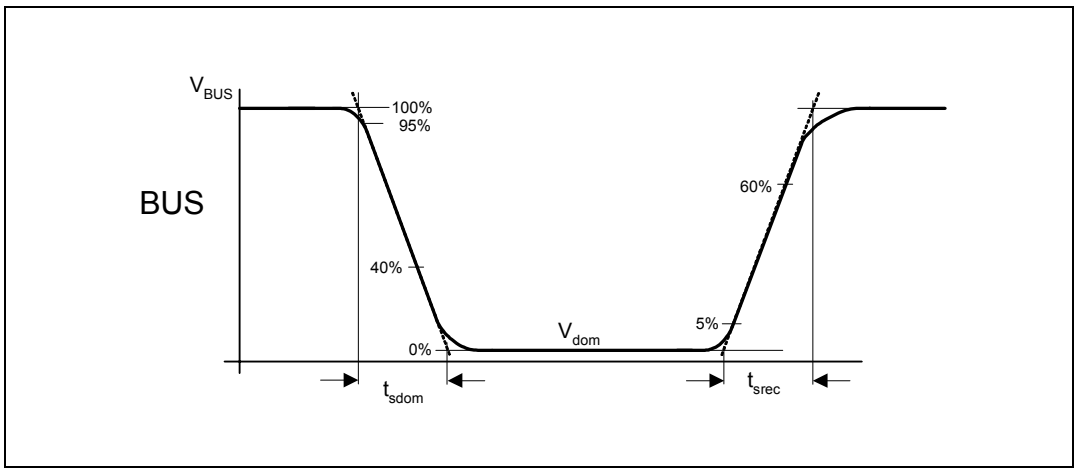


Figure 3 - Timing diagram for slope times

2.6 Test Circuit for Dynamic and Static Characteristics

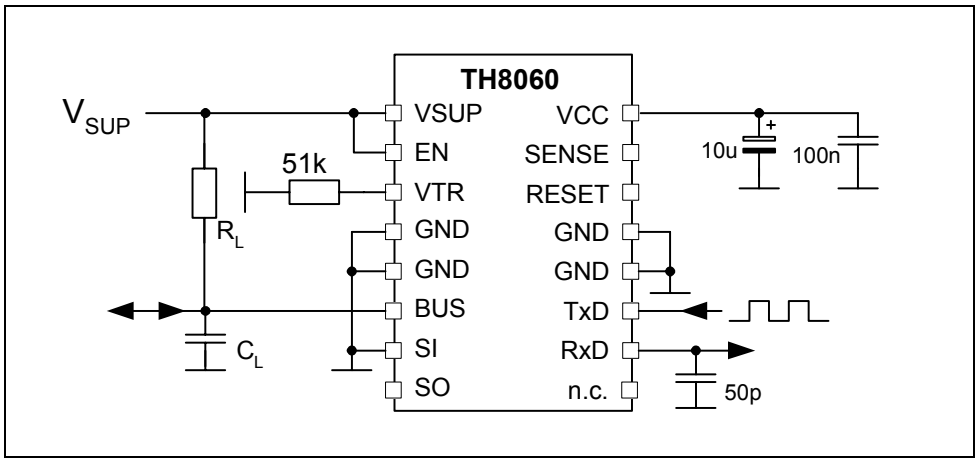


Figure 4 - Test circuit for delay time and slope control

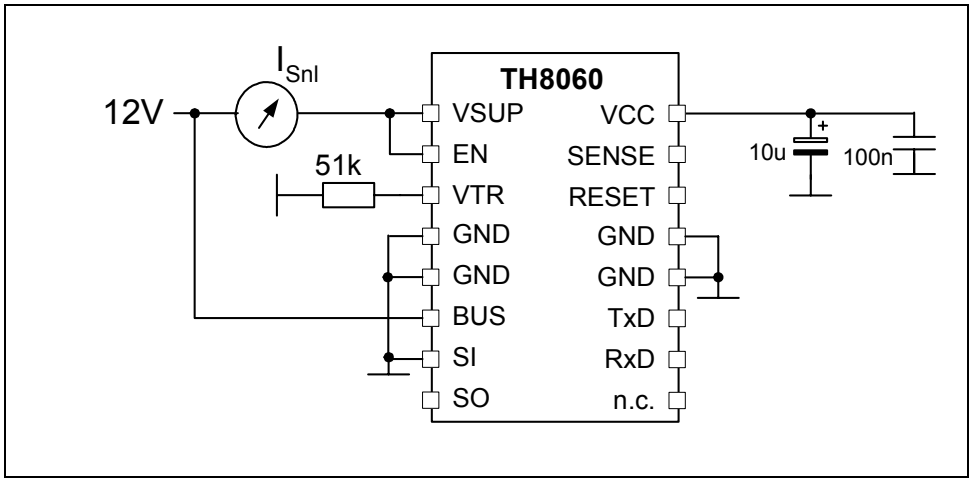


Figure 5 - Test circuit for supply current I_{SnI}

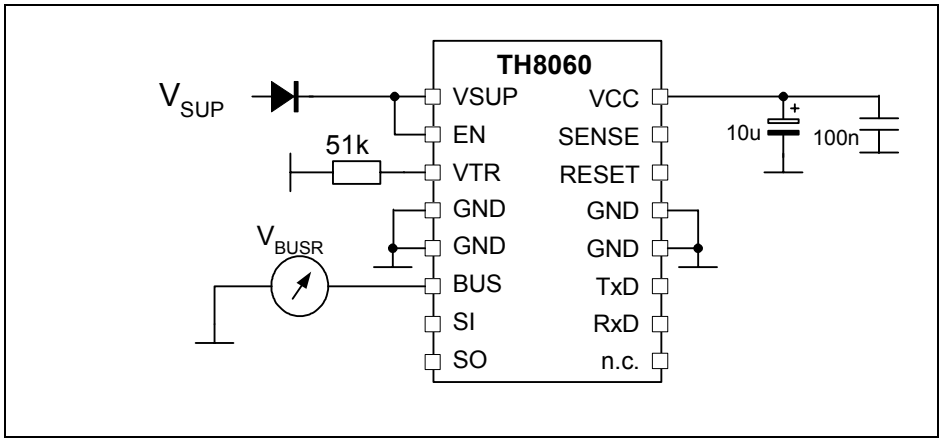


Figure 6 - Test circuit for bus voltage "recessiv" V_{BUSR}

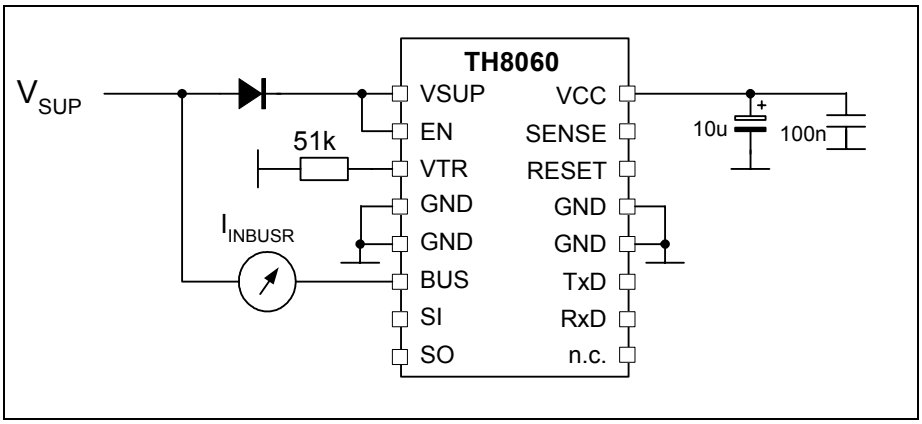


Figure 7 - Test circuit for bus current "recessiv" I_{INBUSR}

3. Functional Description

The TH8060 consists a voltage regulator 5V/100mA and a LIN Bus transceiver, which is a bi-directional bus interface device for data transfer between LIN-Bus and the LIN protocol controller.
Also integrated into the transceiver is a voltage and time controlled reset management, power down, wake up function and a universal comparator for extended applications.

3.1 Operating Modes

Via the EN pin it is possible to switch the TH8060 into different operating modes:

Normal Mode

The whole TH8060 is active. Switching to normal mode can be done via the following actions:

- Rising edge at EN (EN=high) (local wake-up)
- Activity on the LIN bus (remote wake-up)
- Power On Reset

Sleep Mode

The sleep mode is most current saving mode. With a falling edge on EN (EN=low) it is possible to switch to this mode. The voltage regulator will be switched off and the LIN transceiver is in recessive state.
Switching into sleep mode can be done independent from the current transceiver state. If the transmitter is in dominant state this state will be cancelled and it will be switched to recessive state.

Thermal Shutdown Mode

If the junction temperature T_J is higher than 150°C, the TH8060 will be switched into the thermal shutdown mode. The impact of this mode is comparable with the sleep mode.
If T_J falls below the thermal shutdown temperature (typ. 140°C) the TH8060 will be switched to the previous state.

3.2 LIN BUS Transceiver

The TH8060 is a bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller.
The transceiver consist a pnp-driver (1.2V@40mA) with slew rate control, wave shaping and current limitation and consists as well in the receiver a high voltage comparator followed by a debouncing unit.

Transmit Mode

During transmission the data at the pin TxD will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.
Transmitting will be interrupted in the following cases:

- Sleep mode
- Thermal Shutdown active
- Master Reset (V_{CC} < 3.15V)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with a active diode. This diode prevent the reverse current of V_{BUS} during differential voltage between VSUP and BUS (V_{BUS}>V_{SUP}).
No additional termination resistor is necessary to use the TH8060 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via a external 1kΩ resistor in serial with a diode to VBAT.

Receive Mode

The data signals from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit (τ = 2.8µs).

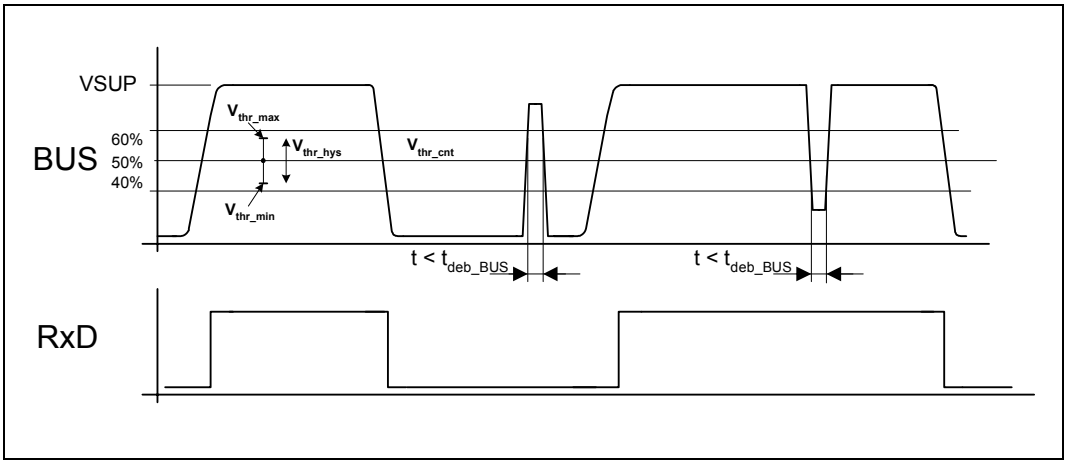


Figure 8 - Receive mode impulse diagram

The receive threshold values V_{thr_max} and V_{thr_min} are symmetrical to the centre voltage of $0.5*V_{SUP}$ with a hysteresis of $0.135*V_{SUP}$. Including all tolerances the LIN specific receive threshold values of $0.4*V_{SUP}$ and $0.6*V_{SUP}$ will be secure observed.

Datarate

The TH8060 is a ***constant slew rate*** transceiver that means the bus driver works with a fixed slew rate range of 1.0 V/µs ≤ $\Delta V/\Delta T$ ≤ 2.5V/µs. This principle secures a very good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}). The TH8060 guarantees data rates up to 20kbit within the complete bus load range under worst case conditions. The constant slew rate principle is very robust against voltage drops and can operate with RC-oscillator systems with a clock tolerance up to ±2% between 2 nodes.

Input TxD

The 5V input TxD controls directly the BUS level:

TxD = low	->	BUS = low (dominant level)
TxD = high	->	BUS = high (recessive level)

The TxD pin has an internal pull up resistor connected to VCC. This secures that an open TxD pin generates a recessive BUS level.

Output RxD

The received BUS signal will be output to the 5V RxD pin:

$BUS < V_{thr\_cnt} - 0.5 * V_{thr\_hys}$	->	RxD = low
$BUS > V_{thr\_cnt} + 0.5 * V_{thr\_hys}$	->	RxD = high

This output is a push-pull driver between VCC and GND with a output current of 1mA.

3.3 Linear Regulator

The TH8060 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±2% and a current of ≤100mA within an input voltage range of 5.5V ≤ V_{SUP} ≤ 18V. The current limitation unit limits the output current for short circuits or over load to 200mA respectively drops down the V_{CC} voltage.

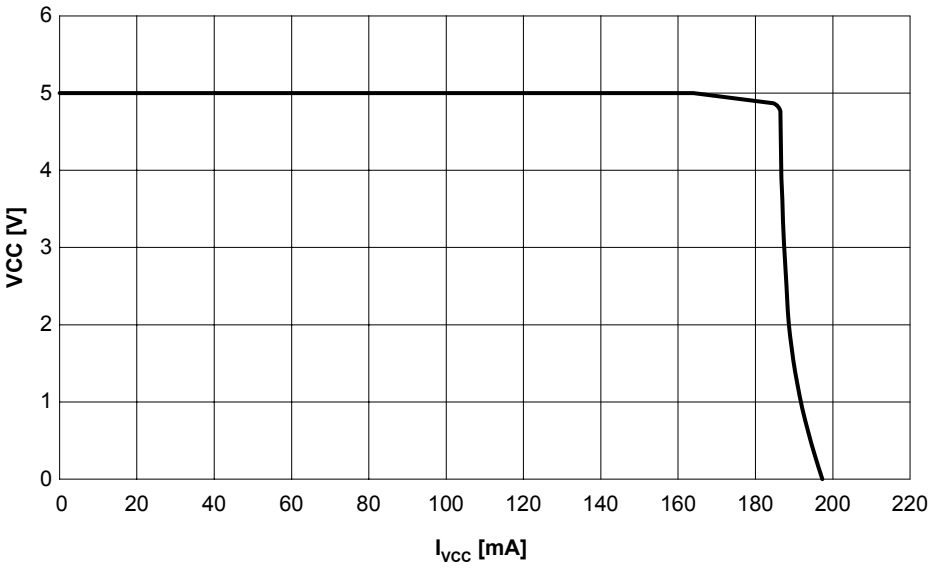


Figure 9 - Characteristic of current limitation VCC = f(I_{VCC})

3.4 RESET

The RESET pin output the reset state of the TH8060. This output is switched from low to high if V_{SUP} is switched on and V_{CC}>V_{RES} after the time t_{Res}.

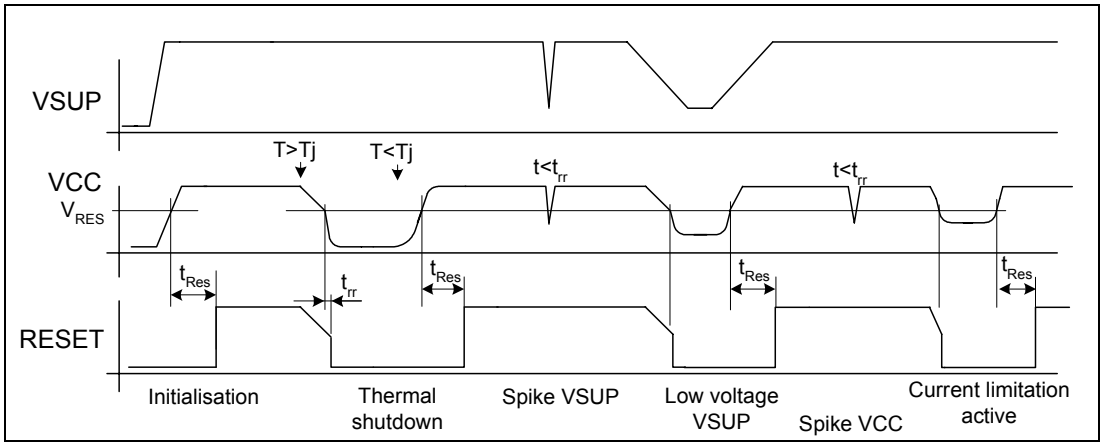


Figure 10 - Reset behaviour

If the voltage V_{CC} drop below V_{RES1} or V_{RES2} then the RESET output is switched from high to low after the time t_{rr} has been reached. For this reason short breaks of the V_{CC} voltage and uncontrolled reset generations will be inhibit.
The voltage level for V_{RES1} and V_{RES2} or the corresponding times t_{RES} can be programmed via the analogue input VTR.
The RESET output driver secures that the RESET state will be secure observed if the VCC voltage drops down. The output high level will be generated from an internal pull-up current source.

3.5 Reset Programmming on VTR

With the VTR pin the reset threshold and delay time can be programmed.

VTR-Programming

VTR-Mode	V_{RES}	t_{Res}
VTR = GND	$V_{RES} = V_{RES1} = 3.15V$	100ms
VTR = VCC	$V_{RES} = V_{RES2} = 4.65V$	100ms
VTR with R ≥ 50kΩ to GND	$V_{RES} = V_{RES1} = 3.15V$	15ms
VTR with R ≥ 50kΩ to VCC	$V_{RES} = V_{RES2} = 4.65V$	15ms

The voltage on VTR input is read out if the voltage at this pin is higher than V_{RES1} (Master-Reset). This value defines the reset threshold voltage V_{RES} and switches on with the next oscillator cycle the pull up current source if VTR=low or the pull down current source if VTR=high. The sources are active for one oscillator cycle. The level changes during this procedure on VTR, which depends on the external pull up or pull down resistors control the reset time t_{RES}

3.6 Initialization

The initialization is started if the power supply is switched on respectively every start of the voltage regulator after switching off.

VSUP- Power ON

The TH8060 start with the normal mode if V_{SUP} is switched on. The internal circuitry on VCC as well as the internal help supply starts the initialisation with power-on-reset. The voltage regulator is switched on.
If V_{CC}>V_{RES1} the bus-interface will be activated and the VTR state will be detected.
If the V_{CC} voltage level is higher than V_{RESEIN}, the reset time t_{Res} is started, depending on the VTR state. After t_{Res} the RESET output switches from low to high (see Figure 10).
The initialisation procedure at power on starts independent from the EN state.

Start of Linear Regulator

The initialization is only being done for the VCC circuitry parts. This procedure begins with leaving the master reset state (V_{CC} > V_{RES1}) and runs in the same manner as the VSUP-Power-On.

3.7 Mode Input EN

The TH8060 is switched into the sleep mode with a falling edge and into normal mode with a rising edge at the EN pin. The normal mode will be kept as long as EN = high.
The deactivation of TH8060 with a falling edge at EN can be done independent from the state of the bus-transceiver.
The EN input is internal pulled down so that it is secured if this pin is not connected a low level will be generated. In the high state the pull down current will be switched off to reduce the quiescent current.

3.8 Wake-Up

If the regulator is put in standby mode it can be wake up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 60µs switches on the regulator.
After the BUS has wake up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

3.9 Overtemperature Shut Down

If the Junction temperature is 150ºC < T_j < 170ºC the over temperature shut down will be active and the regulator voltage is switched off. The V_{CC} voltage drops down, the reset state is entered and the bus-transceiver is switched off (recessive state).
After T_j fall below 140ºC the TH8060 will be initialized (see Figure 10), independent from the voltage levels on EN and BUS. Within the thermal shutdown mode the transceiver can't switched to the normal mode neither with local nor with remote wake-up.
The function of the TH8060 is possible between T_{Amax} (125°C) and the switch off temperature, but small parameter differences can appear.
After over temperature switch off the IC behave as described in chapter 3.4 RESET.

3.10 Low Voltage Detection at VSUP

Low voltage on VSUP is monitored on SENSE output.
If VSUP drops down below V_{SUP} = 6.8V then SENSE generates a low level. If V_{SUP} > 7.8V the TH8060 switches to the normal mode and SENSE generates a high level.

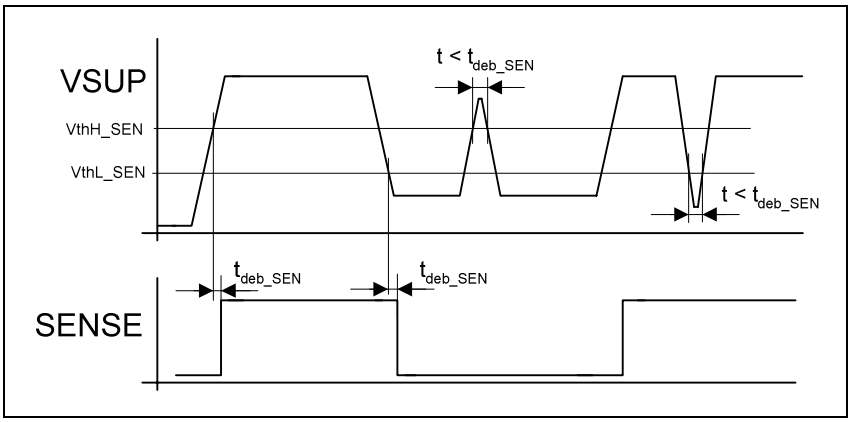


Figure 11 - Low Voltage Detection

SENSE is a push pull output driver with a drive capability of 1mA

3.11 Universal Comparator

The TH8060 consist a universal comparator for general use. The Comparator compares the input signal SI with a internal bandgap reference voltage and the result will be output at SO as digital signal. The High voltage SI input has a voltage range from -24V to 30V referring to GND. The function is also possible during low voltage from VCC to V_{RES1}. If the supply voltage drops below V_{RES1} SO outputs a low level, independent from the input voltage at SI.
The SO output driver secures that the low level is kept down to VCC voltages of 0V with low resistance.

4. Application Hints

4.1 LIN System Parameter

4.1.1. Bus loading requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating voltage range	V_{BAT}	8		18	V
Voltage drop of reverse protection diode	V_{Drop_rev}	0.4	0.7	1	V
Voltage drop at the serial diode in pull up path	$V_{SerDiode}$	0.4	0.7	1	V
Battery shift voltage	V_{Shift_BAT}	0		0.1	V_{BAT}
Ground shift voltage	V_{Shift_GND}	0		0.1	V_{BAT}
Master termination resistor	R_{master}	900	1000	1100	Ω
Slave termination resistor	R_{slave}	20	30	60	kΩ
Number of system nodes	N	2		16	
Total length of bus line	LEN_{BUS}			40	m
Line capacitance	C_{LINE}		100	150	pF/m
Capacitance of master node	C_{Master}		220		pF
Capacitance of slave node	C_{Slave}		220	250	pF
Total capacitance of the bus including slave and master capacitance	C_{BUS}	0.47	4	10	nF
Network Total Resistance	$R_{Network}$	500		862	Ω
Time constant of overall system	τ	1		5	µs

Table 1 - Bus loading requirements

4.1.2. Recommendations for system design

The goal of the LIN physical layer standard is to be universal valid definition of the LIN system for plug &play solutions in LIN networks up to 20kbd bus speed.
In case of small and medium LIN networks no problems occurring. It's recommended to adjust the total network capacitance to at least 4nF for good EMC and EMI behavior. This can be done by adapting only the master node capacitance. The slave node capacitance should have a unit load of typically 220pF for good EMC/EMI behavior.
In large networks with long bus lines and the maximum number of nodes some system parameters can exceed the defined limits and an intervention of the LIN system designer is required.
The whole capacitance of a slave node is not only the unit load capacitor itself. Additionally there is a capacitance of wires and connectors and the internal capacitance of the LIN transmitter. This internal capacitance is strongly dependent from the technology of the IC manufacturer and should be in the range of 30 to 150pF. If the bus lines have a total length of nearly 40m, the total bus capacitance can exceed 10nF.
A second reason for exceeding these limits is the tolerance of the integrated slave termination resistor. If most of the slave nodes have a slave termination resistance near by the allowed maximum of 60kΩ, the total network resistance is more than 700Ω. Even if the total network capacitance is below or equal to the maximum specified value of 10nF, the network time constant is higher than 7µs!
This problem can be removed only by adapting the master termination resistor to realize the required maximum network time constant of 5µs.
The LIN output driver of the TH8060 provides a higher driving capability than necessary within the LIN standard (40mA @ 1.2V). With this driver stage the system designer have more degrees of freedom in case of maximum LIN networks with a total network capacitance of more than 10nF. The total network resistance can be decreased to:

$$R_{tl\_min} = (V_{Bat\_max} - V_{BUSdom}) / I_{BUS\_max} = (18V - 1.2V) / 40mA = 420\Omega$$

Note:
The adaptation of the network time constant is necessary in large networks (Master resistance)and also in small networks (master capacitance).
The intervention in the LIN network has only to be done in the master ECU! The limits of the system have to be known by the system designer and shouldn't have any influence to the LIN physical layer.

The TH8060 meets the requirements for implementation in RC-based slave nodes (oscillator tolerance <2% at baudrate 20Kbit/s)under all worst case conditions in V_{BAT}- or ground shift, operating voltage and load conditions, and independent from the method of reverse polarity protection .

4.2 Min/max slope time calculation

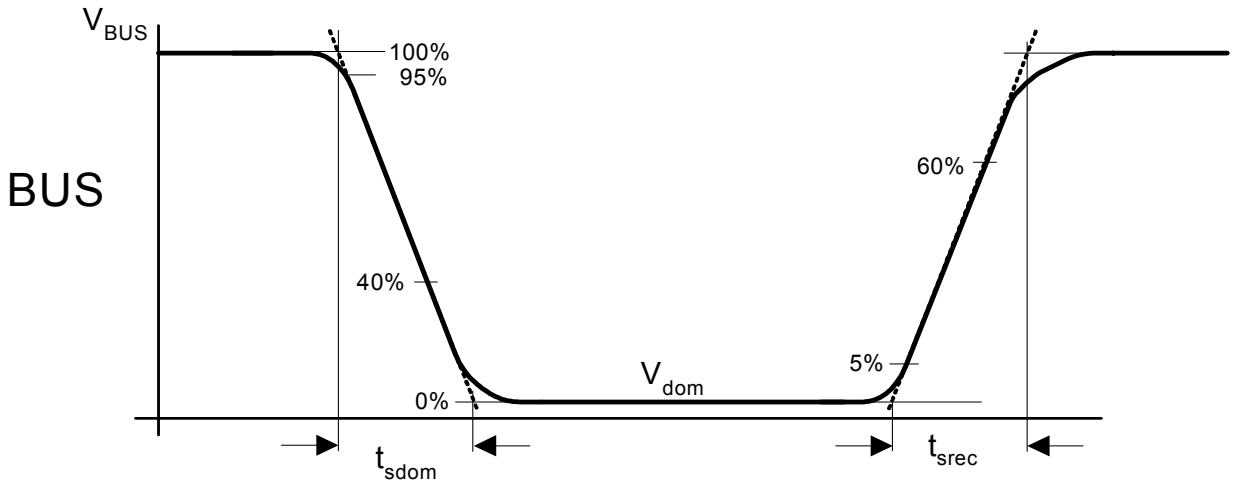


Figure 12 - Slope time calculation

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2*V_{swing} / (t_{40\%} - t_{60\%})$$

The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%} - t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing} / dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.

4.3 Power Dissipation and operating range

The max power dissipation depends on the thermal resistance of the package and the PCB, the temperature difference between Junction and Ambient as well as the airflow.
The power dissipation can be calculated with:

$$P_D = (V_{SUP} - V_{CC}) * I_{VCC} + P_{BUS}$$

The power dissipation of the transmitter P_{BUS} is max. 25mW (V_{SUP}=18V, continuous data transmission with duty cycle of 50%)
The permitted package power dissipation can be calculated:

$$P_{Dmax} = \frac{T_j - T_A}{R_{THJ-A}}$$

T_j-T_A is the temperature difference between junction and ambient and R_{th} is the thermal resistance of the package. The thermal energy is transferred via the package and the 4 GND pins to the ambient. This transfer can be improved with additional ground areas on the PCB as well as ground areas under the IC.

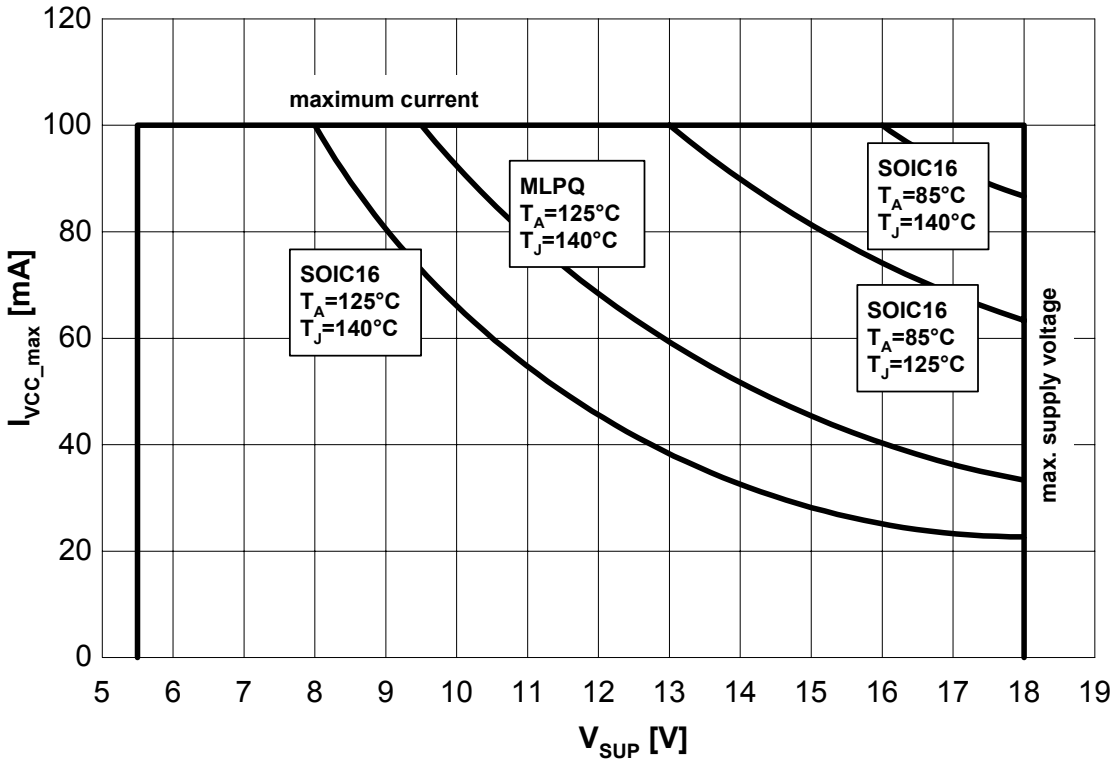


Figure 13 - Save operating area

The linear regulator of the TH8060 operates with input voltages up to 18V and can output a current of 100mA, but maximum power dissipation don't allow this at the same time. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 100mA at an ambient temperature of T_A = 125°C is only possible with small voltage differences between V_{SUP} and V_{CC}. See Figure 13 for save operating areas for different ambient and junction temperatures.

4.4 Regulator circuitry

Pin VCC

The linear regulator needs a minimum load capacity of 2µF connected to V_{CC} for stable operating within the whole operating area.
The choice of type and dimension of the load capacity must be done from the application point of view (e.g. Tantal 10µF). Essential parameters are the switch on time of the VCC and the load regulation.
Small capacity values don't should combine with small ESR values to avoid stability problems.

Pin VSUP

The capacity connected to the VSUP pin influences the regulation behaviour especially the line regulation and load regulation.
Big capacity values improve the line regulation and in parallel with a ceramic capacitor it archives good disturbance suppressing.

4.5 Application circuitry

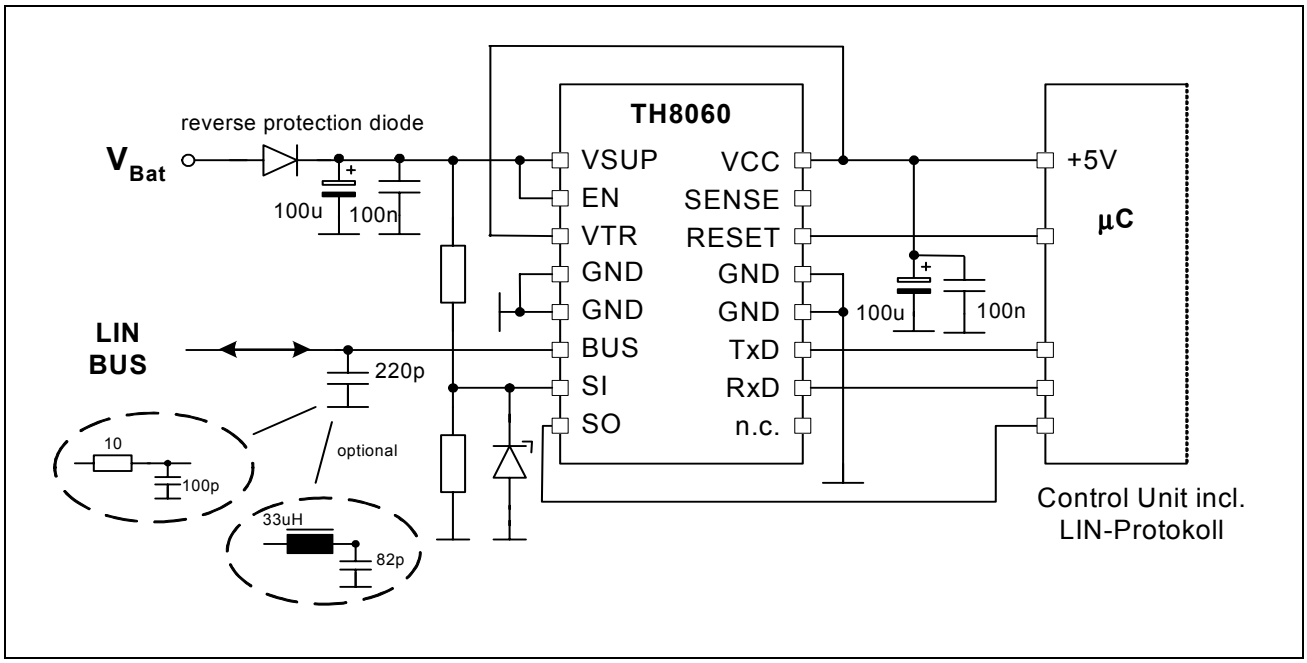


Figure 14 - Application circuit (slave node)

4.6 EMI Supressing

To minimize the influence of EMI on the bus line a 220pF capacitor should be direct connected to the BUS pin (see Figure 14). This EMI-Filter causes that the RF immissions into the IC from the BUS line have no affect resp. will be limited.
The value of the filter capacity can be adjusted to the size of the LIN network. 220pF should be used for bigger networks. Values from 333pF up to 1nF should be used for middle to small LIN networks. Finally the size of the filter capacity influences the effectiveness of the EMI suppressing in observation of the maximum LIN bus capacity of 10nF.
Alternatively to a pure C-filter it is also possible to use LC- or RC-filter. The dimension of C, L or R, L depends on the corner frequency, the maximum LIN bus capacity (10nF) and the compliance with the DC- and AC LIN bus parameters.

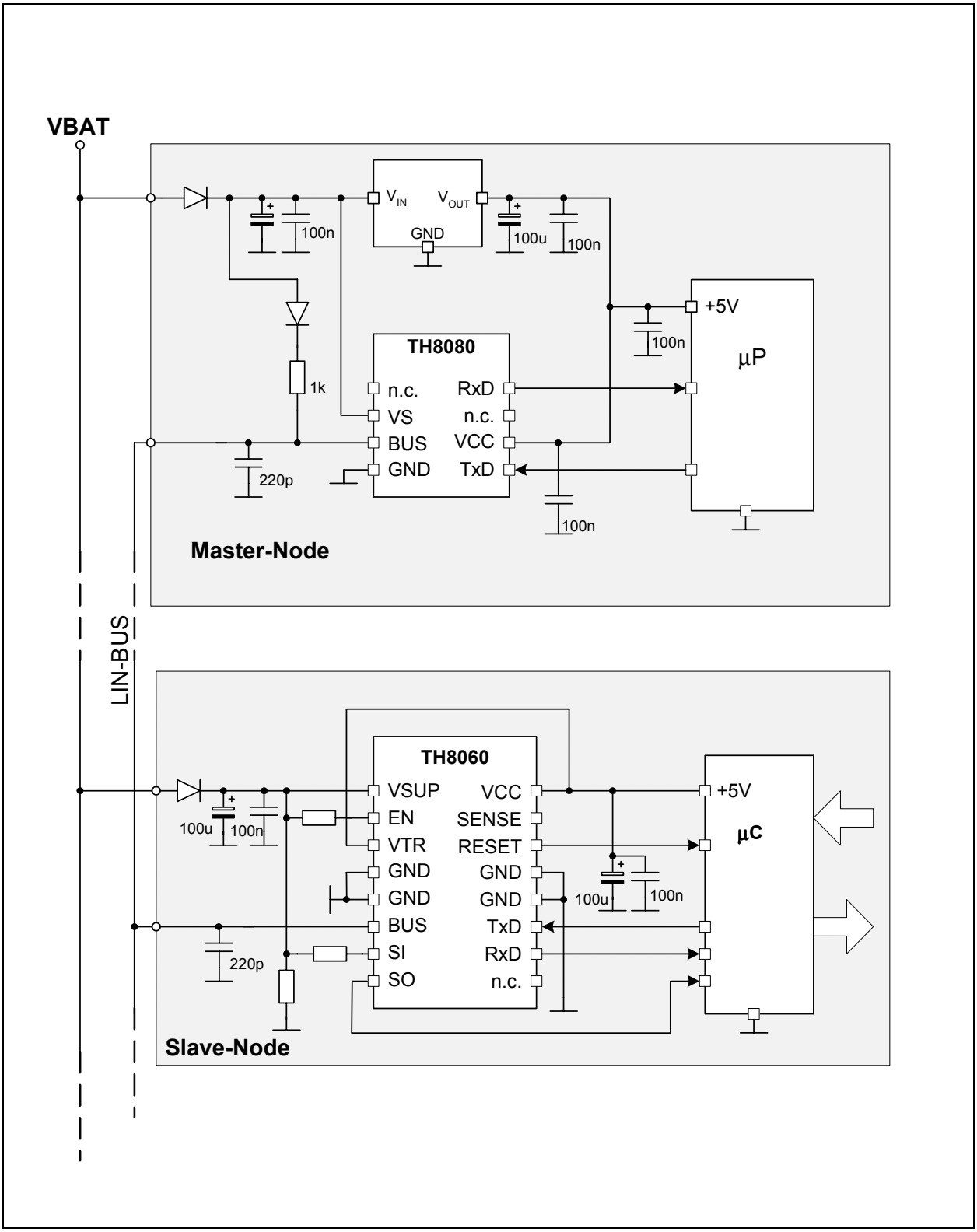


Figure 15 - Application circuit for LIN subbus with TH8060 as slave node

4.7 Connection to Flash-MCU

During programming of a flash MCU the TH8060 should be disconnected from the MCU. This can be done via disconnecting the supply voltage of the TH8060 or via switch off with the EN pin. The reverse current supply of the IC via the RxD pin if the connected MCU pin is used as normal signal input and programming input must be inhibit via decoupling with a diode. In this case the MCU must be supplied via the programming interface.

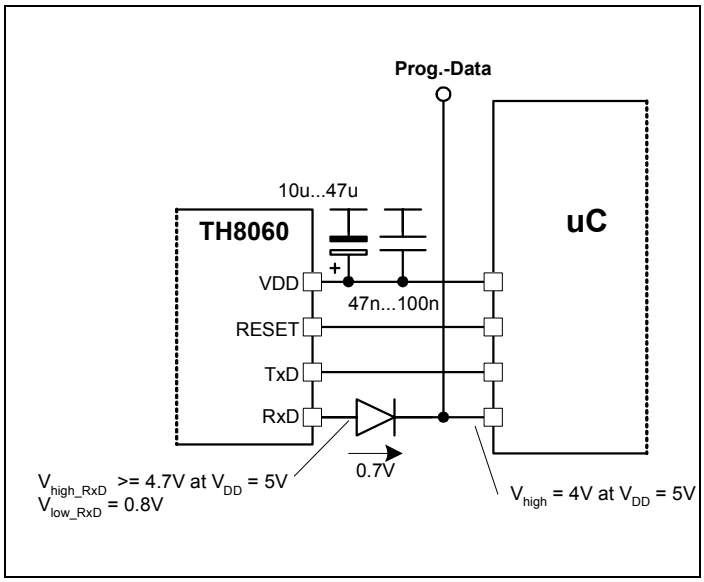


Figure 16 - Example circuitry for connection of RxD to MCU for flash programming

5. Operating during Disturbance

5.1 Operating without VSUP or GND

The BUS pin is designed for voltages of GND-24V up to GND+30V and this inhibit that the absence of V_{SUP} or GND connection influence or disturb the communication between other bus nodes. No reverse supply of the IC can appear if without GND or VSUP connection the BUS pin is on VBAT level.

5.2 Short Circuit BUS against VBAT

The reaction of the IC depends on the send state of the transceiver:

- Recessive LIN bus is blocked, no influence to the TH8060
- Dominant Current limitation, thermal shut down of TH8060 if the power dissipation will make an overrun of T_J

5.3 Short Circuit BUS against GND

LIN bus is blocked. No influence to the TH8060.

5.4 Short Circuit TxD against GND

The LIN transceiver is permanent in the dominant state that mean the whole LIN bus. This state can only be detected from the LIN controller. In this case the controller must switch off the LIN node via the EN input of the TH8060. A thermal shut down of TH8060 will appear if the power dissipation will make an overrun of $T_{J.}$

5.5 TxD open

The internal pull up resistor forces the LIN node to the recessive state. The communication between the other bus-nodes will not disturb.

5.6 Short Circuit VCC against GND

The VCC pin is protected via a current limitation. This state is comparable with the behaviour in the sleep mode.

5.7 Overload of VCC

Thermal switch off

The power dissipation is increasing if the load current is between I_{VCC_max} and I_{LVCC}. If the max junction temperature of 150°C is reached the IC will be switched off. The voltage regulator will also be switched off and a reset signal is forced.

Over current

If the current limitation is active the voltage on VCC drops down. If this voltage under-run the adjusted threshold V_{RES1} or V_{RES2} a reset will be forced.

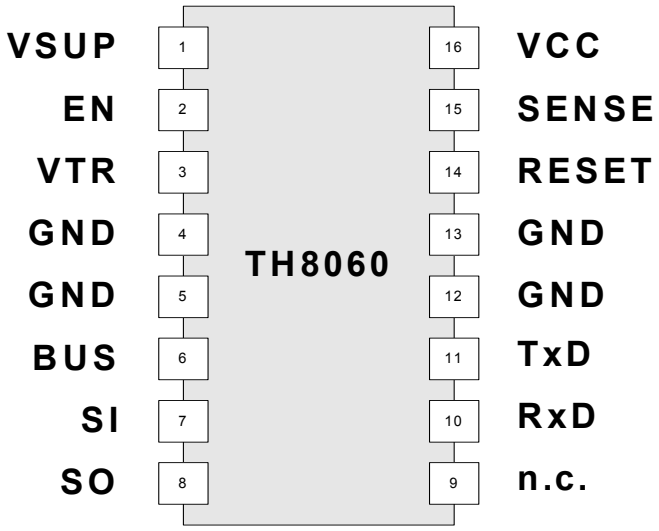
5.8 Undervoltage VSUP, VCC

The reset unit secures the correct behaviour of the driver during undervoltage. The BUS pin generates the recessive state if $V_{CC} < V_{RES1}$. The inputs EN and TxD have pull-up or pull-down characteristics.
If $V_{RES1} \leq V_{CC} \leq 4.5V$ the TxD signal is transmitted to the bus. The receive is also active.
If $V_{CC} > V_{RES1}$ SENSE and SO outputs the correct signal.

5.9 Short circuit RxD, RESET against GND or VCC

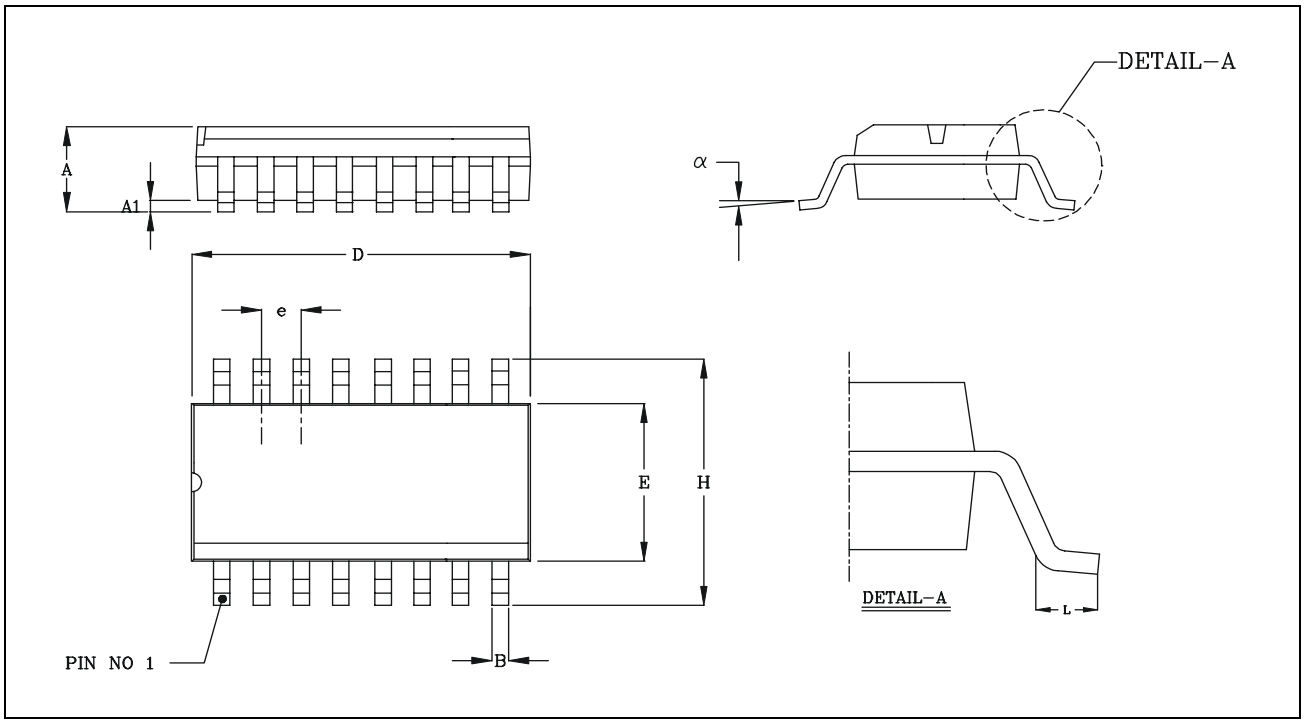
Both outputs are short circuit proof to VCC and ground.

6. PIN Description SOIC16WB



Pin	Name	I/O	Function
1	VSUP		Supply voltage
2	EN	I	Enable Input voltage regulator, HV-pull-down-Input, High-active
3	VTR	I	Analogue Input - definition of reset time und Reset voltage level
4	GND		Ground
5	GND		Ground
6	BUS	I/O	Bi-directional bus line
7	SI	I	Comparator Input, HV-Input
8	SO	O	5V-Comparator Output
9	n.c.		not connected
10	RxD	O	Receive Output, 5V-push-pull
11	TxD	I	5V-Transmit Input, pull-up-Input
12	GND		Ground
13	GND		Ground
14	RESET	O	5V-output reset, active low
15	SENSE	O	5V-output of VSUP-Monitoring
16	VCC	O	Regulator output 5V/100mA

7. Mechanical Specification - SOIC16WB



Small Outline Integrated Circiut (SOIC), SOIC 16, 300 mil

	D	E	H	A	A1	e	b	L	H
All Dimension in mm, coplanarity < 0.1 mm									
min max	10.1 10.5	7.40 7.60	10.00 10.65	2.35 2.65	0.10 0.30	1.27	0.33 0.51	0.40 1.27	0° 8°
All Dimension in inch, coplanarity < 0.004”									
min max	0.398 0.413	0.291 0.299	0.394 0.419	0.093 0.104	0.004 0.012	0.050	0.013 0.020	0.016 0.050	0° 8°

8. ESD/EMC Remarks

8.1 General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

8.2 ESD-Test

The TH8060 is tested according MIL883D (human body model).

8.3 EMC

The test on EMC impacts is done according to ISO 7637-1 for power supply pins and ISO 7637-3 for data- and signal pins.

Power Supply pin VSUP:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	5000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	5000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms / U_P+U_S = 40 V	10 pulses every 1min

Data- and signal pins EN, SI, BUS:

Testpulse	Condition	Duration
1	t_1 = 5 s / U_S = -100 V / t_D = 2 ms	1000 pulses
2	t_1 = 0.5 s / U_S = 100 V / t_D = 0.05 ms	1000 pulses
3a/b	U_S = -150 V/ U_S = 100 V burst 100ns / 10 ms / 90 ms break	1000 burst

9. Reliability Information

Melexis devices are classified and qualified regarding suitability for infrared, vapor phase and wave soldering with usual (63/37 SnPb-) solder (melting point at 183degC).
The following test methods are applied:

- IPC/JEDEC J-STD-020A (issue April 1999)
- Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices
- CECC00802 (issue 1994)
- Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality
- MIL 883 Method 2003 / JEDEC-STD-22 Test Method B102
- Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

For more information on manufacturability/solderability see quality page at our website: http://www.melexis.com/

10. Disclaimer

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