REVISIONS		
NO.	DESCRIPTION	APPROVED
1	V1.0	2000-02-25

DATA-SHEET

MZP404

Impulse Intermediate Buffer IC

Purpose

- *buffer short pulse transients from resolver converter MIP200*
- *especially for connection to optoelectronical encoders with resolver converter MIP200*
- *applications in high-resolution linear and rotary position measurement*

Index

MAZeT GmbH Sales office Göschwitzer Straße 32 D-07745 Jena / Germany Phone: +49/3641-2809-0 Fax: +49/3641-2809-12 Email: sales@MAZeT.de	**Approvals**	**Date**	**MAZeT GmbH**	
	Drawn	2000-02-25	Status: Data sheet	
	Checked	2000-02-25		
	Released	2000-02-25	DOC. NO: DB-99-050e	Sheet 1 OF 4

1. DESCRIPTION

The interpolation principle of the MIP200GC circuit uses an integrated clock generator. The non-stabilised frequency depends on processing technology and environmental parameters like voltage and temperature. It is typically at 25 MHz, but may vary up to approx. 38 MHz. Since the square wave output signals are a result of the system clock frequency, edges of the output signals occur at integer multiples of the clock frequency only. The minimum time interval between successive edges is approx. 27ns at maximum clock frequency. That means in order to keep track with the square waves it is necessary t use a counter with a counter frequency of at least 40 MHz (e.g. MAC4124A).
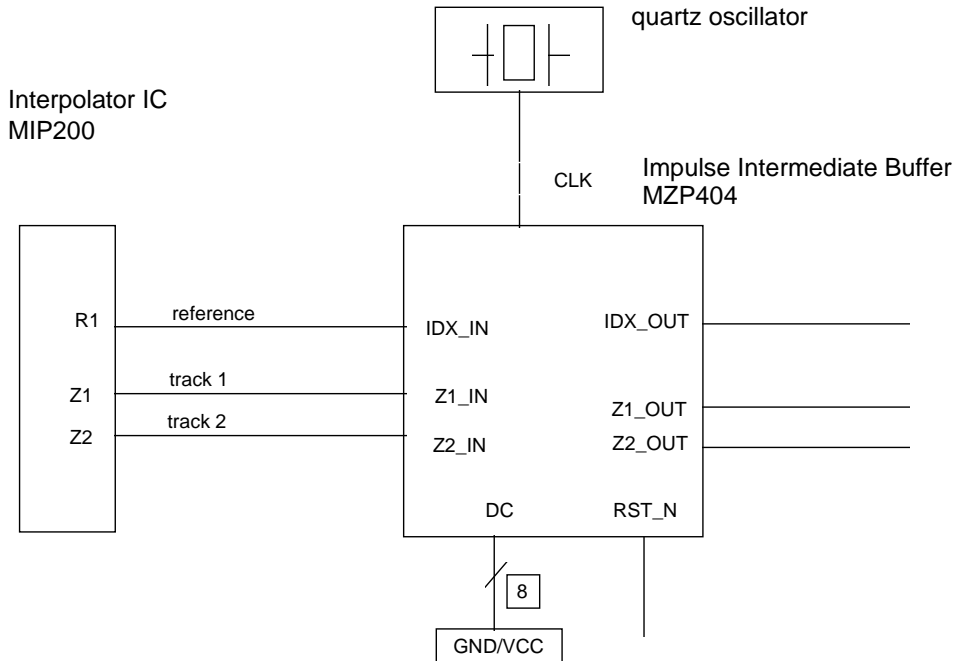

Figure: Application for MZP404

The pulse transient buffer IC MZP404 targets at applications with counter IC's having a lower input frequency then 40 MHz.

The square wave output signals Z1 and Z2 of the encoder resolver MIP200, connected to the inputs Z1_IN and Z2_IN of the IC MZP404, are sampled with the frequency at pin CLK and the edge events are saved to the internal FIFO memory. The MZP404 outputs square wave signals at pins Z1_OUT and Z2_OUT at frequency adjustable with DC[7:0]. The index signal (also known as reference signal) at IDX_IN outputs at IDX_OUT in-phase to the square wave signals Z1_OUT and Z2_OUT.

The resources of the used CPLD limit the „FIFO-depth" of the MZP404, i.e. it's possible to record 7 sequent edges of the same direction. Because of the sporadic nature of sequent edges with minimum time interval and simultaneously output of accumulated edge events at pins Z1_OUT and Z2_OUT at clock CLK the function of the MZP404 is warranted. The conditions for this is that the frequency of the square wave input of the MZP404 (i.e. interpolation factor * resolution of the encoder * rotations per second) is lower the frequency of the square wave output signals at Z1_OUT and Z2_OUT (= fCLK/4*[1+dc]). The value "dc" is binary adjustable at the inputs DC[7:0]. The value dc=0 is illegal.

The externally provided clock frequency at pin CLK has to be higher than 40 MHz to sample the minimum time interval of about 27ns between sequent edges of the square wave input signals. With 40 MHz clock frequency a maximum frequency at outputs Z1_OUT and Z2_OUT of 5 MHz can be reached (dc=1).

In order to reach the maximum square wave output frequency of MIP200 (6.25 MHz) at it's typical clock frequency f_{typ} =25 MHz it requires a clock frequency of 50 MHz at pin CLK of MZP404 and dc=1.

The function of the MZP404 results in a time delay of the edges of the output square waves in respect to the input square waves. The maximum time delay is fCLK/[1+dc].
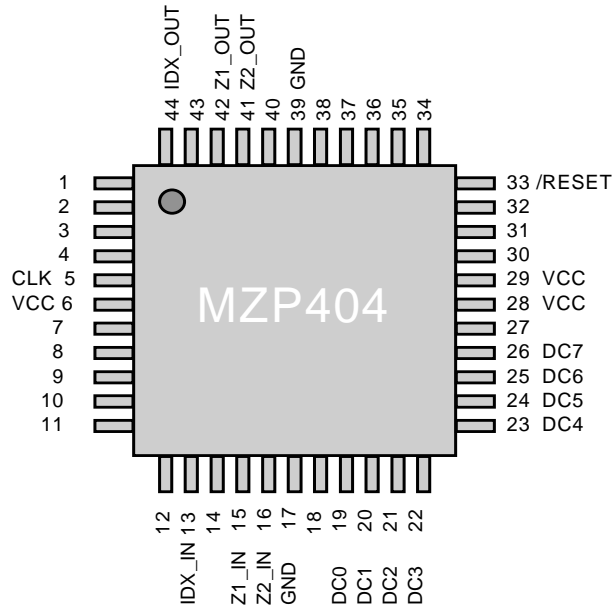
Example: f $_{CLK}$ = 50 MHz

dc	f$_{out}$ [MHz]	Delay [µs]
1	6.25	0.04
9	1.25	0.20
24	500 kHz	0.50
49	250 kHz	1.00
99	125 kHz	2.00
255	48.75 kHz	5.12

2. PIN OUT

IC: Lattice ispLSI 2032
Package: TQFP44

Inputs:	Name	Pin-No.
	Z1_IN	15
	Z2	16
	IDX	13
	DEL-	26..
	CTR[7..0]	19
	CLK	5
	/RESET	33

Outputs:	Z1_OUT	42
	Z2_OUT	41
	IDX_OUT	44

The information in this publication is believed to be accurate in all respects at the time of publication. MAZeT reserves the right to make changes in its products without notice in order to improve design or performance characteristics.

DOC. NO:

DB-99-050e

Sheet 3 of 4

	REVISIONS	
NO	DESCRIPTION	APPROVED
1	V1.0	2000-02-25

3. SPECIFICATION

Absolute maximum ratings (from Lattice datasheet of CPLD ispLSI 2023)

parameter	symbol	min	max	unit
supply voltage	VDD	-0,3	7,0	V
power dissipation	PD		0,15	W
operating temperature	Ta	0	70	°C
storage temperature	Tstg	-55	150	°C

Recommended operating conditions

Parameter	symbol	conditions	min	max	unit
supply voltage	V_{DDA}		4,75	5,25	V

For more detailed information, please contact

MAZeT GmbH
Herr Dr. Mahler
Göschwitzer Str. 32
D-07745 Jena/Germany
Phone: +49 3641 2809-0
Telefax: +49 3641 2809-12
EMAIL: sales@MAZeT.de
http://www.MAZeT.de

DOC. NO:	Sheet 4 of 4
DB-99-050e	