19-3943; Rev 0; 1/06

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers



## General Description

The MAX9248/MAX9250 digital video serial-to-parallel converters deserialize a total of 27 bits during data and control phases. In the data phase, the LVDS serial input is converted to 18 bits of parallel video data and in the control phase, the input is converted to 9 bits of parallel control data. The separate video and control phases take advantage of video timing to reduce the serial-data rate. The MAX9248/MAX9250 pair with the MAX9247 serializer to form a complete digital video transmission system. For operating frequencies less than 35MHz, the MAX9248/MAX9250 can also pair with the MAX9217 serializer.

The MAX9248 features spread-spectrum capability, allowing output data and clock to spread over a specified frequency range to reduce EMI. The data and clock outputs are programmable for a spectrum spread of ±4% or ±2%. The MAX9250 features output enable input control to allow data busing.

Proprietary data decoding reduces EMI and provides DC balance. The DC balance allows AC-coupling, providing isolation between the transmitting and receiving ends of the interface. The MAX9248/MAX9250 feature a selectable rising or falling output latch edge.

ESD tolerance is specified for ISO 10605 with ±10kV Contact Discharge and ±30kV Air-Gap Discharge.

The MAX9248/MAX9250 operate from a +3.3V ±10% core supply and feature a separate output supply for interfacing to 1.8V to 3.3V logic-level inputs. These devices are available in 48-lead TQFP and TQFN packages and are specified from -40°C to +85°C.

## Features

- **Programmable ±4% or ±2% Spread-Spectrum Output for Reduced EMI (MAX9248)**
- **Proprietary Data Decoding for DC Balance and Reduced EMI**
- **Control Data Deserialized During Video Blanking**
- **Five Control Data Inputs are Single-Bit-Error Tolerant**
- **Output Transition Time is Scaled to Operating Frequency for Reduced EMI**
- **Staggered Output Switching Reduces EMI**
- **Output Enable Allows Busing of Outputs (MAX9250)**
- **Clock Pulse Stretch on Lock**
- **Wide ±2% Reference Clock Tolerance**
- **Synchronizes to MAX9247 Serializer Without External Control**
- **ISO 10605 and IEC 61000-4-2 Level 4 ESD Protection**
- **Separate Output Supply Allows Interface to 1.8V to 3.3V Logic**
- **+3.3V Core Power Supply**
- **Space-Saving TQFP and TQFN Packages**
- **-40°C to +85°C Operating Temperature Range**

## Applications

Navigation System Displays

In-Vehicle Entertainment Systems

Video Cameras

LCD Displays

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|---|---|---|---|
| **MAX9248**ECM+ | -40°C to +85°C | 48 TQFP | C48-5 |
| MAX9248ETM+* | -40°C to +85°C | 48 TQFN-EP** | T4866-1 |
| **MAX9250**ECM+* | -40°C to +85°C | 48 TQFP | C48-5 |
| MAX9250ETM+* | -40°C to +85°C | 48 TQFN-EP** | T4866-1 |

*Future product—contact factory for availability.

**EP = Exposed pad.

+Denotes lead-free package.

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

## ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to _GND .....-0.5V to +4.0V
Any Ground to Any Ground .....-0.5V to +0.5V
IN+, IN- to LVDSGND .....-0.5V to +4.0V
IN+, IN- Short Circuit to LVDSGND or $V_{CCLVDS}$ .....Continuous
(R/$\overline{F}$, OUTEN, RNG_, REFCLK, SS $\overline{PWRDWN}$) to GND ..... -0.5V to ($V_{CC}$ + 0.5V)
(RGB_OUT[17:0], CNTL_OUT[8:0], DE_OUT, PCLK_OUT, $\overline{LOCK}$) to $V_{CCOGND}$ .....-0.5V to ($V_{CCO}$ + 0.5V)
Continuous Power Dissipation ($T_A$ = +70°C)
48-Lead TQFP (derate 20.8mW/°C above +70°C).....1667mW
48-Lead TQFN (derate 37mW/°C above +70°C).....2963mW

ESD Protection
Human Body Model ($R_D$ = 1.5kΩ, $C_S$ = 100pF)
All Pins to GND .....±3.0kV
ISO 10605 ($R_D$ = 2kΩ, $C_S$ = 330pF)
Contact Discharge (IN+, IN-) to GND .....±10kV
Air-Gap Discharge (IN+, IN-) to GND .....±30kV
IEC 61000-4-2 ($R_D$ = 330Ω, $C_S$ = 150pF)
Contact Discharge (IN+, IN-) to GND .....±8kV
Air-Gap Discharge (IN+, IN-) to GND .....±15kV
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to $V_{CC}$ - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.2V, $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SINGLE-ENDED INPUTS (R/$\overline{F}$, OUTEN, RNG0, RNG1, REFCLK, $\overline{PWRDWN}$, SS)** | | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | | 2.0 | | $V_{CC}$ + 0.3 | V |
| Low-Level Input Voltage | $V_{IL}$ | | | -0.3 | | +0.8 | V |
| Input Current | $I_{IN}$ | $\overline{PWRDWN}$ = high or low | $V_{IN}$ = -0.3V to 0 | -100 | | +20 | µA |
| | | | $V_{IN}$ = $V_{CC}$ to ($V_{CC}$ + 0.3V) | | | | |
| | | | $V_{IN}$ = 0 to $V_{CC}$ | -20 | | +20 | |
| Input Clamp Voltage | $V_{CL}$ | $I_{CL}$ = -18mA | | | | -1.5 | V |
| **SINGLE-ENDED OUTPUTS (RGB_OUT[17:0], CNTL_OUT[8:0], DE_OUT, PCLK_OUT, $\overline{LOCK}$)** | | | | | | | |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -100µA | | $V_{CCO}$ - 0.1 | | | V |
| | | $I_{OH}$ = -2mA, RNG1 = high | | $V_{CCO}$ - 0.35 | | | |
| | | $I_{OH}$ = -2mA, RNG1 = low | | $V_{CCO}$ - 0.4 | | | |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 100µA | | | | 0.1 | V |
| | | $I_{OL}$ = 2mA, RNG1 = high | | | | 0.3 | |
| | | $I_{OL}$ = 2mA, RNG1 = low | | | | 0.35 | |
| High-Impedance Output Current | $I_{OZ}$ | $\overline{PWRDWN}$ = low or OUTEN = low, $V_O$ = -0.3V to ($V_{CCO}$ + 0.3V) | | -10 | | +10 | µA |
| Output Short-Circuit Current | $I_{OS}$ | RNG1 = high, $V_O$ = 0 | | -10 | | -50 | mA |
| | | RNG1 = low, $V_O$ = 0 | | -7 | | -40 | |

## DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to $V_{CC}$ - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.2V, $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **LVDS INPUT (IN+, IN-)** | | | | | | | | |
| Differential Input High Threshold | $V_{TH}$ | (Note 3) | | | | | 50 | mV |
| Differential Input Low Threshold | $V_{TL}$ | (Note 3) | | | -50 | | | mV |
| Input Current | $I_{IN+}$, $I_{IN-}$ | $\overline{PWRDWN}$ = high or low (Note 3) | | | -40 | | +40 | µA |
| Input Bias Resistor (Note 3) | $R_{IB}$ | $\overline{PWRDWN}$ = high or low | | | 42 | 60 | 78 | kΩ |
| | | $V_{CC\_}$ = 0 or open, $\overline{PWRDWN}$ = 0 or open, Figure 1 | | | 42 | 60 | 78 | |
| Power-Off Input Current | $I_{INO+}$, $I_{INO-}$ | $V_{CC\_}$ = 0 or open, $\overline{PWRDWN}$ = 0 or open (Note 3) | | | -60 | | +60 | µA |
| **POWER SUPPLY** | | | | | | | | |
| Worst-Case Supply Current | | MAX9248 $C_L$ = 8pF, worst-case pattern, Figure 2 | RNG1 = low, RNG0 = low | 2.5MHz | | | 31 | mA |
| | | | | 5MHz | | | 48 | |
| | | | RNG1 = low, RNG0 = high | 5MHz | | | 40 | |
| | | | | 10MHz | | | 70 | |
| | | | RNG1 = high, RNG0 = low | 10MHz | | | 49 | |
| | | | | 20MHz | | | 87 | |
| | | | RNG1 = high, RNG0 = high | 20MHz | | | 68 | |
| | | | | 42MHz | | | 120 | |
| Power-Down Supply Current | $I_{CCZ}$ | (Note 4) | | | | | 50 | µA |

## AC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, $C_L$ = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to $V_{CC}$ - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.2V, $T_A$ = +25°C.) (Notes 3, 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **REFCLK TIMING REQUIREMENTS** | | | | | | | |
| Period | $t_T$ | | | 23.8 | | 400.0 | ns |
| Frequency | $f_{CLK}$ | | | 2.5 | | 42.0 | MHz |
| Frequency Variation | $\Delta f_{CLK}$ | REFCLK to serializer PCLK_IN | | -2.0 | | +2.0 | % |
| Duty Cycle | DC | | | 40 | 50 | 60 | % |
| Transition Time | $t_{TRAN}$ | 20% to 80% | | | | 6 | ns |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| Output Rise Time | $t_R$ | Figure 3 | RNG1 = high | 2.2 | | 4.6 | ns |
| | | | RNG1 = low | 2.8 | | 5.2 | |
| Output Fall Time | $t_F$ | Figure 3 | RNG1 = high | 1.9 | | 4.0 | ns |
| | | | RNG1 = low | 2.3 | | 4.3 | |
| PCLK_OUT High Time | $t_{HIGH}$ | Figure 4 | | 0.4 x $t_T$ | 0.45 x $t_T$ | 0.6 x $t_T$ | ns |

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

## AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, $C_L$ = 8pF, $\overline{PWRDWN}$ = high, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID} / 2|$ to $V_{CC}$ - $|V_{ID} / 2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.2V, $T_A$ = +25°C.) (Notes 3, 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| PCLK_OUT Low Time | $t_{LOW}$ | Figure 4 | | 0.4 x $t_T$ | 0.45 x $t_T$ | 0.6 x $t_T$ | ns |
| Data Valid Before PCLK_OUT | $t_{DVB}$ | Figure 5 | | 0.35 x $t_T$ | 0.4 x $t_T$ | | ns |
| Data Valid After PCLK_OUT | $t_{DVA}$ | Figure 5 | | 0.35 x $t_T$ | 0.4 x $t_T$ | | ns |
| PLL Lock to REFCLK | $t_{PLLREF}$ | MAX9248, Figure 8 | | | | 33,600 x $t_T$ | ns |
| Spread-Spectrum Output Frequency (MAX9248) | $f_{PCLK\_OUT}$ | SS = high, Figure 11 | Maximum output frequency | $f_{REFCLK}$ + 3.6% | $f_{REFCLK}$ + 4.0% | $f_{REFCLK}$ + 4.4% | MHz |
| | | | Minimum output frequency | $f_{REFCLK}$ - 4.4% | $f_{REFCLK}$ - 4.0% | $f_{REFCLK}$ - 3.6% | |
| | | SS = low, Figure 11 | Maximum output frequency | $f_{REFCLK}$ + 1.8 % | $f_{REFCLK}$ + 2.0% | $f_{REFCLK}$ + 2.2% | |
| | | | Minimum output frequency | $f_{REFCLK}$ - 2.2% | $f_{REFCLK}$ - 2.0% | $f_{REFCLK}$ - 1.8% | |
| Spread-Spectrum Modulation Frequency | $f_{SSM}$ | Figure 11 | | | $f_{REFCLK}$ / 1024 | | kHz |
| Power-Down Delay | $t_{PDD}$ | Figures 7, 8 | | | | 100 | ns |
| SS Change Delay | $t_{\Delta SSPLL}$ | MAX9248, Figure 17 | | | | 32,800 x $t_T$ | ns |

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except $V_{TH}$ and $V_{TL}$.

**Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at $T_A$ = +25°C.

**Note 3:** Parameters are guaranteed by design and characterization, and are not production tested. Limits are set at ±6 sigma.

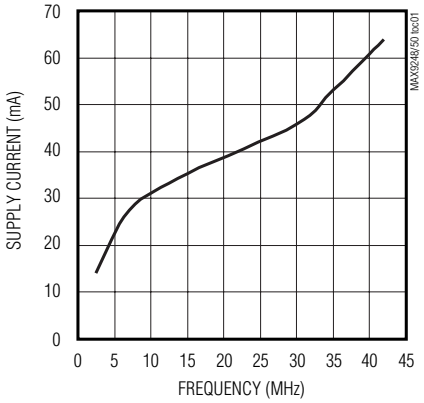
**Note 4:** All LVTTL/LVCMOS inputs, except $\overline{PWRDWN}$ at ≤ 0.3V or ≥ $V_{CC}$ - 0.3V. $\overline{PWRDWN}$ is ≤ 0.3V, REFCLK is static.

**Note 5:** $C_L$ includes probe and test jig capacitance.

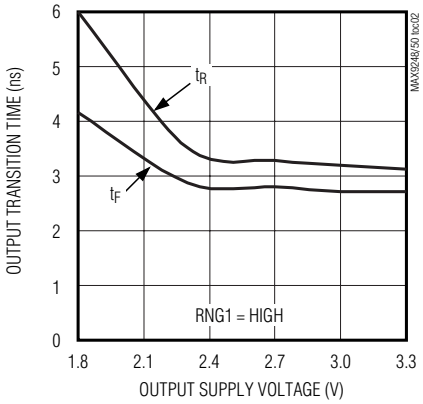
## Typical Operating Characteristics

($V_{CC\_}$ = +3.3V, $C_L$ = 8pF, $T_A$ = +25°C, unless otherwise noted.)

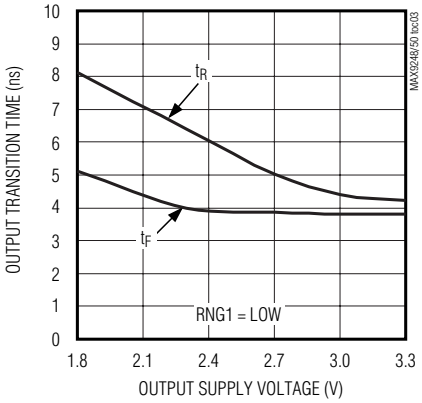
**WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY (MAX9248)**



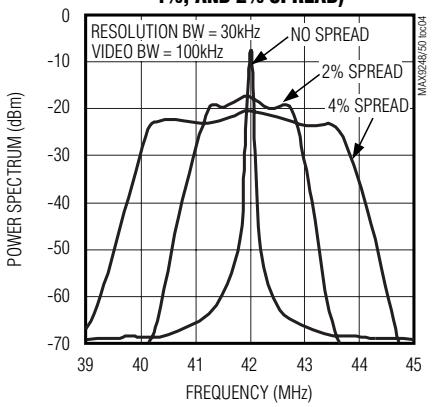

**OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE ($V_{CCO}$)**



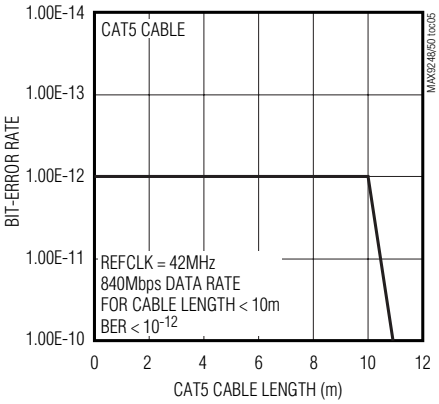

**OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE ($V_{CCO}$)**



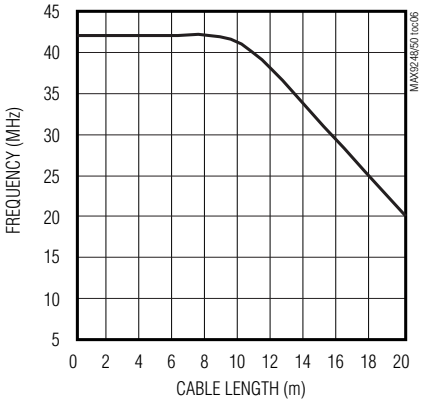

**OUTPUT POWER SPECTRUM vs. FREQUENCY (REFCLK = 42MHz, NO SPREAD, 4%, AND 2% SPREAD)**




**BIT-ERROR RATE vs. CABLE LENGTH**




**CABLE LENGTH vs. FREQUENCY BIT-ERROR RATE < 10E-9**



# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

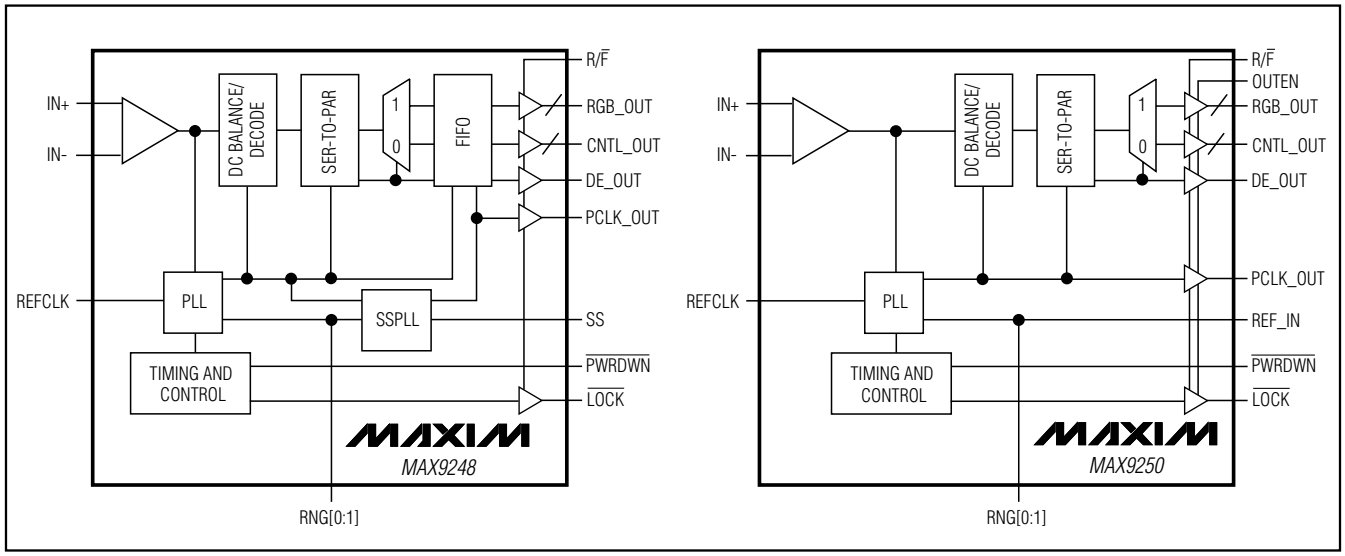
## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX9248 | MAX9250 | | |
| 1 | 1 | R/$\overline{F}$ | Rising or Falling Latch Edge Select. LVTTL/LVCMOS input. Selects the edge of PCLK_OUT for latching data into the next chip. Set R/$\overline{F}$ = high for a rising latch edge. Set R/$\overline{F}$ = low for a falling latch edge. Internally pulled down to GND. |
| 2 | 2 | RNG1 | LVTTL/LVCMOS Range Select Input. Set to the range that includes the serializer parallel clock input frequency. Internally pulled down to GND. |
| 3 | 3 | $V_{CCLVDS}$ | LVDS Supply Voltage. Bypass to LVDSGND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin. |
| 4 | 4 | IN+ | Noninverting LVDS Serial-Data Input |
| 5 | 5 | IN- | Inverting LVDS Serial-Data Input |
| 6 | 6 | LVDSGND | LVDS Supply Ground |
| 7 | 7 | PLLGND | PLL Supply Ground |
| 8 | 8 | $V_{CCPLL}$ | PLL Supply Voltage. Bypass to PLLGND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin. |
| 9 | 9 | RNG0 | LVTTL/LVCMOS Range Select Input. Set to the range that includes the serializer parallel clock input frequency. Internal pulldown to GND. |
| 10 | 10 | GND | Digital Supply Ground |
| 11 | 11 | $V_{CC}$ | Digital Supply Voltage. Supply for LVTTL/LVCMOS inputs and digital circuits. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin. |
| 12 | 12 | REFCLK | LVTTL/LVCMOS Reference Clock Input. Apply a reference clock that is within ±2% of the serializer PCLK_IN frequency. Internally pulled down to GND. |
| 13 | 13 | $\overline{PWRDWN}$ | LVTTL/LVCMOS Power-Down Input. Internally pulled down to GND. |
| 14 | — | SS | LVTTL/LVCMOS Spread-Spectrum Input. SS selects the frequency spread of PCLK_OUT and output data relative to PCLK_IN. Drive SS high for 4% spread and pull low for 2% spread. |
| 15–23 | 15–23 | CNTL_OUT0–CNTL_OUT8 | LVTTL/LVCMOS Control Data Outputs. CNTL_OUT[8:0] are latched into the next chip on the rising or falling edge of PCLK_OUT as selected by R/$\overline{F}$ when DE_OUT is low, and are held at the last state when DE_OUT is high. |
| 24 | 24 | DE_OUT | LVTTL/LVCMOS Data-Enable Output. High indicates RGB_OUT[17:0] are active. Low indicates CNTL_OUT[8:0] are active. |
| 25, 37 | 25, 37 | $V_{CCOGND}$ | Output Supply Ground |
| 26, 38 | 26, 38 | $V_{CCO}$ | Output Supply Voltage. Bypass to GND with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin. |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX9248 | MAX9250 | | |
| 27 | 27 | $\overline{LOCK}$ | LVTTL/LVCMOS Lock Indicator Output. Outputs are valid when $\overline{LOCK}$ is low. |
| 28 | 28 | PCLK_OUT | LVTTL/LVCMOS Parallel Clock Output. Latches data into the next chip on the edge selected by R/$\overline{F}$. |
| 29–36, 39–48 | 29–36, 39–48 | RGB_OUT0–RBG_OUT7, RGB_OUT8–RGB_OUT17 | LVTTL/LVCMOS Red, Green, and Blue Digital Video Data Outputs. RGB_OUT[17:0] are latched into the next chip on the edge of PCLK_OUT selected by R/$\overline{F}$ when DE_OUT is high, and are held at the last state when DE_OUT is low. |
| — | 14 | OUTEN | LVTTL/LVCMOS Output Enable Input. High activates the single-ended outputs. Driving low places the single-ended outputs in high impedance. Internally pulled down to GND. |
| EP | EP | GND | Exposed Pad (TQFN Package Only). Connect to GND. |

## Functional Diagram



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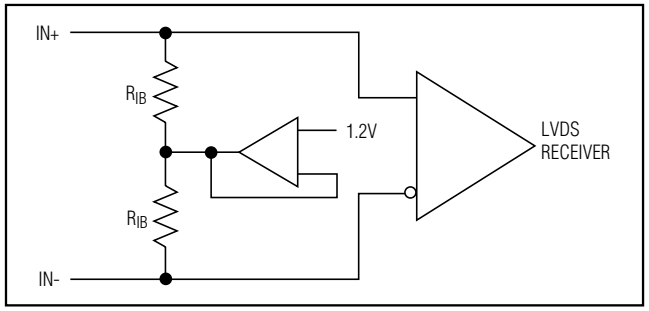



*Figure 1. LVDS Input Bias*

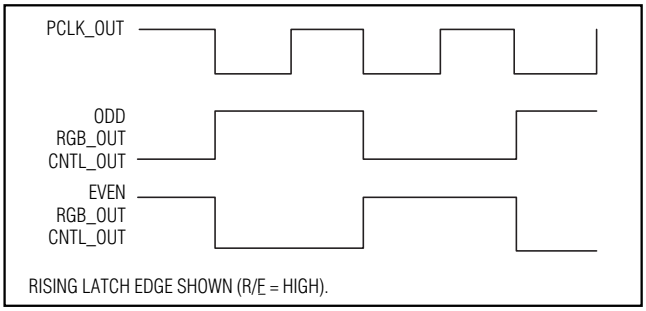



*Figure 2. Worst-Case Output Pattern*

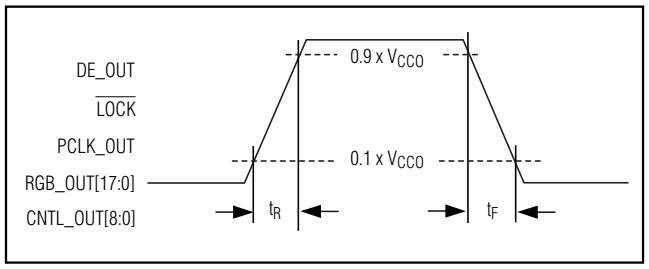



*Figure 3. Output Rise and Fall Times*

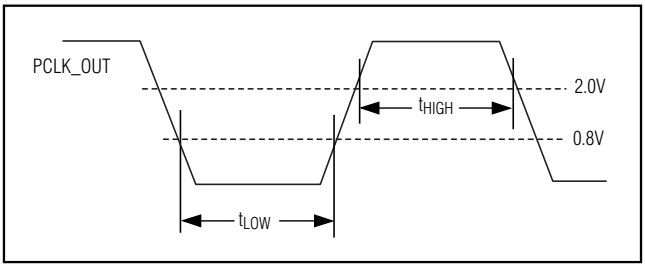



*Figure 4. High and Low Times*

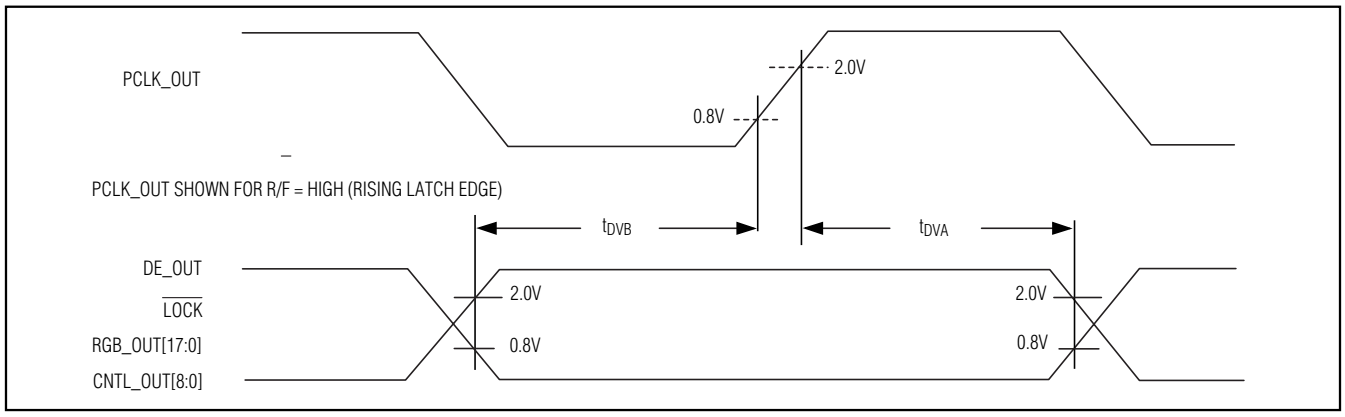



*Figure 5. Synchronous Output Timing*

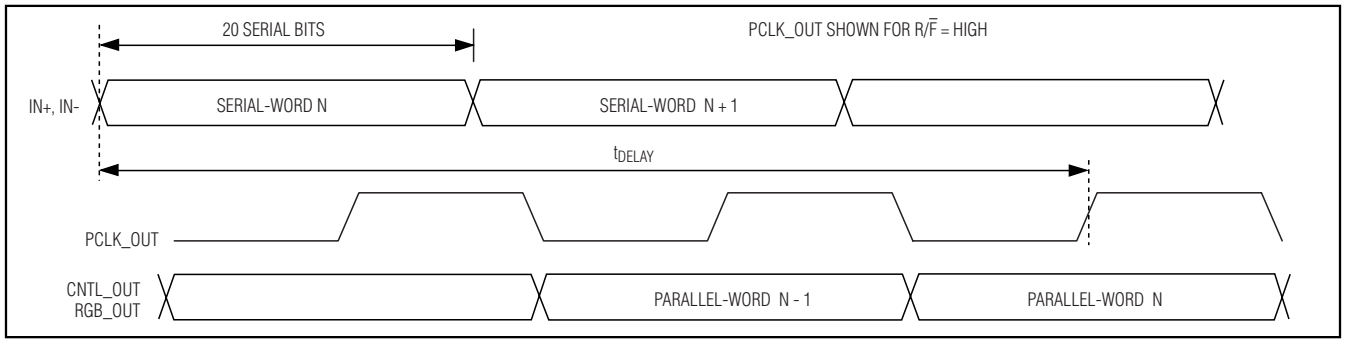



*Figure 6. Deserializer Delay*

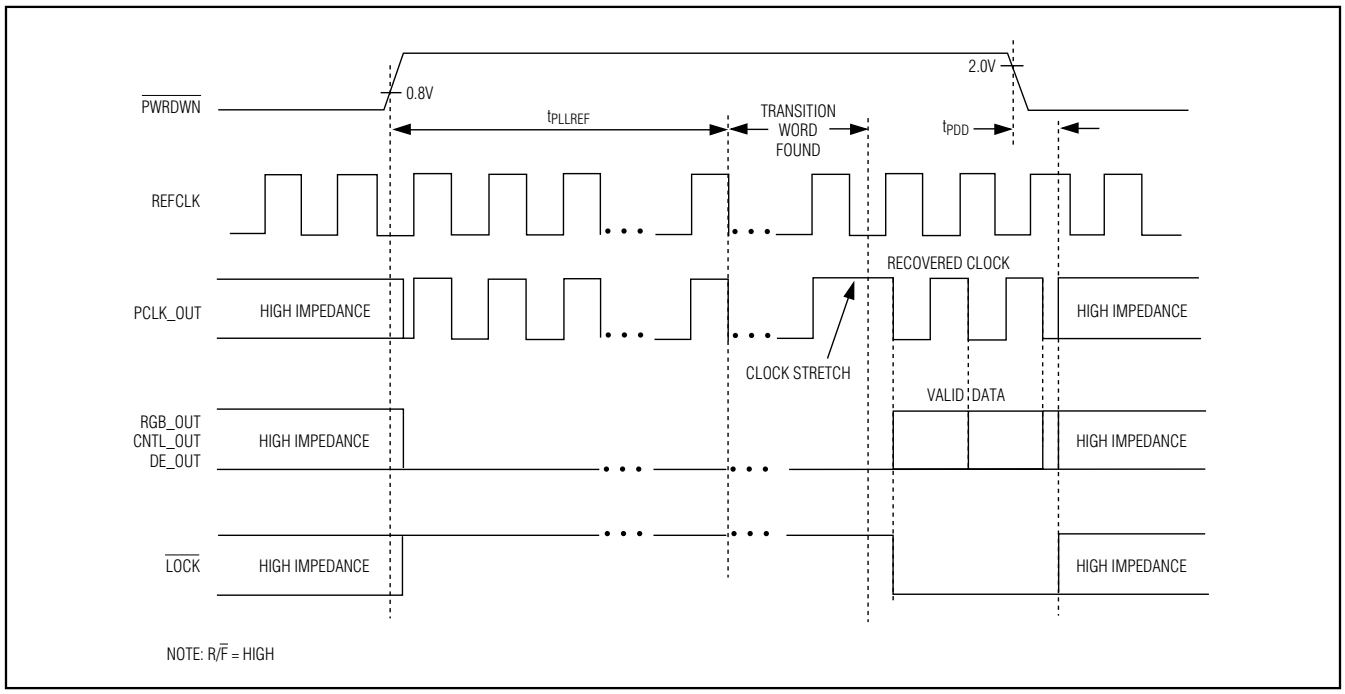



*Figure 7. PLL Lock to REFCLK and Power-Down Delay for MAX9250*

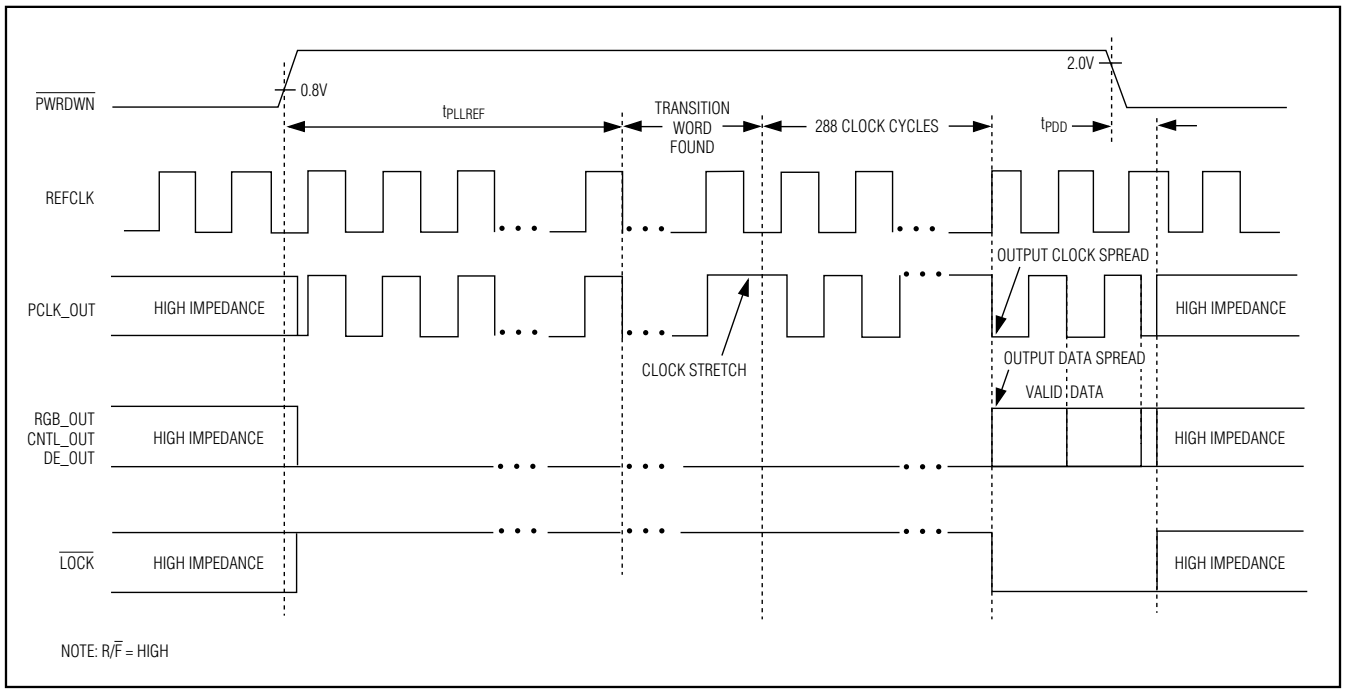



*Figure 8. PLL Lock to REFCLK and Power-Down Delay for MAX9248*

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

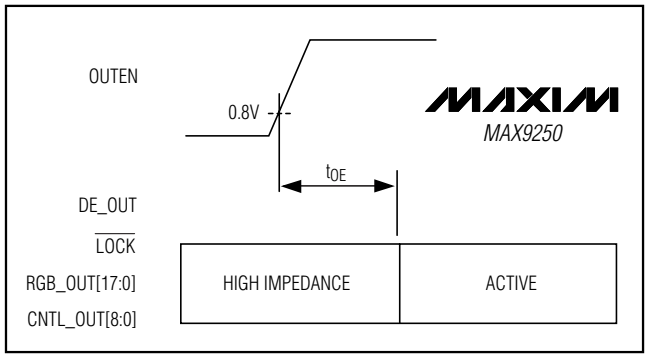



*Figure 9. Output Enable Time*

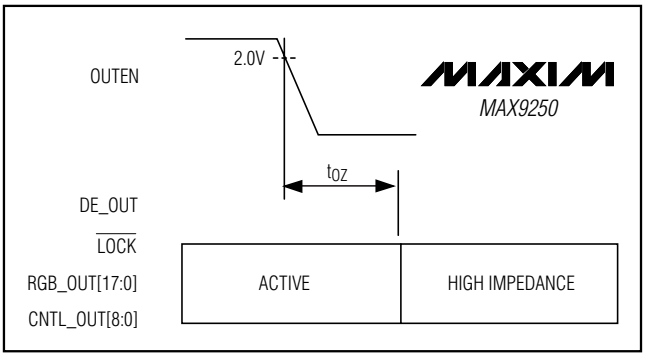



*Figure 10. Output Disable Time*

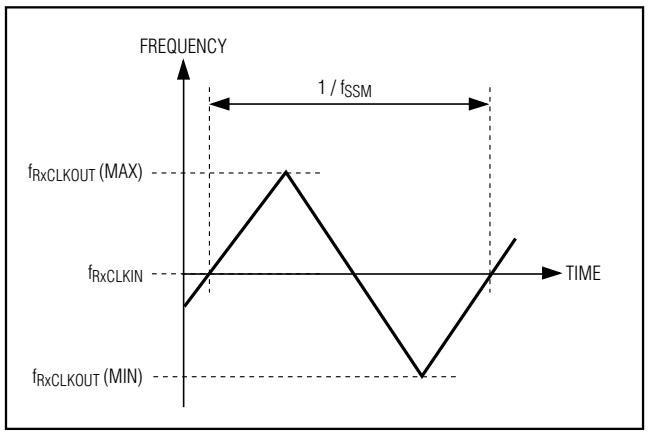



*Figure 11. Simplified Modulation Profile*

## Detailed Description

The MAX9248/MAX9250 DC-balanced deserializers operate at a 2.5MHz-to-42MHz parallel clock frequency, deserializing video data to the RGB_OUT[17:0] outputs when the data-enable output DE_OUT is high, or control data to the CNTL_OUT[8:0] outputs when DE_OUT is low. The outputs on the MAX9248 are programmable for ±2% or ±4% spread relative to the LVDS input clock frequency, while the MAX9250 has no spread, but has an output-enable input that allows output busing. The video phase words are decoded using two overhead bits, EN0 and EN1. Control phase words are decoded with one overhead bit, EN0. Encoding, performed by the MAX9247 serializer, reduces EMI and maintains DC balance across the serial cable. The serial-input word formats are shown in Tables 1 and 2.

Control data inputs C0 to C4, each repeated over three serial bit times by the serializer, are decoded using majority voting. Two or three bits at the same state determine the state of the recovered bit, providing single bit-error tolerance for C0 to C4. The state of C5 to C8 is determined by the level of the bit itself (no voting is used).

### AC-Coupling Benefits

AC-coupling increases the input voltage of the LVDS receiver to the voltage rating of the capacitor. Two capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise.

The MAX9247 serializer can also be DC-coupled to the MAX9248/MAX9250 deserializers. Figures 12 and 14 show the AC-coupled serializer and deserializer with two capacitors per link, and Figures 13 and 15 show the AC-coupled serializer and deserializer with four capacitors per link.

## Applications Information

### Selection of AC-Coupling Capacitors

See Figure 16 for calculating the capacitor values for AC-coupling depending on the parallel clock frequency. The plot shows capacitor values for two- and four-capacitor-per-link systems. For applications using less than 18MHz clock frequency, use 0.125µF capacitors.

### Termination and Input Bias

The IN+ and IN- LVDS inputs are internally connected to +1.2V through 42kΩ (min) to provide biasing for AC-coupling (Figure 1). Assuming 100Ω interconnect, the LVDS input can be terminated with a 100Ω resistor. Match the termination to the differential impedance of the interconnect.

Use a Thevenin termination, providing 1.2V bias, on an AC-coupled link in noisy environments. For interconnect with 100Ω differential impedance, pull each LVDS line up to $V_{CC}$ with 130Ω and down to ground with 82Ω at the deserializer input (Figures 12 and 15). This termination provides both differential and common-mode termination. The impedance of the Thevenin termination should be half the differential impedance of the interconnect and provide a bias voltage of 1.2V.

**Table 1. Serial Video Phase Word Format**

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EN0 | EN1 | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 | S17 |

*Bit 0 is the LSB and is deserialized first. EN[1:0] are encoding bits. S[17:0] are encoded symbols.*

**Table 2. Serial Control Phase Word Format**

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EN0 | C0 | C0 | C0 | C1 | C1 | C1 | C2 | C2 | C2 | C3 | C3 | C3 | C4 | C4 | C4 | C5 | C6 | C7 | C8 |

*Bit 0 is the LSB and is deserialized first. C[8:0] are the mapped control inputs.*

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

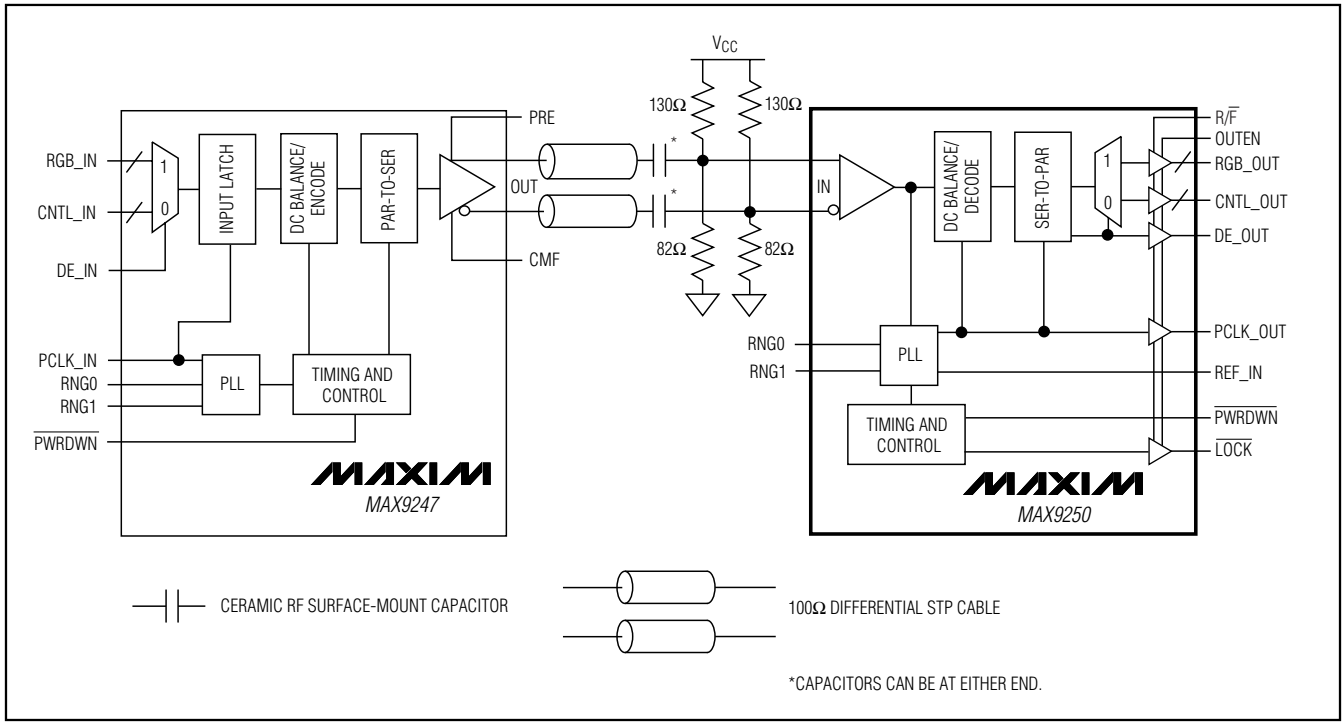



*Figure 12. AC-Coupled MAX9247 Serializer and MAX9250 Deserializer with Two Capacitors per Link*

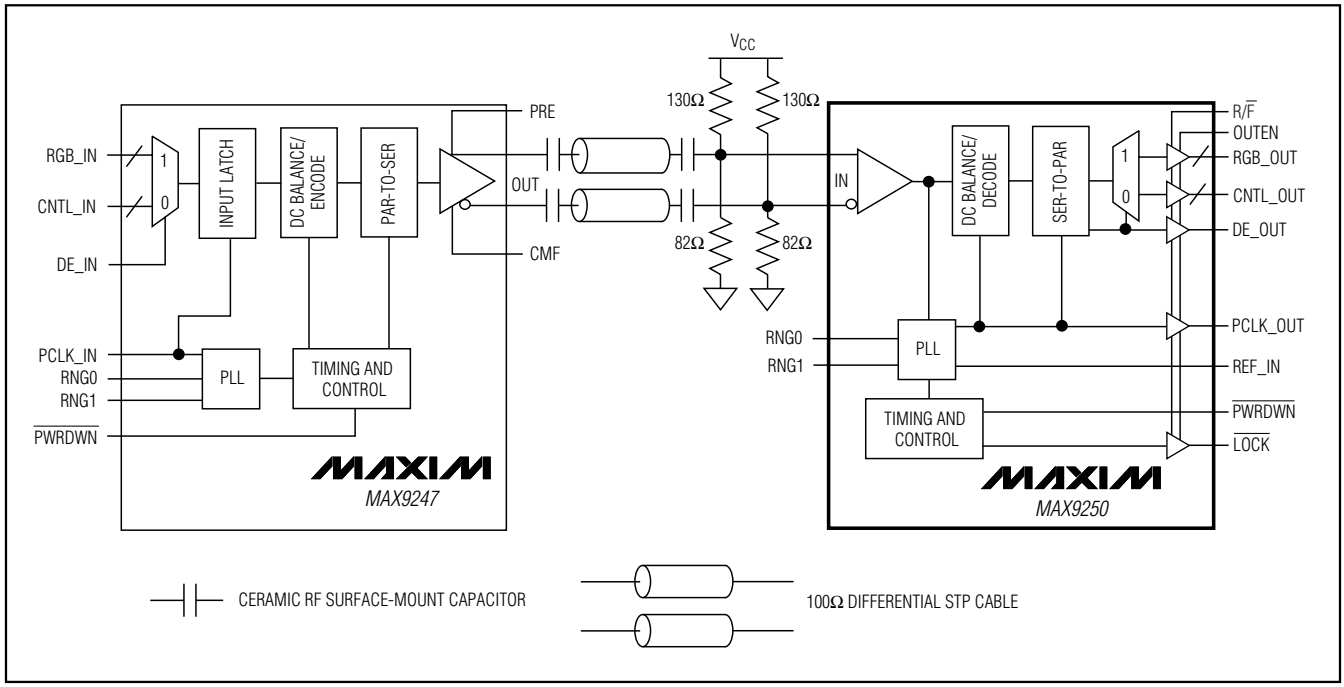



*Figure 13. AC-Coupled MAX9247 Serializer and MAX9250 Deserializer with Four Capacitors per Link*

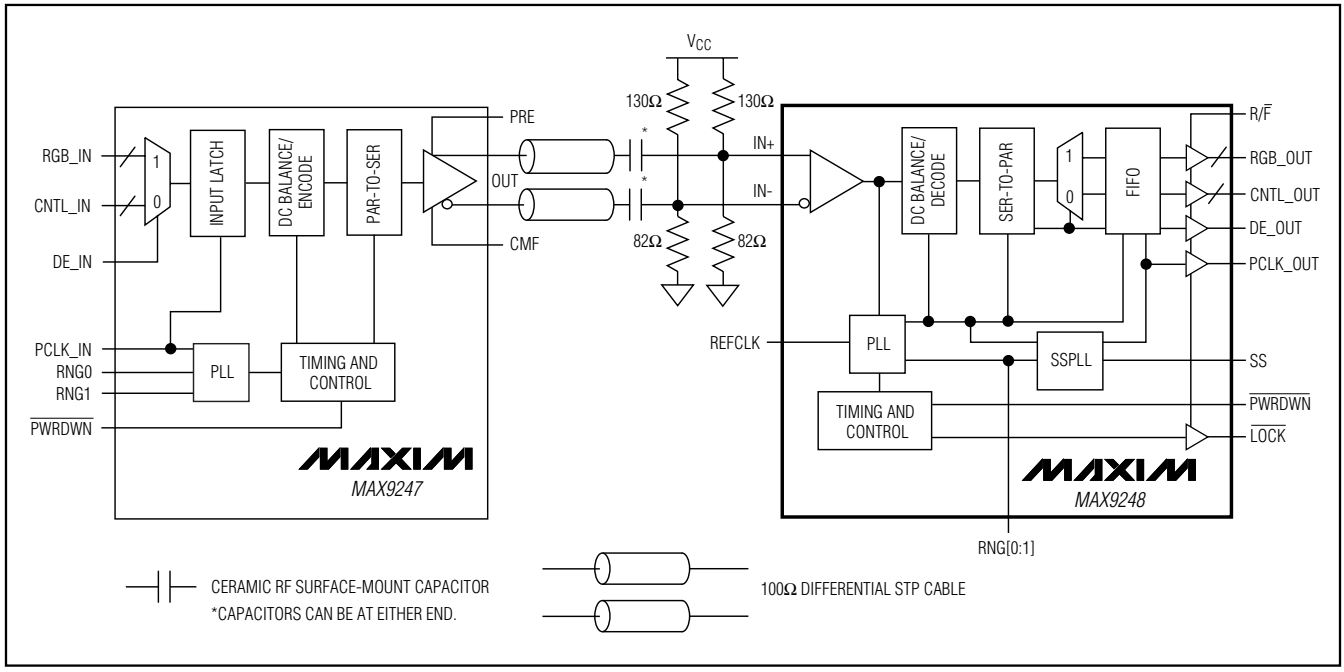



*Figure 14. AC-Coupled MAX9247 Serializer and MAX9248 Deserializer with Two Capacitors per Link*

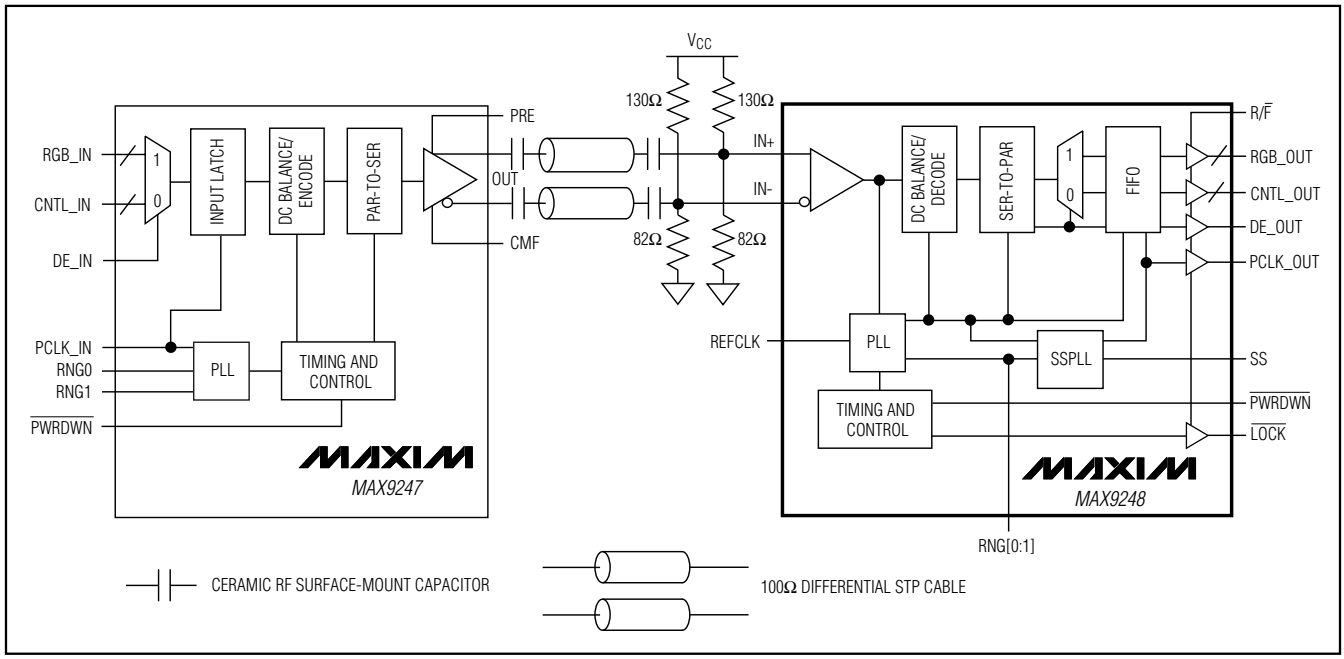



*Figure 15. AC-Coupled MAX9247 Serializer and MAX9248 Deserializer with Four Capacitors per Link*

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

### Input Frequency Detection

A frequency-detection circuit detects when the LVDS input is not switching. When not switching, all outputs except $\overline{LOCK}$ are low, $\overline{LOCK}$ is high, and PCLK_OUT follows REFCLK. This condition occurs, for example, if the serializer is not driving the interconnect or if the interconnect is open.

### Frequency Range Setting (RNG[1:0])

The RNG[1:0] inputs select the operating frequency range of the MAX9248/MAX9250 and the transition time of the outputs. Select the frequency range that includes the MAX9247 serializer PCLK_IN frequency. Table 3 shows the selectable frequency ranges and the corresponding data rates and output transition times.

## Table 3. Frequency Range Programming

| RNG1 | RNG0 | PARALLEL CLOCK (MHz) | SERIAL-DATA RATE (Mbps) | OUTPUT TRANSITION TIME |
|---|---|---|---|---|
| 0 | 0 | 2.5 to 5.0 | 50 to 100 | Slow |
| 0 | 1 | 5 to 10 | 100 to 200 | |
| 1 | 0 | 10 to 20 | 200 to 400 | Fast |
| 1 | 1 | 20 to 42 | 400 to 840 | |

### Power Down

Driving $\overline{PWRDWN}$ low puts the outputs in high impedance and stops the PLL. With $\overline{PWRDWN}$ ≤ 0.3V and all LVTTL/LVCMOS inputs ≤ 0.3V or ≥ $V_{CC}$ - 0.3V, the supply current is reduced to less than 50µA. Driving $\overline{PWRDWN}$ high initiates lock to the local reference clock (REFCLK) and afterwards to the serial input.

### Lock and Loss-of-Lock ($\overline{LOCK}$)

When $\overline{PWRDWN}$ is driven high, the PLL begins locking to REFCLK, drives $\overline{LOCK}$ from high impedance to high and the other outputs from high impedance to low, except PCLK_OUT. PCLK_OUT outputs REFCLK while the PLL is locking to REFCLK. Lock to REFCLK takes a maximum of 16,928 REFCLK cycles for the MAX9250. The MAX9248 has an additional spread-spectrum PLL (SSPLL) that also begins locking to REFCLK. Locking both PLLs to REFCLK takes a maximum of 33,600 REFCLK cycles for the MAX9248.

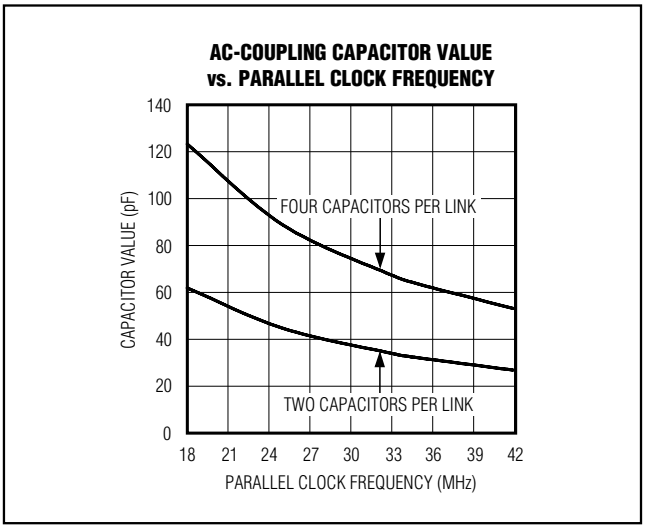



*Figure 16. AC-Coupling Capacitor Values vs. Clock Frequency of 18MHz to 42MHz*

When the MAX9248/MAX9250 complete their lock to REFCLK, the serial input is monitored for a transition word. When a transition word is found, $\overline{LOCK}$ output is driven low, indicating valid output data and the parallel rate clock recovered from the serial input is output on PCLK_OUT. The MAX9248 SSPLL waits an additional 288 clock cycles after the transition word is found before $\overline{LOCK}$ is driven low and sequence takes effect. PCLK_OUT is stretched on the change from REFCLK to recovered clock (or vice versa) at the time when the transition word is found.

If a transition word is not detected within $2^{22}$ cycles of PCLK_OUT, $\overline{LOCK}$ is driven high, the other outputs except PCLK_OUT are driven low. REFCLK is output on PCLK_OUT and the deserializer continues monitoring the serial input for a transition word. See Figure 7 for the MAX9250 and Figure 8 for the MAX9248 regarding the synchronization timing diagram.

The MAX9248 input-to-output delay can be as low as $(4.5t_T + 8.0)$ns or as high as $(36t_T + 16)$ns and due to spread-spectrum variations (see Figure 6).

### Spread-Spectrum Selection

The MAX9248 single-ended data and clock outputs are programmable for a variation of ±2% or ±4% around the LVDS input clock frequency. The modulation rate of the frequency variation is 32kHz for a 33MHz LVDS clock input and scales linearly with the clock frequency (see Table 4). The output spread is controlled through the SS input (see Table 5). Driving SS high spreads all data and clock outputs by ±4%, while pulling low spreads ±2%.

## Table 4. Modulation Rate

| $f_{PCLK\_IN}$ | $f_M$(kHz) = $f_{PCLK\_IN}$ / 1024 |
|---|---|
| 8 | 7.81 |
| 10 | 9.77 |
| 16 | 15.63 |
| 32 | 31.25 |
| 40 | 39.06 |
| 42 | 41.01 |

## Table 5. SS Function

| SS INPUT LEVEL | OUTPUT SPREAD |
|---|---|
| High | Data and clock output spread ±4% relative to REFCLK |
| Low | Data and clock output spread ±2% relative to REFCLK |

Any spread change causes a delay time of 32,000 x $t_T$ before output data is valid. When the spread amount is changed from ±2% to ±4% or vice versa, the data outputs go low for one $t_{\Delta SSPLL}$ delay (see Figure 17). The data outputs stay low, but are not valid when the spread amount is changed.

### Output Enable (OUTEN) and Busing Outputs

The outputs of two MAX9250s can be bused to form a 2:1 mux with the outputs controlled by the output enable. Wait 30ns between disabling one deserializer (driving OUTEN low) and enabling the second one (driving OUTEN high) to avoid contention of the bused outputs. OUTEN controls all outputs.

### Rising or Falling Output Latch Edge (R/$\overline{F}$)

The MAX9248/MAX9250 have a selectable rising or falling output latch edge through a logic setting on R/$\overline{F}$. Driving R/$\overline{F}$ high selects the rising output latch edge, which latches the parallel output data into the next chip on the rising edge of PCLK_OUT. Driving R/$\overline{F}$ low selects the falling output latch edge, which latches the parallel output data into the next chip on the falling edge of PCLK_OUT. The MAX9248/MAX9250 output-latch-edge polarity does not need to match the MAX9247 serializer input-latch-edge polarity. Select the latch-edge polarity required by the chip being driven by the MAX9248/MAX9250.

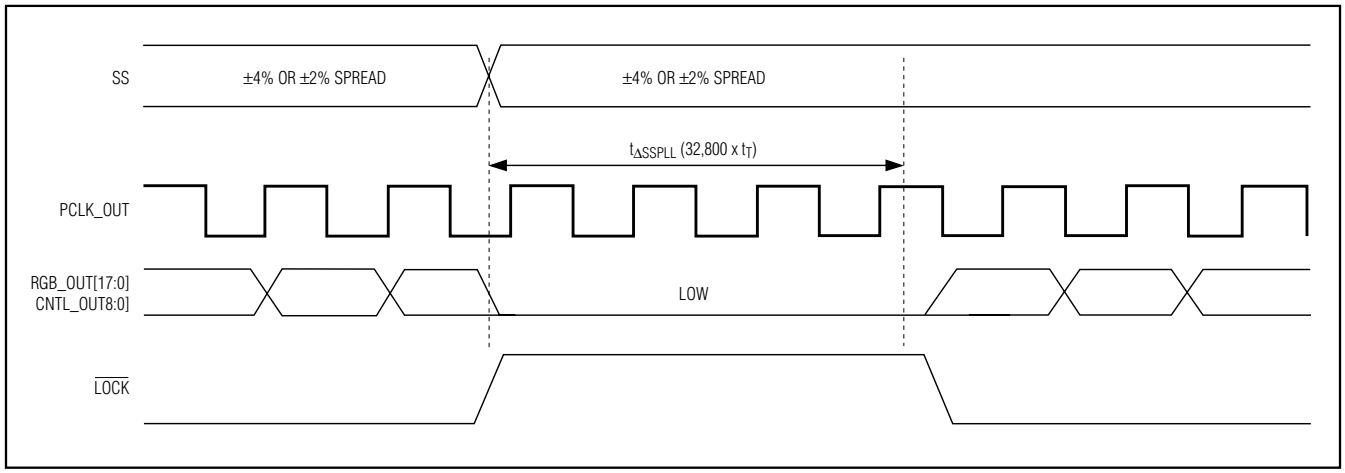



*Figure 17. Output Waveforms when Spread Amount is Changed*

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

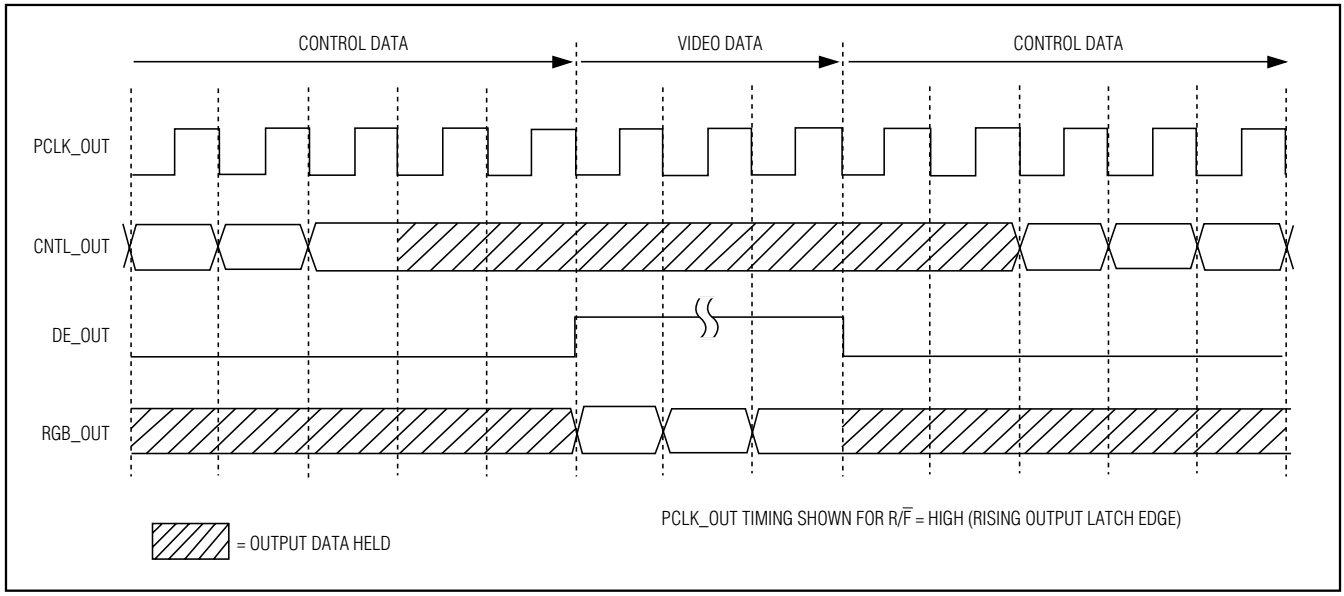



*Figure 18. Output Timing*

### Staggered and Transition Time Adjusted Outputs

RGB_OUT[17:0] are grouped into three groups of six, with each group switching about 1ns apart in the video phase to reduce EMI and ground bounce. CNTL_OUT[8:0] switch during the control phase. Output transition times are slower in the 2.5MHz-to-5MHz and 5MHz-to-10MHz ranges and faster in the 10MHz-to-20MHz and 20MHz-to-42MHz ranges.

### Data-Enable Output (DE_OUT)

The MAX9248/MAX9250 deserialize video and control data at different times. Control data is deserialized during the video blanking time. DE_OUT high indicates that video data is being deserialized and output on RGB_OUT[17:0]. DE_OUT low indicates that control data is being deserialized and output on CNTL_OUT[8:0]. When outputs are not being updated, the last data received is latched on the outputs. Figure 18 shows the DE_OUT timing.

### Power-Supply Circuits and Bypassing

There are separate on-chip power domains for digital circuits and LVTTL/LVCMOS inputs ($V_{CC}$ supply and GND), outputs ($V_{CCO}$ supply and $V_{CCOGND}$), PLL ($V_{CCPLL}$ supply and PLLGND), and the LVDS input ($V_{CCLVDS}$ supply and LVDSGND). The grounds are isolated by diode connections. Bypass each $V_{CC}$, $V_{CCO}$, $V_{CCPLL}$, and $V_{CCLVDS}$ pin with high-frequency, surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin. The outputs are powered from $V_{CCO}$, which accepts a 1.71V to 3.6V supply, allowing direct interface to inputs with 1.8V to 3.3V logic levels.

### Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

### Board Layout

Separate the LVTTL/LVCMOS outputs and LVDS inputs to prevent crosstalk. A four-layer PC board with separate layers for power, ground, and signals is recommended.

### IEC 61000-4-2 Level 4 and ISO 10605 ESD Protection

The MAX9248/MAX9250 ESD tolerance is rated for Human Body Model, IEC 61000-4-2 and ISO 10605.

The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. All LVDS inputs on the MAX9248/MAX9250 meet ISO 10605 ESD protection at ±30kV Air-Gap Discharge and ±10kV Contact Discharge and IEC 61000-4-2 ESD protection at ±15kV Air-Gap Discharge and ±8kV Contact Discharge. All other pins meet the Human Body Model ESD tolerance of ±3kV. The Human Body Model discharge components are $C_S$ = 100pF and $R_D$ = 1.5kΩ (Figure 19). The IEC 61000-4-2 discharge components are $C_S$ = 150pF and $R_D$ = 330Ω (see Figure 20). The ISO 10605 discharge components are $C_S$ = 330pF and $R_D$ = 2kΩ (Figure 21).

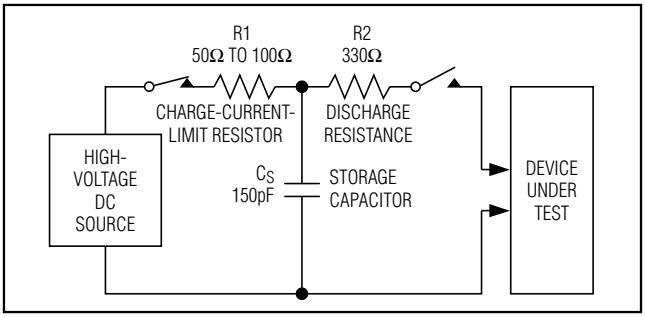



*Figure 20. IEC 61000-4-2 Contact Discharge ESD Test Circuit*

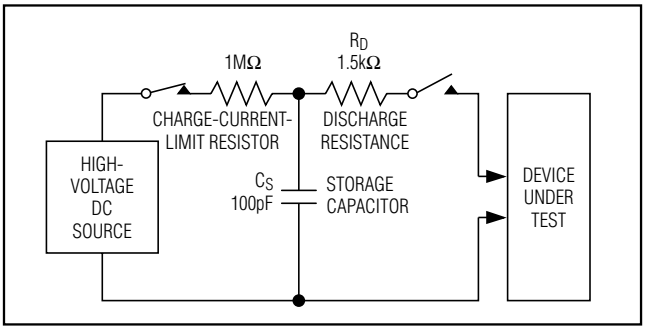



*Figure 19. Human Body ESD Test Circuit*

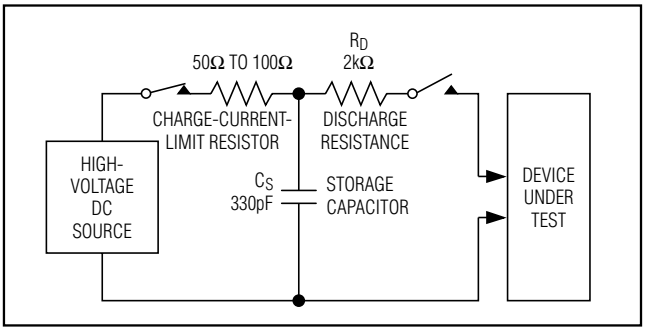
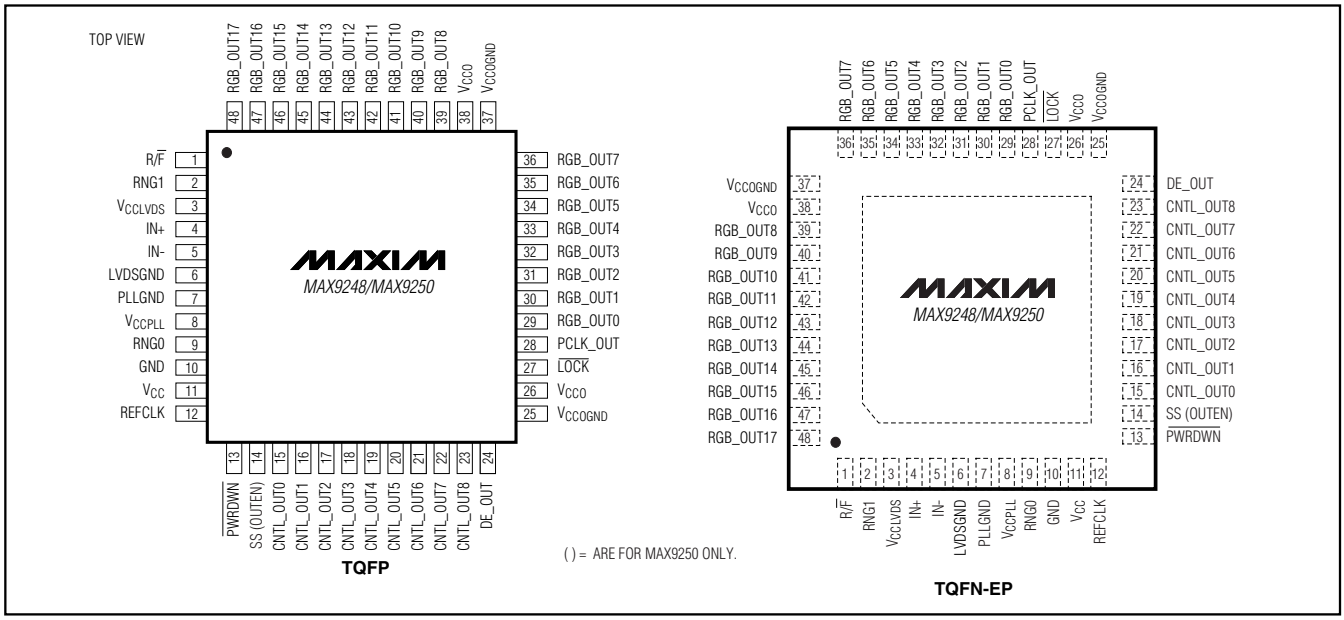



*Figure 21. ISO 10605 Contact Discharge ESD Test Circuit*

## Pin Configurations



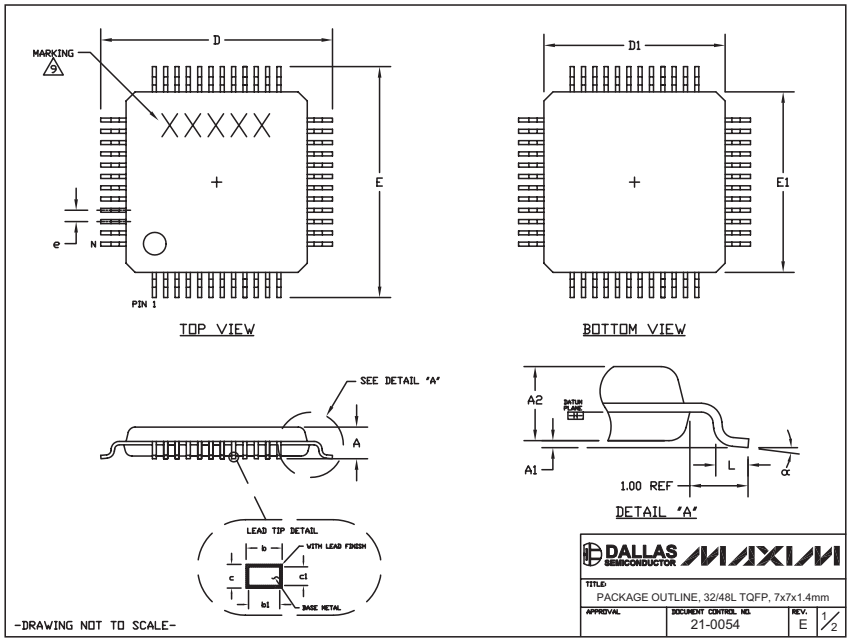

## Chip Information

PROCESS: CMOS

# 27-Bit, 2.5MHz-to-42MHz DC-Balanced LVDS Deserializers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)




NOTES:

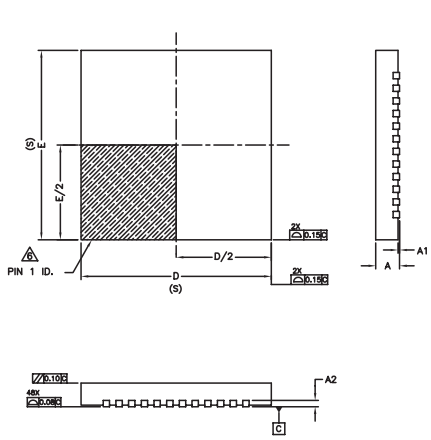
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

| JEDEC VARIATION | BBA | | BBC | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | -- | 1.60 | -- | 1.60 |
| $A_1$ | 0.05 | 0.15 | 0.05 | 0.15 |
| $A_2$ | 1.35 | 1.45 | 1.35 | 1.45 |
| D | 8.90 | 9.10 | 8.90 | 9.10 |
| $D_1$ | 6.90 | 7.10 | 6.90 | 7.10 |
| E | 8.90 | 9.10 | 8.90 | 9.10 |
| $E_1$ | 6.90 | 7.10 | 6.90 | 7.10 |
| e | 0.8 BSC. | | 0.5 BSC. | |
| L | 0.45 | 0.75 | 0.45 | 0.75 |
| b | 0.30 | 0.45 | 0.17 | 0.27 |
| b1 | 0.30 | 0.40 | 0.17 | 0.23 |
| c | 0.09 | 0.20 | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 | 0.09 | 0.16 |
| N | 32 | | 48 | |
| α | 0° | 7° | 0° | 7° |

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

48L THIN QFN.EPS




DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 48L THIN QFN 6x6x0.8mm BODY / 0.4mm LEAD PITCH

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0160 | A | 1/2 |

NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER TO JEDEC MO-220.
6. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
7. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

| | COMMON DIMENSIONS | | |
|---|---|---|---|
| SYMBOLS | MIN. | NOM. | MAX. |
| A | 0.700 | 0.750 | 0.800 |
| A1 | 0.000 | -- -- | 0.050 |
| A2 | | 0.200 REF. | |
| b | 0.150 | 0.200 | 0.250 |
| D | 5.900 | 6.000 | 6.100 |
| e | | 0.400 TYP. | |
| E | 5.900 | 6.000 | 6.050 |
| k | 0.250 | 0.350 | 0.450 |
| k1 | 0.350 | 0.450 | 0.550 |
| L | 0.400 | 0.500 | 0.600 |
| L1 | 0.300 | 0.400 | 0.500 |
| N | | 48 | |
| ND | | 12 | |
| NE | | 12 | |

| | EXPOSED PAD VARIATONS | | | | | |
|---|---|---|---|---|---|---|
| PKG. CODE | D2 | | | E2 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T4866-1 | 4.20 | 4.30 | 4.40 | 4.20 | 4.30 | 4.40 |

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 48L THIN QFN 6x6x0.8mm BODY / 0.4mm LEAD PITCH

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0160 | A | 2/2 |