19-3486; Rev 0; 11/04

10Gbps Clock and Data Recovery with Limiting Amplifier

General Description

The MAX3991 is a 10Gbps clock and data recovery (CDR) with limiting amplifier IC for XFP optical receivers. The MAX3991 and the MAX3992 (CDR with equalizer) form a signal conditioner chipset for use in XFP transceiver modules. The chipset is XFI compliant and offers multirate operation for data rates from 9.95Gbps to 11.1Gbps.

The MAX3991 has $7mV_{P-P}$ input sensitivity (BER ≤ 10^{-12}), which allows direct connection to a transimpedance amplifier without the use of a stand-alone limiting amplifier. The phase-locked loop (PLL) is optimized for jitter tolerance and provides 0.6UI of high-frequency tolerance in SONET, Ethernet, and Fibre-Channel applications. The MAX3991 output provides 27% margin to the XFP eye mask specification.

An AC-based power detector toggles the loss-of-signal (LOS) output when the input signal swing is below the user-programmed assert threshold. An external reference clock, with frequency equal to 1/64 or 1/16 of the serial data rate is used to aid in frequency acquisition. A loss-of-lock (LOL) indicator is provided to indicate the lock status of the receiver PLL.

The MAX3991 is available in a 4mm x 4mm, 24-pin QFN package. It consumes 350mW from a single +3.3V supply and operates over the 0°C to +85°C temperature range.

Applications

9.95Gbps to 11.1Gbps Optical XFP Modules

SONET OC-192/SDH STM-64 XFP Transceivers

10.3Gbps/11.1Gbps Ethernet XFP Transceivers

10.5Gbps Fibre-Channel XFP Transceivers

10Gbps DWDM Transceivers

Typical Application Circuit appears at end of data sheet.

Features

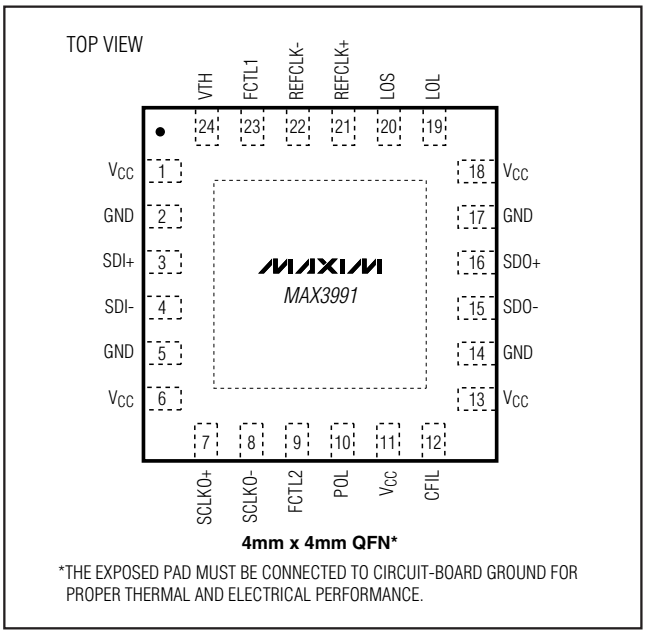
- **Multirate Operation from 9.95Gbps to 11.1Gbps**
- **$7mV_{P-P}$ Input Sensitivity (BER ≤ 10^{-12})**
- **$0.6UI_{P-P}$ Total High-Frequency Jitter Tolerance**
- **Low-Output Jitter Generation: $7mUI_{RMS}$**
- **Low-Output Deterministic Jitter: $4.6ps_{P-P}$**
- **XFI-Compliant Output Interface**
- **LOS Indicator with Programmable Threshold**
- **LOL Indicator**
- **Power Dissipation: 350mW**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3991UTG	0°C to +85°C	24 QFN	T2444-4
MAX3991UTG+*	0°C to +85°C	24 QFN	T2444-4

**Future product—contact factory for availability.*
+Denotes lead-free package.

Pin Configuration



4mm x 4mm QFN*

*THE EXPOSED PAD MUST BE CONNECTED TO CIRCUIT-BOARD GROUND FOR PROPER THERMAL AND ELECTRICAL PERFORMANCE.

10Gbps Clock and Data Recovery with Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +4.0V
Input Voltage Levels
(SDI+, SDI-, REFCLK+, REFCLK-) .....(V_{CC} - 1.0V) to (V_{CC} + 0.5V)
CML Output Voltage
(SDO+, SDO-, SCLKO+, SLCKO-) .....(V_{CC} - 1.0V) to (V_{CC} + 0.5V)
Voltage at (CFIL, LOL, VTH, POL, LOS, FCTL1, FCTL2) .....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
24-Pin QFN (derate 20.8mW/°C above +85°C) 1355mW
Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range.....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(See Table 1 for operating conditions. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			106	140	mA
DATA INPUT SPECIFICATION (SDI±)						
Single-Ended Input Resistance	R_{SE}		42	50	58	Ω
Differential Input Resistance	R_D		84	100	116	Ω
Single-Ended Input Resistance Matching					±5	%
Differential Input Return Loss	SDD11	0.1GHz to 5.5GHz (Note 1)		12.5		dB
		5.5GHz to 12GHz (Note 1)		6		
DC Cancellation Loop Low-Frequency Cutoff				30		kHz
REFERENCE CLOCK SPECIFICATION (REFCLK±)						
Single-Ended Input Resisitance			84	100	116	Ω
Differential Input Resistance			168	200	232	Ω
CML OUTPUT SPECIFICATION (SDO±)						
SDO± Differential Output Swing		(Note 2)	575	650	725	mV_{P-P}
SDO± Output Common-Mode Voltage		RL = 50Ω to V_{CC}		V_{CC} - 0.16		V
SCLKO± Differential Output				380		mV_{P-P}
Single-Ended Output Resistance			42	50	58	Ω
Differential Output Resistance	R_O		84	100	116	Ω
Single-Ended Output Resistance Matching					±5	%
Differential Output Return Loss	SDD22	0.1GHz to 5.5GHz (Note 1)		13		dB
		5.5GHz to 12GHz (Note 1)		8		
Common-Mode Output Return	SCC22	0.1GHz to 15GHz (Note 1)		5		dB
Rise/Fall Time		(20% to 80%) (Note 2)	18	23	30	ps
Output AC Common Mode		(Note 2)			10	mV_{RMS}
Power-Down Assert Time		(Note 3)			50	µs

ELECTRICAL CHARACTERISTICS (continued)

(See Table 1 for operating conditions. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
JITTER SPECIFICATION							
Jitter Peaking	J_P	120kHz < f ≤ 8MHz (Notes 2, 4)			0.05	0.25	dB
		f ≤ 120kHz (Notes 2, 4)				0.03	
Jitter Transfer Bandwidth	J_{BW}	(Notes 2, 4)			5.6	8.0	MHz
Sinusoidal Jitter Tolerance		(Notes 2, 4, 6)	f = 400kHz	3.0	>3 (Note 5)		UI_{P-P}
			f = 4MHz	0.55	>0.6 (Note 5)		
			f = 80MHz	0.45	>0.5 (Note 5)		
Jitter Generation		(Notes 2, 4, 7)			4.5	11.0	mUI_{RMS}
Serial Data Output Deterministic Jitter	DJ	PRBS 2^7 - 1 (Note 2)			4.6	13	ps_{P-P}
PLL ACQUISITION/LOCK SPECIFICATION							
Acquisition Time		Figures 1, 2 (Note 2)				200	µs
LOL Assert Time		Figure 1 (Note 2)				90	µs
Maximum Frequency Pullin Time		(Note 8)			2		ms
Frequency Difference at which LOL is Asserted	$\Delta f/f_{REFCLK}$	$\Delta f = \lvert f_{VCO} / N - f_{REFCLK} \rvert$, N = 16 or 64			651		ppm
Frequency Difference at which LOL is DeAsserted	$\Delta f/f_{REFCLK}$	$\Delta f = \lvert f_{VCO} / N - f_{REFCLK} \rvert$, N = 16 or 64			500		ppm
LOSS-OF-SIGNAL (LOS) SPECIFICATION							
VTH Control Voltage Range	VTH			150		500	mV
LOS Gain Factor	VTH/ V_{LOS_ASSERT}				10		V/V
Minimum LOS Assert Voltage	V_{LOS_ASSERT}				15		mV
Maximum LOS Assert Voltage	V_{LOS_ASSERT}				50		mV
LOS Gain-Factor Accuracy		(Notes 2, 9)		-1.5		+1.5	dB
LOS Hysteresis		(Notes 2, 10)		3.5	3.7	3.9	dB
LOS Gain-Factor Stability		(Note 2) Overtemperature and supply		-10		+10	%
LOS Assert Time		Figure 2 (Note 2)		3		90	µs
LOS Deassert Time		Figure 2 (Note 2)				90	µs
VTH Input Current				-5		+5	µA
LVTTL INPUT/OUTPUT SPECIFICATION (LOL, LOS, FCTL1, FCTL2)							
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Current				-30		+30	µA
Output High Voltage	V_{OH}	Sourcing 30µA		V_{CC} - 0.5			V
Output Low Voltage	V_{OL}	Sinking 1mA				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(See Table 1 for operating conditions. Typical values at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

Note 1: Measured with 100mV_{P-P} differential amplitude.
Note 2: Guaranteed by design and characterization.
Note 3: Measured from the time that the FCTL1 input goes high with FCTL2 = 0 to the time when the supply current drops to less than 40% of the nominal value.
Note 4: Measured with PRBS = 2^{31} - 1.
Note 5: Measurement limited by test equipment.
Note 6: Jitter tolerance is for BER ≤ 10^{-12}, measured with additional 0.1UI deterministic jitter and 40mV_{P-P} differential input.
Note 7: Measured with 50kHz to 80MHz SONET filter.
Note 8: Applies on power-up, after standby.
Note 9: Over process, temperature, and supply.
Note 10: Hysteresis is defined as 20Log($V_{LOS-DEASSERT}$ / $V_{LOS-ASSERT}$).

Table 1. Operating Conditions (Unless otherwise noted, FCTL1 = FCTL2 = 0.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.0		3.6	V
Ambient Temperature	T_A		0		+85	°C
Input Data Rate	Rb			(See Table 2)		Gbps
SDI± Differential Input Voltage Swing	V_D		15		1000	mV_{P-P}
Load Resistance	RL	RL is AC-coupled		50		Ω
REFCLK± Differential Input Voltage Swing			300		1600	mV_{P-P}
REFCLK Duty Cycle			30		70	%
REFCLK Frequency	f_{REFCLK}			Rb / 16		GHz
				Rb / 64		
REFCLK Accuracy		Relative to Rb / 16 or Rb / 64	-100		+100	ppm
REFCLK Rise/Fall Times (20% to 80%)		f_{REFCLK}= Rb / 64			1200	ps
		f_{REFCLK}= Rb / 16			300	
REFCLK Random Jitter		Noise bandwidth < 100MHz			10	ps_{RMS}

Table 2. Serial Data Rate and Reference Clock Frequency

APPLICATION	DATA RATE (Rb) (Gbps)	/16 REFERENCE CLOCK FREQUENCY (MHz)	/64 REFERENCE CLOCK FREQUENCY (MHz)
OC-192 SONET – SDH64	9.95328	622.08	155.52
OC-192 SONET Over FEC	10.664	666.5	166.625
ITU G.709	10.709	669.3125	167.328125
10Gbps Ethernet, IEEE 802.3ae	10.3125	644.53125	161.1328125
10 Gigabit Ethernet Over ITU G.709	11.09573	693.483125	173.3707813
10Gbps Fibre Channel	10.51875	657.421875	164.355469

***Note**: The part should be in standby mode when data rates are being switched.*

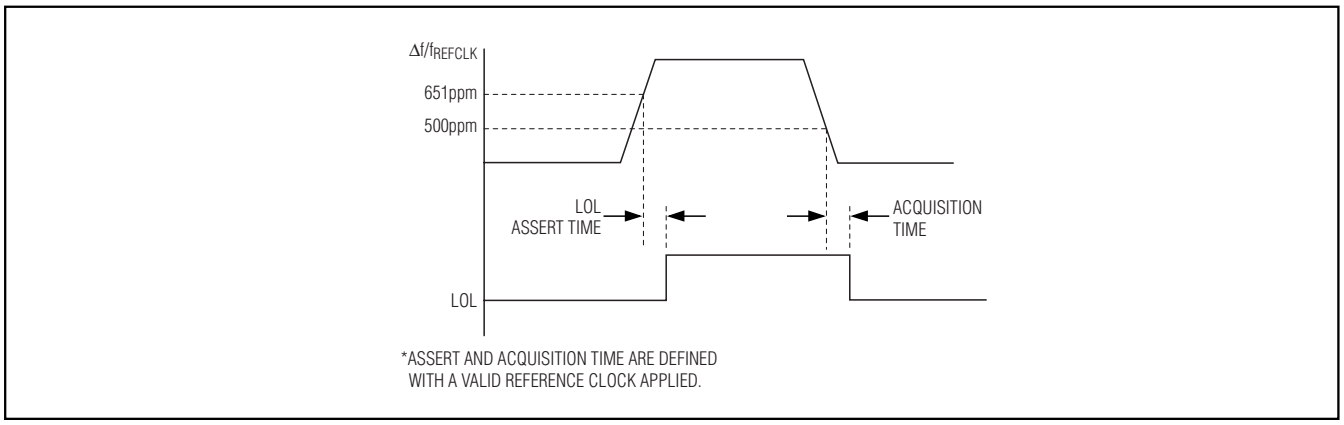


Figure 1. RX LOL Assert and PLL Acquisition Time

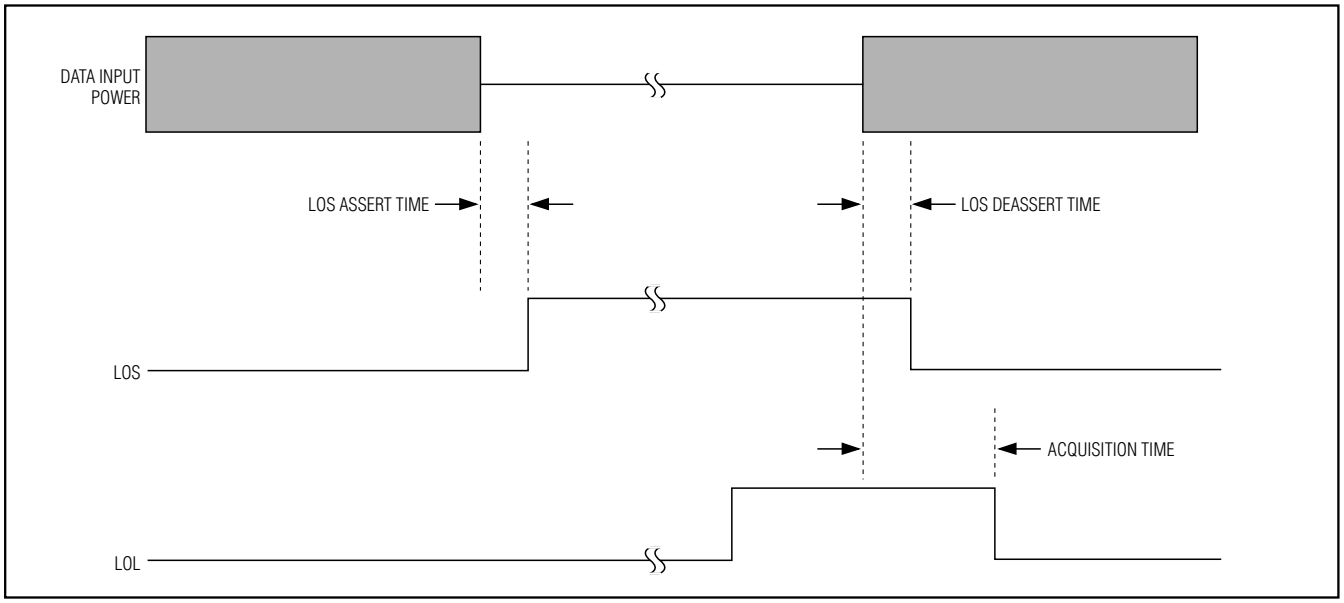


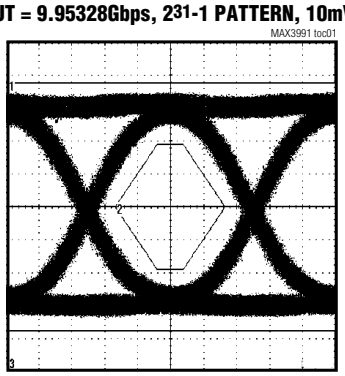
Figure 2. LOS Assert/Deassert Time

10Gbps Clock and Data Recovery with Limiting Amplifier

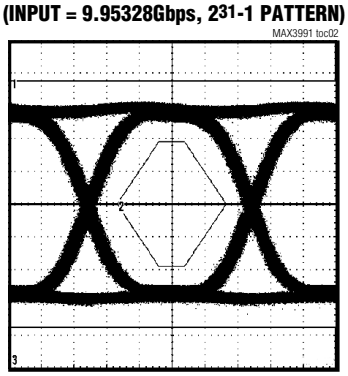
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

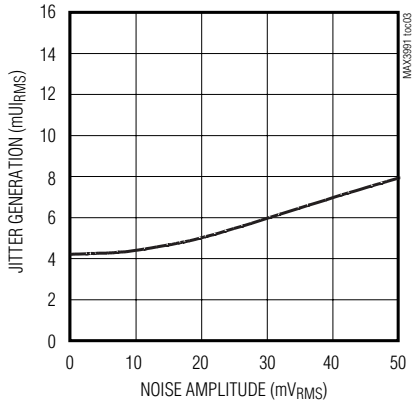
MAX3991 OUPTUT AFTER XFP CONNECTOR (INPUT = 9.95328Gbps, 2^{31}-1 PATTERN, 10mV$_{P-P}$)



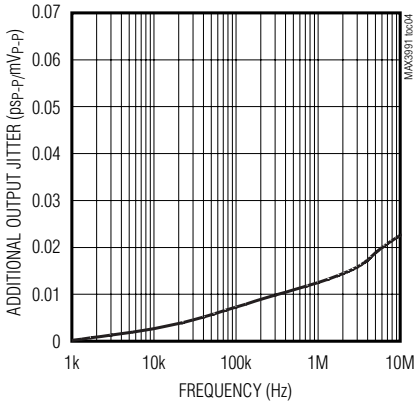
MAX3991 OUTPUT (INPUT = 9.95328Gbps, 2^{31}-1 PATTERN)



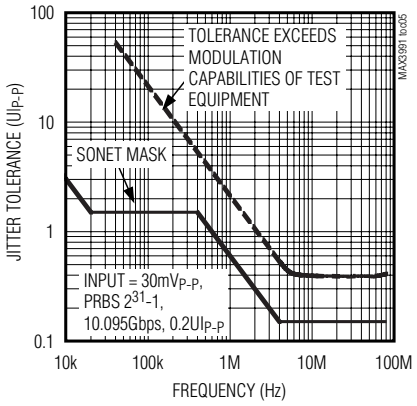
JITTER GENERATION vs. POWER-SUPPLY WHITE NOISE AMPLITUDE (BW < 100kHz)



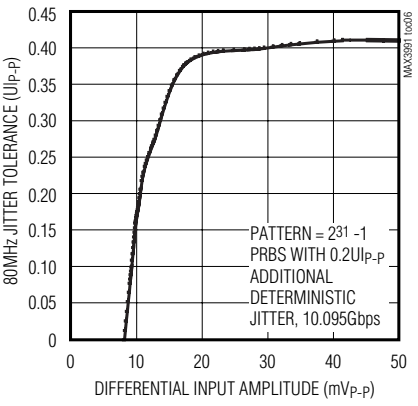
SUPPLY-INDUCED OUTPUT JITTER



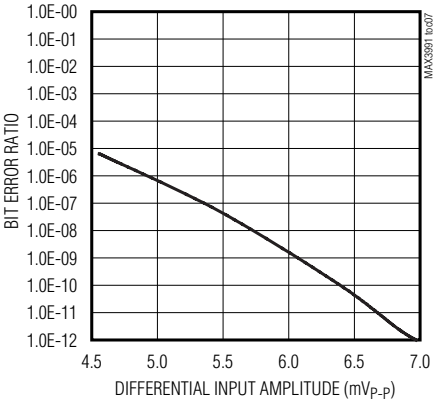
JITTER TOLERANCE vs. FREQUENCY



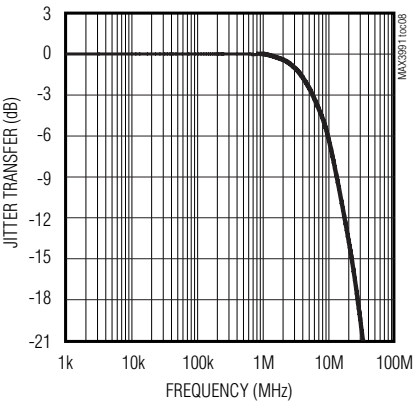
SINUSOIDAL JITTER TOLERANCE vs. INPUT AMPLITUDE



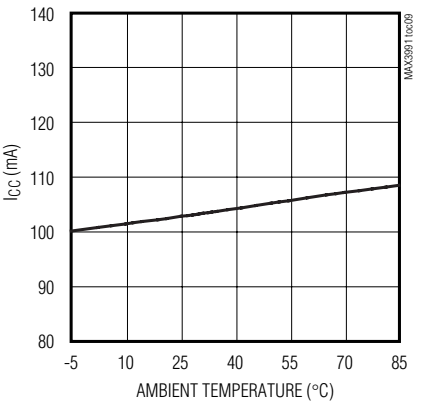
BIT ERROR RATIO vs. INPUT AMPLITUDE



JITTER TRANSFER



SUPPLY CURRENT vs. TEMPERATURE

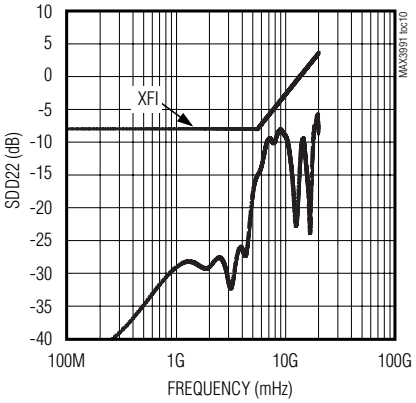


10Gbps Clock and Data Recovery with Limiting Amplifier

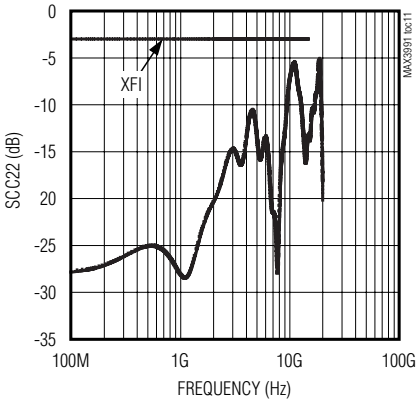
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

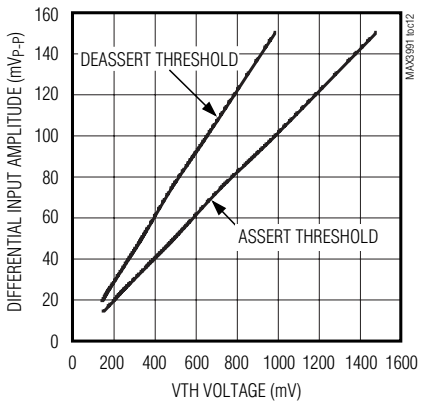
SDD22 vs. FREQUENCY



SCC22 vs. FREQUENCY



LOS ASSERT/DEASSERT LEVELS vs. VTH VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 6, 11, 13, 18	V_{CC}	+3.3V Power Supply
2, 5, 14, 17	GND	Supply Ground
3	SDI+	Positive Serial Input, CML
4	SDI-	Negative Serial Input, CML
7	SCLKO+	Positive Clock Output, CML. See Table 3 for information about enabling the SCLKO output (for use in device testing).
8	SCLKO-	Negative Clock Output, CML. See Table 3 for information about enabling the SCLKO output (for use in device testing).
9	FCTL2	Function Control Input 2, TTL. See Table 3 for more information.
10	POL	Data Polarity Control Input, TTL. Connect to V_{CC} or leave open to maintain the same polarity as the input. Connect to GND to invert the polarity of the data.
12	CFIL	Loop-Filter Capacitor Connection. Connect a 0.047µF capacitor between CFIL and V_{CC}.
15	SDO-	Negative Serial Data Output, CML
16	SDO+	Positive Serial Data Output, CML
19	LOL	Lock Status Indicator, TTL. This output goes high to indicate the receiver is out of lock.
20	LOS	Receiver Loss-of-Signal Indicator, TTL . This output goes high when the input signal drops below the programmed threshold.

10Gbps Clock and Data Recovery with Limiting Amplifier

Pin Description (continued)

PIN	NAME	FUNCTION
21	REFCLK+	Positive Reference Clock Input, Digital. The REFCLK inputs are designed to be AC-coupled to the reference clock source. REFCLK± have a 200Ω differential impedance. See the *Detailed Description* section for more information. See Table 2.
22	REFCLK-	Negative Reference Clock Input, Digital. The REFCLK inputs are designed to be AC-coupled to the reference clock source. REFCLK± have a 200Ω differential impedance. See the *Detailed Description* section for more information. See Table 2.
23	FCTL1	Function Control Input 1, TTL. See Table 3 for more information.
24	VTH	LOS Threshold Input, Analog. A voltage applied to this input sets the LOS assert threshold. The LOS power detector can be disabled if VTH is connected to V_{CC}, which forces LOS low.
EP	Exposed Pad	Supply Ground. The exposed pad must be soldered to the circuit-board ground for proper thermal and electrical performance. The MAX3991 uses exposed-pad variation T2444-4 in the package outline drawing. See the exposed-pad package.

Functional Diagram

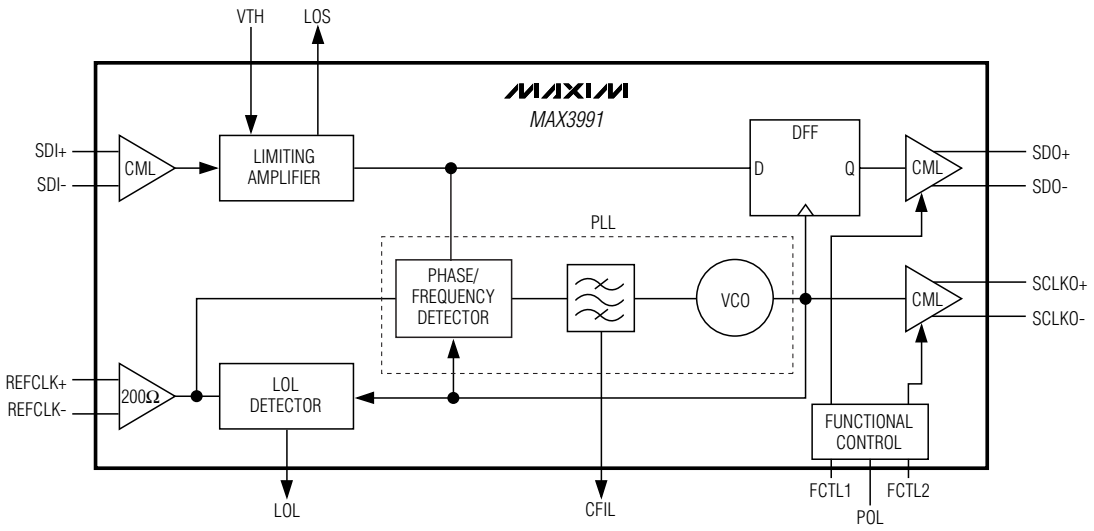


Figure 3. Functional Diagram

Detailed Description

The MAX3991 clock and data recovery with limiting amplifier restores data to XFI specifications. It consists of a limiting amplifier with LOS power detector, and a PLL data retimer with LOL indicator. An optional recovered clock may also be enabled for performance testing.

Limiting Amplifier

The SDI inputs of the MAX3991 accept serial NRZ data from the optical receiver assembly. The limiting amplifier accepts signals as small as $7mV_{P-P}$ and amplifies them to allow recovery by the CDR. The limiting amplifier uses an offset cancellation circuit to compensate for device mismatch within the gain stages. The low-frequency cut-off of the offset cancellation loop is typically 30kHz.

PLL Retimer

The integrated PLL recovers a synchronous clock, which is used to retime the input data. Connect a 0.047µF capacitor between CFIL and V_{CC} to provide PLL dampening. The external reference connected to REFCLK aids in frequency acquisition. Because the reference clock is only used for frequency acquisition, a low-quality reference clock can be used with no penalty in performance. The reference clock should be within ±100ppm of the bit rate divided by 16 or 64.

Loss-of-Lock Monitor

The LOL output indicates that the frequency difference between the recovered clock and the reference clock is excessive. LOL may assert due to excessive jitter at the data input, incorrect frequency, or loss of input data. The LOL detector monitors the frequency difference between the recovered clock and the reference clock. The LOL output is asserted high when the frequency difference exceeds 650ppm.

Loss-of-Signal Monitor

The LOS output indicates low, receive-signal power. The LOS output is asserted high when the input signal is below the threshold set by VTH.

$$VTH = 10 \times V_{LOS\_ASSERT}(mV_{P-P}) \text{ (typ)}$$

The hysteresis value of the LOS detector is internally fixed at 1.5. Hysteresis values above 1.5 can be achieved using external resistors as shown in Figure 4.

The new hysteresis value is:

$$\text{Hysteresis} = 1.5 \times \frac{3 \times R1 + V_{REF} \times R2}{0.2 \times R1 + V_{REF} \times R2}$$

Resistor R2 is selected to prevent loading of the LOS pin. A value of >40kΩ is recommended. Refer to applications note *HFDN 34-0.*

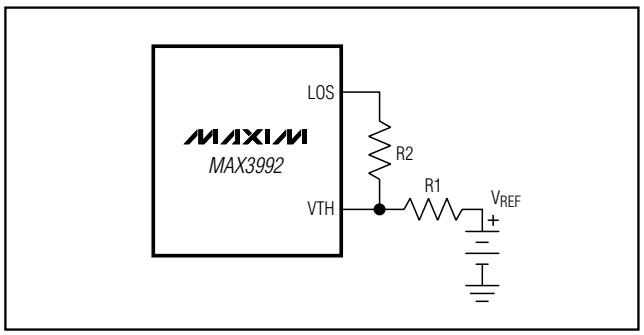


Figure 4. Added Hysteresis Circuit

Reference Clock Input

The REFCLK inputs are internally terminated and self-biased to allow AC-coupling. The input impedance is 100Ω single-ended (200Ω differential). The REFCLK inputs of the MAX3991 and MAX3992 should be connected close together in parallel. The impedance looking into the parallel combination is 100Ω differential. This allows both the MAX3991 and MAX3992 to easily interface with one reference clock without using additional components. See Figure 5.

Design Procedure

Modes of Operation

The MAX3991 has a standby mode, jitter test mode, and squelch mode in addition to its normal operating mode. Standby is used to conserve power. In the standby mode, the power consumption of the MAX3991 falls below 40% of the normal-operation power consumption. The jitter test mode enables the SCLK outputs to clock a BERT when testing jitter generation, jitter transfer, and jitter tolerance. In the squelch mode, the SDO± outputs are held static at V_{CC}. The FCTL1 and FCTL2 TTL inputs are used to select the mode of operation as shown in Table 3.

Serial Data Rate and Reference Clock Frequency

Input Configuration

The SDI± inputs of the MAX3991 are current-mode logic (CML) compatible. The inputs have internal 50Ω terminations for minimum external components. See Figure 6 for the input structure. AC-coupling is recommended. The common-mode levels of DC-coupled parts must be matched. For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML.*

Output Configuration

The MAX3991 uses CML for its high-speed digital outputs (SDO± and SCLKO±). The configuration of the output circuit includes internal 50Ω back terminations to V_{CC}. See Figure 7 for the output structure. CML outputs may be terminated by 50Ω to V_{CC}, or by 100Ω differential impedance. The relation of the output polarity to input can be reversed using the POL pin (see Figure 8). For additional information on logic interfacing, refer to Maxim Application Note HFAN 1.0: *Introduction to LVDS, PECL, and CML.*

10Gbps Clock and Data Recovery with Limiting Amplifier

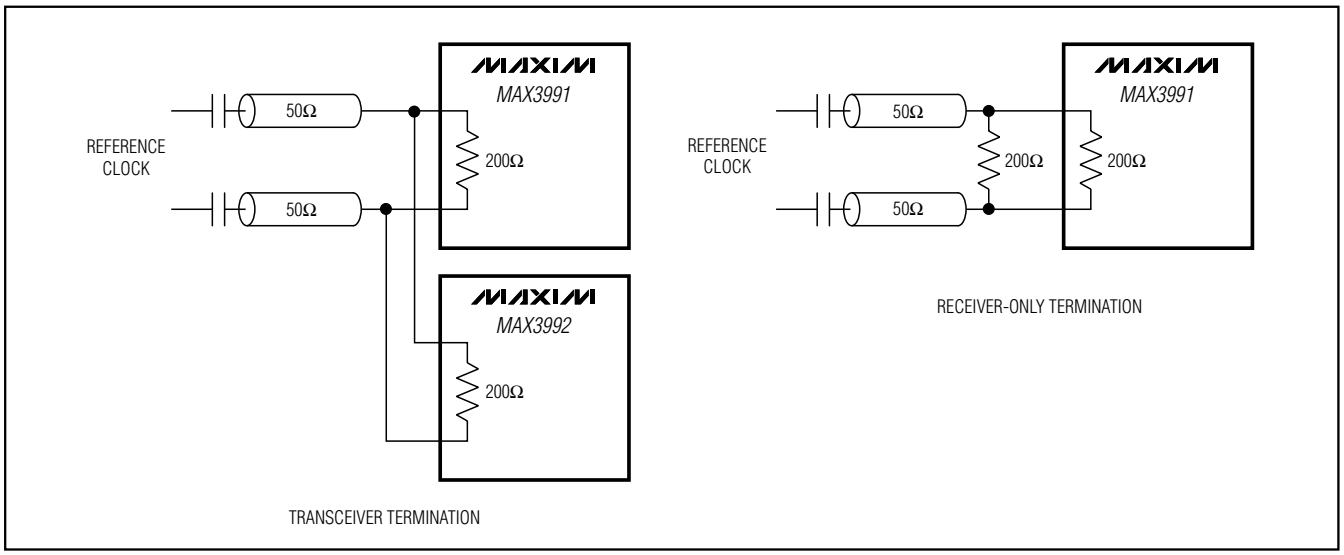


Figure 5. Reference Clock Termination

Table 3. Functional Control

FCTL1	FCTL2	DESCRIPTION
0	0	Normal operation, serial clock output disabled.
1	0	Standby power-down mode.
0	1	Serial data output disabled.
1	1	Serial clock output enabled for jitter testing.

Applications Information

Exposed Pad (EP) Package

The exposed pad, 24-pin QFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3991 and must be soldered to the circuit board for proper thermal and electrical performance.

Layout Considerations

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3991 high-speed inputs and outputs. Power-supply decoupling should be placed as close to V_{CC} as possible. To reduce feedthrough, take care to isolate the input signals from the output signals.

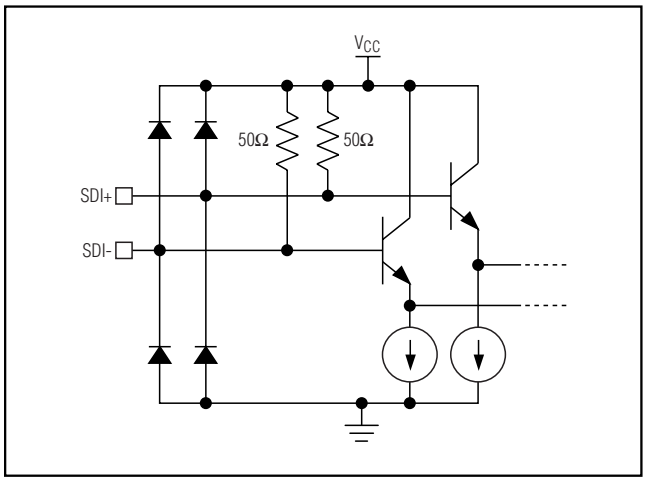


Figure 6. CML Input Model

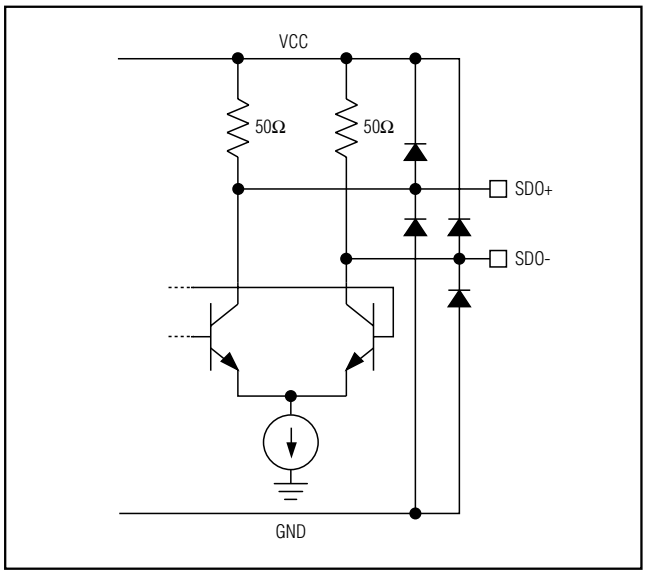


Figure 7. CML Output Model

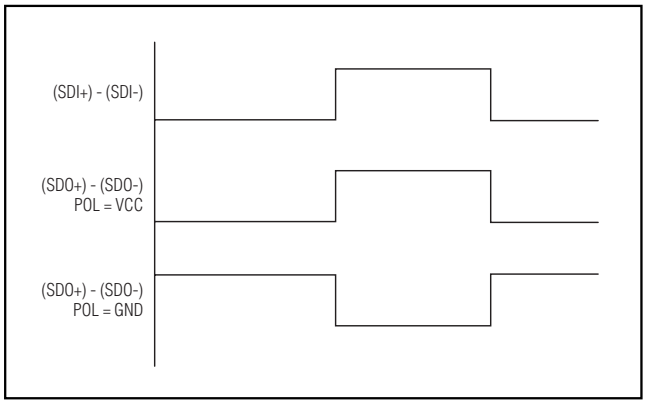
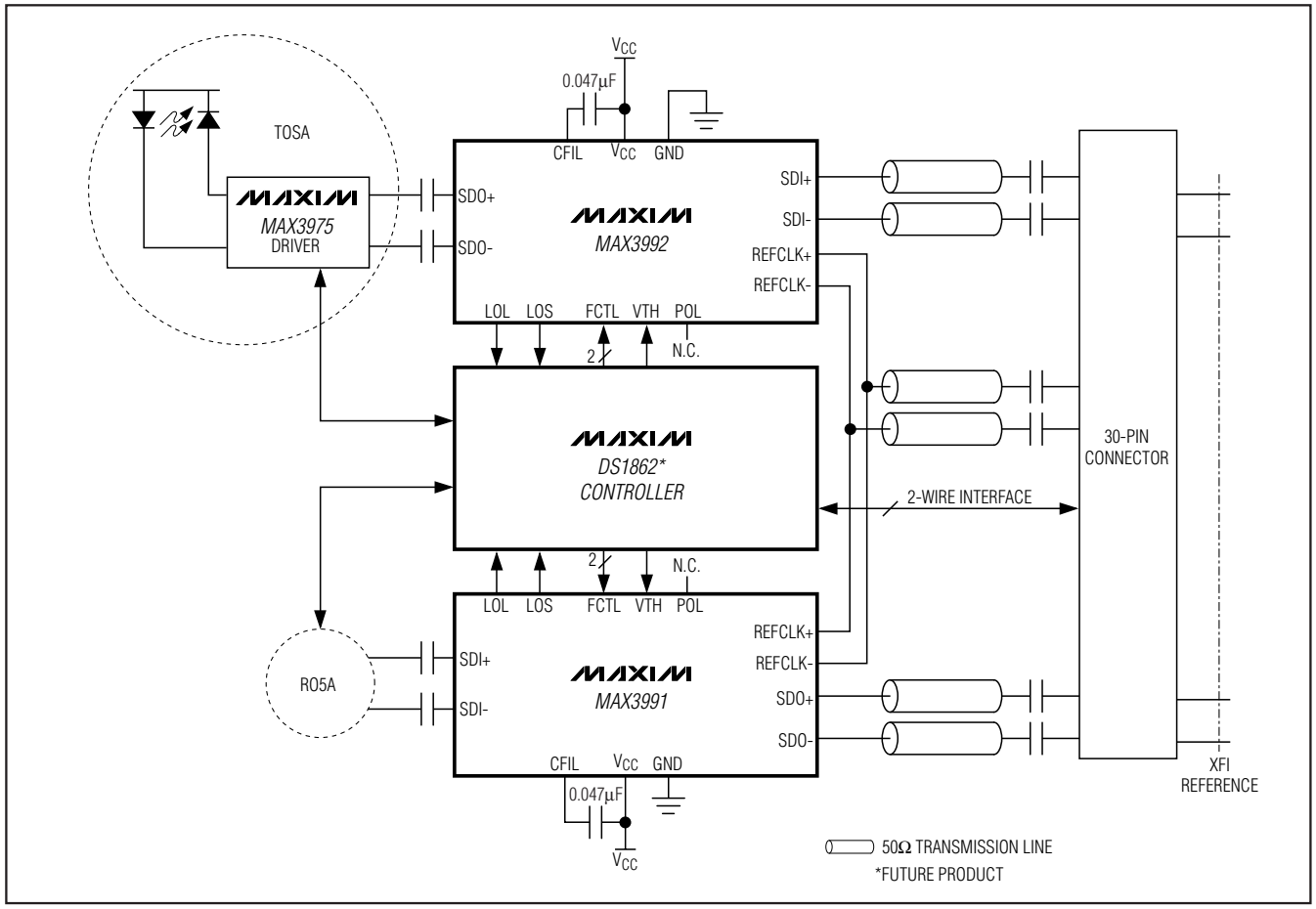


Figure 8. Polarity (POL) Function

10Gbps Clock and Data Recovery with Limiting Amplifier

Typical Application Circuit



Chip Information

TRANSISTOR COUNT: 10,300

PROCESS: SiGe bipolar

SUBSTRATE: SOI

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.) (QFN 4mm x 4mm x 0.8mm, package code: T2444-4)