



155Mbps to 3.2Gbps, Low-Power SFP Limiting Amplifiers

General Description

The MAX3747/MAX3747A multirate limiting amplifiers function as data quantizers for OC-3 through OC-48 synchronous optical network (SONET), Fibre-Channel, and Gigabit Ethernet optical receivers. They are pin-for-pin compatible with the SY88993V from Micrel Semiconductor, Inc. The amplifiers accept a wide range of input voltages and provide constant-level, current-mode logic (CML) output voltages with controlled edge speeds. The MAX3747 output voltage level is 500mVp-p and the MAX3747A output voltage is 800mVp-p.

The MAX3747/MAX3747A limiting amplifiers feature a programmable loss-of-signal detect (LOS) and an optional disable function (DISABLE). Output disable can be used to implement squelch.

The MAX3747/MAX3747A are available in a 3mm, 10-pin μ MAX® package ideal for small form-factor receivers.

Applications

Gigabit Ethernet SFP/SFF Optical Transceiver Modules

1G/2G Fibre-Channel SFP/SFF Optical Transceiver Modules

Multirate OC-3 to OC-48 FEC SFP/SFF Optical Transceiver Modules

10G LX4 Transceiver Modules

Features

- ◆ Pin Compatible with Micrel SY88993V
- ◆ 155Mbps to 3.2Gbps Operation
- ◆ >57dB of Gain for the MAX3747 and MAX3747A
- ◆ <10⁻¹² BER with 2mVp-p Input Amplitude
- ◆ 18mA Supply Current
- ◆ Chatter-Free LOS with Programmable Threshold
- ◆ Output DISABLE Function
- ◆ PECL-Compatible Inputs

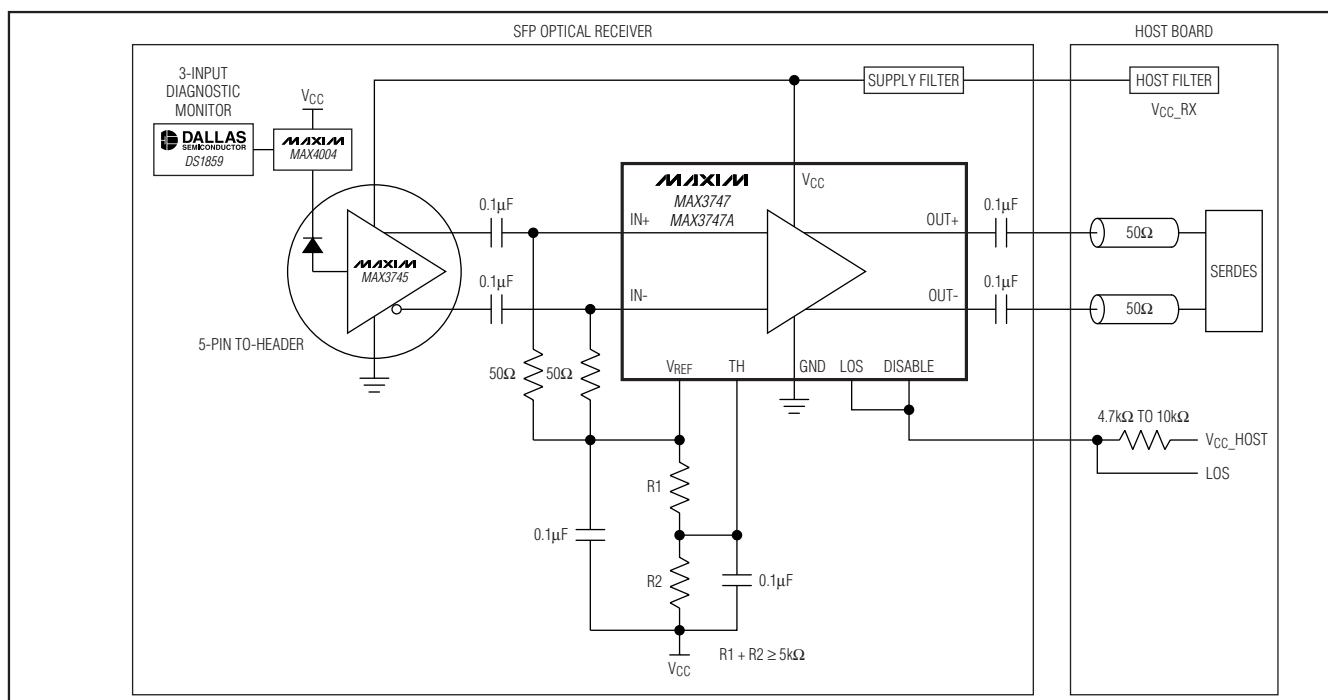
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3747EUB	-40°C to +85°C	10 μ MAX	U10C-4
MAX3747AEB	-40°C to +85°C	10 μ MAX	U10C-4

μ MAX is a registered trademark of Maxim Integrated Products, Inc.

Pin Configuration appears at end of data sheet.

Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) -0.5V to +4.5V
 Voltage at IN+, IN- ($V_{CC} - 2.4V$) to ($V_{CC} + 0.5V$)
 Voltage at DISABLE, LOS, TH, V_{REF} -0.5V to ($V_{CC} + 0.5V$)
 Current into LOS -1mA to +9mA
 Current into V_{REF} 2mA
 Differential Input Voltage (IN+ - IN-) 2.5V

Continuous Current at CML Outputs
 (OUT+, OUT-) -25mA to +25mA
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 10-Pin μMAX (derate 6.9mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 552mW
 Operating Junction Temperature Range (T_J) -55°C to $+150^\circ\text{C}$
 Storage Ambient Temperature Range (T_S) -55°C to $+150^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.97V$ to $+3.63V$, CML output load is 50Ω to V_{CC} , $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ\text{C}$, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current (Note 2)	I_{CC}	MAX3747 includes the CML output current		30	35	mA
		MAX3747A includes the CML output current		36	41	
		MAX3747/MAX3747A exclude the CML output current		18	24	
Power-Supply Noise Rejection	PSNR	$f < 2\text{MHz}$		30		dB
INPUT SPECIFICATION						
Input Sensitivity	V_{IN-MIN}	(Note 3)			4	mV _{P-P}
Input Overload	V_{IN-MAX}	(Note 3)	1200			mV _{P-P}
OUTPUT SPECIFICATION						
Output Resistance	R_{OUT}		42	50	58	Ω
Differential Output Return Loss		DUT is powered on, $f < 3\text{GHz}$		15		dB
CML Differential Output Voltage		MAX3747A $4\text{mV}_{P-P} \leq V_{IN} \leq 1200\text{mV}_{P-P}$	600	800	1000	mV _{P-P}
		MAX3747 $4\text{mV}_{P-P} \leq V_{IN} \leq 1200\text{mV}_{P-P}$	400	500	600	
Differential Output Signal When Disabled		AC-coupled outputs, V_{IN-MAX} applied to the input (Note 4)			15	mV _{P-P}
Data-Output Transition Time		20% to 80% (Note 4)		70	120	ps
TRANSFER CHARACTERISTIC						
Deterministic Jitter (Notes 4, 5)	DJ	K28.5 pattern at 3.2Gbps		13.2	19	ps _{P-P}
		PRBS 2 ²³ - 1 equivalent pattern at 2.7Gbps (Note 6)		14	25	
		K28.5 pattern at 2.1Gbps		12	17	
		PRBS 2 ²³ - 1 equivalent pattern at 155Mbps (Note 6)		85	150	
Random Jitter		$V_{IN} = 4\text{mV}_{P-P}$ (Notes 4, 7)		3.5	5	ps _{RMS}
Input-Referred Noise		$V_{IN} = 4\text{mV}_{P-P}$ (Note 4)		120	150	μV_{RMS}
Low-Frequency Cutoff				6.4		kHz

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MAX3747/MAX3747A

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.97V$ to $+3.63V$, CML output load is 50Ω to V_{CC} , $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOSS OF SIGNAL						
LOS Hysteresis		$10\log(V_{DEASSERT} / V_{ASSERT})$ (Note 4)	1.25			dB
LOS-Assert/Deassert Time		(Notes 4, 8)	2.3		40.0	μs
Low LOS Assert Level		$V_{TH} = -1.3V$ (Notes 4, 9)	2.5	4.1	5.9	mV _{P-P}
Low LOS Deassert Level		$V_{TH} = -1.3V$ (Notes 4, 9)		6.2	9.3	mV _{P-P}
Medium LOS Assert Level		$V_{TH} = -0.68V$ (Notes 4, 9)	22	29	31	mV _{P-P}
Medium LOS Deassert Level		$V_{TH} = -0.68V$ (Notes 4, 9)		44.8	57	mV _{P-P}
High LOS Assert Level		$V_{TH} = -0.114V$ (Notes 4, 9)	36.0	53.7	63.6	mV _{P-P}
High LOS Deassert Level		$V_{TH} = -0.114V$ (Notes 4, 9)		86	115	mV _{P-P}
TTL/CMOS I/O						
V_{REF} Voltage	V_{REF}		$V_{CC} - 1.35$	$V_{CC} - 1.3V$	$V_{CC} - 1.19$	V
LOS Output High Voltage	V_{OH}	$R_{LOS} = 4.7k\Omega$ to $10k\Omega$ to V_{CC_HOST} (3V)	2.4			V
LOS Output Low Voltage	V_{OL}	$R_{LOS} = 4.7k\Omega$ to $10k\Omega$ to V_{CC_HOST} (3.6V)			0.4	V
DISABLE Input High	V_{IH}		2.0			V
DISABLE Input Low	V_{IL}				0.8	V
DISABLE Input Current		$R_{LOS} = 4.7k\Omega$ to $10k\Omega$ to V_{CC_HOST}			10	μA

Note 1: The data-input transition time is controlled by a 4th-order Bessel filter with $f_{-3dB} = 0.75 \times 2.667GHz$ for all data rates of 2.667Gbps and below. The $f_{-3dB} = 0.75 \times 3.2GHz$ for a data rate of 3.2Gbps.

Note 2: Supply current is measured with unterminated outputs or with AC-coupled output termination (see Figure 1).

Note 3: Between sensitivity and overload, all AC specifications are met and the output is $0.95 \times$ limited output amplitude.

Note 4: Guaranteed by design and characterization.

Note 5: The deterministic jitter (DJ) caused by the input filter is not included in the DJ generation specification.

Note 6: The PRBS $2^{23} - 1$ equivalent pattern consists of a K28.5 pattern plus 240 ones plus K28.5 pattern plus 240 zeros.

Note 7: Random jitter was measured without using a filter at the input.

Note 8: The signal at the input is switched between two amplitudes, Signal_ON and Signal_OFF, as shown in Figure 2.

Note 9: V_{TH} is the voltage at pin 5 referenced to V_{CC} (see Figure 5).

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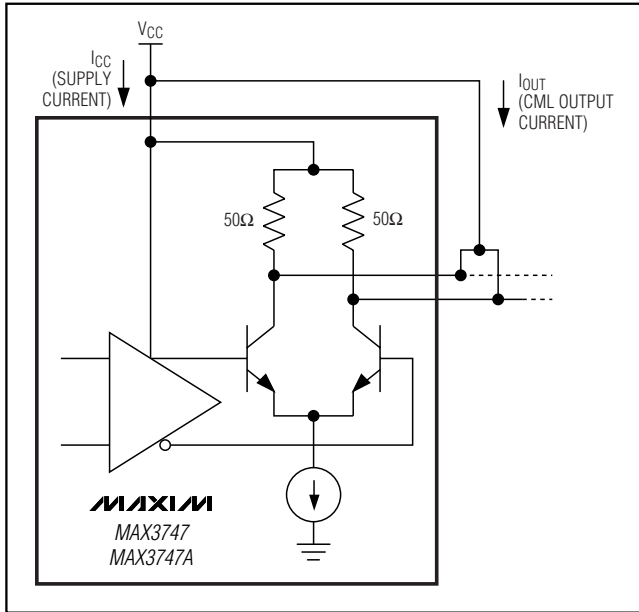


Figure 1. Power-Supply Current Measurement

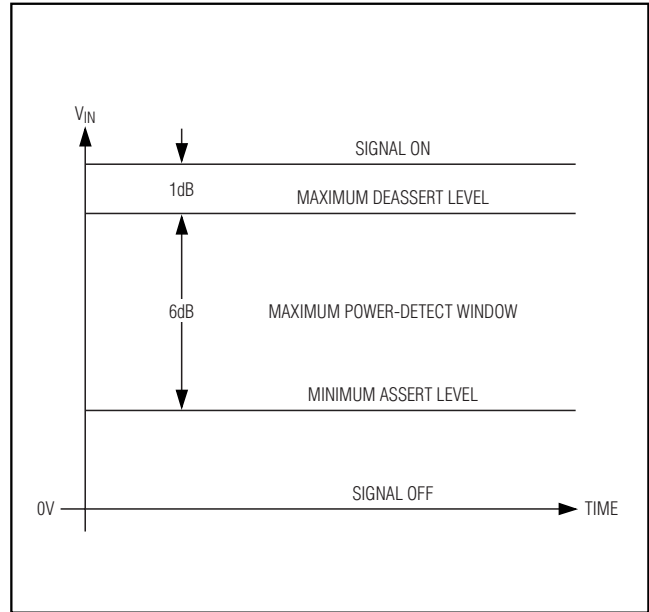
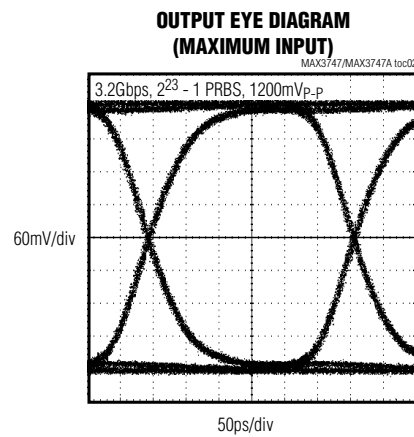
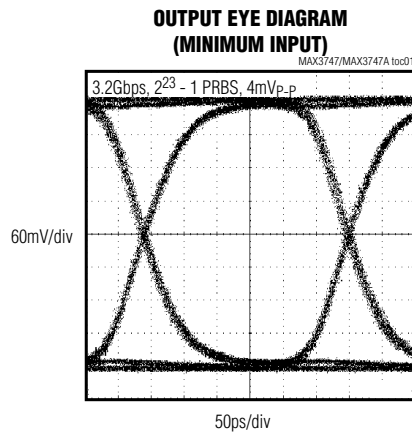


Figure 2. LOS Deassert Threshold—Set 1dB Below the Minimum by Receiver Sensitivity

Typical Operating Characteristics

(VCC = +3.3V, TA = +25°C, unless otherwise noted.)

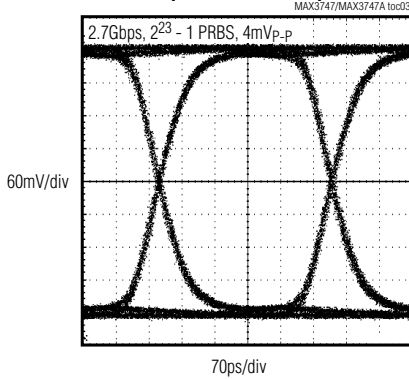


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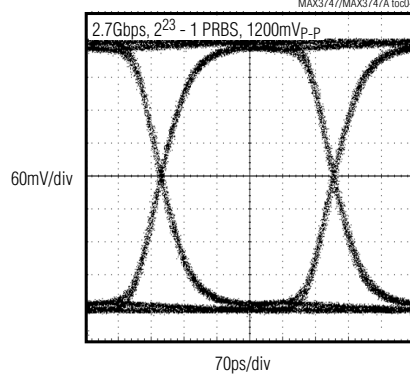
Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

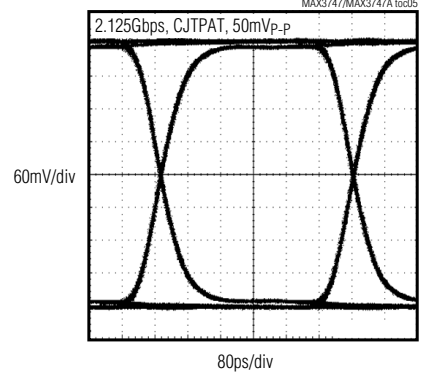
**OUTPUT EYE DIAGRAM
(MINIMUM INPUT)**



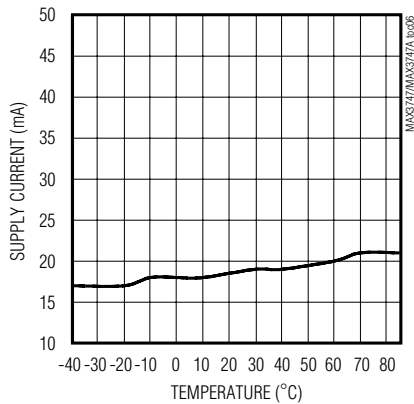
**OUTPUT EYE DIAGRAM
(MAXIMUM INPUT)**



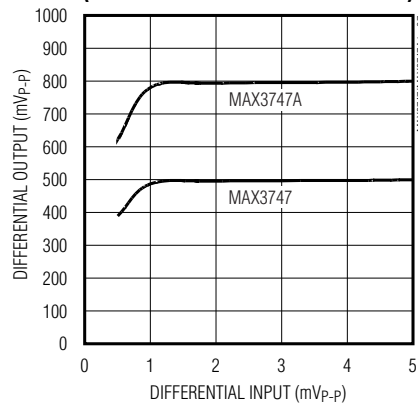
OUTPUT EYE DIAGRAM AT $+100^\circ C$



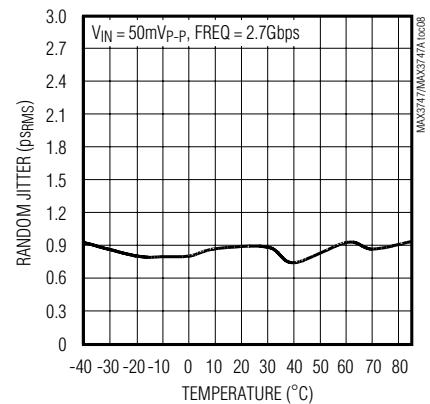
**SUPPLY CURRENT vs. TEMPERATURE
(EXCLUDES OUTPUT CURRENT)**



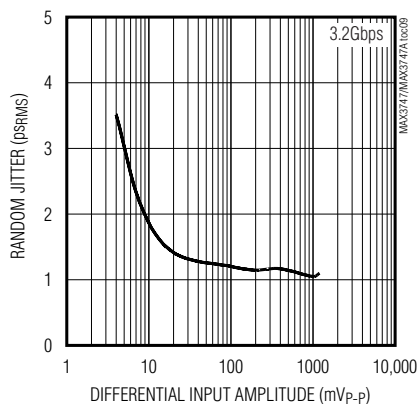
**TRANSFER FUNCTION
(OUTPUT VOLTAGE vs. INPUT VOLTAGE)**



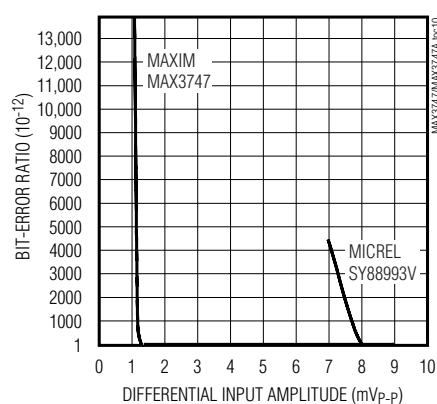
RANDOM JITTER vs. TEMPERATURE



RANDOM JITTER vs. INPUT AMPLITUDE



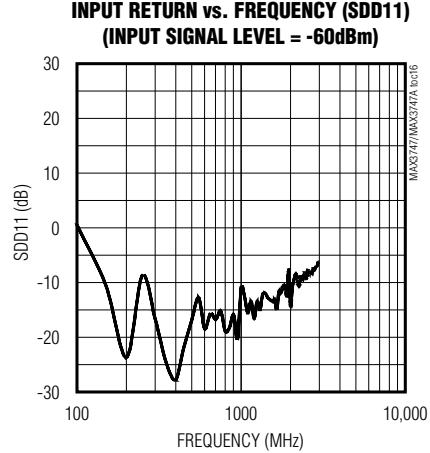
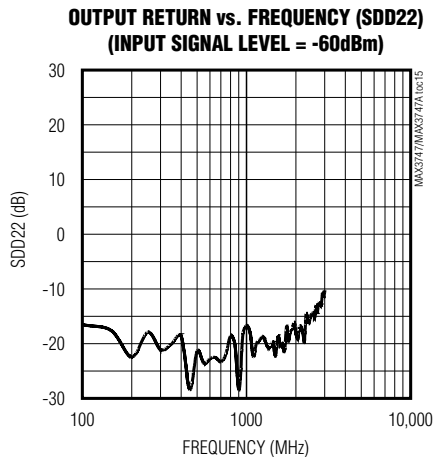
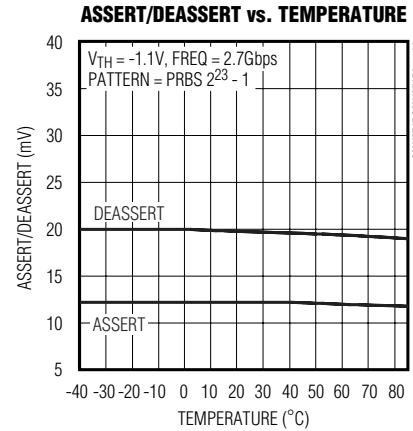
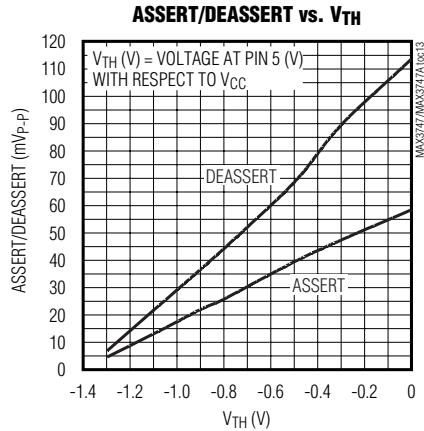
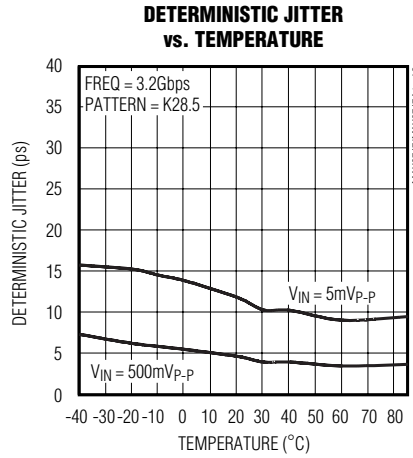
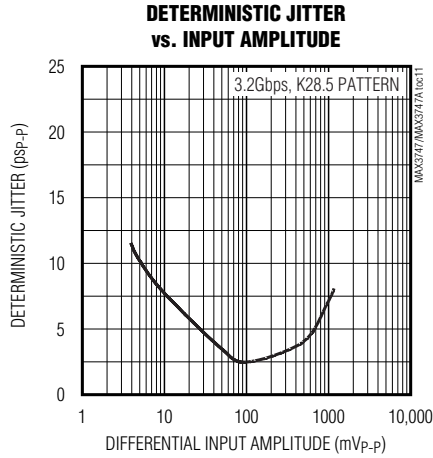
BIT-ERROR RATIO vs. INPUT VOLTAGE



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Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN	MAX3747/ MAX3747A	MICREL SY8893V	FUNCTION
	NAME	NAME	
1	DISABLE	$\overline{\text{EN}}$	Disable Function Pin. The data outputs are held static when this pin is asserted high, transistor-to-transistor logic (TTL).
2	IN+	DIN	Noninverted Input Signal, CML
3	IN-	$\overline{\text{DIN}}$	Inverted Input Signal, CML
4	VREF	VREF	Reference Voltage for LOS Threshold Setting
5	TH	LOSLVL	Loss-of-Signal Level Set. A voltage on this pin created by a two-resistor divider sets the threshold level. Connect one resistor from this pin to VCC and another from this pin to VREF (see Figure 5).
6	GND	GND	Ground
7	LOS	LOS	Loss-of-Signal, Open Collector. LOS is high when the level of the input signal drops below the preset threshold set by the TH input. LOS is deasserted low when the signal level is above the threshold.
8	OUT-	$\overline{\text{DOUT}}$	Inverted Data Output, CML
9	OUT+	DOUT	Noninverted Data Output, CML
10	VCC	VCC	Positive Power Supply

Detailed Description

The limiting amplifiers consist of a multistage amplifier, offset-correction circuitry, an output buffer, and loss-of-signal detect circuitry (see the *Functional Diagram*).

Input Stage

The input stage is shown in Figure 3. It provides 50 Ω termination to VREF for each input signal, IN+ and IN-. The MAX3747/MAX3747A should be AC-coupled.

Multistage Amplifier

The high-bandwidth multistage amplifier provides approximately 57dB of gain for the MAX3747 and 61dB of gain for the MAX3747A.

Offset Correction Loop

The MAX3747/MAX3747A are susceptible to DC offsets in the signal path because they have high gain. In communication systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated in the transimpedance amplifier appears as an input offset and is reduced by the offset correction loop.

The offset correction loop sets a low-frequency cutoff of 3.2kHz.

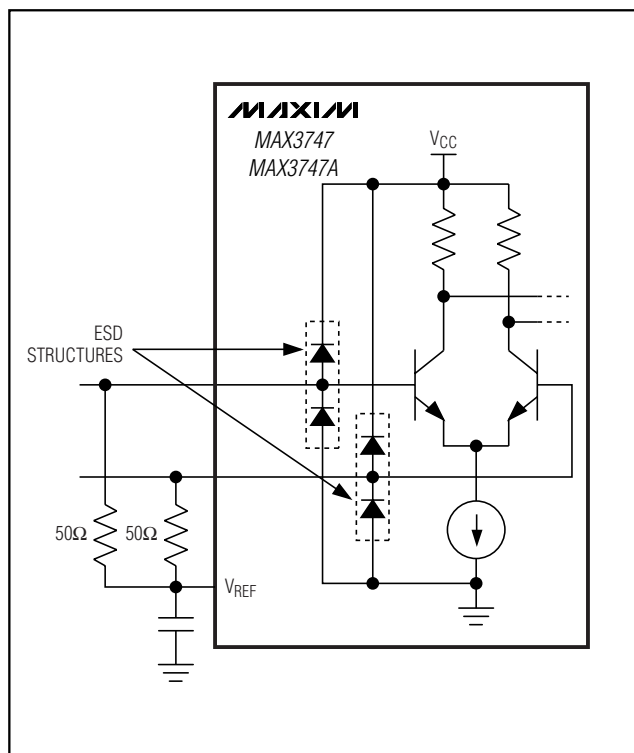


Figure 3. CML Input Stage

MAX3747/MAX3747A

MAX3747/MAX3747A



MAX3747/MAX3747A

MAX3747/MAX3747A

MAX3747/MAX3747A



MAX3747/MAX3747A

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Loss-of-Signal Indicator

The MAX3747/MAX3747A are equipped with LOS circuitry that indicates when the input signal is below a programmable threshold, set by a voltage on the TH pin (see the *Typical Operating Characteristics*). The voltage on the TH pin is set by two resistors, one connecting from the TH pin to V_{CC} and the other connecting from TH to V_{REF} (Figure 5). An RMS power detector compares the input signal amplitude with this threshold and feeds the signal-detect information to the LOS output, which is open collector. To prevent LOS chatter in the region of the programmed threshold, approximately 2dB of hysteresis is built into the LOS assert/deassert function. Once asserted, LOS is not deasserted until the input amplitude rises to the required level. Figure 6 shows the LOS output circuit.

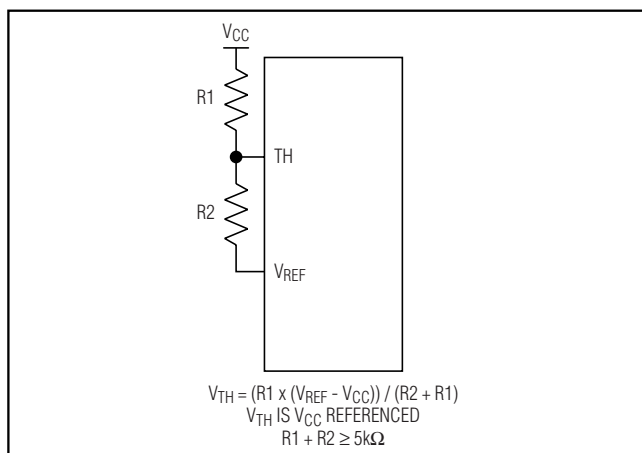


Figure 5. MAX3747/MAX3747A LOS Threshold Circuit

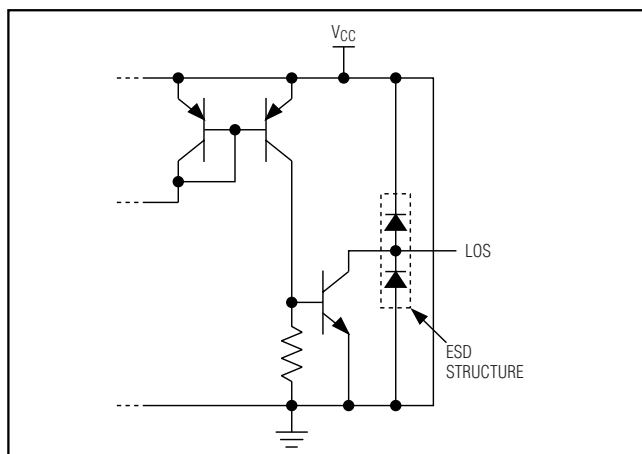


Figure 6. MAX3747/MAX3747A LOS Output Circuit

Applications Information

Program the LOS Assert Threshold

Program the LOS assert threshold according to Figure 5. The combination of R1 and R2 should be greater than or equal to 5kΩ, see the Assert/Deassert vs. V_{TH} graph in the *Typical Operating Characteristics*.

Select the Coupling Capacitor

When AC-coupling is desired, coupling capacitors C_{IN} and C_{OUT} should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased:

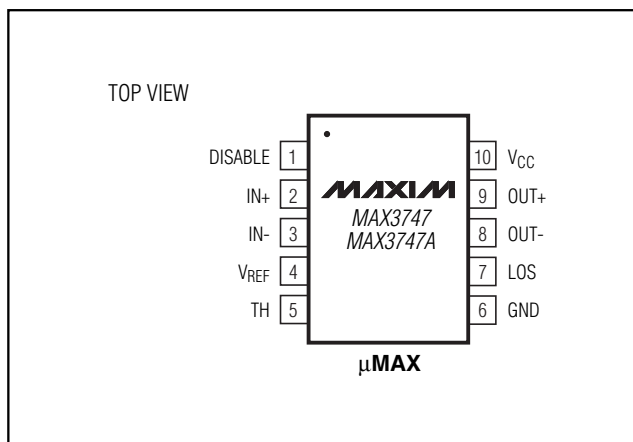
$$f_{IN} = 1 / [2\pi(50)(C_{IN})]$$

For all applications, the recommended value for C_{IN} and C_{OUT} is 0.1μF, which provides f_{IN} equal to 32kHz. Refer to Application Note HFAN-1.1: *Choosing AC-Coupling Capacitors* on the Maxim website (www.maxim-ic.com).

EMI Performance

The MAX3747/MAX3747A have been designed for better EMI performance. To help reduce EMI, special care has been taken to produce symmetrical signal outputs.

Pin Configuration



Chip Information

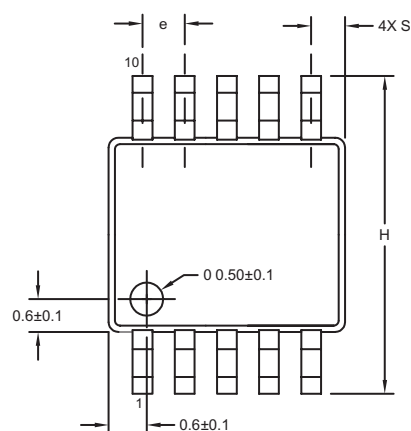
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PROCESS: SiGe Bipolar

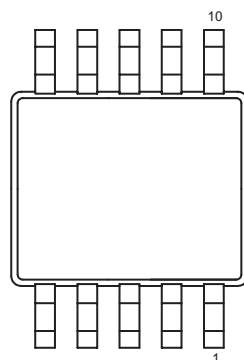
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Package Information

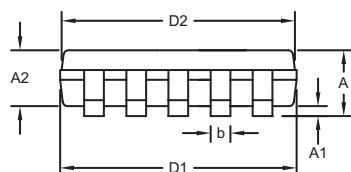
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



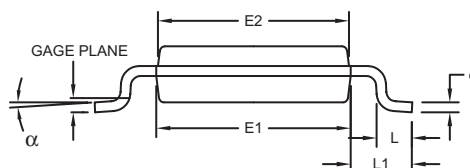
TOP VIEW



BOTTOM VIEW



FRONT VIEW



SIDE VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE:			
PACKAGE OUTLINE, 10L uMAX/uSOP			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1
	21-0061	I	/

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