TECHNICAL MANUAL

LSI53C141
SCSI Bus Expander

Version 2.1

November 2000

LSI LOGIC®

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This document describes the LSI Logic LSI53C141 SCSI Bus Expander and will remain the official reference source for all revisions/releases of this product until rescinded by an update.

To receive product literature, visit us at http://www.lsilogic.com.

Preface

This book is the primary reference and technical manual for the LSI53C141 SCSI Bus Expander chip which supports single-ended to single-ended SCSI bus expansion (Repeater) or single-ended to low voltage differential SCSI bus conversion (Converter). It contains a functional description for the LSI53C141 and includes complete physical and electrical specifications.

Audience

This document was prepared for logic designers and applications engineers.

This document assumes that you have some familiarity with current and proposed SCSI standards. For background information please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1994 (SCSI-2) or X3.253-1995 (SPI)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 397-7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253 *(SCSI-3 Parallel Interface)*

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642

Document names: *SCSI Bench Reference, SCSI Encyclopedia or SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

LSI Logic World Wide Web Home Page
www.lsilogic.com

Organization

This document has the following chapters and appendix:

- Chapter 1, **Introduction**, includes a general description of the LSI53C141, its benefits and features.
- Chapter 2, **Functional Description**, describes the LSI53C141 functions.
- Chapter 3, **Signal Descriptions**, describes the signals of the LSI53C141.
- Chapter 4, **Specifications**, includes the electrical requirements for DC characteristics, TolerANT Technology Electrical Characteristics, and the AC timing characteristics. Also contains the outline drawing of the 128-pin PQFP package.
- Appendix A, **Glossary of Terms and Abbreviations**, provides definitions of various terminology that is referenced throughout this user's guide.

Conventions Used in This Manual

The first time a word or phrase is defined in this manual, it is *italicized.*

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x”—for example, 0x32CF. Binary numbers are indicated by the prefix “0b”—for example, 0b0011.0010.1100.1111.

The following is a list of notational conventions used throughout this manual:

Notation	Example	Meaning and Use
courier typeface	`.nwk` file	Names of commands, files, signals, symbols, pins, parts, directories, modules, and macrocells are shown in courier typeface.
bold typeface	**fd1sp**	In a command line, keywords are shown in bold, nonitalic typeface. Enter them exactly as shown.
italics	*module*	In command lines and names italics indicate user variables. Italicized text must be replaced with appropriate user-specified items. Enter items of the type called for, using lower case.
italic underscore	*full_pathname*	When an underscore appears in an italicized string, enter a user-supplied item of the type called for with no spaces.

Revision Record

Page No.	Date	Version	Remarks
All	7/97	1.0	Draft of the Data Manual
	11/97	1.1	
3-4			RBIAS description changed
3-6			V_{DD} and V_{SS} type changes 5VBIAS description change NC with pullups and pulldown description changes
4-1			I_{DD} Supply Current change
	5/99	2.0	Final version, Preliminary removed, LSI53C141 has reached GCA (General Customer Availability)
4-2			New table 4-6, Input Signal - Clock, input leakage change from 10 µA to 20 µA.
4-4			Table 4-11 (was 4-10) Control Signals - RESET/, WS_ENABLE, changed 3-state leakage from 10 µA to 20 µA.
4-7			Added new Figure 4.3 and renamed Figure 4.4
All	11/00	2.1	All product names changed from SYM to LSI.

Contents

Tables

Chapter 1
Introduction

1.1 General Description

The LSI53C141 SCSI Bus Expander is a single chip solution allowing the extension of device connectivity and/or cable length limits of the SCSI bus. A SCSI bus expander couples bus segments together without any impact to the SCSI protocol, software, or firmware. The LSI53C141 attaches Single-Ended (SE) SCSI peripherals to the Low Voltage Differential (LVD) signaling a bus used by Ultra2 SCSI.

The LSI53C141 does not boost the transfer rates of SE devices to Ultra2 SCSI rates, but instead enables system architects to take advantage of the inherent cable distance, device connectivity, and data reliability benefits of LVD with Ultra SCSI peripherals.

The LSI53C141 operates in one of two modes:

- SE to SE (Extender Mode)
- SE to LVD (Converter mode)

For applications requiring SE to High-Voltage Differential (HVD), use the LSI53C120 Bus Expander. Table 1.1 shows all modes of operation.

Table 1.1 Mode of Operation

LSI Logic Product	Extender	Converter
LSI53C120	SE to SE	SE to HVD
LSI53C141	SE to SE	SE to LVD

In both SCSI Bus Extender and Converter modes, cable segments are electrically isolated from each other. This feature maintains the signal integrity of each cable segment. For bus isolation applications, the LSI53C141 is ideally suited for the LSI53C895 Ultra2 SCSI controller.

The LSI53C141 provides additional control capability through the pin level electrical isolation mode. This feature permits logical disconnection of both the A-side bus and the B-side bus without disrupting SCSI transfers currently in progress. For example, devices on the logically disconnected B-side can be swapped out while the A-side bus remains active.

The LSI53C141 is based upon bus expander technology resulting in some signal filtering and retiming to maintain signal skew budgets. In addition, the LSI53C141 has no programmable registers, therefore, it does not require any software.

1.1.1 Applications

Use the LSI53C141 for the following:

- Server clustering environments
- Expanders create distinct SCSI cable segments which are electrically isolated from each other

1.1.2 Features

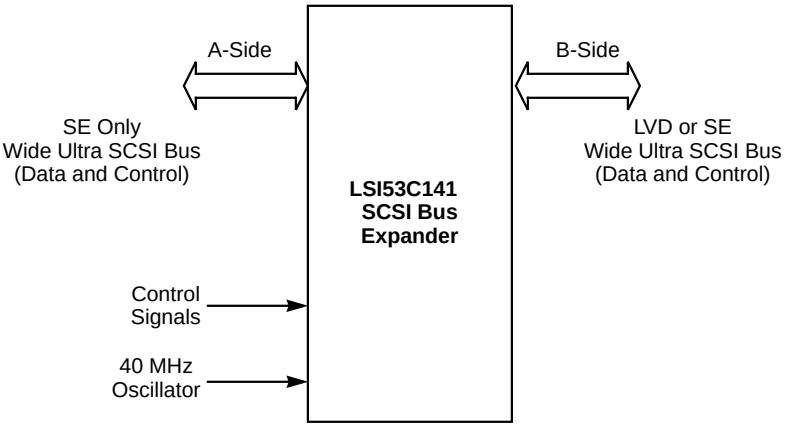
- Attaches SE SCSI devices to an LVD SCSI bus
- Operates as a SCSI Bus Converter or Extender
- Provides SCSI Bus electrical isolation for high availability and scalable server clustering technologies
- Allows targets and initiators to be located on either the A-side or B-side of the device
- Allows each side of the device to be logically disconnected from the other by using the pin level electrical isolation mode
- Accepts any asynchronous or synchronous transfer speed up to Ultra SCSI
- Does not consume a SCSI ID
- Provides on-chip LVD Link™ transceivers
- Supports TolerANT® transceiver technology
- Can cascade up to three LSI53C141s
- Provides complete support for SCSI-1, SCSI-2, and SCSI-3

- Does not require software

The LSI53C141 works with the LSI Logic extensive LSI53C7XX and LSI53C8XX family of SCSI products. It also works with other industry SCSI controllers, disk drives, and SCSI peripherals. Use the LSI53C141 for those difficult SCSI subsystem designs.

Figure 1.1 illustrates the signal grouping of the LSI53C141. A SCSI SE bus connects directly to the SCSI A-side. The interface signals are SCSI bus compatible driver and receiver signals with no internal termination. The SCSI B-side connects directly to a SCSI SE bus or to a SCSI LVD bus. The interface signals utilize LVD Link technology.

Figure 1.1 LSI53C141 SCSI Bus Device



1.1.3 Specifications

The LSI53C141 is designed with the following specifications:

- 40 MHz Input Clock
- 128-Pin Plastic Quad Flat Pack (PQFP)
- Compliant with these reference specifications:
  - SCSI Parallel Interface-2 (SPI-2) (Ultra2)
  - SCSI Enhanced Parallel Interface (EPI)

1.2 Benefits of LVD Link

The LSI53C141 supports LVD for SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than supported by SE SCSI. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. LVD provides the reliability of High Voltage Differential (HVD) SCSI without the added cost of external differential transceivers. LVD allows a longer SCSI cable and more devices on the bus, with the same cables defined in the SCSI-3 Parallel Interface standard for Ultra SCSI. LVD provides a long-term migration path to even faster SCSI transfer rates without compromising signal integrity, cable length, or connectivity.

For backward compatibility to existing SE devices, the LSI53C141 features universal LVD Link transceivers that can switch between LVD SCSI and SE modes.

1.2.1 LVD Link Benefits

Integrated LVD Link universal transceivers provide these benefits:

- Supports LVD
- Allows greater device connectivity and longer cable length
- Saves cost of external differential transceivers by using LVD Link transceivers
- Supports a long-term performance migration path

1.3 Application Examples

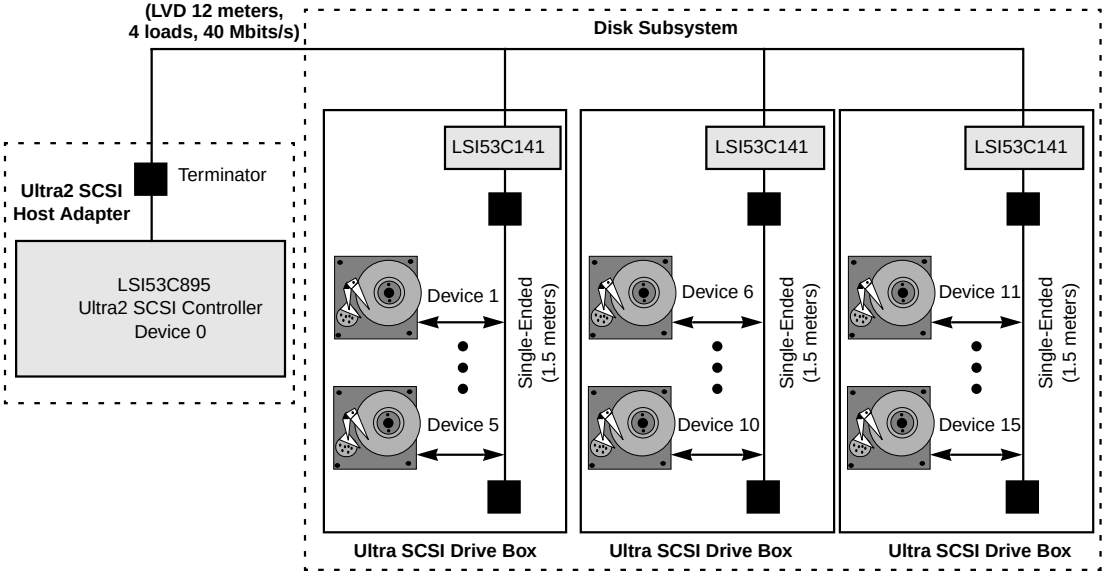
The following examples represent typical applications for the LSI53C141. Many other configurations are possible and are only limited by the imagination of the system architect.

1.3.1 LVD to SE Example

Figure 1.2 illustrates how to use the LSI53C141 to attach SE devices to an LVD bus. This application permits system architects to take advantage

of the longer cable lengths associated with LVD using today's SE devices.

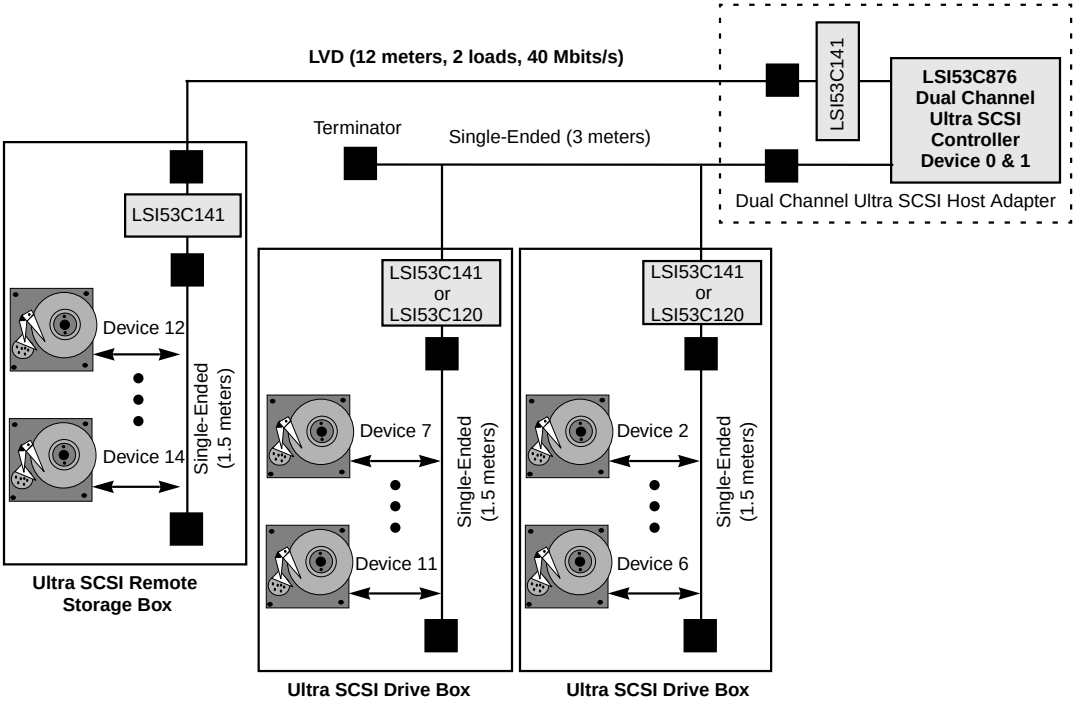
Figure 1.2 SCSI Extender Application (SE to SE Mode of Operation)



1.3.2 SE to SE and SE to LVD Example

Figure 1.3 illustrates both SE to SE and SE to LVD modes of the LSI53C141 to create a remote storage configuration.

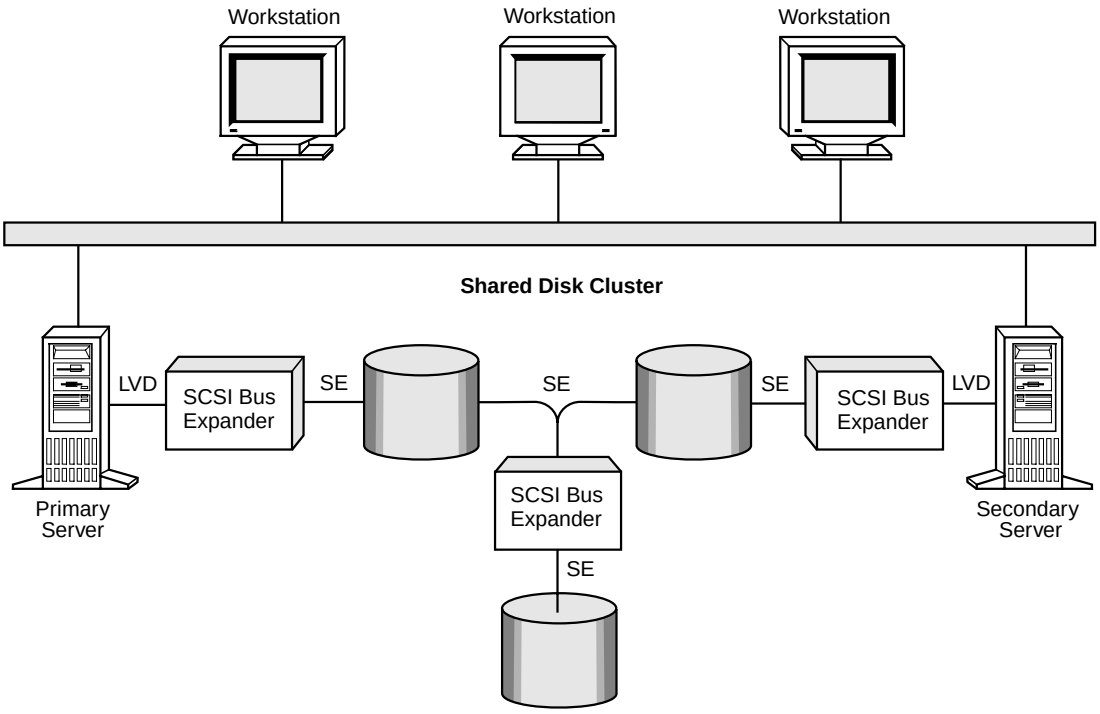
Figure 1.3 SCSI Extender or Converter Application (SE to LVD Mode of Operation)



1.3.3 Clustering Example

Figure 1.4 illustrates how servers share the same storage within a cluster. When a server fails, the other server ensures data availability to client workstations (often transparently to client applications). The LSI53C141s create distinct SCSI segments that are electrically isolated from each other. The LSI53C141 logical disconnection feature aids in the failure recovery process. Cluster configuration improves data availability, fault tolerance, and performance.

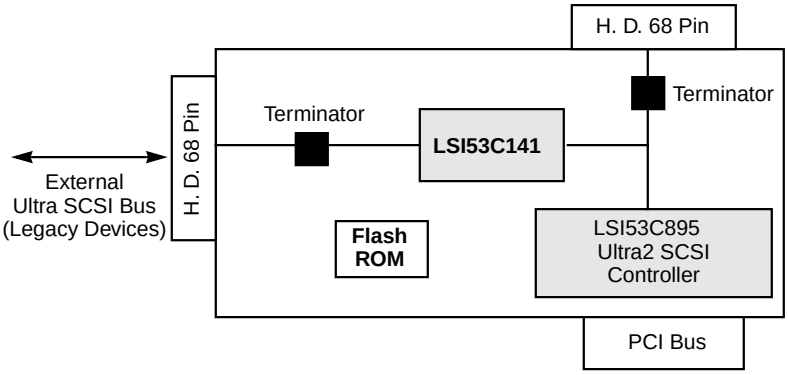
Figure 1.4 SCSI Bus Expanders in Clustering Environment



1.3.4 SCSI Bus Electrical Isolation

Figure 1.5 illustrates how to use the LSI53C141 to electrically isolate an external SCSI bus from an internal SCSI bus. This configuration ensures externally attached peripherals will not affect the operation of internal peripherals.

Figure 1.5 SCSI Bus Electrical Isolation

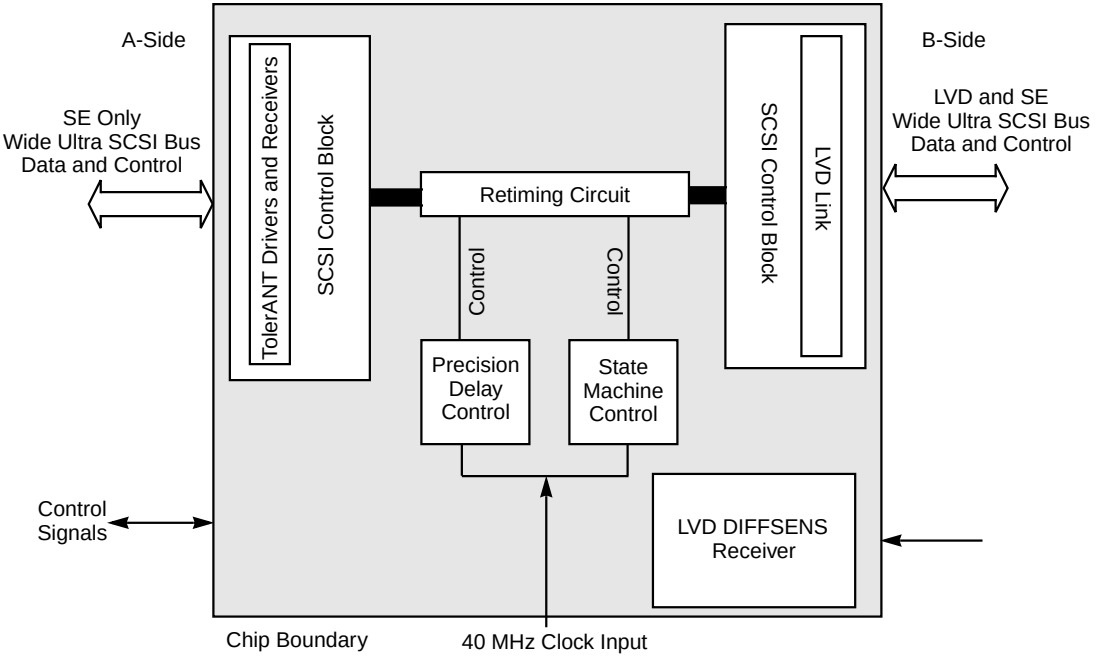


Chapter 2
Functional Description

The LSI53C141 has no programmable registers, therefore, no software requirements. SCSI control signals control all LSI53C141 functions. This chapter describes all signals, their groupings, and functions. Figure 2.1 shows a block diagram of the LSI53C141, which is divided into these specific areas:

- A-side SCSI Control Block
  - TolerANT Drivers and Receivers
- B-side SCSI Control Block
  - LVD Link Technology
- Retiming Circuit
- Precision Delay Control
- State Machine Control
- LVD Control

Figure 2.1 LSI53C141 Block Diagram



In its simplest form, the LSI53C141 passes data and parity from a source bus to a load bus. The side asserting, deasserting, or releasing the SCSI signals is the source side. The simplest model is that the LSI53C141 is just pieces of wire that allow corresponding SCSI signals to flow from side to side. In reality, the LSI53C141 needs to know which side is driving the signals so it can enable the proper drivers to pass the signals along. In addition, the LSI53C141 does some signal retiming to maintain the signal skew budget from source bus to load bus as if the source was a local bus member.

2.1 SCSI A-Side and B-Side SE Control Blocks

In the SE to SE mode, the SCSI A-side pins are connected internally to the corresponding SCSI B-side pins, forming bidirectional connections to the SCSI bus.

The SCSI A-side and B-side SE control blocks connect to both targets and initiators and accept any asynchronous or synchronous data transfer

rates up to the 40 Mbytes/s rate of Wide Ultra SCSI. LVD Link technology is part of the SCSI B-side SE control block. TolerANT technology is part of the SCSI A-side SE control block.

2.1.1 TolerANT Technology

The LSI53C141 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven HIGH rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, which is the single biggest reliability issue with SCSI operations.

The benefits of TolerANT include increased immunity to noise on the deasserting signal edge, better performance due to balanced duty cycles, and improved SCSI transfer rates. In addition, TolerANT SCSI devices prevent glitches on the SCSI bus at power up or power down, so other devices on the bus are also protected from data corruption.

2.1.2 LVD Link Technology

To support greater device connectivity and a longer SCSI cable, the LSI53C141 features LVD Link technology, the LSI Logic implementation of universal LVD SCSI. LVD Link transceivers provide the inherent reliability of differential SCSI, and a long-term migration path of faster SCSI transfer rates.

LVD Link technology is based on current drive. Since its low output current reduces the power needed to drive the SCSI bus, the I/O drivers can be integrated directly onto the chip. This reduces the cost and complexity compared to traditional (high power) differential designs. LVD Link lowers the amplitude of noise reflections and allows higher transmission frequencies.

The LVD Link transceivers operate in LVD and SE modes. The LSI53C141 automatically detects which type of signal is connected, based on voltage detected by DIFFSENS, pin 46.

2.2 Retiming Logic

The SCSI signals, as they propagate from one side of the LSI53C141 to the other side, are processed by logic that retimes the bus signals as needed to guarantee or improve required SCSI timings. This logic is governed by the state machine controls that keep track of SCSI phases, the location of initiator and target devices, and various timing functions. In addition, this logic contains numerous precision delay elements that are periodically calibrated by the precision delay control block. The purpose of this calibration is to guarantee specified timings, such as output pulse widths, setup and hold times, and other timings.

2.3 Precision Delay Control

The precision delay control block provides calibration information to the precision delay elements in the retiming logic block. The purpose of this information is to maintain precise timings as signals propagate through the device. The operating conditions for the LSI53C141, such as voltage and temperature, vary over time. The precision delay control block periodically updates the delay settings in the retiming logic to maintain constant and precise control over bus timings.

2.4 State Machine Control

The state machine controls keep track of the SCSI bus phase protocol and other internal operating conditions. This block provides signals to the retiming logic that identifies how to properly handle SCSI bus signal retiming and protocol, based on observed bus conditions.

2.5 Dynamic Mode Switching

The LSI53C141 supports dynamic transmission mode changes on the bus segment that supports both LVD and SE (B-side SCSI bus). The DIFFSENS circuitry detects a valid mode switch on the bus segment. The new DIFFSENS state must be present for 100 ms before the LSI53C141 declares a valid shift in transmission mode. The LSI53C141 then generates a SCSI reset on the opposite bus (A-side SCSI bus). This reset informs any initiators residing on this opposing segment of the change in transmission mode. These initiators may then analyze the integrity of this mode change versus performance capabilities and conduct any necessary renegotiations.

2.6 DIFFSENS Receiver

The LSI53C141 contains an LVD DIFFSENS receiver that detects the voltage level on the DIFFSENS line for purposes of informing the LSI53C141 of the transmission mode being used by the B-side SCSI bus. The LVD DIFFSENS receiver is capable of detecting the voltage level of an incoming SCSI signal to determine whether it is from a SE or LVD device. A device does not change its present signal driver or receiver mode based on the DIFFSENS voltage level unless a new mode is sensed continuously for at least 100 ms.

Transmission mode detection for SE or LVD is accomplished through the use of the DIFFSENS line. Table 2.1 shows the corresponding voltages and what mode they indicate.

Table 2.1 DIFFSENS Voltage Levels

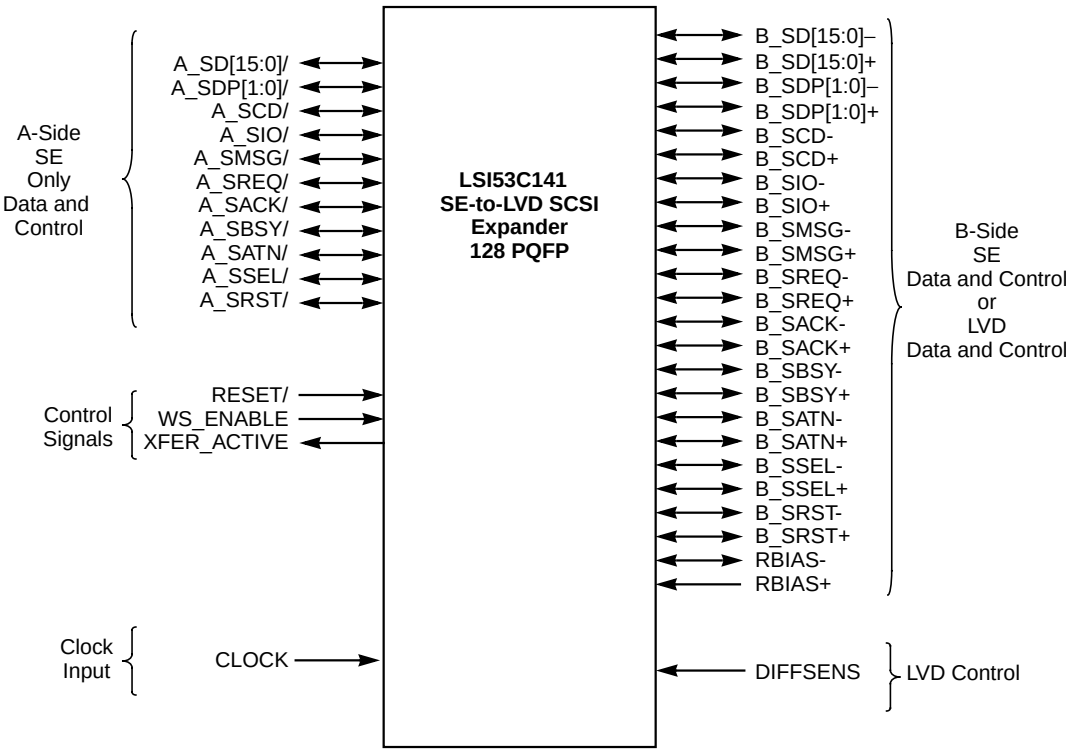
Mode	SE	LVD
Voltage	– 0.35 to + 0.5	0.7 to 1.9

Note: The maximum voltage allowed to this pin is 3.3 volts.

2.7 Signal Descriptions

Figure 2.2 illustrates the LSI53C141 signal groupings. A description of the signals follows. For specific signal timings, see Section 4.3, "AC Characteristics," in Chapter 4.

Figure 2.2 LSI53C141 Signal Grouping



2.7.1 Data and Parity

The signals named A_SD[15:0]/ and A_SDP[1:0]/ are the data and parity signals from the A-side; the signals named B_SD[15:0] and B_SDP[1:0]± are the data and parity signals from the B-side of the LSI53C141. These signals are sent and received from the LSI53C141 through a SCSI compatible driver and receiver logic designed into the LSI53C141 interfaces. This logic provides the necessary drive, sense thresholds, and input hysteresis to function correctly in a SCSI bus environment as defined in ANSI Standard for SCSI-1, SCSI-2, and SCSI-3.

The LSI53C141 receives data and parity signals and passes them from the source bus to the load bus and provides any necessary edge shifting to guarantee the skew budget for the load bus. Either side of the LSI53C141 can be the source bus or the load bus. The side asserting, deasserting, or releasing the SCSI signals is the source side. The following steps are a part of the LSI53C141 data path:

1. Asserted data is accepted from the receiver logic as soon as it is received. Once the clock signal has been received, data is gated from the receiver latch.
2. The path is tested to ensure the signal, if being driven by the LSI53C141, is not misinterpreted as an incoming signal.
3. The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The duration is then controlled by the input signal.
4. The next stage is a latch that samples the signal. This provides a stable data window for the load bus.
5. The final stage develops pull-up and pull-down controls for the SCSI I/O logic, including 3-state controls for the pull-up.
6. A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal deassertion on each signal line.

2.7.2 Busy (BSY) Control

A_SBSY/ and B_SBSY± signals are propagated from the source bus to the load bus. These signals go through the following processing steps:

1. The path is tested to ensure the signal, if being driven by the LSI53C141, is not misinterpreted as an incoming signal.
2. The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The duration is then controlled by the input signal.
3. The next stage has two modes. One mode simply passes data through. The other mode behaves like a large filter. The current state in the LSI53C141 state machine that tracks SCSI phases selects the mode. The large filter mode is used where the Busy (BSY) and Select (SEL) sources may switch from side to side. This output is then fed to the output driver which is a pull-down open collector only.

A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal deassertion on each signal line.

2.7.3 Request (REQ)/Acknowledge (ACK) Control

A_SACK/, B_SACK±, A_SREQ/ and B_SREQ± are clock and control signals. Their signal paths contain controls to guarantee minimum pulse width, filter edges, and does some retiming when used as data transfer clocks. Each signal, REQ and ACK, has paths from A to B and B to A. The received signal goes through the following processing steps before being sent to the opposite bus.

1. The asserted input signal is sensed and forwarded to the next stage if the direction control permits it. The direction controls are developed from state machines that are driven by the sequence of bus control signals.
2. The signal must then pass the test of not being generated by the LSI53C141.
3. In the A to B bus direction, the next stage is a leading edge filter. This ensures that the output does not switch during the specified hold time after the leading edge. The duration of the input signal determines the duration of the output after the hold time. In the B to A direction, the circuit guarantees a minimum pulse.
4. The next stage passes the signal if it is not a data clock. If REQ or ACK is a data clock, it delays the leading edge to improve data output setup times. The duration is again controlled by the input signal.
5. The following stage is a trailing edge signal filter. When the signal deasserts, the filter does not permit any signal bounce. The output signal deasserts at the first deasserted edge of the input signal.
6. The last stage develops pull-up and pull-down signals with drive and 3-state control.
7. A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal deassertion on each signal line.

2.7.4 Reset (RST) Control

A_SRST/ and B_SRST± are also passed from the source to the load bus. These reset signals are processed in the following steps.

1. The input signal is blocked if it is already being driven by the LSI53C141.
2. The next stage is a leading edge filter. This ensures that the output does not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
3. A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal deassertion on each signal line.

2.7.5 Control/Data (C/D), Input/Output (I/O), Message (MSG) and Attention (ATN) Controls

A_SCD/, A_SIO/, A_SMSG/, A_SATN/, B_SCD±, B_SIO±, B_SMSG±, and B_SATN± are control signals that have the following processing steps:

1. The input signal is blocked if it is being driven by the LSI53C141.
2. The next stage is a leading edge filter. This ensures that the output does not switch for a specified time after the leading edge. The duration of the input signal determines the duration of the output.
3. The final stage develops pull-up and pull-down controls for the SCSI I/O logic, including 3-state controls for the pull-up.
4. A parallel function ensures that bus (transmission line) recovery is for a specified time after the last signal deassertion on each signal line.

2.7.6 Select (SEL) Control

A_SSEL/ and B_SSEL± are control signals used during bus arbitration and selection. Whichever bus asserts SEL propagates it to the other side. If both signals are asserted at the same time, the A-side receives SEL and sends it to the B-side. The signal goes through the following processing steps.

1. The input signal is blocked if it is being driven by the LSI53C141.

2. The next stage is a leading edge filter. This ensures that the output does not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
3. A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal deassertion on each signal line.

2.7.7 Clock (CLOCK)

This is the 40 MHz oscillator input to the LSI53C141. This is the clock source for protocol control state machines and timing generation logic. This clock is not used in any bus signal transfer paths.

2.7.8 Chip Reset (RESET/)

This general chip reset is intended to force all the internal elements of the LSI53C141 into a known state. This brings all state machines to an idle state and force all controls to a passive state. The minimum RESET input asserted pulse width is 100 nanoseconds.

The LSI53C141 also contains an internal Power On Reset (POR) function that is wire ORed with the chip reset pin. This function eliminates the need for an external chip reset.

Table 2.2 RESET/ Control Signal Polarity

Signal Level	State	Effect
LOW = 0	Asserted	Reset is forced to all internal LSI53C141 elements.
HIGH = 1	Deasserted	LSI53C141 is not in a forced reset state.

2.7.9 Warm SWAP Enable and Transfer Active (WS_ENABLE and XFER_ACTIVE)

These two pins provide additional control capability for the LSI53C141. They allow both the SCSI A-side bus and the SCSI B-side bus to be logically disconnected. The XFER_ACTIVE output changes state only with the detection of a SCSI bus free state; this guarantees that transfers

currently in progress are not disrupted by the assertion or deassertion of the WS_ENABLE pin.

Assertion or deassertion of the WS_ENABLE pin may not be effective immediately since it may take several milliseconds for a bus free state to be detected and then indicated by a change in state of the XFER_ACTIVE output signal.

Table 2.3 WS_ENABLE Signal Polarity

Signal Level	State	Effect
LOW = 0	Asserted	The LSI53C141 discontinues transfers through the device (off-line) upon detection of a SCSI bus free state.
HIGH = 1	Deasserted	The LSI53C141 performs normal transfers through the device.

Table 2.4 XFER_ACTIVE Signal Polarity

Signal Level	State	Effect
HIGH = 1	Asserted	Indicates normal operation, transfers through the LSI53C141 are enabled.
LOW = 0	Deasserted	The LSI53C141 has detected a bus free state due to WS_ENABLE being LOW, disabling transfers through the device.

2.8 SCSI Termination

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and to match the impedance seen at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of the SCSI chain, and only at the ends. No system should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed so that,

if they are not needed, they may be removed. Otherwise, there should be a means of disabling them with software.

The use of active termination is highly recommended. For information on terminators that support LVD, refer to the SPI-2 Draft standard.

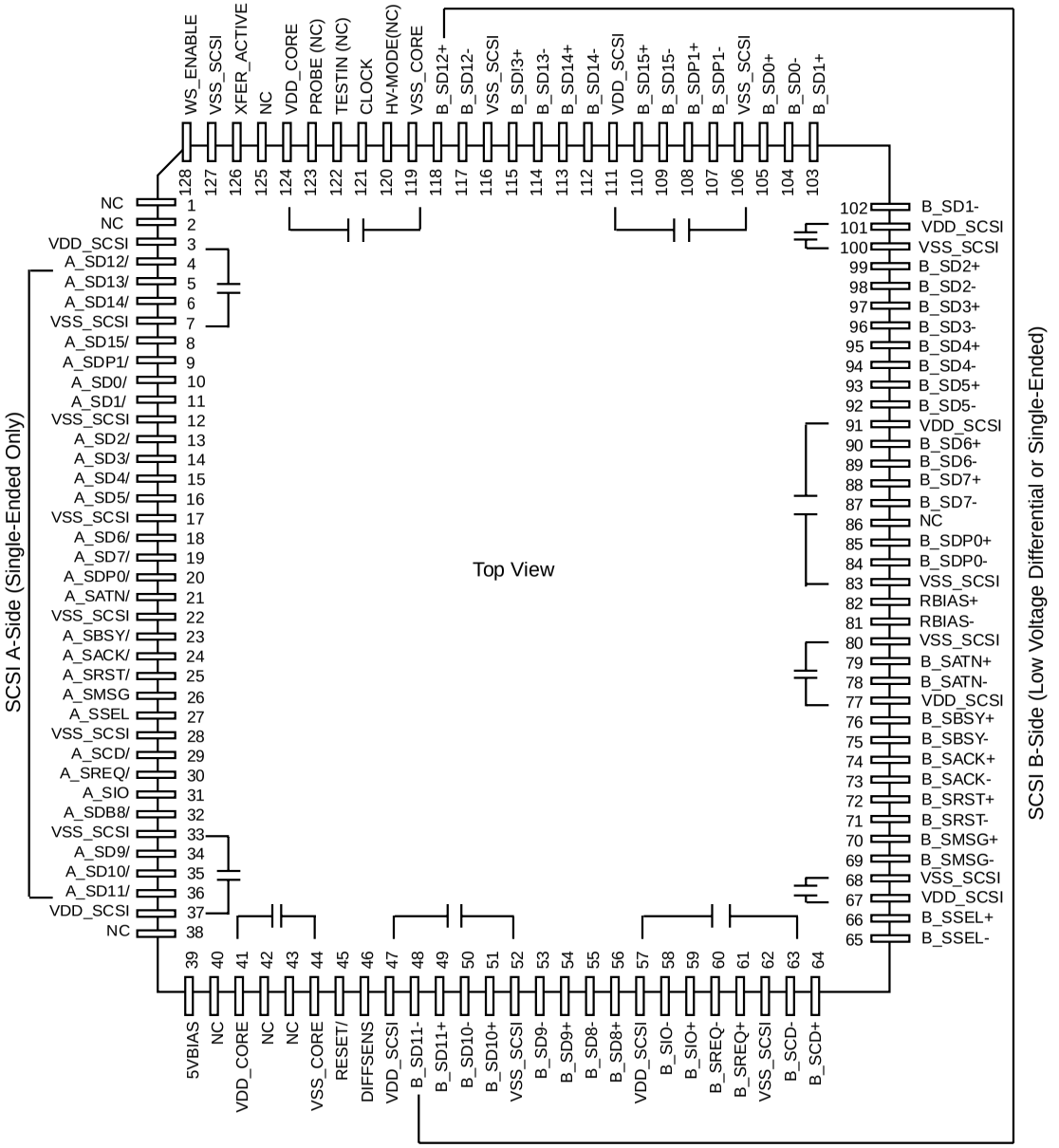
Important: If the LSI53C141 is to be used in a design with only an 8-bit SCSI bus, all 16 data lines must still be terminated or pulled HIGH.

Chapter 3
Signal Descriptions

The LSI53C141 is packaged in a 128-pin PQFP. Figure 3.1 shows the decoupling capacitor arrangement recommended to maximize the benefits of the internal split ground system. Capacitor values should be between 0.01 µF and 0.1 µF. Figure 3.2 shows the signals, their grouping, and their I/O direction. A slash (/) at the end of a signal name indicates that it is an active LOW signal.

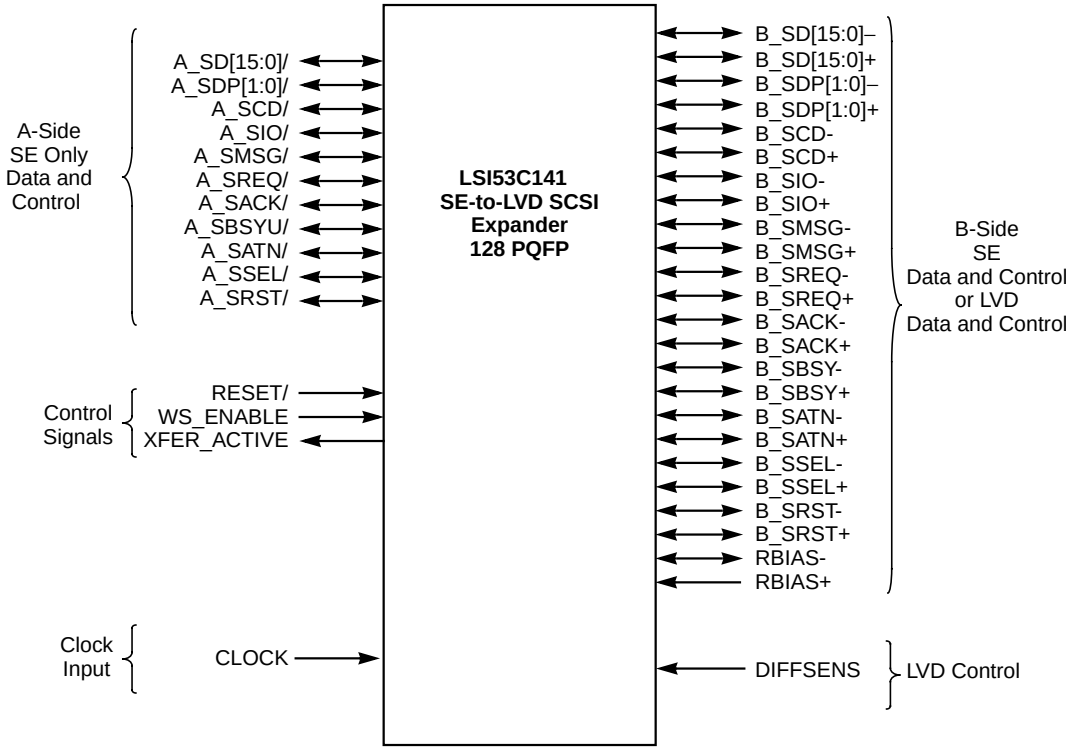
3.1 LSI53C141 Pin Diagram

Figure 3.1 LSI53C141 Pin Diagram



3.2 LSI53C141 Signal Grouping

Figure 3.2 LSI53C141 Functional Signal Grouping



3.3 SCSI A Interface Pins

Table 3.1 SCSI A Signal Description

SCSI A	Pin	Type	Description
A_SD[15:0]/	8, 6, 5, 4, 36, 35, 34, 32, 19, 18, 16, 15, 14, 13, 11, 10	I/O	Data (16-bit SCSI bus)
A_SDP[1:0]/	9, 20	I/O	Data parity bits
A_SCD/	29	I/O	Phase line, command/data
A_SIO/	31	I/O	Phase line, input/output
A_SMSG/	26	I/O	Phase line, message
A_SREQ/	30	I/O	Data handshake signal from target device
A_SACK/	24	I/O	Data handshake signal from initiator device
A_SBSY/	23	I/O	Bus arbitration signal, busy
A_SATN/	21	I/O	Attention, the initiator is requesting a message out phase
A_SSEL/	27	I/O	Bus arbitration signal, select device
A_SRST/	25	I/O	Bus reset

3.4 SCSI B SE and LVD Interface Pins

Table 3.2 SCSI B Signal Description

SCSI B	Pin	Type	Description
B_SD[15:0]+	110, 113, 115, 118, 49, 51, 54, 56, 88, 90, 93, 95, 97, 99, 103, 105	I/O	Differential+ Signal Data (16-bit SCSI bus)
B_SD[15:0]–	109, 112, 114, 117, 48, 50, 53, 55, 87, 89, 92, 94, 96, 98, 102, 104	I/O	Differential– Signal Data (16-bit SCSI bus)
B_SDP[1:0]+	108, 85	I/O	Differential+ Signal Data parity bits
B_SDP[1:0]–	107, 84	I/O	Differential– Signal Data parity bits
B_SCD±	63, 64	I/O	Differential Signal Phase line, command/data
B_SIO±	58, 59	I/O	Differential Signal Phase line, input/output
B_SMSG±	69, 70	I/O	Differential Signal Phase line, message
B_SREQ±	60, 61	I/O	Differential Signal Data handshake signal from target device
B_SACK±	73, 74	I/O	Differential Signal Data handshake signal from initiator device
B_SBSY±	75, 76	I/O	Differential Signal Bus arbitration signal, busy
B_SATN±	78, 79	I/O	Differential Signal Attention, the initiator is requesting a message out phase
B_SSEL±	65, 66	I/O	Differential Signal Bus arbitration signal, select device
B_SRST±	71, 72	I/O	Differential Signal Bus Reset
RBIAS±	81, 82	I	The RBIAS± pins need to have a 2.0 kΩ, 1% resistor between them to provide the correct bias current to the LVD pads. Additionally, +3.3 V needs to be connected to the RBIAS–, pin 81

Note: An SE interface uses only the – (minus) signals. LVD interface uses both the + and – signals.

3.5 Interface Control Pins

Table 3.3 Chip Control Signal Description

Control	Pin	Type	Description
RESET/	45	I	Master reset, active LOW
WS_ENABLE	128	I	Enable/disable SCSI transfers through LSI53C141
XFER_ACTIVE	126	O	Transfers through the LSI53C141 are enabled/disabled

3.6 SCSI Control Pins

Table 3.4 SCSI Control Signal Description

SCSI Control	Pin	Type	Description
CLOCK	121	I	40 MHz input clock
DIFFSENS	46	I	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it originates from an SE, LVD, or high-power source. This pin should be connected to the DIFFSENS signal on the SCSI cable. Note: The maximum voltage allowed to this pin is 3.3 V

3.7 Power and Ground Pins

Table 3.5 Power and Ground Signal Description

Power and Ground	Pin	Type	Description
V_{DD}_SCSI	3, 37, 47, 57, 67, 77, 91, 101, 111	I	Power supplies to the SCSI bus I/O pins
V_{SS}_SCSI	7, 12, 17, 22, 28, 33,52, 62, 68, 80, 83, 100, 106, 116, 127	I	Ground for the SCSI bus I/O pins
V_{DD}_CORE	41, 124	I	Power supplies to the CORE logic
V_{SS}_CORE	44, 119	I	Ground for the CORE logic
5VBIAS	39	I	5 V biasing pin. This pin must be supplied with 5 V in a 5 V environment Connecting 5VBIAS pin to 5 V allows for 5 V inputs on the CLK, WS_ENABLE, and RESET/ Connecting 5VBIAS pin to 3.3 V allows for 3.3 V inputs on the CLK, WS_ENABLE, and RESET/ pins

Note: All V_{DD} pins must be supplied 3.3 volts. The LSI53C141 output signals drive 3.3 volts.

Note: If you separate the power supplies to V_{DD}_IO and V_{DD}_CORE pins in a chip testing environment, either power up the pins simultaneously or power up V_{DD}_CORE before V_{DD}_IO. The V_{DD}_IO pin must always power down before the V_{DD}_CORE pin.

3.8 No Connection Pins

Table 3.6 No Connect Pins

No Connects	Pin	Type	Description
NC	2, 38, 40, 43, 86, 123, 125	NC	Make no external connection

Table 3.7 Internal Test Pins

Internal Test	Pin	Type	Description
Reserved	1, 42, 122	Reserved	Pull-ups should be connected to the following pins: 1, 42, and 122. (4.5K resistor to +5 V or 3.3 V)
Reserved	120	Reserved	A pull-down should be connected to pin 120 (100 Ω resistor to ground)

Chapter 4
Specifications

4.1 DC Characteristics

Table 4.1 Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	–55	150	°C	–
V_{DD}	Supply voltage	–0.5	5.0	V	–
V_{IN}	Input Voltage	V_{SS} –0.3	V_{DD} +0.3	V	–
I_{LP}[1]	Latch-up current	±150	–	mA	–
ESD[2]	Electrostatic discharge	–	2 K	V	MIL-STD 883C, Method 3015.7

1. $-2\ V < V_{PIN} < 8\ V$.
2. SCSI pins only.

Note: Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.

Table 4.2 Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	3.1	3.45	V	–
I_{DD}	Supply current (dynamic SE) Supply current (dynamic LVD) Supply current (static)	– – –	130 600 1	mA mA mA	– RBIAS = 2.0 kΩ, 1% V_{DD} = 3.3 V –
T_A	Operating free air	0	70	°C	–
θ_{JA}	Thermal resistance (junction to ambient air)	–	67	°C/W	–

Note: Conditions that exceed the operating limits may cause the device to function incorrectly.

Table 4.3 SCSI Signals—A_SD[15:0]/, A_SDP[1:0]/, A_SREQ/, A_SACK/, B_SD[15:0], B_SDP[1:0], B_SREQ, B_SACK

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	1.9	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	1.0	V	–
V_{OH}*	Output high voltage	2.4	3.5	V	2.5 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	48 mA
I_{OZ}	3-state leakage	–10	10	µA	–

Note: TolerANT active negation enabled.

Table 4.4 SCSI Signals—A_SCD/, A_SIO/, A_SMSG/, A_SBSY/, A_SATN/, A_SSEL/, A_SRST/, B_SCD, B_SIO, B_SMSG, B_SBSY, B_SATN, B_SSEL, B_SRST

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	1.9	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	1.0	V	–
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage (SRST/ only)	–10 –500	10 –50	µA	–

Table 4.5 Input Signal—CLOCK

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{IN}	Input leakage	–20	20	µA	–

Table 4.6 Input Signal—DIFFSENS

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{IN}	Input leakage	–10	10	µA	–

Table 4.7 Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

Table 4.8 SCSI Signals, LVD Drivers—B_SD[15:0], B_SDP[1:0], B_SCD, B_SIO, B_SMSG, B_SREQ, B_SACK, B_SBSY, B_SATN, B_SSEL, B_SRST*

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	7	11	mA	Asserted state
I_O-	Sink (–) current	–7	–11	mA	Asserted state
I_O+	Source (+) current	–3.5	–5.5	mA	Negated state
I_O-	Sink (–) current	3.5	5.5	mA	Negated state
I_{OZ}	3-state leakage	–20	20	µA	–
*I_{OZ} (SRST-only)	3-state leakage	–500	–50	µA	–

V_{CM} = 0.7–1.8 V.
R_L = 0–110 Ω.
R_{bias} = 2.0 kΩ.

Figure 4.1 LVD Transmitter

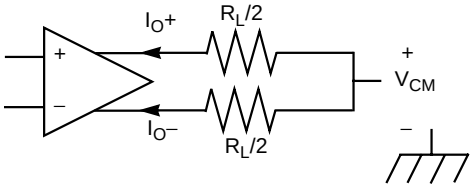


Table 4.9 SCSI Signals, LVD Receivers—B_SD[15:0], B_SDP[1:0] ,B_SCD, B_SIO, B_SMSG, B_SREQ, B_SACK, B_SBSY, B_SATN, B_SSEL, B_SRST

Symbol	Parameter	Min	Max	Units
V_I	LVD receiver voltage asserting	60	–	mV
V_I	LVD receiver voltage negating	–	–60	mV

V_{CM} = 0.7–1.8 V

Figure 4.2 LVD Receiver

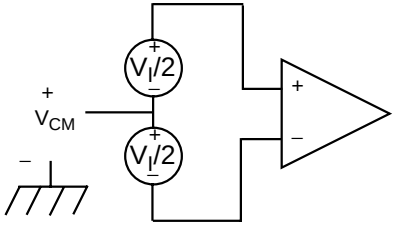


Table 4.10 SCSI Signal—DIFFSENS

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	HVD sense voltage	2.4	V_{DD} +0.3	V	–
V_S	LVD sense voltage	.7	1.9	V	–
V_{IL}	SE sense voltage	V_{SS} –0.3	0.5	V	–
I_{OZ}	3-state leakage	–10	10	µA	–

Table 4.11 Control Signals—RESET/, WS_ENABLE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	V_{SS} –0.5	0.8	V	–
I_{OZ}	3-state leakage	–20	20	µA	–

Table 4.12 Control Signals—XFER_ACTIVE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	3-state leakage	–10	10	µA	–

4.2 TolerANT Technology Electrical Characteristics

Table 4.13 TolerANT Technology Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.5	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	1.9	7.0	V	–
V_{IL}	Input low voltage	–0.5	1.0	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75; I_I = – 20 mA
V_{TH}	Threshold, high to low	1.1	1.3	V	–
V_{TL}	Threshold, low to high	1.5	1.7	V	–
V_{TH}-V_{TL}	Hysteresis	200	400	mV	–
I_{OH}[1]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[1]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–	– 10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	20	–	MΩ	SCSI pins[3]
C_P	Capacitance per pin	–	10	pF	PQFP
t_R[1]	Rise time, 10% to 90%	9.7	18.5	ns	Figure 4.3

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

Table 4.13 TolerANT Technology Electrical Characteristics (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
t_F	Fall time, 90% to 10%	5.2	14.7	ns	Figure 4.3
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.49	V/ns	Figure 4.3
dV_L/dt	Slew rate, HIGH to LOW	0.19	0.67	V/ns	Figure 4.3
ESD	Electrostatic discharge	2	–	kV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	10	15	ns	Figure 4.4

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

1. Active negation outputs only: Data, Parity, SREQ/, SACK/.
2. Single pin only; irreversible damage may occur if sustained for one second.
3. SCSI RESET pin has 10 kΩ pull-up resistor.

Figure 4.3 Rise and Fall Time Test Conditions

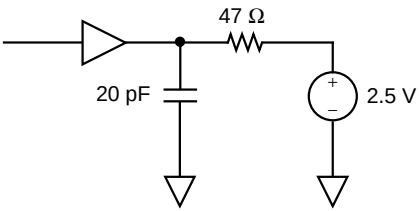


Figure 4.4 SCSI Input Filtering

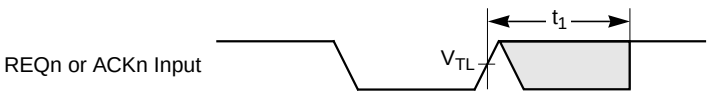


Figure 4.5 Hysteresis of SCSI Receiver

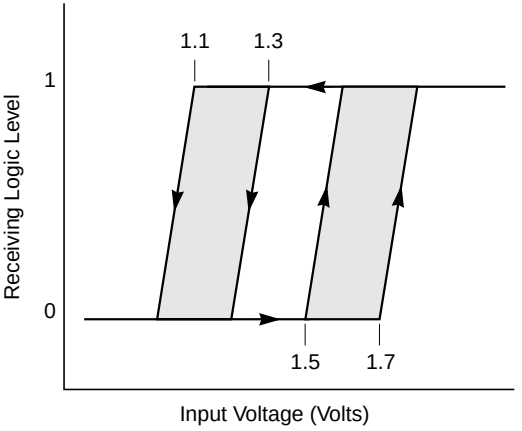


Figure 4.6 Input Current as a Function of Input Voltage

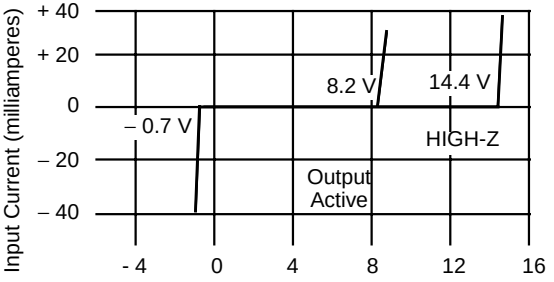
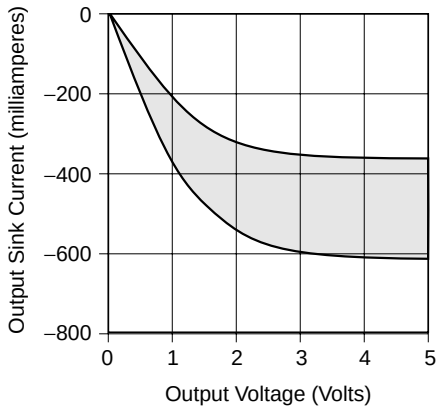
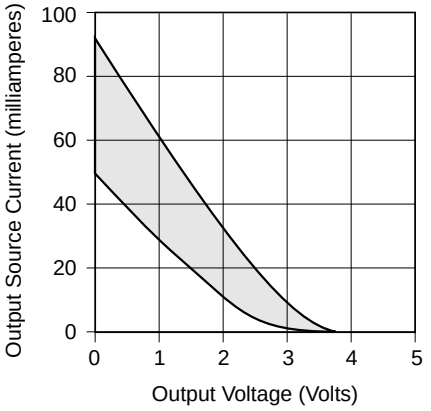


Figure 4.7 Output Current as a Function of Output Voltage





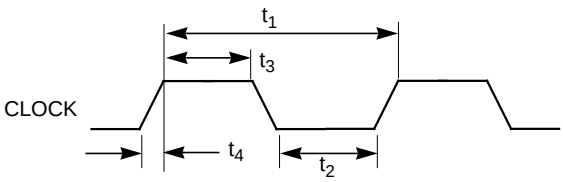
4.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Section 4.1, “DC Characteristics”). Chip timings are based on simulation at worst case voltage, temperature, and processing. The LSI53C141 requires a 40 MHz clock input.

Table 4.14 Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Clock period	24.5	25.5	ns
t_2	Clock LOW time	10	15	ns
t_3	Clock HIGH time	10	15	ns
t_4	Clock rise time	1	–	V/ns

Figure 4.8 Clock Timing



4.3.1 SCSI Interface Timings

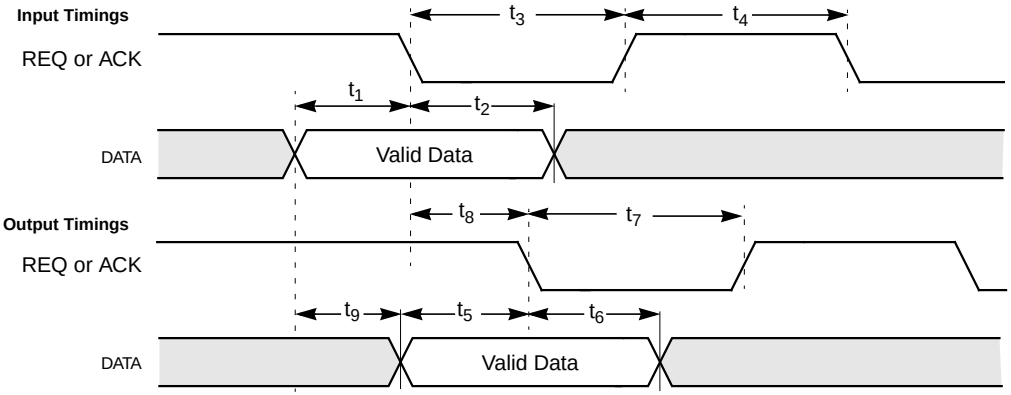
Table 4.15 Input Timings

Symbol	Parameter	Min	Max	Units
t_1	Input data setup	2	–	ns
t_2	Input data hold	6	–	ns
t_3	Input REQ/ACK assertion pulse width	11	–	ns
t_4	Input REQ/ACK deassertion pulse width	16	–	ns

Table 4.16 Output Timings

Symbol	Parameter	Min	Max	Units
t_5	Output data setup	min [t_1 + 18ns, t_4 + 5]	–	ns
t_6	Output data hold	max [18, (t_2 –20), t_3]	–	ns
t_7	Output REQ/ACK pulse width	max [20 ns, t_3 –5]	max [30 ns, t_3 +5]	ns
t_8	REQ/ACK transport delay	25 ns if REQ/ACK is clock for input data,10 ns if not	50 ns if REQ/ACK is clock for input data, 30 ns if not	ns
t_9	Data transport delay	6	[t_3 +35]	ns

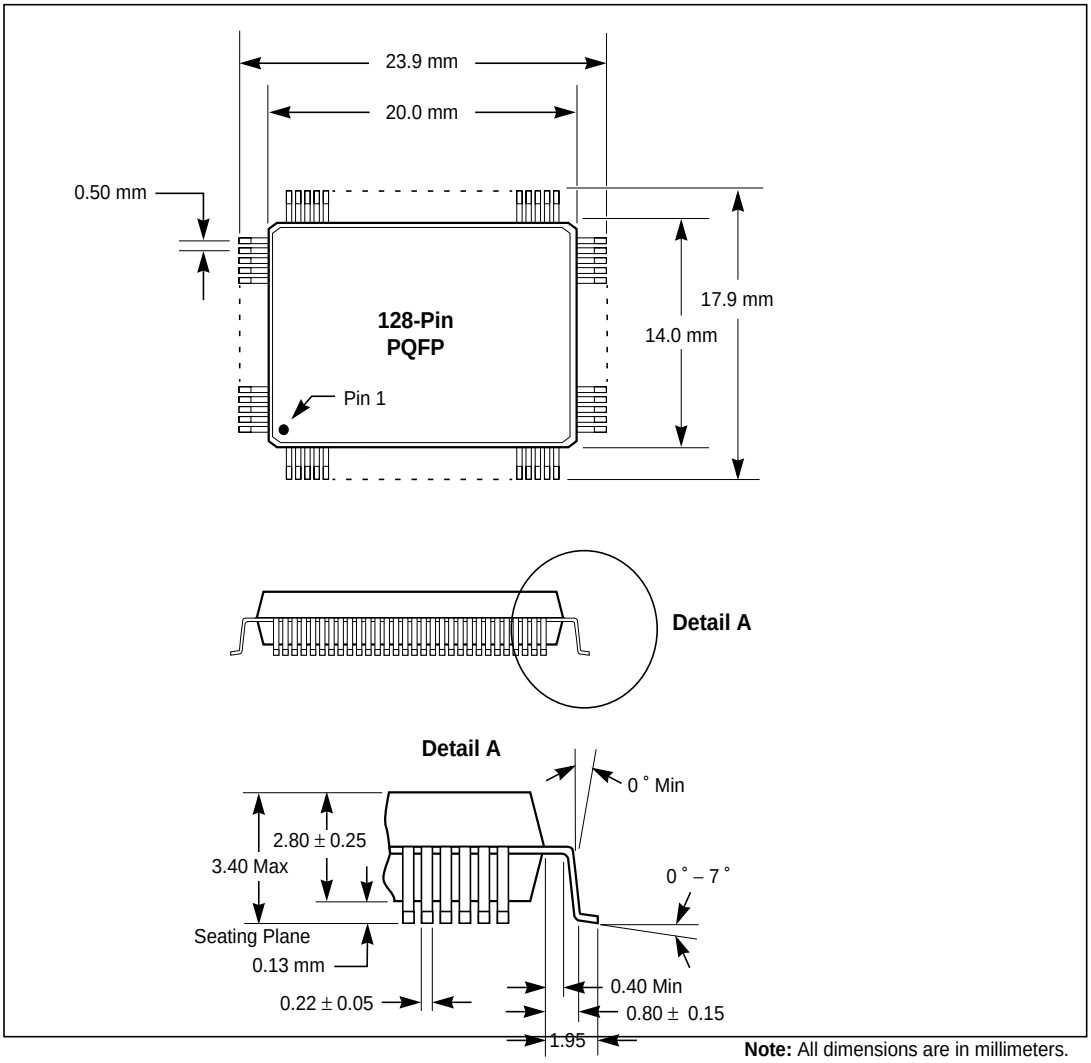
Figure 4.9 Input/Output Timings



4.4 LSI53C141 Mechanical Drawing

The LSI53C141 comes in a 128-pin metric PQFP with a 3.9 mm footprint.

Figure 4.10 LSI53C141 Mechanical Drawing



Note: All dimensions are in millimeters.

Important: This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing.

Appendix A
Glossary of Terms and Abbreviations

ACK/ Acknowledge	Driven by an initiator, ACK/ indicates an acknowledgment for a SCSI data transfer. In the target mode, ACK/ is received as a response to the REQ/ signal.
ANSI	American National Standards Institute.
Arbitration	The process of selecting one respondent from a collection of several candidates that request service concurrently.
Asserted	A signal is asserted when it is in the state which is indicated by the name of the signal. Opposite of negated or deasserted.
Assertion	The act of driving a signal to the true state.
Asynchronous Transmission	Transmission in which each byte of the information is synchronized individually, through the use of Request (REQ/) and Acknowledge (ACK/) signals.
ATN/ Attention	Driven by an initiator, indicates an attention condition. In the target role, ATN/ is received and is responded to by entering the Message Out Phase.
Block	A block is the basic 512 byte region of storage into which the storage media is divided. The Logical Block Address protocol uses sequential block addresses to access the media.
BSY/ Busy	Indicates that the SCSI Bus is being used. BSY/ can be driven by both the initiator and the target device.
Bus	A collection of unbroken signal lines that interconnect computer modules. The connections are made by taps on the lines.
Bus Expander	Bus expander technology permits the extension of a bus by providing some signal filtering and retiming to maintain signal skew budgets.

Cable Skew Delay — Cable skew delay is the minimum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices.

C_D/ Control/Data — Driven by a target, indicates Control or Data Information is on the SCSI Bus. This signal is received by the initiator.

Connect — The function that occurs when an initiator selects a target to start an operation, or a target reselects an initiator to continue an operation.

Control Signals — The set of nine lines used to put the SCSI bus into its different phases. The combinations of asserted and negated control signals define the phases.

Controller — A computer module that interprets signals between a host and a peripheral device. Often, the controller is a part of the peripheral device, such as circuitry on a disk drive.

DB0/-DB7/ — SCSI Data Bits and Parity Bit
These eight Data Bits (DB0/–DB7/), plus a Parity Bit (DBP/), form the SCSI bus. DB7/ is the most significant bit and has the highest priority ID during the Arbitration Phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.

Deasserted — The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition). A signal is deasserted or negated when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.

Device — A single unit on the SCSI bus, identifiable by an SCSI address. It can be a processor unit, a storage unit (such as a disk or tape controller or drive), an output unit (such as a controller or printer), or a communications unit.

Differential — A signaling alternative that employs differential drivers and receivers to improve signal-to-noise ratios and increase maximum cable lengths.

Disconnect — The function that occurs when a target releases control of the SCSI bus, allowing the bus to go to the bus free phase.

Driver — When used in the context of electrical configuration, “driver” is the circuitry that creates a signal on a line.

External Configuration	All SCSI peripheral devices are external to the host enclosure.
External Terminator	The terminator that exists on the last peripheral subsystem that terminates the external end of the SCSI bus.
Free	In the context of bus free phase, “free” means that no SCSI device is actively using the SCSI bus and, therefore, the bus is available for use.
Host	A processor, usually consisting of the central processing unit and main memory. Typically, a host communicates with other devices, such as peripherals and other hosts. On the SCSI bus, a host has an SCSI address.
Host Adapter	Circuitry that translates between a processor's internal bus and a different bus, such as SCSI. On the SCSI bus, a host adapter usually acts as an initiator.
Initiator	A SCSI device that requests another SCSI device (a target) to perform an operation. Usually, a host acts as an initiator and a peripheral device acts as a target.
Internal Configuration	All SCSI peripheral devices are internal to the host enclosure.
Internal Terminator	The terminator that exists within the host that terminates the internal end of the SCSI bus.
I/O	Input/Output Driven by a target, controls the direction of data transfer on the SCSI bus. When active, this signal indicates input to the initiator. When inactive, this signal indicates output from the initiator. This signal is also used to distinguish between the Selection and Reselection Phases.
I/O Cycle	An I/O cycle is an Input (I/O Read) operation or Output (I/O Write) operation that accesses the PC Card’s I/O address space.
Logical Unit	The logical representation of a physical or virtual device, addressable through a target. A physical device can have more than one logical unit.
LOW (logical level)	A signal is in the LOW logic level when it is below approximately 0.5 volts.

LSB Least Significant Bit or Least Significant Byte
That portion of a number, address, or field that occurs right-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the least weight in a mathematical calculation using the value.

LUN Logical Unit Number
Used to identify a logical unit.

Mandatory A characteristic or feature that must be present in every implementation of the standard.

MHz MegaHertz
Measurement in thousands of cycles per second. Used as a measurement of data transfer rate.

µs Microsecond
One millionth of a second.

MSB Most Significant Bit and Most Significant Byte
That portion of a number, address or field that occurs left-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the most weight in a mathematical calculation using the value.

MSG/ Message Driven active by a target during the Message Phase. This signal is received by the initiator.

Negated A signal is negated or deasserted when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.

Negation The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

ns Nanosecond
One billionth of a second.

Parity A method of checking the accuracy of binary numbers. An extra bit, called a parity bit, is added to a number. If even parity is used, the sum of all ones in the number and its corresponding parity is always even. If odd parity is used, the sum of the ones and the parity bit is always odd.

Peripheral Device	A device that can be attached to an SCSI bus. Typical peripheral devices are disk drives, tape drives, printers, CD ROMs, or communications units.
Phase	One of the eight states to which the SCSI bus can be set. During each phase, different communication tasks can be performed.
Port	A connection into a bus. The SCSI bus allows eight ports.
Priority	The ranking of the devices on the bus during arbitration.
Protocol	A convention for data transmission that encompasses timing control, formatting, and data representation.
Receiver	The circuitry that receives electrical signals on a line.
Reconnect	The function that occurs when a target reselects an initiator to continue an operation after a disconnect.
Release	The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).
REQ/ Request	Driven by a target, indicates a request for an SCSI data-transfer handshake. This signal is received by the initiator.
Reselect	A target can disconnect from an initiator in order to perform a time-consuming function, such as a disk seek. After performing the operation, the target can “reselect” the initiator.
RESET Reset	Clears all internal registers when active. It does not assert the SCSI RST/ signal and therefore does not reset the SCSI bus.
RST Reset	Indicates an SCSI Bus reset condition.
SCSI Address	The octal representation of the unique address (0–7) assigned to an SCSI device. This address is normally assigned and set in the SCSI device during system installation.
SCSI ID	(Identification) or SCSI Device ID The bit-significant representation of the SCSI address referring to one of the signal lines DB0/ through DB7/.
SCSI	Small Computer System Interface.

SCAM — SCSI Configured Automatically
SCAM is the new automatic ID assignment protocol for SCSI. SCAM frees SCSI users from locating and setting SCSI ID switches and jumpers. SCAM is the key part of Plug and Play SCSI.

SEL/ Select — Used by an initiator to select a target or by a target to reselect an initiator.

Single-Ended Configuration — An electrical signal configuration that uses a single line for each signal referenced to a ground path common to the other signal lines. The advantage of a single-ended configuration is that it uses half the pins, chips, and board area that differential/low voltage differential configurations require. The main disadvantage of single-ended configurations is that they are vulnerable to common mode noise. Also, cable lengths are limited.

Synchronous Transmission — Transmission in which the sending and receiving devices operate continuously at the same frequency and are held in a desired phase relationship by correction devices. For buses, synchronous transmission is a timing protocol that uses a master clock and has a clock period.

Target — An SCSI device that performs an operation requested by an initiator.

Termination — The electrical connection at each end of the SCSI bus, composed of a set of resistors.

µs — Microsecond
One millionth of a second.

Index

Symbols

Numerics

A

B

C

D

S

T

U

V

W

X

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Tel: 852.2995.7538
Fax: 852.2950.0386

India
Bangalore
Spike Technologies India Private Ltd
951, Vijayalakshmi Complex,
2nd Floor, 24th Main,
J P Nagar II Phase,
Bangalore, India 560078
♦ Tel: 91.80.664.5530
Fax: 91.80.664.9748

Israel
Tel Aviv
Eastronics Ltd
11 Rozanis Street
P.O. Box 39300
Tel Aviv 61392
Tel: 972.3.6458777
Fax: 972.3.6458666

Japan
Tokyo
Daito Electron
Sogo Kojimachi No.3 Bldg
1-6 Kojimachi
Chiyoda-ku, Tokyo 102-8730
Tel: 81.3.3264.0326
Fax: 81.3.3261.3984

Global Electronics Corporation
Nichibei Time24 Bldg. 35 Tansu-cho
Shinjuku-ku, Tokyo 162-0833
Tel: 81.3.3260.1411
Fax: 81.3.3260.7100
Technical Center
Tel: 81.471.43.8200

Marubeni Solutions
1-26-20 Higashi
Shibuya-ku, Tokyo 150-0001
Tel: 81.3.5778.8662
Fax: 81.3.5778.8669

Shinki Electronics
Myuru Daikanyama 3F
3-7-3 Ebisu Minami
Shibuya-ku, Tokyo 150-0022
Tel: 81.3.3760.3110
Fax: 81.3.3760.3101

Yokohama-City
Innotech
2-15-10 Shin Yokohama
Kohoku-ku
Yokohama-City, 222-8580
Tel: 81.45.474.9037
Fax: 81.45.474.9065

Macnica Corporation
Hakusan High-Tech Park
1-22-2 Hadusan, Midori-Ku,
Yokohama-City, 226-8505
Tel: 81.45.939.6140
Fax: 81.45.939.6141

The Netherlands
Eindhoven
Acal Nederland b.v.
Beatrix de Rijkweg 8
5657 EG Eindhoven
Tel: 31.40.2.502602
Fax: 31.40.2.510255

Switzerland
Brugg
LSI Logic Sulzer AG
Mattenstrasse 6a
CH 2555 Brugg
Tel: 41.32.3743232
Fax: 41.32.3743233

Taiwan
Taipei
Avnet-Mercuries Corporation, Ltd
14F, No. 145,
Sec. 2, Chien Kuo N. Road
Taipei, Taiwan, R.O.C.
Tel: 886.2.2516.7303
Fax: 886.2.2505.7391

Lumax International Corporation, Ltd
7th Fl., 52, Sec. 3
Nan-Kang Road
Taipei, Taiwan, R.O.C.
Tel: 886.2.2788.3656
Fax: 886.2.2788.3568

Prospect Technology Corporation, Ltd
4Fl., No. 34, Chu Luen Street
Taipei, Taiwan, R.O.C.
Tel: 886.2.2721.9533
Fax: 886.2.2773.3756

Wintech Microeletronics Co., Ltd
7F., No. 34, Sec. 3, Pateh Road
Taipei, Taiwan, R.O.C.
Tel: 886.2.2579.5858
Fax: 886.2.2570.3123

United Kingdom
Maidenhead
Azzurri Technology Ltd
16 Grove Park Business Estate
Waltham Road
White Waltham
Maidenhead, Berkshire SL6 3LW
Tel: 44.1628.826826
Fax: 44.1628.829730

Milton Keynes
Ingram Micro (UK) Ltd
Garamonde Drive
Wymbush
Milton Keynes
Buckinghamshire MK8 8DF
Tel: 44.1908.260422

Swindon
EBV Elektronik
12 Interface Business Park
Bincknoll Lane
Wootton Bassett,
Swindon, Wiltshire SN4 8SY
Tel: 44.1793.849933
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