L64777
DVB QAM Modulator

Technical Manual

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LSI LOGIC®

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This document describes revision A of the LSI Logic Corporation L64777 DVB QAM Modulator and will remain the official reference source for all revisions of this product until rescinded by an update.

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Preface

This book is the primary reference and technical manual for the L64777 DVB QAM Modulator. It contains a complete functional description for the L64777 and includes complete physical and electrical specifications for the L64777.

Audience

This document assumes that you have some familiarity with digital video broadcasting, QAM modulators, and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the modulator for possible use in a system
- Engineers who are designing the modulator into a system

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, introduces the L64777 DVB QAM Modulator.
- Chapter 2, **Modulator Architecture**, describes the functional components of the L64777.
- Chapter 3, **Interfaces**, describes the L64777 interfaces.
- Chapter 4, **Register Descriptions**, describes the registers used to configure and monitor the L64777.
- Chapter 5, **Signals**, presents the signal definitions for the L64777.

- Chapter 6, **Specifications**, presents the electrical and timing specifications for the L64777. It also presents the pinout and packaging information.
- Appendix A, **Programming the L64777 in Serial Host Interface Mode**, discusses how to program the L64777 internal registers and data tables in serial host interface mode.
- Appendix B, **PLL Divider Settings and L64724/34 Connection**, lists the PLL divider settings for typical applications. It also describes the L64777 connection to the L64724.
- Appendix C, **Monitoring Device Internal Signals**, describes how to program test register (14) for monitoring of device internal signals.

Related Publications

Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems ETS 300 429, September 1996.

Generic Coding of Moving Pictures and Associated Audio, ISO/IEC 13818-1, MPEG2 Systems, November 1994.

G10®-p CW900100 10-Bit Direct Digital Synthesis Digital-to-Analog Converter, Preliminary Datasheet, LSI Logic, September 1998.

L64724 Satellite Receiver Technical Manual, LSI Logic, April 2000, order number I14030.

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

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Chapter 1
Introduction

This chapter provides an introduction to the L64777. It consists of the following sections:

1.1 Overview

The L64777 chip implements a QAM modulator that is digital video broadcasting (DVB)-compliant, as described in document ETS 300 429. The input is an MPEG-2 system layer-compliant transport stream either in parallel byte-wide or serial format. The chip contains digital signal processing functions, digital-to-analog converters, and sampling clock circuitry that generates a quadrature amplitude modulation (QAM)-modulated output signal in baseband. Users can configure the device by means of its serial interface.

The L64777 chip design is based on the existing LSI Logic L64767 device and includes the following major enhancements:

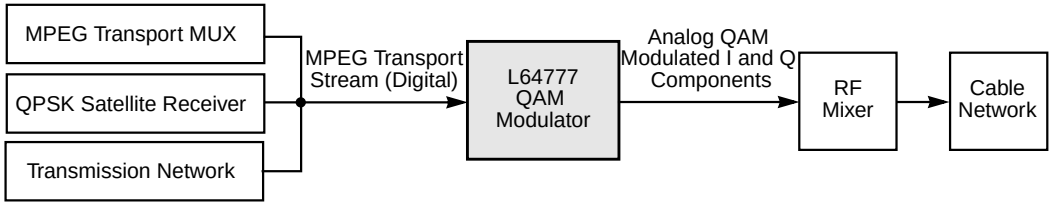
- Two internal digital-to-analog converters generate in-phase and quadrature (I and Q) baseband signals.
- An on-chip voltage-controlled oscillator improves the symbol rate PLL to support most frequently used application ranges.
- A serial interface replaces the eight-bit microprocessor interface.
- A digital numerically controlled oscillator (NCO) and interpolation mode support operation with the L64724 device.

1.2 Operating Environment

The modulator is intended to follow either an MPEG transport stream source (for example, a transport multiplexer) or a satellite receiver, such as the LSI Logic L64724 (see Figure 1.1). It processes MPEG-2 system-compliant frames at the input.

You can program the sync word and block length, and the chip can reinsert the sync information. The device handles the MPEG-specific transport-packet error indication (TEI) bit internally.

Figure 1.1 L64777 Operating Environment



The features of the L64777 include:

- DVB standard ETS 300 429-compliant modulation operation
- Highly integrated global synchronization and clock control
- On-chip VCO to support symbol rates up to 10 Msymbols/s
- Digital NCO and interpolation mode to support operation with the L64724
- Four-fold Nyquist filter oversampling
- Maskable interrupts for all error conditions
- Individual module bypass configuration modes
- I and Q baseband outputs both in digital and analog formats
- I^2C-compatible serial interface for control, setup, and monitoring of various chip parameters
- User-controllable input synchronization schemes
- 16, 32, 64, 128, and 256 QAM modes
- Reed-Solomon encoder

- Frame sync byte reinsertion
- Input jitter handling and Reed-Solomon gap insertion by a 128-word circular FIFO buffer
- IEEE 1149.1 JTAG interface for testing
- Up to 10 Mbytes/s parallel data input
- Up to 60 Mbits/s serial data input
- Up to 11.25 Mbaud operation in NCO mode of operation
- Easy interface to most input sources
- 85 ˚C ambient operation without special cooling devices
- Unconstrained serial mode to allow modulation of non-MPEG data stream

Chapter 2
Modulator Architecture

This chapter briefly introduces the standard modulator chain and the architecture the device uses to implement the chain. This chapter consists of the following sections:

2.1 Introduction

The L64777 implements the modulator processing chain defined in ETS 300 429. This processing chain is illustrated in Figure 2.1.

Figure 2.1 ETS 300 429-Compliant Modulation Operation

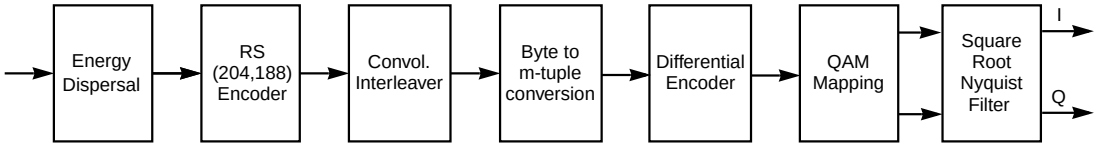
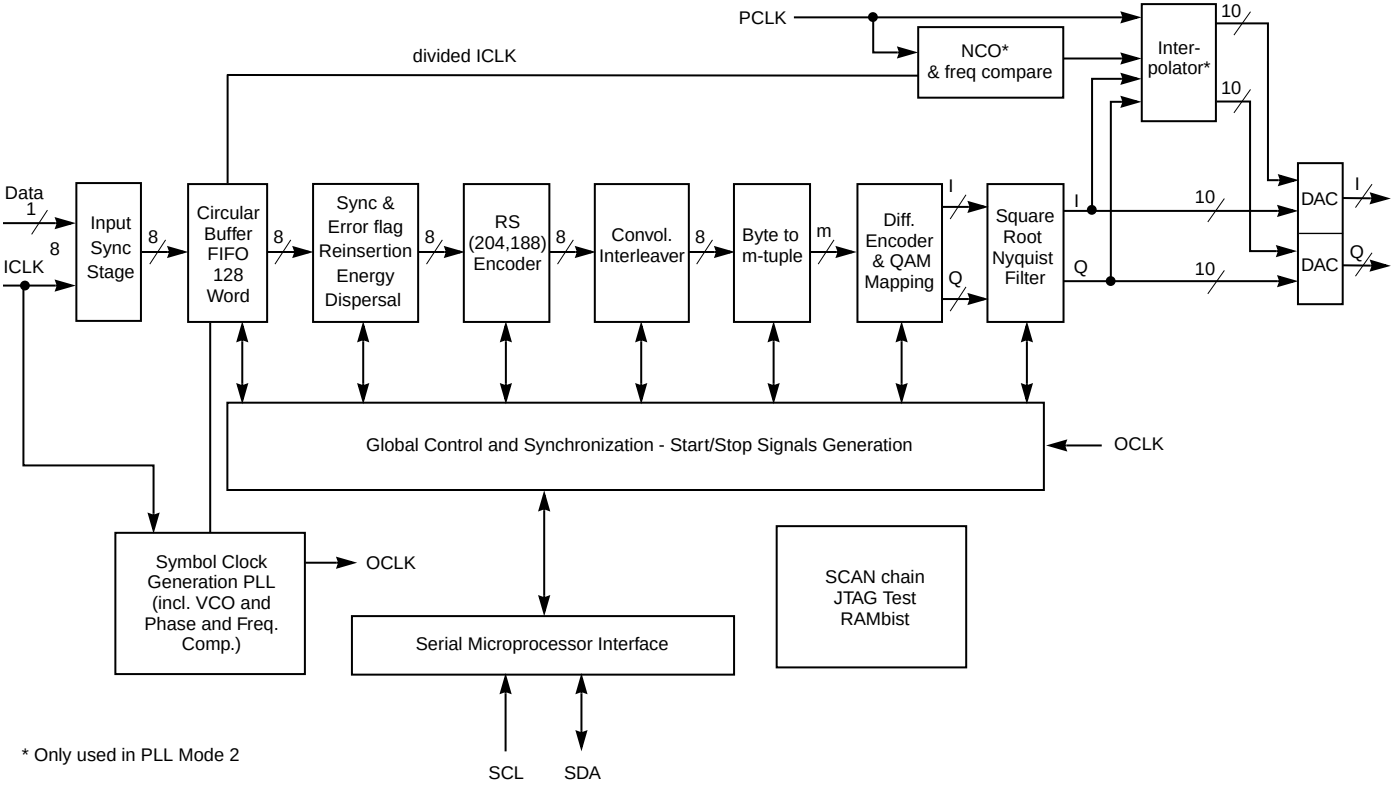


Figure 2.2 is a block diagram of the L64777 architecture. The input clock drives only the input synchronizing stage. The OCLK, which is four times the QAM symbol rate, is the base of all residual processing.

A numerically controlled oscillator (NCO) module allows the L64777 to interface with LSI Logic L64724. In this case, the chip must receive the L64724 PCLK clock; thus, the byte_clock output from L64724 must be applied to ICLK. This assumes the PCLK has generated the byte clock.

Figure 2.2 Data Path



The QAM mapping supports 16, 32, 64, 128, and 256 QAM. The input to the device is an MPEG-2 compliant transport stream; its output consists of baseband QAM signals in I and Q.

2.2 PLL Modes

Connecting the L64777 to a satellite receiver and the LSI Logic satellite decoder chip set requires the PLL circuits to lock the input and output clocks. Two modes can achieve this:

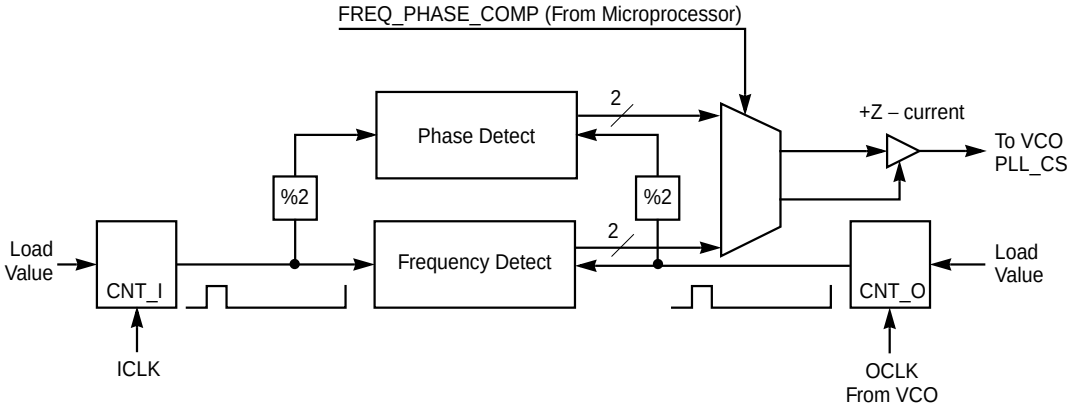
- **Mode 1** uses the phase/frequency detector and the dividers of L64777 to accept an external VCO.
- **Mode 2** connects the PCLK output of L64724 or L64734 to the L64777 PCLK clock input, and connects the byte clock output to the ICLK input of the L64777. This is also called the Numerically Controlled Oscillator (NCO) mode of operation. This mode is dedicated to the connection of the L64724 (see Appendix B, PLL Divider Settings and L64724/34 Connection).

Set the PLL_MODE[1:0] pins to the values shown on page 5-6. Do not change it during operation.

2.2.1 PLL Mode 1

Figure 2.3 shows the phase and frequency detection for an external voltage-controlled oscillator (VCO) loop. Choose between frequency and phase detection through the microprocessor interface.

Figure 2.3 Phase and Frequency Detection with an External VCO



Prescalers (CNT_I) and a divider (CNT_O) in the feedback loop of the PLL generate the internal operating clock (OCLK). Program the 15-bit prescalers through the microprocessor interface, selecting values for CNT_I and CNT_O that minimize CNT_O and reach the required ratio.

2.2.2 PLL Mode 2

In Mode 2, the PCLK input provides an external clock. The L64777 uses the internal NCO to lock to the transport byte clock, provided at ICLK. The chip generates an OCLK internally. Select PCLK to be at least twice the frequency of the internal OCLK. Appendix B, PLL Divider Settings and L64724/34 Connection, describes the connection between the L64777 and the L64724 in Mode 2 operation.

Consecutive sync blocks can have any gap length between them. Thus, the L64777 can convert an input block to a block with a gap for RS insertion, as long as the size of the 128-byte circular input buffer is sufficient to insert RS gaps and to cope with possible PLL jitter. For an encoder with 16-parity RS insertion, the L64777 selects the size of the circular input buffer with sufficient margin.

When operating on public synchronous networks (such as the synchronous digital hierarchy, SDH, or plesiochronous digital hierarchy, PDH), the system designer must consider possible jitter on the input network. The design of the L64777 permits short-term deviations of input-to-output frequency of $\pm$ 56 bytes before a FIFO overrun condition occurs. This is sufficient for operations on SDH or PDH networks.

On ATM networks, you must prebuffer input data to get a continuous frame rate at the chip input. If high input jitter occurs over an ATM without a prebuffer, the whole PLL regulation of the input-to-output frame rate fails. You must design the size of the prebuffer according to the maximum jitter expected over the asynchronous transfer mode (ATM) network.

2.3 I/O

The following subsections describe the input and output of the L64777.

2.3.1 Input

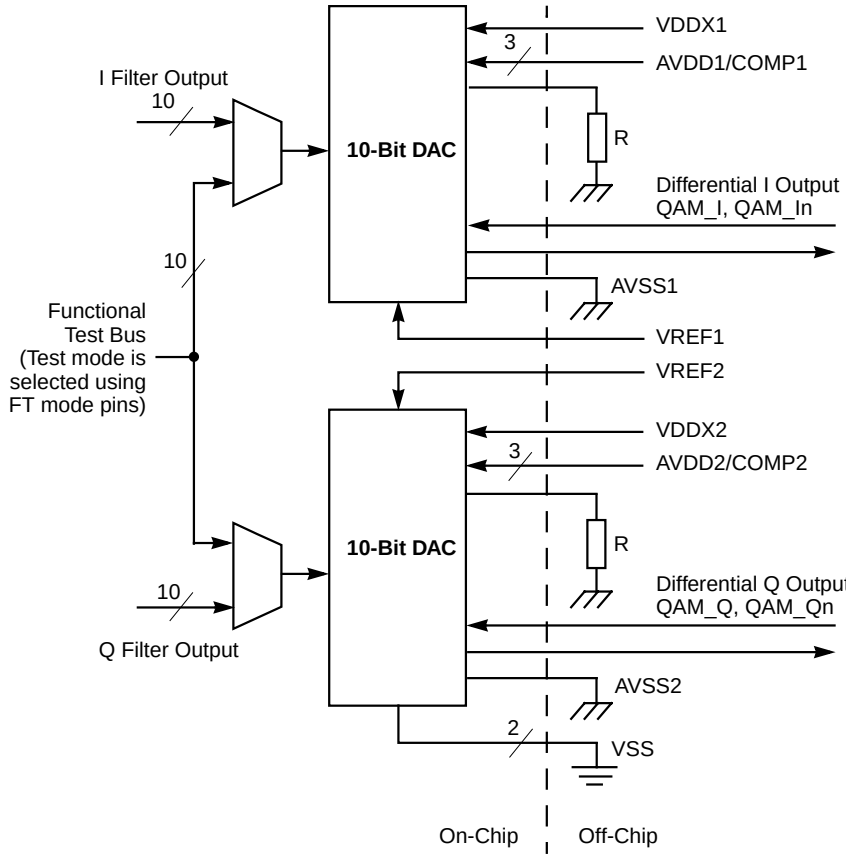
The QAM Modulator accepts serial input data at a maximum 54 MHz clock frequency on the ICLK pin. In Byte-Parallel Input mode (Parallel mode), the maximum frequency on ICLK is 10 MHz. DVALIDIN distinguishes between valid and invalid input data on DIN[7:0]. ERRORIN marks incorrect packets in the transport header, in case a preceding device passes erroneous information. The input error flag is transferred into the TRANSPORT_ERROR_INDICATOR bit of MPEG transport packets. Either the FSTARTIN pulse or the SYNC_BYTE detection (0x47 for MPEG transport packets) establishes input synchronization.

The FSTARTIN pulse marks the first bit, the most significant bit of an MPEG SYNC_BYTE in Serial Input mode (Serial mode), or the SYNC_BYTE in Parallel mode. The FSTARTIN pulse synchronizes the process of forming bytes from bits in Serial mode. If no such synchronization signal is applied, the input synchronizer searches for the programmed SYNC_BYTE occurring in the programmed sync length. In Parallel mode, the L64777 assumes the byte boundaries are correct and compares the SYNC_BYTE in parallel to the incoming bytes. A flywheel circuit stabilizes the synchronization to a SYNC_BYTE, while synchronization by external pulses feeds directly into the internal control circuits (see Section 2.4, “Input Synchronization,” page 2-10).

2.3.2 Output Signals

The L64777 outputs the I and Q components of its signal on two separate analog output interfaces (see Figure 2.4). The output interface contains two internal 10-bit digital-to-analog converters.

Figure 2.4 Analog I/Q Output Interface Diagram



The differential outputs terminate externally (the external components must provide termination to both differential lines, and the DAC achieves maximum linearity in differential mode).

The L64777 I and Q component outputs are available in 10-bit digital format. The related clock depends on the PLL mode: OCLK is used in Mode 1; PCLK is used in Mode 2. The output format can be programmed either as a two's complement, or as a sign magnitude representation.

The analog I- and Q-modulated output signals are at a sampling rate of OCLK, which is four times the QAM symbol rate. The input to the digital-to-analog conversion is available also in a digital format at the DIG_I and DIG_Q bus pins.

The internal VCO of the L64777 can generate OCLK, or it can use the OCLK input. The L64777 selects OCLK based on the selected PLL mode.

OCLK drives the Nyquist filter and generates the symbol-processing clock inside the chip after the input circular buffer. The beginning of a sync frame at the I and Q output is indicated by the FSTARTOUT signal. FSTARTOUT lets the L64777 watch for gap insertion in the RS code at the FIFO read side. As long as the read pointers are halted to generate gaps, FSTARTOUT remains HIGH for the number of RS check words plus one cycle. For example, FSTARTOUT is one symbol clock cycle long if no gap is inserted; it is 17 symbol clock cycles long if a gap for 16 RS check words is inserted.

The signal FIRSTOUT indicates the head of a sequence after reset with the SSTARTIN signal. The negative slope of the SSTARTIN input pin controls sequence reset.

Note: DVALIDIN must be active for at least one ICLK cycle when SSTARTIN is HIGH and when SSTARTIN is LOW.

2.3.3 Control Interface

An external CPU uses the L64777 serial control interface to control and setup the programmable parameters of the chip. This interface is a slave-type only, connected to the same serial bus as LSI Logic L64724.

The chip has five hardwired MSBs and takes two LSBs directly from the input pins SB_BASE[1:0].

Bit 6, MSB	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0, LSB
1	1	0	1	0	SB_BASE.1	SB_BASE.0

The addressing scheme in the L64777 complies with that of the LSI Logic L64724, but due to its small, seven-bit internal address space, the L64777 supports only group 0 and group 2 registers. It ignores all others. Bits [2:0] within the first data byte transmitted to the device specify the group.

Group 0 is the address pointer register (APR); the I^2C-Compatible Serial Control Interface loads the address byte into APR0 (see Appendix A, "Programming the L64777 in Serial Host Interface Mode"), for programming details. Reading or writing from Group 2 causes a data transfer with the device address specified by APR0:

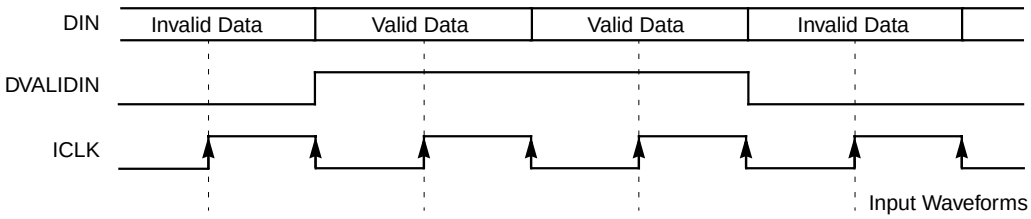
- If APR0 is set to zero, the Serial Control Interface expects a write access with 196 data bytes to load the filter coefficients; it does not apply an autoincrement to APR0.
- If APR0 is not at zero, the Serial Control Interface expects only a single data byte and applies an autoincrement to the APR0.

The detailed timing of the serial bus is given in Appendix A. The serial bus runs at a maximum 400 kHz clock rate. The serial control interface can transfer reads and writes in single-byte or burst mode. It must access the status registers 12 and 13 with single-byte reads.

The division factor for converting OCLK down to the symbol clock is always four. Input synchronization works at the ICLK rate, either on a bit or byte clock. Energy dispersal (scrambling), Reed-Solomon encoding, convolutional interleaving, byte to m-tuple conversion, differential encoding, and QAM mapping operate at the symbol clock rate (OCLK/4). The final Nyquist filter works on the OCLK rate.

Incoming bits are provided with an input clock (ICLK) and a validation signal (DVALIDIN), which indicates the rising edges of ICLK that are carrying valid data. These inputs feed into a 128-word circular FIFO buffer. The output carries a continuous data stream if the PLL is properly locked.

Figure 2.5 Required Relation of ICLK and DIN/DVALIDIN



2.3.4 Serial Microprocessor Interface

A bidirectional microprocessor interface allows write and confidence read-back of internal registers. No interaction during operation is required with the microprocessor, but all registers must be configured after a RESET to guarantee proper operation of the device. A default setup that requires no microprocessor download is built in for 64 QAM.

In the L64777, the Group 2 register 0 acts as a sequential download register that feeds the 196 bytes of filter coefficients. After every write, the user can read back the last written coefficient to verify the tail entry of the coefficients shift register. The L64777 uses all other registers nonsequentially; these can be read back directly.

2.4 Input Synchronization

The L64777 transport interface reads the data stream from the transport source, identifies the position of the synchronization bytes, and strips off invalid data. The transport interface can operate in either Parallel or Serial mode.

The L64777 can synchronize the transport interface in two ways. In both modes, it works synchronously with ICLK and reads all signals, including input data, on the raising edge of ICLK.

- In **external synchronization** mode, the transport interface specifies the position of the external sync byte by asserting FSTARTIN HIGH during sync byte input. In serial mode, the interface must assert the signal HIGH during the first bit (MSB) of the input stream.
- In **internal synchronization** mode, the L64777 does not require a block start indication and finds the position of the programmed sync byte automatically.

The transport interface also can apply the signal DVALIDIN, indicating valid input data, to allow gaps between input bytes. To avoid cyclic buffer overrun or underrun, the average data input rate, measured over the programmed block length, must not differ from the nominal payload rate of the generated QAM signal. The circular buffer inside the L64777 allows a maximum 64-byte compensation of the input stream.

Synchronizing the QAM modulator with an input pulse at SSTARTIN sets the byte and block boundaries with this external pulse. The transport interface can reinsert the programmed sync byte at the location defined by the external pulse.

In both the internal and external modes, the transport interface can program the block length and the value of the sync byte. The block length must be less than 256 bytes.

After the L64777 achieves synchronization, it either takes the sync byte from the FIFO, or it inserts the sync byte into the modulated stream according to the programmed sync byte. Only the latter action eliminates any error in the input sync byte, as long as the modulator remains synchronized (see Section 2.6.3, “Energy Dispersal (Scrambler) Unit” for more information).

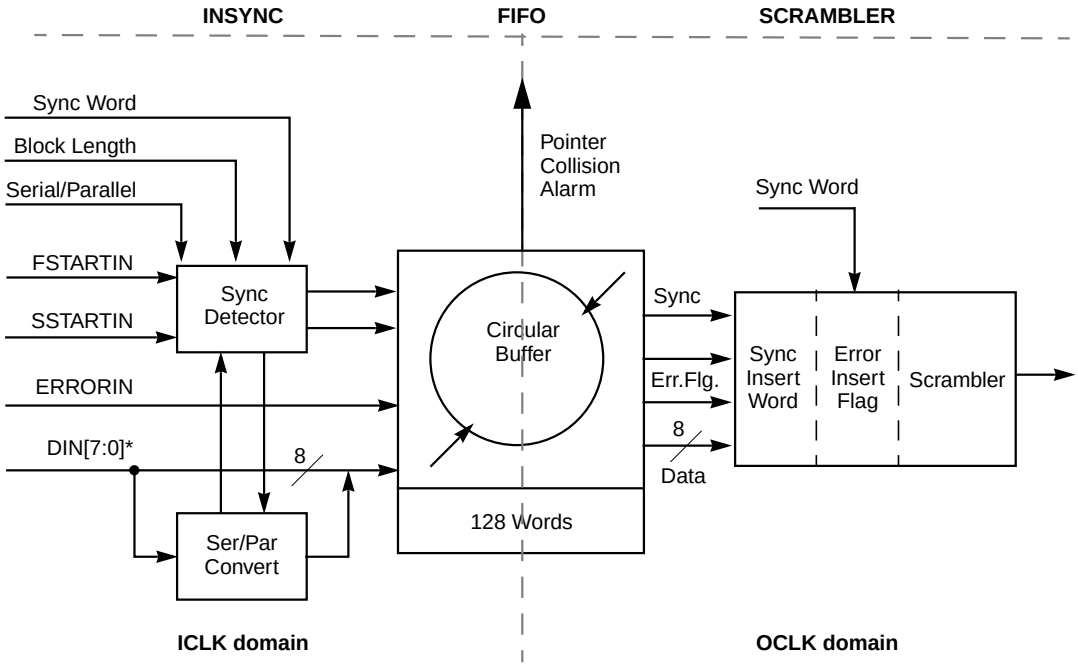
Given a bit stream consisting of a sequence of TS packets, the sync stage searches for the preprogrammed sync byte (0x47). Upon meeting the sync acquisition criteria, the sync stage issues the control strobes for the downstream modules. In addition to synchronizing the L64777 to SYNC_BYTEs contained in the input stream, the L64777 can be forced into synchronization by external sync pulses; the modulator can be made to reinsert the programmed SYNC_BYTE at the sync pulse position.

The transport interface can either pass on a transport error indicator (TEI) unchanged from the input transport stream, or it can force the TEI to indicate an error with the ERRORIN signal. The L64777 observes the forced signal during the sync byte input and ignores it for the rest of the input packet.

The L64777 input stage can operate either in Parallel or Serial mode. The device receives parallel input for connection to transport layer multiplexers at low frequency but with 11 input lines (CLK, 8 lines data, FSTARTIN, and DVALIDIN, if required). The L64777 can mark the MPEG frame SYNC_BYTE with a pulse on FSTARTIN to identify the beginning of a frame. Together with FSTARTIN, the L64777 can insert sync bytes and error-correction information into the 204 byte frames.

Figure 2.6 shows the FIFO clock conversion from the ICLK domain to the OCLK domain.

Figure 2.6 FIFO Clock Conversion



* Note that DIN[7:0] is valid data, which is the result of D[7:0] and DVALIDIN HIGH

The L64777 synchronizes the input in the ICLK domain and transfers it to the OCLK domain with a reserved bit in the circular buffer. It uses a second bit to transfer the incoming error flag for further insertion into the most significant bit (MSB) of the second byte of a sync frame, according to the MPEG-2 standard.

The L64777 also synchronizes the SSTARTIN pin through the circular buffer, allowing it to lock the beginning of any long-term sequence to the SYNC_BYTE location of the next sync block. If this pin is not activated after a reset, all generated sequences run free.

When using the L64777 with the L64724, select Parallel mode, which is supported with external synchronization pulses. Use the SPI of L64724 in Mode 2 (204 cycle frames with DVALIDIN LOW during the check bytes). A TEI bit set in the transport stream indicates frames with errors.

A single-line transmission connection to the serial input of the L64777 device generally requires synchronizing on the SYNC_BYTE within the

bitstream. If the microprocessor interface selects internal synchronization, the L64777 looks for an 8-bit sync pattern S, repeated in the DIN[0] input data stream with a given period of P bytes. For an MPEG-2 DVB transmission, S = 0x47 and P = 204. The values S and P are programmable in the chip to accommodate all applications based on MPEG and MPEG-derived standards.

Parallel operation requires byte-aligning the SYNC_BYTE to achieve data-dependant synchronization. For serial input, the L64777 searches the SYNC_BYTE in all possible bit positions and automatically detects the byte-alignment.

In the L64777, the sync algorithm is fixed to a procedure with programmable values of S and P. In order to achieve the required functionality at the lowest possible gate count, you can select from three values of track steps, which are the number of flywheel repetitions required to declare the states SYNCOK and loss-of-sync. There are two phases to the sync algorithm procedure: the sync acquisition phase, and the sync tracking phase.

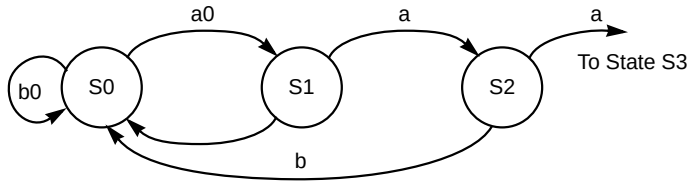
2.4.1 Sync Acquisition Phase

In the sync acquisition phase, the number of sync detections required for sync and loss is programmable from 3 to 5. TS is the designation for the number of track steps. After TS error-free consecutive detections of the sync byte S at the correct locations, the L64777 declares synchronization; if a mismatch occurs, it goes back to the search state.

Validating the detection of the sync word three times ensures a probability of false alarm equal to $P_{fa} = (2^{-8})^3 = 6*10^{-8}$. Validating the detection of the sync word five times insures a probability of false alarm equal to $P_{fa} = (2^{-8})^5 = 9*10^{-13}$.

Figure 2.7 shows the states occurring in the sync acquisition phase.

Figure 2.7 Sync Acquisition Phase



The abbreviations in the illustration indicate the following states:

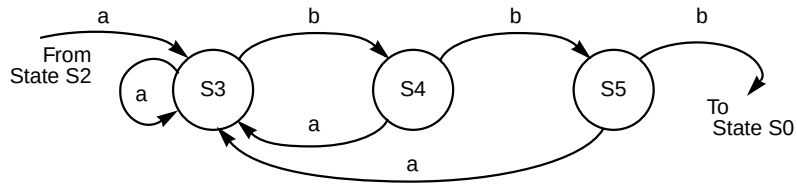
- S0 is the sync pattern research state. When S is detected, transition a0 leads to state S1. If S is not detected, transition b0 maintains state S0.
- S1 is a retest state. Period (P) bytes after S detection in state S0, the detection of S is retested. If S is detected again, transition “a” leads to state S2. If S is not detected, transition “b” leads back to state S0.
- S2 again tests detection of S after period P. If correct detection occurs, transition “a” leads to the sync tracking phase. If not, transition “b” leads back to S0.

2.4.2 Sync Tracking Phase

The sync tracking phase checks the detection of S at the correct location (i.e., every P bytes). TS – 1 mismatches are tolerated, but at the last mismatch the L64777 declares a loss-of-sync and goes back to state S0 to look for new synchronization.

Figure 2.8 shows the states occurring in the sync tracking phase.

Figure 2.8 Sync Tracking Phase



The abbreviations in the illustration indicate the following states:

- S3 is a synchronized state. If no mismatches occur, transition “a” maintains this state. If a wrong word is detected at the location where S is expected, transition “b” leads to state S4.
- S4 tests the detection of S after an interval of P bytes since the last detection test. If S is detected, transition “a” leads back to synchronized state S3. If not, transition “b” leads to S5.

- S5 again test the detection of S after period P. If S is detected, transition “a” leads back to synchronized state S3. If not, transition “b” leads back to S0 to look for another sync location.

To review the transitions in the sync acquisition and sync tracking phases:

- Transition a0 occurs when word S is detected.
- Transition b0 occurs when word S is not detected.
- Transition “a” occurs when word S is detected exactly P bytes after the last detection test.
- Transition “b” occurs when word S has not been detected P bytes after the last detection test. This transition activates a declaration of loss-of-sync.

The L64777 activates output SYNCOK in state S3, S4, or S5. This allows easy measurement of synchronization conditions from outside and monitoring during normal operation. The microprocessor interface also provides SYNCOK information. At this interface, the L64777 can read the actual status and a glitch trap (which detects any sync losses between two sync status reads). SYNCOK can also generate interrupts, if the SYNCOK interrupt is not masked (see Section 4.2.1, “Register 12,” page 4-10).

In order to use a subset of the device with random data (without frame structure), bypass the synchronization mechanism by setting the unconstrained bit in the register map (see Section 4.1.10, “Register 11,” page 4-9).

2.5 FIFO Clock Conversion

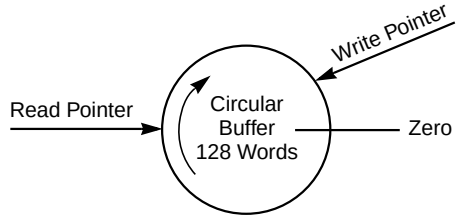
The L64777 uses a dual-ported RAM to implement the circular buffer FIFO function. The circular buffer has a write pointer driven by ICLK and a read pointer driven by the Symbol clock, OCLK/4. The device does not prevent collisions of the pointers; rather, the PLL-VCO follow-up time and proper initial setup of the pointer distance must guarantee this.

For FIFO initialization, the L64777 loads a user-programmable pointer distance of 0 to 127 cycles (the FIFO delay value of Register 2 in Group 2) into the read address pointer (after each microprocessor delay register access) and sets the write address pointer to zero (see Figure 2.9). After this initialization, both pointers run free, and the OCLK to ICLK frequency relationship determines how the read and write pointers advance.

To allow outside watching of the asynchronous pointers, an alarm comparator indicates when both pointers are equal. Because both counters are Gray Code counters (in which changes occur only in one bit) the spikes and glitches of the asynchronous signals are minimized.

When specifying the microprocessor download value for the read pointer initialization, you must use Gray Code. The write pointer also is Gray Code counter-driven; it initializes to zero when the read counter is loaded.

Figure 2.9 FIFO Pointer Concept



Properly programmed delay values in Gray Code guarantee that the read pointer is directly opposite the write pointer most of the time; this increases system immunity against PLL frequency swings, which might occur during the phases of an unstable input signal. Smaller distances also can reduce system delay.

The hexidecimal address sequence of the read (underlined) and write pointers is:

00, 01, 03, 02, 06, 07, 05, 04, 0C, 0D, 0F, 0E, 0A, 0B, 09, 08,

18, 19, 1B, 1A, 1E, 1F, 1D, 1C, 14, 15, 17, 16, 12, 13, 11, 10,

30, 31, 33, 32, 36, 37, 35, 34, 3C, 3D, 3F, 3E, 3A, 3B, 39, 38,

28, 29, 2B, 2A, 2E, 2F, 2D, 2C, 24, 25, 27, 26, 22, 23, 21, 20,

60, 61, 63, 62, 66, 67, 65, 64, 6C, 6D, 6F, 6E, 6A, 6B, 69, 68,

78, 79, 7B, 7A, 7E, 7F, 7D, 7C, 74, 75, 77, 76, 72, 73, 71, 70,

50, 51, 53, 52, 56, 57, 55, 54, 5C, 5D, 5F, 5E, 5A, 5B, 59, 58,

48, 49, 4B, 4A, 4E, 4F, 4D, 4C, 44, 45, 47, 46, 42, 43, 41, 40.

The L64777 download through the microprocessor interface starts with the beginning read pointer value. The write pointer start value is always fixed to zero. Every time the L64777 accesses the FIFO delay value in the microprocessor interface (FDEL, see Section 4.1.3, “Register 2,” page 4-5), the pointers are reset to the these values. If the L64777 is programmed to the FIFO Autoreset mode (see Section 4.1.7, “Register 6,” page 4-7), it forces the pointers to the value in the FDEL register on the read side and to zero on the write side after every FIFO collision.

Attention: The only legal load values for the read pointer are Gray Code numbers with even parity, which means an even number of 1s (underlined in the above table). Therefore, the FIFO delay increment can only be in steps of two. The device achieves maximum delay with a value of 0x41; the optimum (center) distance to overrun and underruns is 0x60.

2.6 Sync/EF Reinsertion Unit

The following subsections describe the Sync/EF modes, error flag insertion, and scrambler.

2.6.1 Sync Insertion Mode

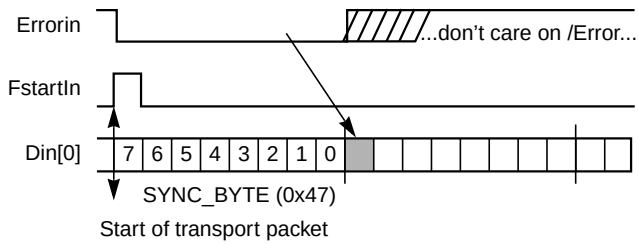
The Sync/EF unit inserts new sync words if that mode is programmed (see Section 4.1.2, “Register 1,” page 4-4). Sync insertion can be useful to work against bit errors in sync bytes, even if sync is already inserted in the stream. If the bitstream contains sync bytes that the device uses for synchronization, the regenerated sync bytes conceal single errors in the synchronization pattern.

In unsynchronized states S0, S1, and S2, the L64777 bypasses data bits without any modification of the sync byte. After it establishes synchronization (in states S3, S4 and S5), the device inserts the regenerated sync pattern based on the programming of Register 1.

2.6.2 Error Flag Insertion

The next processing task is the error flag handling for MPEG-2 transport packets. If ERRORIN indicates a decoder error at the first byte of a frame, the L64777 sets the TRANSPORT_ERROR_INDICATOR bit of the MPEG-2 packet. This is the MSB of the second byte in a packet (see Figure 2.10). If there is no error indication, the L64777 passes the TRANSPORT_ERROR_INDICATOR bit transparently.

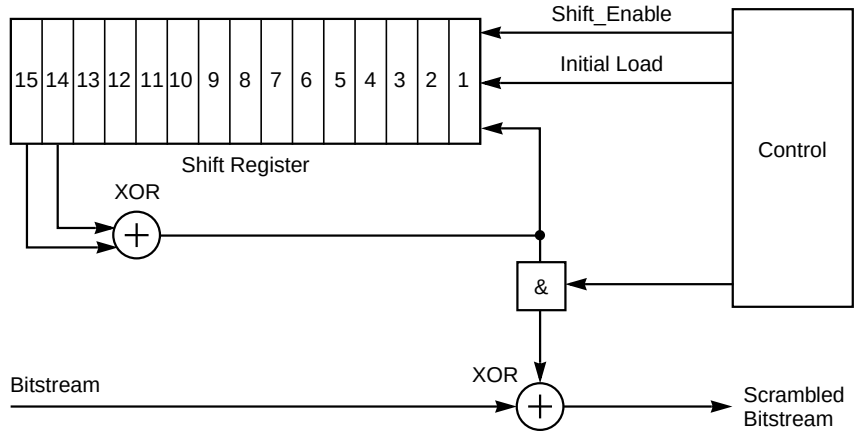
Figure 2.10 Transport Error Flag Insertion



2.6.3 Energy Dispersal (Scrambler) Unit

The function of the Scrambler is specified for the serial domain by the *Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems*. The energy dispersal module (scrambler) operates in Parallel mode based on the algorithm of the serial domain. Figure 2.11 illustrates the basic serial architecture of the Scrambler.

Figure 2.11 Scrambler Basic Serial Architecture



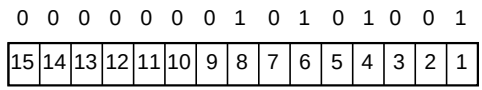
The scrambler block consists of two major modules: one to generate a pseudo-random binary sequence (PRBS) that modifies the incoming data stream, and the other a control module that properly aligns data with the PRBS.

The PRBS the descrambler module produces is characterized by the following generator polynomial:

$$1 + x^{14} + x^{15}$$

For initialization, choose a specific value for the 15-tap shift register (see Figure 2.12).

Figure 2.12 Shift Register Initialization Sequence



The L64777 uses a special sync word (0xB8), generated by inverting every eighth transport sync word (0x47), to align the descrambler with the incoming data stream. The L64777 applies the first bit of the PRBS to the first data bit following the inverted sync byte and freezes the scrambler register contents during gaps for RS check words. During the following noninverted sync words, the descrambler sequence generator is kept in operation but does not modify the data stream. The L64777 resets the descrambler sequence after every inverted sync word. The

SSTARTIN input signal can preset the phase of the inverted SYNC_BYTE and the whole scrambler sequence.

The microprocessor can switch off the scrambler module through Register 3 (see Section 4.1.4, “Register 3,” page 4-5). The selected microprocessor control applies the sequence of Start, Run, and Disable modes, depending on the programmed sync block length values in Register 4 (see page 4-6).

2.7 Reed-Solomon Encoder

Reed-Solomon (RS) error correction codes are systematic and operate on bytes rather than single-bit data streams. The codes are expressed by convention as two numbers, the first indicating the total code word length (N), and the second indicating the number of message bytes (K). The difference between these two numbers (N – K) is the number of check bytes.

DVB uses this generator polynomial for RS codes:

$$\prod_{i=0}^{R-1} (x + \alpha^i)$$

where R = 16 (checkbytes), and α is a root of the binary primitive polynomial:

$$x^8 + x^4 + x^3 + x^2 + 1$$

A data byte (d_7, d_6,...d_1, d_0) is identified with the element $d_7\alpha^7 + d_6\alpha^6 + ... + d_1\alpha + d_0$ in GF (256), the finite field with 256 elements.

The error-correcting power of an RS code is related to the number of redundant check symbols in its code words. In general, an RS code with 2t check symbols per code word can correct up to “t” byte errors per code word. Higher redundancy allows more errors to be corrected.

ECC devices have a specific lexicon associated with their ability to correct transmission messages; the terms used for variables in the Reed-Solomon Core are as follows:

R **Check Bytes**
The encoder generates and appends check bytes to the incoming message according to the Reed-Solomon error-correction encoding. The decoder uses check bytes to locate and correct errors due to transmission.

d **Detection Power**
Detection power has a minimum value of $\left\lfloor \frac{R}{2} \right\rfloor$ and a maximum value of R.

K **Message Length**
The message is comprised of multiple bytes. The size of the message varies depending on the code word length and the check bytes used, where K = N – R.

m **Symbol Size**
The symbol size m is 8 bits fixed.

N **Code Word Length**
This is the sum of the number of message bytes and the number of check bytes (K + R).

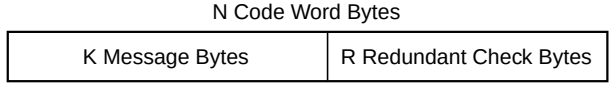
t **Number of Error Corrections**
This variable is the maximum number of error corrections performed by the decoder. Its maximum value is:

$$\left\lfloor \frac{R}{2} \right\rfloor$$

2.7.1 Forward Error Correction (FEC)

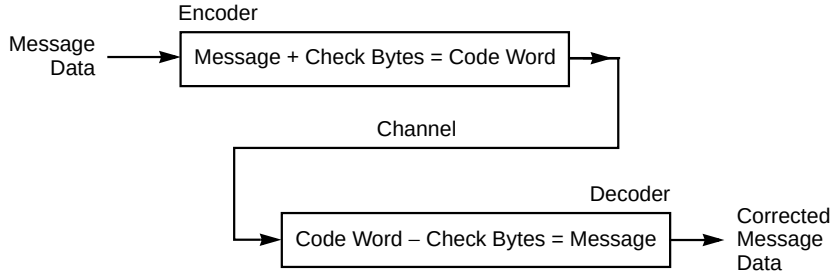
FEC requires an encoder that appends redundant check information to the message before transmission. The bytes with an indeterminate number of bits are referred to as symbols. The message symbols and following redundant check symbols make up code words. The check symbols are redundant because they are derived from the message and are appended to the message. Check symbols are also referred to as “redundant check bytes,” and sometimes as “correction bytes.” Figure 2.13 illustrates a code word.

Figure 2.13 Code Word Structure



A code word is a block of N bytes that includes K message symbols and N – K check bytes (R). The check bytes, or symbols, are some fraction of the message symbols. A large number of check symbols allows the decoder to correct a large number of transmission errors. The redundant check symbols in a message allow a decoder at the receiving end of a transmission line to detect transmission errors and reconstruct the original message content. Figure 2.14 shows a block diagram of the basic encoder and decoder functions in a transmission system.

Figure 2.14 Forward Error Correction Data Path



After generating a code word, the encoder transmits it to a decoder. The decoder compares the bitstream in the message data to the encoding in the check bytes to detect transmission errors. The L64777 can reconstruct the original message precisely from the check symbols, as long as the code word has no more than $\lfloor (R)/2 \rfloor$ byte errors, where R = the number of redundant check bytes.

2.7.2 Error Handling and Correction

A bit error occurs when a transmitted 0 is received as a 1, or vice versa. A byte error occurs when one or more bits in the byte have errors. For example, a byte with only one bit error is counted as one byte error, and a byte with m bit errors (all bits are inverted) is also counted as 1 byte error. As long as a code word has no more than t = $\lfloor (R)/2 \rfloor$ byte errors, the RS decoder corrects all errors.

To achieve RS encoding at the lowest possible gate count and power consumption, the check byte parameters of the RS encoder in the L64777 are fixed to R = 16, according to the DVB standard. When the RS encoder is switched off, data feeds through without check-word insertion at an internal delay of two clock cycles.

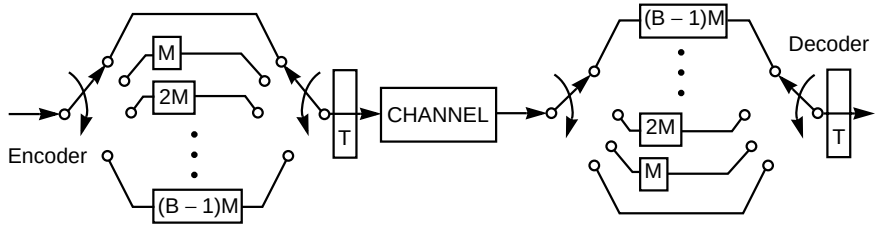
2.8 Convolutional Interleaver

Figure 2.15 is a block diagram of a convolutional interleaver system, which rearranges the ordering of a sequence of symbols in a deterministic manner. A (B, N) periodic interleaver has the following characteristics:

- The minimum separation at the interleaver output is B symbols for any two symbols that are separated by less than N symbols at the interleaver input.
- Any burst of b < B errors inserted by the channel results in single errors at the deinterleaver output.

The scheme is also referred to as a convolutional interleaver/ deinterleaver (based on the Forney approach).

Figure 2.15 Interleaver Block Diagram



The L64777 interleaver performs periodic interleaving with two fixed parameters: B, the desired interleaving depth, and M, defined as:

$$M = \left\lceil \frac{N}{B} \right\rceil$$

The values of the interleaver in the L64777 are: N = 204, B = 12, and M = 17. You can switch off the interleaver. It is fully transparent with an intrinsic delay of three clock cycles.

The main modules are a set of configured RAM-based delay lines to implement the proper delay for individual data bytes, and a controller to handle and generate the strobes needed by subsequent modules in the data path.

The interleaver must recover the block boundaries, and the SSTARTIN pin indicates them by internal strobes; it also resets the interleaver sequence. You can program the interleaver so that all data fed into the interleaver RAM before the very first arrival of a SSTARTIN negative slope is set to zero. This eases operation verification and debugging during development when the interleaver RAM is completely initialized with zero values. You must apply a fresh reset to feed zeros after an active SSTARTIN slope.

The interleaver and the deinterleaver, in sequence, output the original byte stream after a delay of

$$Delay = (B-1) \times B \times M$$

In the L64777, the Delay = (11 x 12 x 17) = 2244 clock cycles. Thus, the delay from the time of the first input byte to the first valid output byte in the maximum delay path of the interleaver is half of this value, which is 1122 valid clock cycles.

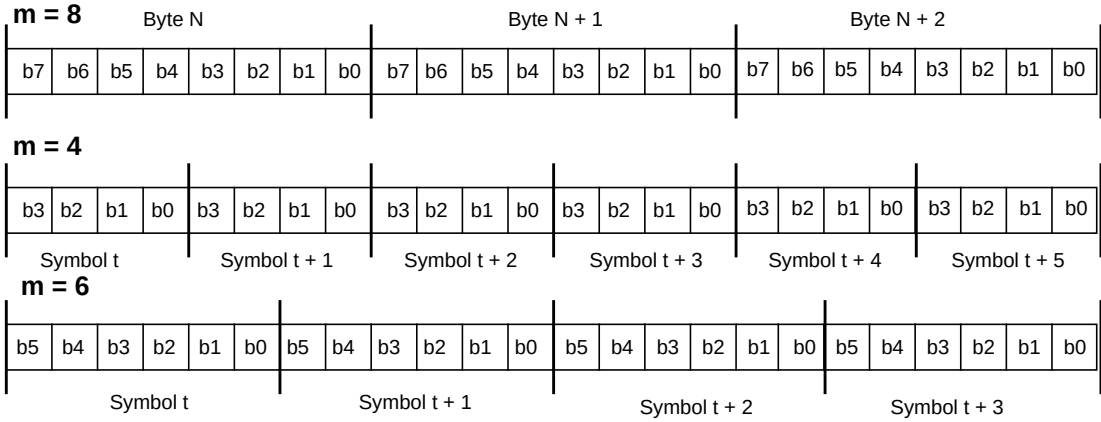
If the QAM is not in 256 mode, the interleaver inserts invalid cycles in an eight-byte sequence, which proportionally increases the delay time. The zero delay path in the interleaver delivers data with a propagation delay of three clock cycles. This is equal to the delay of the interleaver when it is off.

2.9 Bytes to M-tuples Converter

This unit cuts down bytes to slices of m = 1, 2, 3, 4, 5, 6, 7, and 8 bits. The programming parameter, mSize (see Section 4.1.2, “Register 1,” page 4-4), must be set to m – 1. The order is the MSB of the oldest byte first. See the *Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems* for a detailed specification. When cutting six-bit symbols, it cuts three bytes into four symbols. The case of four-bit symbols is trivial (eight bits are split into two sets of four bits each).

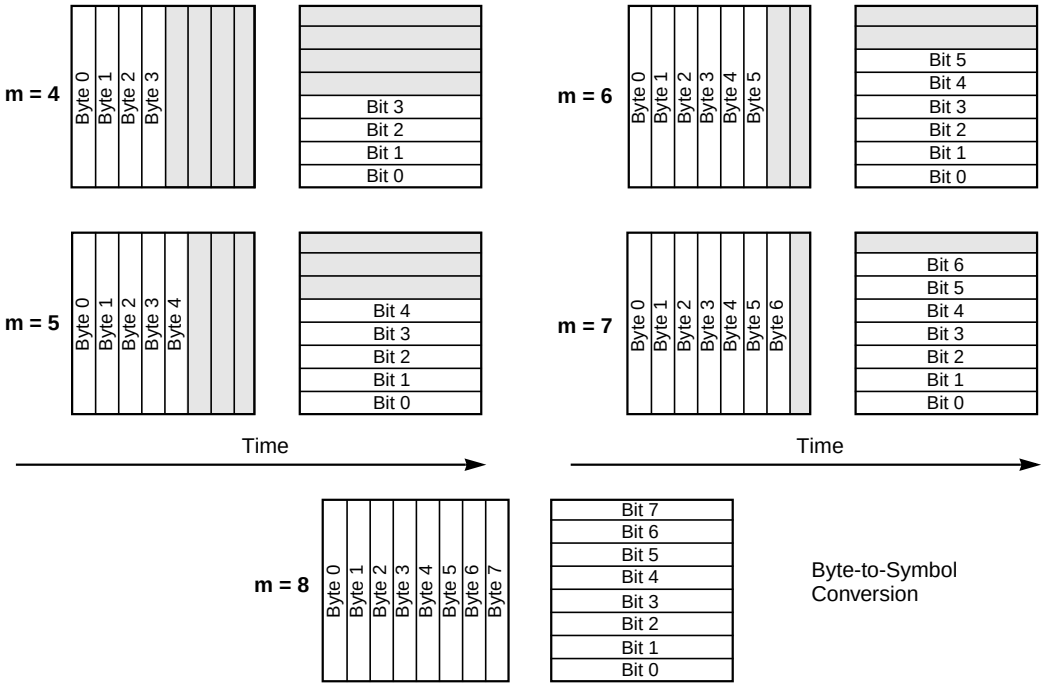
Figure 2.16 outlines the basic principle for symbol cutting out of bytes. Modes for m = 5 and m = 7 are similar.

Figure 2.16 Symbol Cutting From Bytes



The general control unit feeds packets of eight bytes and a valid indicator to the convertor. Thus, the conversion is as shown in Figure 2.17.

Figure 2.17 Byte to Symbol Conversion

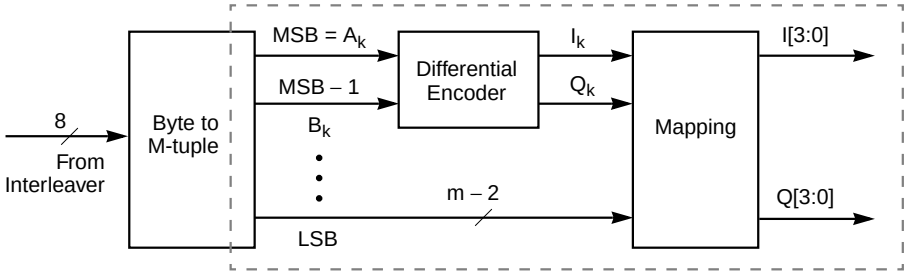


2.10 Differential Encoder and QAM Mapping

This block performs differential encoding and mapping for 16 and 64 QAM, as specified in the *Digital Broadcasting Systems for Television Sound and Data Services: Framing Structure, Channel Coding and Modulation Cable Systems*, the baseline document, and its extensions. The QAM 256 mapping is taken from the DVB document 1190.

The encoder performs differential encoding on the two most significant bits of each symbol, as shown in the block diagram in Figure 2.18 and specified in equations 2.1 and 2.2.

Figure 2.18 Differential Encoder and QAM Mapping



To clarify the underlying concepts in Figure 2.18, here are two examples:

1. If m = 4, A_k is bit 3, B_k is bit 2, and the LSB = (m – 2) bits = bits [1:0].
2. If m = 6, A_k is bit 5, B_k is bit 4, and the LSB = (m – 2) bits = bits [3:0].

Equation 2.1 $$I_k = (\neg(A_k \oplus B_k))(A_k \oplus I_{k-1}) + (A_k \oplus B_k)(A_k \oplus Q_{k-1})$$

Equation 2.2 $$Q_k = (\neg(A_k \oplus B_k))(B_k \oplus Q_{k-1}) + (A_k \oplus B_k)(B_k \oplus I_{k-1})$$

Mapping performs a table look-up for the concatenation of the (m – 2) least significant bits of each symbol with the differentially generated bits I_k and Q_k.

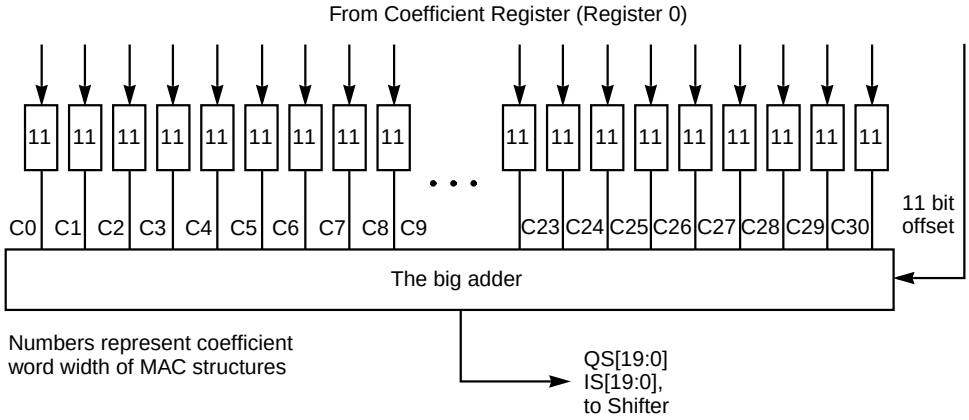
In 64 QAM mode, the mapping block of the differential encoder maps the 6-tuples to two 3-bit values for I and Q output. In 16 QAM mode, it maps the 4-tuples to two 2-bit values. For lower QAM modes, it aligns the I and Q output values to the MSB and stuffs the least-significant bit (LSB) with ones.

Differential encoding has an infinite error propagation. You can switch it off independently from the mapping function (see bit 3 of Register 6, on page 4-8).

2.11 Square Root Nyquist Filter

This pulse-shaper module implements a programmable square-root raised cosine filtering function with a default 15% roll-off factor. The precision of the internal Nyquist filter computations, and the width of the output data bus, are sufficient for QAM modulations up to 256. The filter operates at four times the oversampling rate. Figure 2.19 illustrates the structure of the pulse shaper.

Figure 2.19 Pulse Shaper Structure



Note that the 20 bits per channel is a result of the length of each coefficient register (2^{11}) plus the length of INQ (2^4) plus the number of stages ($30 = 2^5$). The total number of coefficients is 124 (there is one coefficient set for each of the four phases multiplied by the MAC structure, which contains 31 multipliers).

Each of the two I and Q branches has one filter, realized as polyphase structures. Each filter consists of four filter branches, which compute 1-phase filter results at the symbol rate. Thus, the L64777 Nyquist filter module generates the desired pulse shape by combining the outputs of four identical filter branches for I and Q.

For an oversampling factor of four, the filter executes the above sequence at four times the symbol rate (60 MHz in PLL mode).

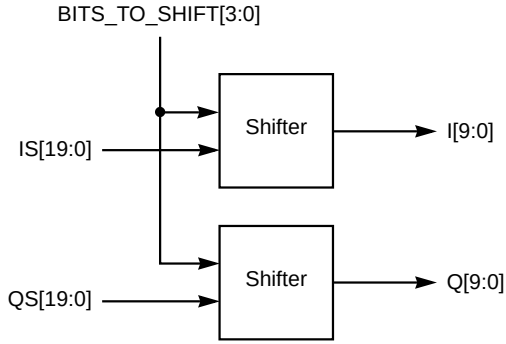
Each multiply accumulator (MAC)-structure contains 31 multipliers whose outputs add up to the desired result. The pulse shaper module connects one input of each multiplier to a delayed version of the filter input data; the other multiplier input is connected to one of four coefficient registers through a multiplexer. The pulse shaper clocks the delay line for IData and QData with the symbol clock rate. The coefficient and multiplier width are as described below.

The pulse shaper interprets all data as two's complement. Each MAC-structure contains an additional input to the adder array to allow for the addition of an 11-bit value to compensate for an offset. The pulse shaper treats these offset coefficients like regular coefficients, except that it adds them directly to the MAC outputs. There is one offset coefficient for each phase.

The shifter block adjusts the internally generated filter result to accommodate the limited range of the internal D/A-converter. The standard mapping after reset is a five-bit shift to the right, which means IS[5] to I[0], IS[6] to I[1] and so on. The shifter treats the Q-branch accordingly.

By applying a value different from zero to the BITS_TO_SHIFT[3:0] input of the shifter (using Register 0), the shifter connects IS to I, and QS to Q, so that the lowest bits of IS and QS are truncated, while the more significant bits are hooked to the I and Q outputs. The BITS_TO_SHIFT input can assume a maximum value of 15, thus mapping IS[15] to I[0], IS[16] to I[1], and so on. The filter output value is not limited to maximum positive or negative values before shifting, so it is the user's responsibility to download coefficients and an appropriate shifting value to avoid output overflow and underflow. Figure 2.20 illustrates the output scaling by an arithmetic shift to the right.

Figure 2.20 Output Scaling by Arithmetic Shift Right



The shifter treats the value of BITS_TO_SHIFT[3:0] like a coefficient, and the value is available separately for every phase. This means that the hardware of the filter is multiplexed in such a way that there are the same coefficient registers for the I and Q channel, and each of the two MACs switches between four banks of coefficients cyclically, driven by OCLK. Setting all coefficients to zero (except the center coefficient, which is 1), offers a bypass mode for the filter.

The interpolator following the Nyquist filter receives 12-bit resolution in PLL Mode 2. Program the shifter accordingly to make the increase precision available to the interpolator; for example: to 3 rather than 5.

2.11.1 Filter Setup Procedure

The filter module is loaded with 31 filter coefficients sequentially, with four blocks of 49 bytes in the PHASE_0, PHASE_1, PHASE_2, and PHASE_3 registers (Register 0 of Group 2). The same data controls the I and Q data path in parallel. Also, the filter is loaded with four BITS_TO_SHIFT and an 11-bit offset value for each phase. It is specified within 49 bytes in each phase, as shown in Table 2.1. The complete setup sequence consists of 4 * 49 = 196 bytes for all four phases. The filter organizes the coefficient registers for each register bank as described below, using the coefficient enumeration shown in the block diagram. Note that no meaningful operation can be performed while the filter is being programmed, since the old coefficients are being shifted out while the new ones are programmed in.

As shown in Figure 2.18, the filter shifts four coefficient register banks (Register 0) sequentially, starting with register 48 and proceeding down to 0. In this configuration, it shifts bank 3 first, then 49 bytes of bank 2, bank 1, and, finally, bank 0. Table 2.1 shows the exact allocation of bits within each bank.

2.11.2 Example

Assuming all filter configuration bits are located in a host microprocessor ROM array of bytes addressed with [0 to 195], the filter coefficients place phase 0 coefficients in registers [0 to 48], phase 1 in [49 to 97], phase 2 in [98 to 146], and phase 3 in [147 to 195]. To download this array, the microprocessor must write bytes [195 down to 0] sequentially into address 0 register, highest array address first.

After 196 write cycles, the four coefficient register banks are completely configured. During configuration, the filter is not operational to save gates by avoiding double buffering of the coefficient registers. For different QAM modes, the filter must load the appropriate sets of coefficients and shifter values.

The default set of coefficients is a square-root raised cosine filter. The filter sets the coefficients in Table 2.2 after reset, and it can overwrite them with external programming through the I^2C-compatible interface.

Table 2.1 Allocation of Coefficient-Bits for Phase 0

B7	B6	B5	B4	B3	B2	B1	B0	Reg #
c0.7	c0.6	c0.5	c0.4	c0.3	c0.2	c0.1	c0.0	0
c1.7	c1.6	c1.5	c1.4	c1.3	c1.2	c1.1	c1.0	1
–	c0.10	c0.9	c0.8	–	c1.10	c1.9	c1.8	2
c2.7	c2.6	c2.5	c2.4	c2.3	c2.2	c2.1	c2.0	3
c3.7	c3.6	c3.5	c3.4	c3.3	c3.2	c3.1	c3.0	4
–	c2.10	c2.9	c2.8	–	c3.10	c3.9	c3.8	5
c4.7	c4.6	c4.5	c4.4	c4.3	c4.2	c4.1	c4.0	6
c5.7	c5.6	c5.5	c5.4	c5.3	c5.2	c5.1	c5.0	7
–	c4.10	c4.9	c4.8	–	c5.10	c5.9	c5.8	8

Table 2.1 Allocation of Coefficient-Bits for Phase 0 (Cont.)

B7	B6	B5	B4	B3	B2	B1	B0	Reg #
c6.7	c6.6	c6.5	c6.4	c6.3	c6.2	c6.1	c6.0	9
c7.7	c7.6	c7.5	c7.4	c7.3	c7.2	c7.1	c7.0	10
–	c6.10	c6.9	c6.8	–	c7.10	c7.9	c7.8	11
c8.7	c8.6	c8.5	c8.4	c8.3	c8.2	c8.1	c8.0	12
c9.7	c9.6	c9.5	c9.4	c9.3	c9.2	c9.1	c9.0	13
–	c8.10	c8.9	c8.8	–	c9.10	c9.9	c9.8	14
c10.7	c10.6	c10.5	c10.4	c10.3	c10.2	c10.1	c10.0	15
c11.7	c11.6	c11.5	c11.4	c11.3	c11.2	c11.1	c11.0	16
–	c10.10	c10.9	c10.8	–	c11.10	c11.9	c11.8	17
c12.7	c12.6	c12.5	c12.4	c12.3	c12.2	c12.1	c12.0	18
c13.7	c13.6	c13.5	c13.4	c13.3	c13.2	c13.1	c13.0	19
–	c12.10	c12.9	c12.8	–	c13.10	c13.9	c13.8	20
c14.7	c14.6	c14.5	c14.4	c14.3	c14.2	c14.1	c14.0	21
c15.7	c15.6	c15.5	c15.4	c15.3	c15.2	c15.1	c15.0	22
–	c14.10	c14.9	c14.8	–	c15.10	c15.9	c15.8	23
c16.7	c16.6	c16.5	c16.4	c16.3	c16.2	c16.1	c16.0	24
c17.7	c17.6	c17.5	c17.4	c17.3	c17.2	c17.1	c17.0	25
–	c16.10	c16.9	c16.8	–	c17.10	c17.9	c17.8	26
c18.7	c18.6	c18.5	c18.4	c18.3	c18.2	c18.1	c18.0	27
c19.7	c19.6	c19.5	c19.4	c19.3	c19.2	c19.1	c19.0	28
–	c18.10	c18.9	c18.8	–	c19.10	c19.9	c19.8	29
c20.7	c20.6	c20.5	c20.4	c20.3	c20.2	c20.1	c20.0	30
c21.7	c21.6	c21.5	c21.4	c21.3	c21.2	c21.1	c21.0	31
–	c20.10	c20.9	c20.8	–	c21.10	c21.9	c21.8	32
c22.7	c22.6	c22.5	c22.4	c22.3	c22.2	c22.1	c22.0	33

Table 2.1 Allocation of Coefficient-Bits for Phase 0 (Cont.)

B7	B6	B5	B4	B3	B2	B1	B0	Reg #
c23.7	c23.6	c23.5	c23.4	c23.3	c23.2	c23.1	c23.0	34
–	c22.10	c22.9	c22.8	–	c23.10	c23.9	c23.8	35
c24.7	c24.6	c24.5	c24.4	c24.3	c24.2	c24.1	c24.0	36
c25.7	c25.6	c25.5	c25.4	c25.3	c25.2	c251	c25.0	37
–	c24.10	c24.9	c24.8	–	c25.10	c25.9	c25.8	38
c26.7	c26.6	c26.5	c26.4	c26.3	c26.2	c26.1	c26.0	39
c27.7	c27.6	c27.5	c27.4	c27.3	c27.2	c271	c27.0	40
–	c26.10	c26.9	c26.8	–	c27.10	c27.9	c27.8	41
c28.7	c28.6	c28.5	c28.4	c28.3	c28.2	c28.1	c28.0	42
c29.7	c29.6	c29.5	c29.4	c29.3	c29.2	c29.1	c29.0	43
–	c28.10	c28.9	c28.8	–	c29.10	c29.9	c29.8	44
c30.7	c30.6	c30.5	c30.4	c30.3	c30.2	c30.1	c30.0	45
offset.7	offset.6	offset.5	offset.4	offset.3	offset.2	offset.1	offset.0	46
–	c30.10	c30.9	c30.8	–	offset.10	offset.9	offset.8	47
–	–	–	–	shift.3	shift.2	shift.1	shift.0	48

Table 2.2 Default Nyquist Filter Coefficients

Tap	Phase0	Phase1	Phase2	Phase3
#0	0	0	0	0
#1	0	–1	–1	0
#2	0	0	0	0
#3	0	1	1	1
#4	–1	–3	–3	–1
#5	3	5	5	1
#6	–4	–9	–7	–1

Table 2.2 Default Nyquist Filter Coefficients (Cont.)

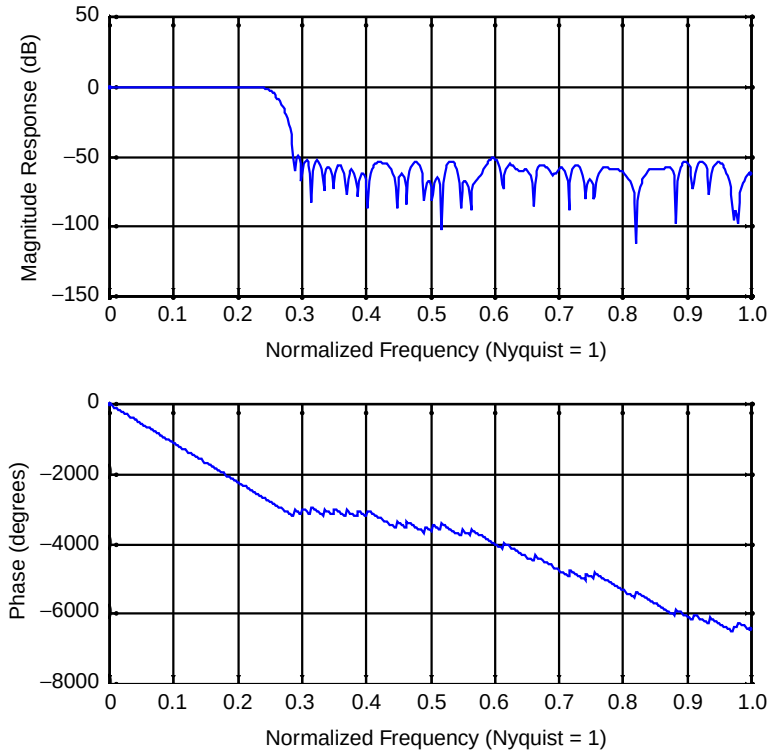
Tap	Phase0	Phase1	Phase2	Phase3
#7	8	13	10	–1
#8	–14	–19	–13	3
#9	20	28	16	–8
#10	–31	–38	–20	15
#11	46	51	23	–27
#12	–69	–71	–26	48
#13	107	105	28	–95
#14	–191	–184	–29	257
#15	593	862	965	862
#16	593	257	–29	–184
#17	–191	–95	28	105
#18	107	48	–26	–71
#19	–69	–27	23	51
#20	46	15	–20	–38
#21	–31	–8	16	28
#22	20	3	–13	–19
#23	–14	–1	10	13
#24	8	–1	–7	–9
#25	–4	1	5	5
#26	3	–1	–3	–3
#27	–1	1	1	1
#28	0	0	0	0
#29	0	0	–1	–1
#30	0	0	0	0

The default offset value for all four phases is 0. To shift the shifter by default, set it to 5 bits.

2.11.3 Default Filter Characteristics

Figure 2.20 shows the characteristics of the L64777 default filter.

Figure 2.21 Square-Root Raised Cosine Filter



2.12 Global Control and PLL Module

The L64777 interface supports serial and parallel input modes at the input interface. The global control generates the clocking for the input and output interfaces; it also controls the data path. It contains all the necessary logic to chain the processing units together.

The global control manages the output data stream so that it is continuous (no gaps between the symbols), assuming that the incoming data rate is constant (on average). To achieve this, a PLL must derive the output clock OCLK from the input transport stream rate.

The PLL module consists of two independent clock dividers for ICLK and OCLK. The dividers are 15-bit binary counters that have a count sequence length that is programmable through Registers 7 through 10.

The default values written by the external microprocessor are: OCLK divider = 32, ICLK divider = 6 for 64 QAM.

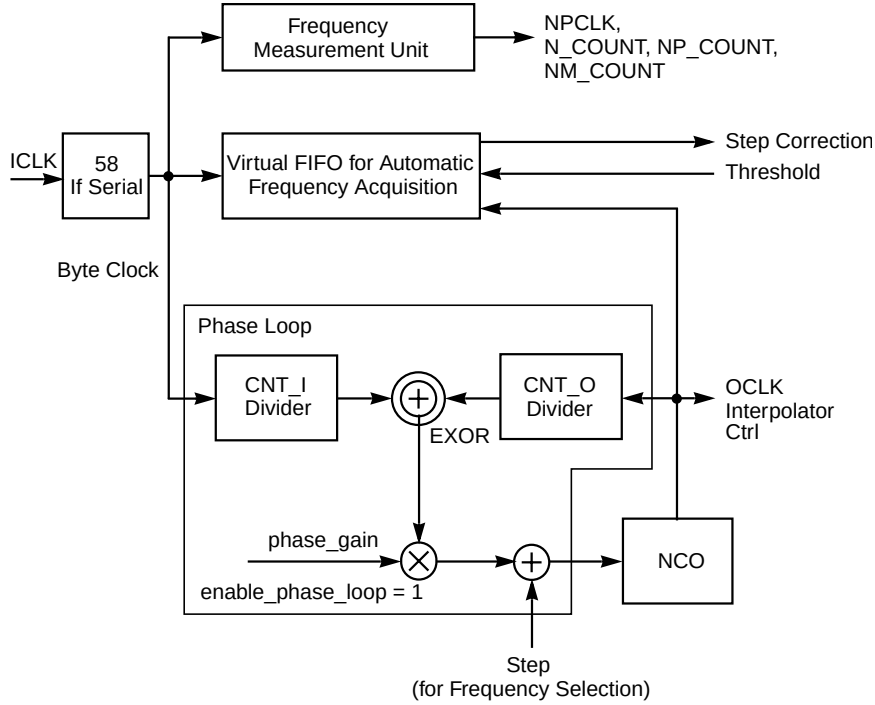
2.12.1 Numerically Controlled Oscillator (NCO)

In PLL Mode 2, an NCO generates the internal clocking (OCLK, SCLK) and the control information for the interpolator. The NCO is locked to ICLK clock and operates with the processing clock PCLK provided from L64724. PCLK must be at least twice as fast as the necessary OCLK.

To lock the loop with low jitter, program the NCO with a frequency close to the ideal value obtained from the formulae given for the other PLL modes. A phase loop in a second step does the fine regulation (see Figure 2.22).

To find the required initial frequency, the device supports two modes: a frequency measurement unit, and an automated frequency acquisition. These are described in the following sections.

Figure 2.22 NCO Loop Diagram



2.12.2 Acquisition Phase Using the Frequency Measurement Unit

During the acquisition phase, the NCO bases the measurement on the assumption that the byte clock on the ICLK input has a duration of either of n – 1, n, or n + 1 PCLK cycles and that the input stays within these bounds for the duration of the measurement. You can program the duration in multiples of 256-byte clock cycles in the REF_DUR register (see Section 4.2.7, “Registers 21 and 22,” page 4-14). The NCO control register (see Section 4.2.3, “Register 14,” page 4-12) can control the start of the measurement, and the Measurement Done bit in register 13 indicates successful completion. If bit 2 of Register 14 enables an interrupt, the measurement generates it.

After completion of the measurement, the host reads the number of byte clock cycles found with the appropriate length of n, n + 1 and n – 1 (from NM_COUNT, N_COUNT, NP_COUNT—see Sections 4.2.10 through 4.2.12), as well as the value of n (from N_PCLK—see Section 4.2.9).

The host computes the following formulae to get the initial step for phase 2, where ñ indicates the average n value.

Equation 2.3 $$\tilde{n} = \frac{(C1(n-1) + C2(n) + C3(n+1))}{(C1 + C2 + C3)}$$

and from this:

Equation 2.4 $$\text{initial step} = \frac{2^{24}}{\tilde{n}} \frac{32}{ld(QAMmode)} \frac{\text{Sync length}}{\text{valid bytes}}$$

In the above formulae:

- C1 is the reading from NM_COUNT register.
- C2 is the reading from N_COUNT register.
- C3 is the reading from NP_COUNT register.
- n is the reading from N_PCLK register.
- Sync length is the number of ICLK cycles between sync bytes (for example, 204).
- Valid bytes are the number of valid bytes during the sync interval (for example, 188).
- ld(QAMmode) is the number of bits per QAM symbol.

If the RS encoder is enabled in DVB mode and the SPI interface of L64724 is programmed to Mode 2, the factor of sync length by valid bytes becomes one.

In order to get an accurate initial step, the measurement must run for a long duration. A recommended duration is 250 ms.

In general the OCLK frequency is calculated as $f_{OCLK} = f_{PCLK} \cdot \frac{step}{2^{24}}$.

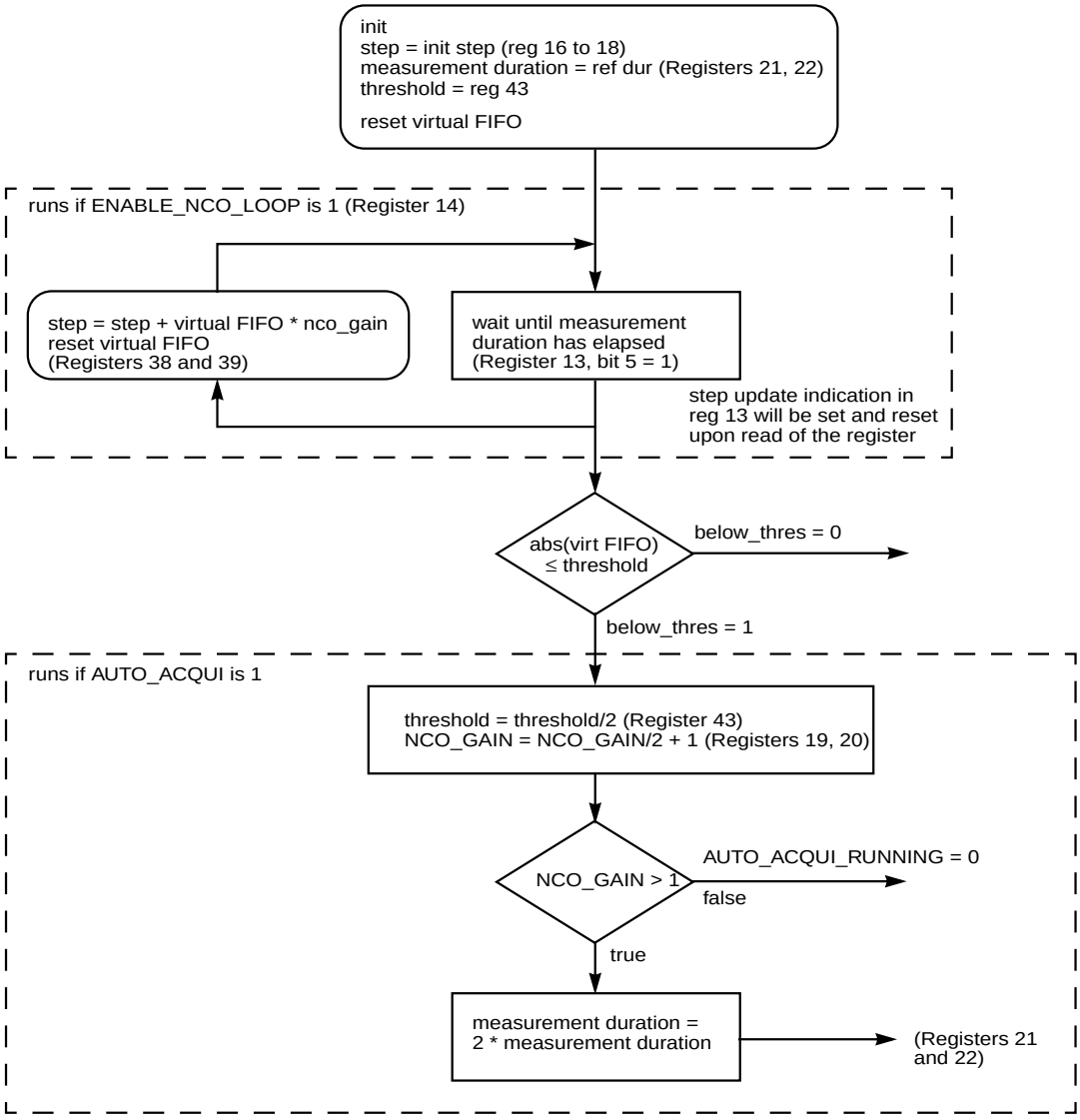
Above, $0 < step < 2^{23} - 1$.

Start measurement by toggling the “start measurement” bit (bit 6) in the NCO control register 14. If the NCO control register is enabled for interrupt (through bit 2 of Register 14), an interrupt indicates completion.

2.12.3 Autoacquisition Mode

To ease the usage of phase 1, the NCO can use an automatic frequency acquisition. Enable regulation of the NCO_LOOP_ENABLE (bit 5) and set the AUTO_ACQUI bit (bit 3) in the NCO control register. Figure 2.23 outlines the parameter usage during automatic frequency acquisition.

Figure 2.23 Frequency Acquisition Loop Overview



Note that the virtual FIFO, which indicates the FIFO under- or over-run, is an internal location.

If the NCO_GAIN has reached the smallest possible value of 1, the AUTO_ACQUISITION terminates. The AUTO_ACQUI_RUNNING bit (Register 13, bit 3) sets to zero, indicating termination. If enabled, the NCO can issue an interrupt on this condition.

This procedure updates the NCO step until the contents of the virtual FIFO is zero during the measurement duration.

If ENABLE_NCO_LOOP and AUTO_ACQUI are not set, it is also possible to set all parameters of the NCO loop through the microprocessor interface and to run a frequency acquisition fully controlled by the microprocessor. For monitoring purposes, it is possible to read the current step and NCO_GAIN using the microprocessor interface.

2.12.4 Regulation Phase

When the ENABLE_PHASE_LOOP bit is set in the NCO control register (Register 14, bit 1), the loop starts running a phase compare between the divided reference and the divided feedback clock. The NCO must set counters CNT_I and CNT_O according to the rules applied for the other PLL modes in Registers 7 through 10. The phase loop has a relatively small gain, which can be adjusted in address 42. The NCO achieves a phase lock only if the initial frequency is already close to the desired range.

2.13 Interpolator

In PLL Mode 2, the interpolator retimes the output samples that the Nyquist filter calculated. The interpolator is clocked with PCLK and generates the output samples in the PCLK sampling grid. The interpolator takes the required retiming information from the NCO.

PCLK is at least twice the frequency of the original OCLK obtained by the formula for PLL Mode 1. The square-root raised cosine filter also compensates for the sin(x)/x frequency characteristic of the digital-to-analog converter with the faster sampling grid.

Another consideration is that the interpolator receives a 12-bit input from the Nyquist filter. Set the shifter in the Nyquist filter accordingly (for example: 2). For PLL Mode 2, the shifter value (which is defined in the filter coefficients in Register 0 of Group 2) is 3; for Mode 1, the shifter value is 5.

2.14 Serial Microprocessor Interface

The external microprocessor controls the QAM modes of operation, 16 to 256 QAM. It also controls the mode of input synchronization, that is, whether to lock synchronization to sync bytes or input pulses. The microprocessor interface downloads the filter coefficients and the delay value for proper FIFO initialization.

The microprocessor interface uses an I^2C-compatible serial control protocol. The signal behavior is described in Appendix A. The interface is slave-only and can not be a master to the serial bus. The base address of the component is composed of a fixed five-bit address and two selectable bits, which are fed through SB_BASE[1:0] (see Figure 2.24). Application of these bits must be on a static basis to ensure proper operation.

Figure 2.24 Serial Bus Base Address

Bit 6, MSB	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0, LSB
1	1	0	1	0	x	x

The L64777 output pins and microprocessor interface provide error indications (for example, the FIFO alarm signal).

The following interface signals are used:

SCL Serial control line

SDA Serial data access

INT_n Interrupt, open drain output

The same type of two-wire serial interface is available on the LSI Logic L64724.

Attention: The internal microprocessor registers are not double-buffered, and they influence the processing modes of the L64777 asynchronously during operation. Thus, all mode changes place the chip in an undefined state until an SSTARTIN pulse synchronously resets the sequences of the data path. When a FIRSTOUT pulse grants the sequence reset at the output, the chip becomes fully operational again. The normal chip initialization procedure is as follows:

- Reset after power-up.
- Initialize ALL microprocessor registers.
- Apply a negative slope of SSTARTIN to reset all sequences at the beginning of the next sync block.
- Apply a negative slope of SSTARTIN after all mode changes from the microprocessor interface and wait for FIRSTOUT.

Also, the serial interface requires a clock for internal operation, either through the OCLK input or from the internal VCO to program the device. Furthermore, there is a lower limit for this clock: its frequency must be at least eight times that of SCL.

2.15 Test Unit

The L64777 supports:

- Full scan test
- BIST for the two RAMs
- JTAG boundary scan
- Digital-to-analog conversion test
- PLL tests

Select the L64777 test modes through the FTMODE pins. The default values for normal operation are:

FTMODE = 000, SCAN_ENABLE = 0, TNn = 1.

If TNn is cleared, all outputs are high-impedance.

To guarantee the proper operation of the L64777 in the printed circuit board environment, an additional IEEE 1149.1 JTAG module is included in the device, which operates on the following pins:

- TRSTn = 0
- TCK = 0
- TMS = 0
- TDI = 0
- TDO (output)

Special test modes are applicable for further functional testing, and the test of the digital-to-analog converters.

Chapter 3
Interfaces

The following chapter describes the interfaces of the chip and the interface operation modes. It consists of the following sections:

3.1 Transport Interface

The task of the transport interface is to read the data stream from the transport source, to identify the position of the synchronization bytes, and to strip off invalid data. The transport interface can operate in either parallel or serial mode.

3.1.1 Synchronization

The L64777 can synchronize the transport interface in two ways. In both modes, it works synchronously with ICLK and reads all signals, including input data, on the raising edge of ICLK.

- In **external synchronization** mode, the transport interface specifies the position of the external sync byte by asserting FSTARTIN to HIGH during the synch byte input. In serial mode, the interface must assert the signal HIGH during the first bit (MSB) of the input stream.
- In **internal synchronization** mode, the L64777 does not require a block start indication and finds the position of the programmed sync byte automatically.

3.1.2 Synchronization Methods

The transport interface also can apply the signal DVALIDIN, indicating valid input data, to allow gaps between input bytes. To avoid cyclic buffer overrun or underrun, the average data input rate, measured over the programmed block length, must not differ from the nominal payload rate of the generated QAM signal. The circular buffer inside the L64777 allows a maximum 64-byte compensation of the input stream.

Synchronizing the QAM modulator with an input pulse at SSTARTIN sets the byte and block boundaries with this external pulse. The transport interface can reinsert the programmed sync byte at the location defined by the external pulse.

In both the internal and external modes, the transport interface can program the block length and the value of the sync byte. The block length must be less than 256 bytes.

After the L64777 achieves synchronization, it inserts the sync byte into the modulated stream according to the programmed sync byte. This has the advantage of eliminating any error in the input sync byte as long as the modulator remains synchronized.

3.1.3 Transport Error Indicator Handling

The transport interface can either pass on a transport error indicator (TEI) unchanged from the input transport stream, or it can force the TEI to indicate an error with the ERRORIN signal. The L64777 observes the forced signal during the sync byte input and ignores it for the rest of the input packet.

3.2 Serial Control Interface

The L64777 uses a serial control interface to control and setup the programmable parameters of the chip. This interface is a slave-type only, connected to the same serial bus as the LSI Logic L64724.

The chip has five hardwired MSBs and takes two LSBs directly from the input pins SB_BASE[1:0].

Bit 6, MSB	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0, LSB
1	1	0	1	0	SB_BASE.1	SB_BASE.0

The addressing scheme in the L64777 complies with that of the LSI Logic L64724, but, due to its small 7-bit internal address space, the L64777 supports only group 0 and group 2. The bit location [2:0] within the first data byte transmitted to the device specifies the group.

Group 0 is the address pointer register (APR); the Serial Control Interface loads the following data byte to APR0. Reading or writing from Group 2 causes a data transfer with the device address specified by APR0:

- If APR0 is set to zero, the Serial Control Interface expects a write access with 196 data bytes to load the filter coefficients; it does not apply an autoincrement to APR0.
- If APR0 is not at zero, the Serial Control Interface expects only a single data byte and applies an autoincrement to the APR0.

The L64777 ignores Group 1 and Groups 3 to 7. It does not apply any reading or writing from them.

The detailed timing of the serial bus is given in Appendix A. The serial bus is designed to run at a maximum 400 kHz clock rate. The serial control interface can transfer reads and writes in single-byte or burst mode. It must do read access to the status registers 12 and 13 as a single-byte read.

3.3 Analog Output Interface

The L64777 puts out the I and Q component of its signal on two separate analog output interfaces (see Figure 3.1). The output interface contains two internal 10-bit digital-to-analog converters.

Figure 3.1 Analog I/Q Output Interface Diagram

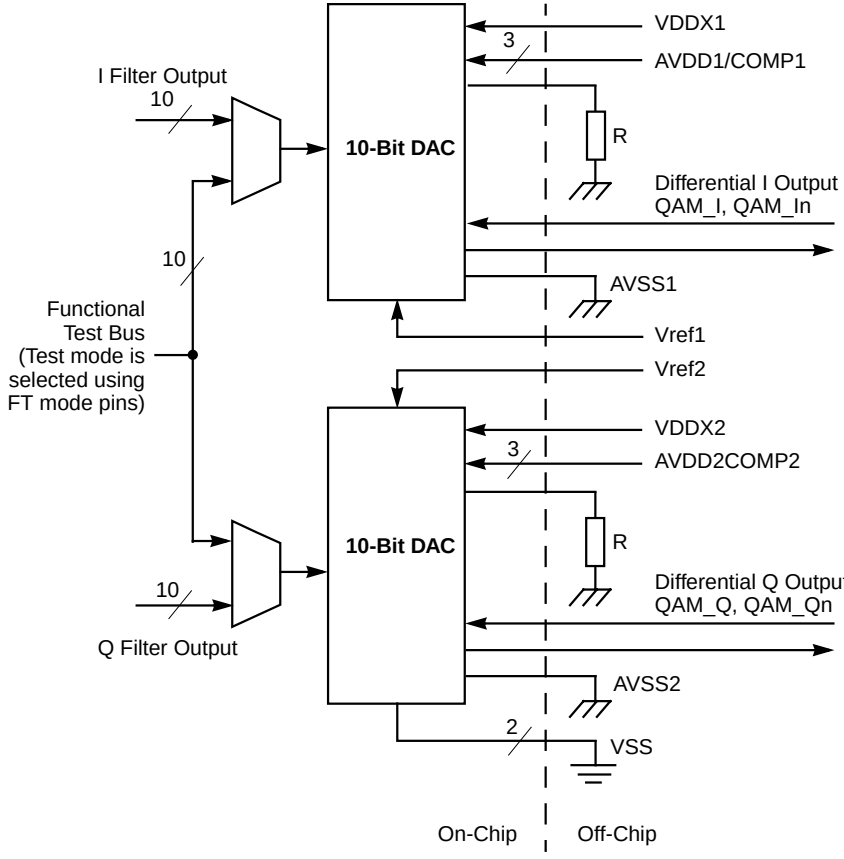
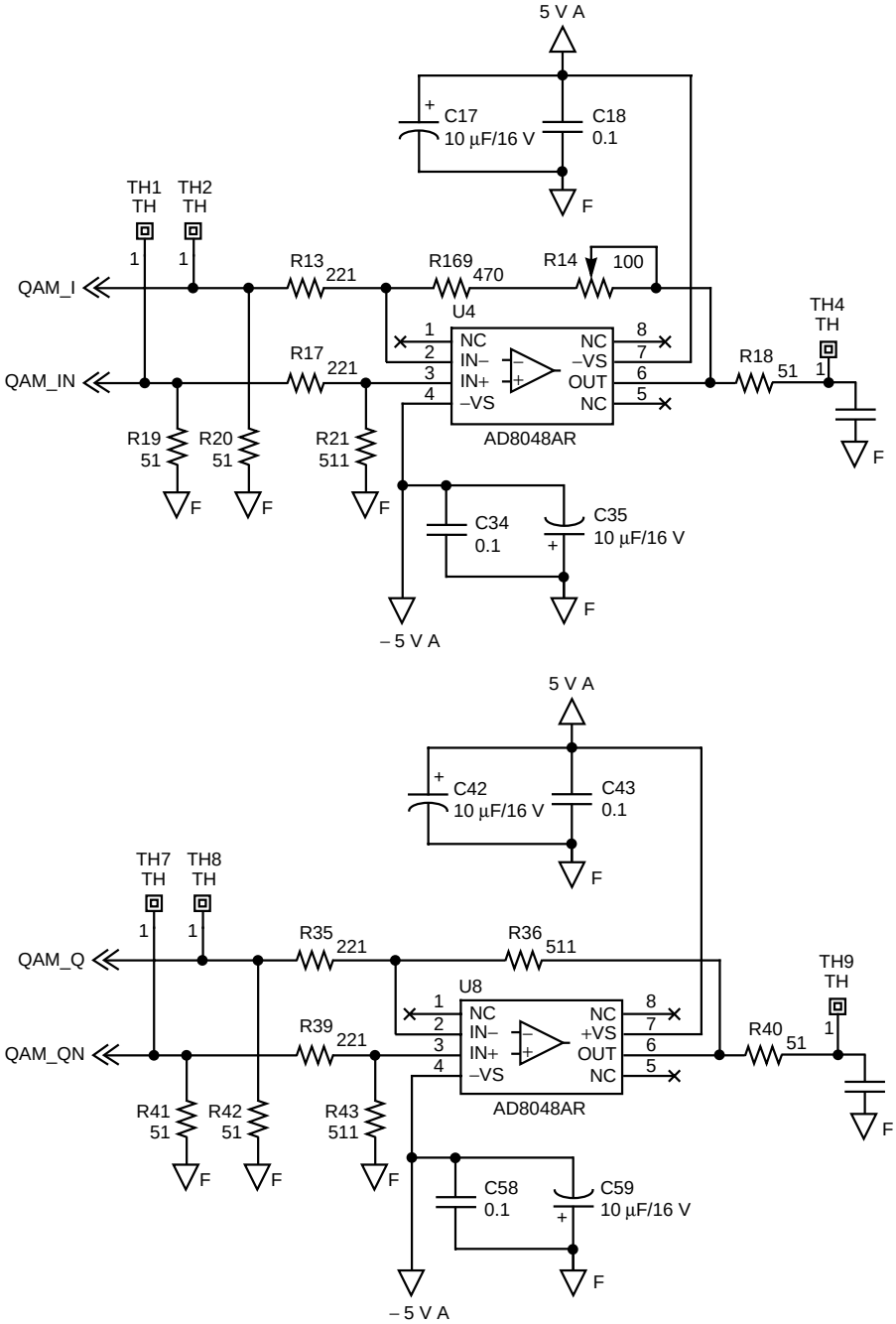


Figure 3.2 shows a typical application for interfacing with the outputs of the two L64777 DACs.

Figure 3.2 I And Q DAC Filter Diagrams



The device has separate differential outputs for the I and Q component. The differential outputs terminate externally (that is, the external components must provide termination to both differential lines, and the DAC achieves maximum linearity in differential mode).

3.4 Digital Output Interface

The L64777 I and Q component outputs are available in 10-bit digital format. Depending on the PLL mode, either OCLK or PCLK is the related clock. The output format can be programmed either as a two's complement, or as a sine magnitude representation.

Chapter 4
Register Descriptions

This chapter describes registers used to configure and monitor the L64777.

The sections in this chapter are:

4.1 Group 2 General-Purpose Registers

The registers listed in Table 4.1 and described subsequently comprise the Group 2 registers. These registers configure and monitor the operations of the L64777. (Note that the L64777 does not use Groups 1, 3–7.) The filter coefficient register A0 is a sequential input register, which sequentially shifts in the 196 bytes of filter coefficients. Therefore, the external microprocessor must make exactly 196 accesses to that register. To verify the filter coefficients, read back the contents of Register 0 after writing each coefficient. This does not influence the shift register shift operation. The remaining registers can be either loaded or read back at random. The address is specified by writing it into the Group 0 Address Pointer register.

All 43 registers of the L64777 are 8-bit. Table 4.1 provides an overview of the bit allocations for the L64777 registers. Note that an R in column A indicates a read-only register; an RW indicates a read/write register.

Table 4.1 Group 2 Bit Allocation

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A
FCOEFF.7	FCOEFF.6	FCOEFF.5	FCOEFF.4	FCOEFF.3	FCOEFF.2	FCOEFF.1	FCOEFF.0	R/W 0
SERIN	NEWSYNC	EXTSYNC	PLLSET	FREQ_PHASE	MSIZE.2	MSIZE.1	MSIZE.0	R/W 1
RESERVED	FDEL.6	FDEL.5	FDEL.4	FDEL.3	FDEL.2	FDEL.1	FDEL.0	R/W 2
SMAG	RESERVED	IQ_EX	RESERVED	SCR_OFF	RS_OFF	INT_OFF	RESERVED	R/W 3
SYNC_ LENGTH.7	SYNC_ LENGTH.6	SYNC_ LENGTH.5	SYNC_ LENGTH.4	SYNC_ LENGTH.3	SYNC_ LENGTH.2	SYNC_ LENGTH.1	SYNC_ LENGTH.0	R/W 4
SYNC_ BYTE.7	SYNC_ BYTE.6	SYNC_ BYTE.5	SYNC_ BYTE.4	SYNC_ BYTE.3	SYNC_ BYTE.2	SYNC_ BYTE.1	SYNC_ BYTE.0	R/W 5
AUTO-RESET	PLL_INV	IRAM_OFF	FIFO_OFF	DIFF_OFF	MAP_OFF	AMPL	RESERVED	R/W 6
ICNT_O.7	ICNT_O.6	ICNT_O.5	ICNT_O.4	ICNT_O.3	ICNT_O.2	ICNT_O.1	ICNT_O.0	R/W 7
RESERVED	ICNT_O.14	ICNT_O.13	ICNT_O.12	ICNT_O.11	ICNT_O.10	ICNT_O.9	ICNT_O.8	R/W 8
ICNT_I.7	ICNT_I.6	ICNT_I.5	ICNT_I.4	ICNT_I.3	ICNT_I.2	ICNT_I.1	ICNT_I.0	R/W 9
RESERVED	I_ICNT_I.14	ICNT_I.13	ICNT_I.12	ICNT_I.11	ICNT_I.10	ICNT_I.9	ICNT_I.8	R/W 10
TRACK-STEPS.1	TRACK-STEPS.0	UNCON-STR. INPUT	GAP.4	GAP.3	GAP.2	GAP.1	GAP.0	R/W 11
SYNCOK	SYNCOK_ STORE	FIFO_ ALARM_ STORE	ERF_ STORE	NCO EVENT	MASK_ERF	MASK_ SYNCOK	MASK_FIFO _ALARM	R/W 12
RESERVED	BELOW_ THRES	MEASURE_ DONE	STEP_ UPDATE	AUTO_ ACQUI_ RUNNING	ACQ_STATE .2	ACQ_STATE .1	ACQ_STATE .0	R 13
RESERVED	START MEASURE-MENT	ENABLE_ NCO_LOOP	MASK_NCO _IRQ	AUTO_ ACQUISITIO N_ON	MASK_ACQ _IRQ	EN_PHASE _LOOP	FIFO_INT	R/W 14
TEST.7	TEST.6	TEST.5	TEST.4	TEST.3	TEST.2	TEST.1	TEST.0	R/W 15
INISTEP.7	INISTEP.6	INISTEP.5	INISTEP.4	INISTEP.3	INISTEP.2	INISTEP.1	INISTEP.0	R/W 16
INISTEP.15	INISTEP.14	INISTEP.13	INISTEP.12	INISTEP.11	INISTEP.10	INISTEP.9	INISTEP.8	R/W 17
INISTEP.23	INISTEP.22	INISTEP.21	INISTEP.20	INISTEP.19	INISTEP.18	INISTEP.17	INISTEP.16	R/W 18
NCO_GAIN. 7	NCO_GAIN. 6	NCO_GAIN. 5	NCO_GAIN. 4	NCO_GAIN. 3	NCO_GAIN. 2	NCO_GAIN. 1	NCO_GAIN. 0	R/W 19
NCO_GAIN. 15	NCO_GAIN. 14	NCO_GAIN. 13	NCO_GAIN. 12	NCO_GAIN. 11	NCO_GAIN. 10	NCO_GAIN. 9	NCO_GAIN. 8	R/W 20

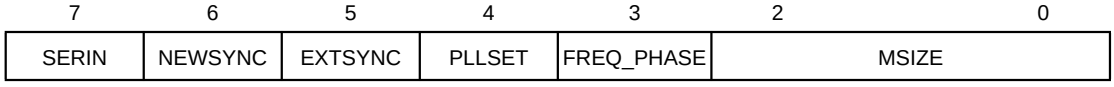
Table 4.1 Group 2 Bit Allocation (Cont.)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A
REF_DUR.7	REF_DUR.6	REF_DUR.5	REF_DUR.4	REF_DUR.3	REF_DUR.2	REF_DUR.1	REF_DUR.0	R/W 21
REF_DUR.15	REF_DUR.14	REF_DUR.13	REF_DUR.12	REF_DUR.11	REF_DUR.10	REF_DUR.9	REF_DUR.8	R/W 22
PROB_DUR.7	PROB_DUR.6	PROB_DUR.5	PROB_DUR.4	PROB_DUR.3	PROB_DUR.2	PROB_DUR.1	PROB_DUR.0	R/W 23
PROB_DUR.15	PROB_DUR.14	PROB_DUR.13	PROB_DUR.12	PROB_DUR.11	PROB_DUR.10	PROB_DUR.9	PROB_DUR.8	R/W 24
N_PCLK.7	N_PCLK.6	N_PCLK.5	N_PCLK.4	N_PCLK.3	N_PCLK.2	N_PCLK.1	N_PCLK.0	R 25
NM_COUNT.7	NM_COUNT.6	NM_COUNT.5	NM_COUNT.4	NM_COUNT.3	NM_COUNT.2	NM_COUNT.1	NM_COUNT.0	R 26
NM_COUNT.15	NM_COUNT.14	NM_COUNT.13	NM_COUNT.12	NM_COUNT.11	NM_COUNT.10	NM_COUNT.9	NM_COUNT.8	R 27
NM_COUNT.23	NM_COUNT.22	NM_COUNT.21	NM_COUNT.20	NM_COUNT.19	NM_COUNT.18	NM_COUNT.17	NM_COUNT.16	R 28
N_COUNT.7	N_COUNT.6	N_COUNT.5	N_COUNT.4	N_COUNT.3	N_COUNT.2	N_COUNT.1	N_COUNT.0	R 29
N_COUNT.15	N_COUNT.14	N_COUNT.13	N_COUNT.12	N_COUNT.11	N_COUNT.10	N_COUNT.9	N_COUNT.8	R 30
N_COUNT.23	N_COUNT.22	N_COUNT.21	N_COUNT.20	N_COUNT.19	N_COUNT.18	N_COUNT.17	N_COUNT.16	R 31
NP_COUNT.7	NP_COUNT.6	NP_COUNT.5	NP_COUNT.4	NP_COUNT.3	NP_COUNT.2	NP_COUNT.1	NP_COUNT.0	R 32
NP_COUNT.15	NP_COUNT.14	NP_COUNT.13	NP_COUNT.12	NP_COUNT.11	NP_COUNT.10	NP_COUNT.9	NP_COUNT.8	R 33
NP_COUNT.23	NP_COUNT.22	NP_COUNT.21	NP_COUNT.20	NP_COUNT.19	NP_COUNT.18	NP_COUNT.17	NP_COUNT.16	R 34
CUR_STEP.7	CUR_STEP.6	CUR_STEP.5	CUR_STEP.4	CUR_STEP.3	CUR_STEP.2	CUR_STEP.1	CUR_STEP.0	R 35
CUR_STEP.15	CUR_STEP.14	CUR_STEP.13	CUR_STEP.12	CUR_STEP.11	CUR_STEP.10	CUR_STEP.9	CUR_STEP.8	R 36
CUR_STEP.23	CUR_STEP.22	CUR_STEP.21	CUR_STEP.20	CUR_STEP.19	CUR_STEP.18	CUR_STEP.17	CUR_STEP.16	R 37
CUR_UPD.7	CUR_UPD.6	CUR_UPD.5	CUR_UPD.4	CUR_UPD.3	CUR_UPD.2	CUR_UPD.1	CUR_UPD.0	R 38
CUR_UPD.15	CUR_UPD.14	CUR_UPD.13	CUR_UPD.12	CUR_UPD.11	CUR_UPD.10	CUR_UPD.9	CUR_UPD.8	R 39
FIFO_FULL.7	FIFO_FULL.6	FIFO_FULL.5	FIFO_FULL.4	FIFO_FULL.3	FIFO_FULL.2	FIFO_FULL.1	FIFO_FULL.0	R 40
PH_GAIN.7	PH_GAIN6	PH_GAIN.5	PH_GAIN.4	PH_GAIN.3	PH_GAIN.2	PH_GAIN.1	PH_GAIN.0	R/W 41
EXT_GAP.7	EXT_GAP.6	EXT_GAP.5	EXT_GAP.4	EXT_GAP.3	EXT_GAP.2	EXT_GAP.1	EXT_GAP.0	R/W 42
THRESH-OLD.7	THRESH-OLD.6	THRESH-OLD.5	THRESH-OLD.4	THRESH-OLD.3	THRESH-OLD.2	THRESH-OLD.1	THRESH-OLD.0	R/W 43

4.1.1 Register 0

FCOEFF **Filter Coefficient Shift** **R/W [7:0]**
Writing to this location shifts the 196-byte filter coefficient shift register forward by one and puts this entry at the end of the queue. Reading this location shows the last entry of the coefficient shift register without shifting it. The reset values for the bit fields in this register are 0.

4.1.2 Register 1



SERIN **Serial/Parallel Input Setting** **R/W 7**
When this bit is 1, the L64777 uses DIN[0] as serial input and considers ICLK as a bit clock. When this bit is 0, the L64777 uses DIN[7:0] as parallel input and ICLK as a byte clock. The reset value is 0.

NEWSYNC **NEWSYNC Insertion** **R/W 6**
When this bit is 1, the L64777 inserts a new sync word (NEWSYNC, see Section 2.6.1) into the data stream. When this bit is 0, the L64777 leaves the data stream unchanged. The reset value is 1.

EXTSYNC **Synchronization Setting** **R/W 5**
When this bit is 1, the L64777 synchronizes positive pulses on the FSTARTIN pin. When this bit is 0, the L64777 synchronizes on SYNC_BYTE in the input stream. The reset value is 0.

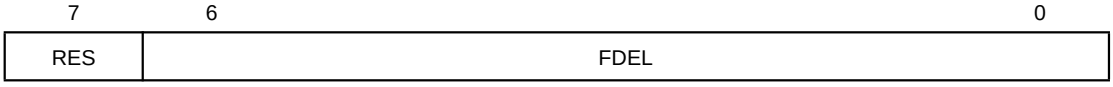
PLLSET **PLL Divider Setting** **R/W 4**
When this bit is 1, the L64777 forces a load of PLL dividers. When this bit is 0, the L64777 runs the PLL dividers normally. The reset value is 0.

FREQ_PHASE **Frequency/Phase Compare** **R/W 3**
When this bit is 1, the L64777 uses frequency compare for external VCO control. When this bit is 0, the L64777 uses phase compare. The reset value is 1.

MSIZE **Symbol Size** **R/W [2:0]**

This value indicates the size of symbols:
0b000 = 1 bit
0b001 = 2 bit
0b010 = 3 bit
0b011 = 4 bit
0b100 = 5 bit
0b101 = 6 bit
0b110 = 7 bit
0b111 = 8 bit.
The reset value is 0b101

4.1.3 Register 2



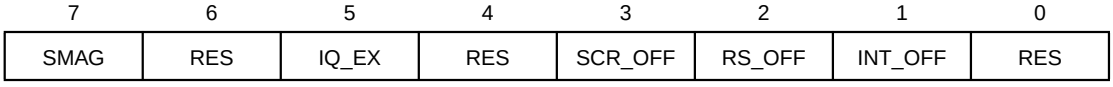
RES **Reserved** **7**

This bit is reserved.

FDEL **FIFO Delay** **R/W [6:0]**

This parameter indicates the FIFO delay value in the Gray Code. Writing to this location loads the ICLK address counter with 0 and the OCLK-driven address counter to the FDEL value. If the FIFO is automatically reset, the L64777 also uses this value for the OCLK-driven address. The reset value is 0b110 0000.

4.1.4 Register 3



SMAG **Sign Magnitude** **R/W 7**

When this bit is 0, the L64777 outputs a two's complement at the Nyquist filter. When this bit is 1, the L64777 inverts the sign bit and the output sign magnitude representation. The reset value is 0.

RES **Reserved** **6, 4, 0**

These bits are reserved.

IQ_EX **I and Q Channel Exchange** **R/W 5**
When this bit is 1, the L64777 exchanges the I and Q channels at the Nyquist filter input. When this bit is 0, the L64777 leaves the data stream unchanged. The reset value is 0.

SCR_OFF **Scrambler Off** **R/W 3**
When this bit is 1, the L64777 stops the scrambler and delays the data in this module by three clock cycles. When this bit is 0, the scrambler runs normally. The reset value is 0.

RS_OFF **Reed-Solomon Off** **R/W 2**
When this bit is 1, the L64777 stops the Reed Solomon (RS) encoder and delays the data in this module by two clock cycles. When this bit is 0, the L64777 runs the RS encoder normally. The reset value is 0.

INT_OFF **Interleaver Off** **R/W 1**
When this bit is 1, the L64777 stops the interleaver and delays the data in this module by three clock cycles. When this bit is 0, the L64777 runs the interleaver in DVB-compliant mode. The reset value is 0.

4.1.5 Register 4

SYNC_LENGTH
Sync Block Length **R/W [7:0]**
This register specifies the distance between consecutive SYNC_BYTE values. Legal register values range from 32 to 255 for sync block length. The reset value is 0b1011 1011.

4.1.6 Register 5

SYNC_BYTE **Sync Reference Pattern** **R/W [7:0]**
This register specifies the sync reference pattern. The reset value is 0b0100 0111.

4.1.7 Register 6

7	6	5	4	3	2	1	0
AUTORESET	PLL_INV	IRAM_OFF	FIFO_OFF	DIFF_OFF	MAP_OFF	AMPL	RES

AUTORESET **Automatic Reset Setting** **R/W 7**

When this bit is 1, the L64777 loads the FIFO address counters with the initial values in register 2 after the detection of a FIFO alarm (pointer collision). When this bit is 0, the FIFO address counters remain unchanged after a pointer collision until an external microcontroller intervenes. The reset value is 1.

PLL_INV **Phase Detector Setting** **R/W 6**

When this bit is 1, the L64777 exchanges the reference and feedback inputs of the frequency and phase detector. When this bit is 0, no exchange takes place. The reset value is 0.

IRAM_OFF **Interleaver RAM Off** **R/W 5**

When this bit is 1, the L64777 switches the interleaver RAM off after reset and initializes the RAM with 0 values (not with the incoming data stream). The interleaver RAM resumes normal operation as soon as the first sequence start from the SSTARTIN pin (pin 90) comes in the data stream. This setting is useful for getting a well-defined chip output sequence. When this bit is 0, the L64777 uses the interleaver RAM in DVB-compliant mode on the input data stream. The reset value is 1.

FIFO_OFF **FIFO Off** **R/W 4**

When this bit is 1, the L64777 switches the FIFO input stage off and clocks the input data stream through three internal registers from the ICLK to the OCLK domain. When this bit is 0, the L64777 uses normal FIFO processing and delay. The reset value is 0.

Note: This mode requires ICLK to be exactly the same signal as OCLK. You must connect these pins to each other.

DIFF_OFF **Differential Encoding Off** **R/W 3**

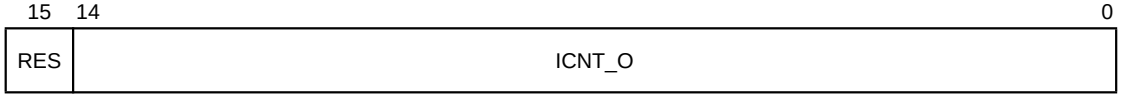
When this bit is 1, the L64777 switches the differential encoding off. When this bit is 0, the L64777 encodes according to the DVB standard. The reset value is 0.

MAP_OFF **QAM Mapping Off** **R/W 2**
When this bit is 1, the L64777 stops QAM mapping. When this bit is 0, the L64777 uses DVB-compliant mapping. The reset value is 0.

AMPL **PLL Oscillator Amplitude** **R/W 1**
This controls the amplitude of the on-chip PLL oscillator. When this bit is 0, the L64777 is in low-power mode with higher jitter. When this bit is 1, the L64777 is in high-power mode with lower jitter. For normal operation, set this bit to 0.

RES **Reserved** **0**
This bit is reserved.

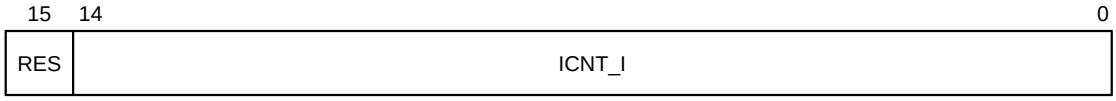
4.1.8 Registers 7 and 8



RES **Reserved** **15**
This bit is reserved.

ICNT_O **Initial OCLK Value** **R/W [14:0]**
This is a 15-bit initial value for the OCLK PLL feedback division. The reset value for bit 3 is 1; for all other bits it is 0.

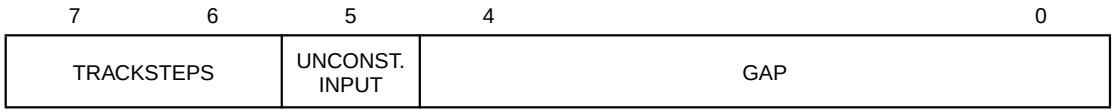
4.1.9 Registers 9 and 10



RES **Reserved** **15**
This bit is reserved.

ICNT_I **Initial ICLK Value** **R/W [14:0]**
This is a 15-bit initial value for the ICLK PLL reference division. The reset value for bit 1 is 1; for all other bits it is 0.

4.1.10 Register 11



TRACKSTEPS

Steps to Sync **R/W [7:6]**

This value indicates the number of steps to acquire synchronization and to declare loss of sync if the sync pattern is missing for this number of events:
0b00 = 3
0b01 = 4
0b11 = 5
The reset value is 0b00.

UNCONST. INPUT

Unconstrained Input **R/W 5**

The default setting of this bit is 0, which indicates that a frame structure with a sync byte is required after every (block length –1) bytes. If this bit is 1, any data stream is accepted. The reset value is 0.

GAP **RS Code Bytes** **R/W [4:0]**

This is the number of bytes to be inserted for the RS code at each end of a sync block. If the value is 0, there is no modification of the incoming data stream. The maximum value is 31 bytes to insert. This control generates the gaps in the incoming stream for RS code insertion. At the end of each block, readout of the FIFO stops for the specified number of bytes. This determines the value of FDEL (Register 2). The gap parameter determines the number of bytes inserted into the symbol stream, but not read from the FIFO. These bytes come from the RS encoder; thus, the setting must be 16 (or 18 for the proprietary mode). The reset value is 0b10000.

4.2 NCO-Related Registers

4.2.1 Register 12

7	6	5	4	3	2	1	0
SYNCOK	SYNCOK _STORE	FIFO_ALARM _STORE	ERF_STORE	NCO_EVENT	MASK_ERF	MASK_SYNC OK	MASK_FIFO _ALARM

SYNCOK **State of SYNCOK Pin** **R/W 7**

This value reflects the actual state of the SYNCOK pin. This signal is slow enough to be sampled by the external microcontroller. When this bit is 1, sync is achieved. When this bit is 0, sync is not achieved. The reset value is 0.

SYNCOK_STORE **R 6**

This read-only bit is set to 1 if a faulty SYNCOK condition is detected since the last read. If this bit is 0, it indicates that the sync lock status continues to be positive. The reset value is 0.

FIFO_ALARM_STORE **R 5**

This read-only bit is set to 1 if a FIFO alarm condition is detected since the last read. If this bit is 0, no FIFO alarm condition was detected. The reset value is 0.

ERF_STORE **Error Flag Store** **R 4**

This read-only bit is set to 1 if an error flag is inserted since the last read. If this bit is 0, no error flag was inserted. The reset value is 0.

NCO_EVENT **R/W 3**

If this bit is 1, the NCO measurement is complete or the AUTO ACQUISITION has terminated. The reset value is 0.

MASK_ERF **Error Flag Mask** **R/W 2**

If this bit is 1, an error flag insertion in the MPEG transport packet does not generate an interrupt. If this bit is 0, an error flag insertion does generate an interrupt. The reset value is 0.

MASK_SYNCOK **1**

If this bit is 1, a missing SYNCOK does not generate an interrupt. If this bit is 0, a missing SYNCOK generates an interrupt. The reset value is 0.

MASK_FIFO_ALARM **0**

If this bit is 1, a FIFO alarm (pointer collision) does not generate an interrupt. If this bit is 0, a FIFO alarm (pointer collision) generates an interrupt. The reset value is 0.

4.2.2 Register 13

7	6	5	4	3	2 0
RES	BELOW_ THRES	MEASUREMENT_ DONE	STEP_ UPDATE	AUTO_ACQUI_ RUNNING	ACQ_STATE

RES **Reserved** **R 7**

This bit is reserved.

BELOW_THRES

FIFO CONTENT THRESHOLD **R 6**

When this bit is 1, the virtual FIFO content is below or equal to the threshold programmed in Register 43. During AUTO_ACQUISITION, the threshold is dynamically changed. The reset value is 0.

MEASUREMENT_DONE **R 5**

A 1 in this bit indicates that the measurement data gained during byte clock probe are valid and that the measurement is complete. The reset value is 0.

STEP_UPDATE **R 4**

A 1 in this bit indicates a step update since the last reading of the register. This is relevant only during NCO acquisition mode. The reset value is 0.

AUTO_ACQUI_RUNNING **R 3**

A 1 in this bit indicates that the internal frequency acquisition is running. The reset value is 0.

ACQ_STATE **Internal Acquisition State** **R [2:0]**

This indicates how many auto acquisition loops have taken place since the initiation of the auto acquisition mode. The reference duration has a length of two ACQ_STATE input packets, and the threshold is divided by two ACQ_STATE times. The reset value is 0b111.

4.2.3 Register 14

7	6	5	4	3	2	1	0
RES	START_ MEASURE-MENT	ENABLE_ NCO_LOOP	MASK_NCO_ IRQ	AUTO_ ACUISITION _ON	MASK_ACQ_ IRQ	EN_PHASE_ LOOP	FIFO_INT

RES **Reserved** **7**

This bit is reserved.

START_MEASUREMENT **R/W 6**

A transition from 0-to-1 starts a measurement of the byte clock connected to the ICLK input. MEASUREMENT_ DONE in status register (13) indicates the end of the measurement. The reset value is 0.

ENABLE_NCO_ LOOP **R/W 5**

Setting this bit allows a step update in the NCO loop based on the FIFO fullness. The REF_DUR parameter can adjust the update frequency. The reset value is 0.

MASK_NCO_IRQ **R/W 4**

Setting this bit enables the interrupt for the MEASUREMENT_DONE event. Even in the case of a disabled interrupt, the status is indicated correctly. The reset value is 0.

AUTO_ACQUISITION_ON **R/W 3**

A 1-to-0 transition in this bit starts an internal procedure to regulate the NCO frequency. The reset value is 0. Setting this bit to 1 activates the autoacquisition mode.

MASK_ACQ_IRQ **R/W 2**

If this bit is 1, a transition from 1 to 0 in the AUTO_ACQUI_RUNNING bit of register 13 causes an interrupt. The interrupt is visible in the NCO_EVENT bit of register 12 and clears upon the reading of register 13. The reset value is 0.

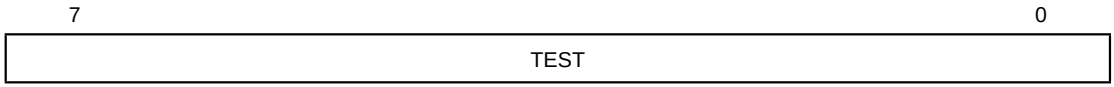
EN_PHASE_LOOP **R/W 1**

Setting this bit enables the phase acquisition loop, after Autofrequency Acquisition is completed in the NCO mode of operation. The reset value is 0.

FIFO_INT **FIFO Interrupt** **R/W 0**

This bit enables generation of an interrupt in response to a FIFO alarm. The reset value is 0.

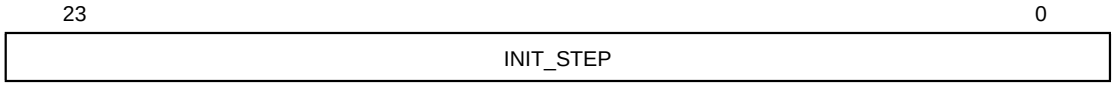
4.2.4 Register 15



TEST **Reserved Test** **R/W [7:0]**

This register is reserved for LSI Logic production testing; each bit field must be set to zero. The reset value is 0.

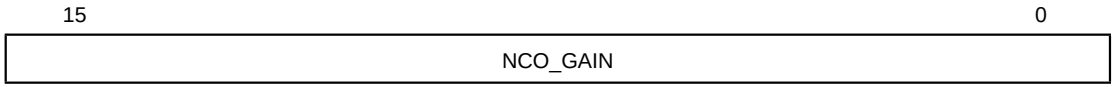
4.2.5 Registers 16, 17, and 18



INIT_STEP **R/W [23:0]**

This value is the initial NCO step parameter. It is loaded into the NCO when the most significant portion is written. These are NCO-related register fields; they are used only in PLL Mode. Bits 8 and 23 are reset to 0; all other bits are reset to 1.

4.2.6 Registers 19 and 20



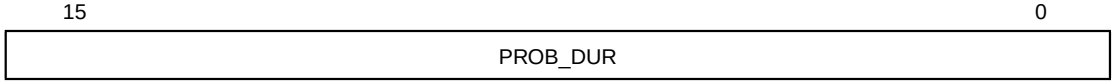
NCO_GAIN **NCO Loop Bandwidth Adjustment** **R/W [15:0]**

The L64777 can use this parameter to adjust the NCO loop bandwidth. The value becomes valid on writing to the most significant portion. These are NCO-related register fields; they are used only in PLL Mode 2. Bit 8 is reset to 1; all other bits are reset to 0.

4.2.7 Registers 21 and 22

REF_DUR **Duration Between NCO Step Updates** **R/W [15:0]**
This parameter determines the duration between the NCO step updates in multiples of the sync length. These are NCO-related register fields; they are used only in PLL Mode 2. Bit 0 resets to 1; all other bits reset to 0.

4.2.8 Registers 23 and 24

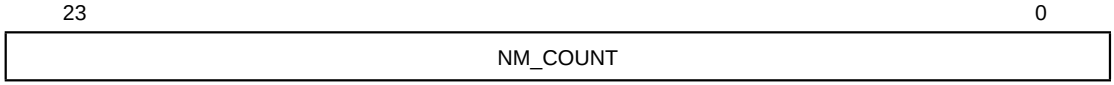


PROB_DUR **Byte Clock Duration** **R/W [15:0]**
This parameter determines the duration for the byte clock measurement in units of 256 ICLK cycles. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.9 Register 25

N_PCLK **PCLK Cycles** **R/W [7:0], R**
This is the number of PCLK cycles during one ICLK byte clock. The value in this register is valid only if the MEASUREMENT_DONE bit in the NCO control register is set. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.10 Registers 26, 27, and 28



NM_COUNT **R [23:0]**
This value is the number of CLK cycles found within the duration of the (n – 1) PCLK cycles. The value in this

register is valid only if the MEASUREMENT_DONE bit in the NCO control register is set. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.11 Registers 29, 30, and 31

N_COUNT **ICLK Cycles** **R [23:0]**

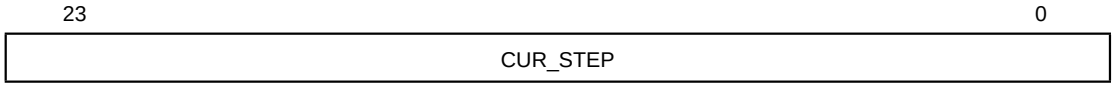
This value is the number of ICLK cycles found within the duration of n PCLK cycles. The value in this register is valid only if the MEASUREMENT_DONE bit in the NCO control register is set. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.12 Registers 32, 33, and 34

NP_COUNT **R [23:0]**

This value is the number of ICLK cycles found within the duration of (n + 1) PCLK cycles. The value in this register is valid only if the MEASUREMENT_DONE bit in the NCO control register is set. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

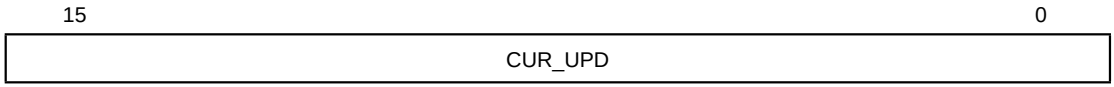
4.2.13 Registers 35, 36, and 37



CUR_STEP **Current NCO Loop Step** **R [23:0]**

This value indicates the current NCO loop step. It differs from the programmed update step if autoacquisition is enabled. The registers are read-only. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.14 Registers 38 and 39

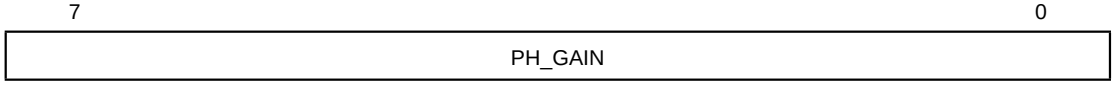


CUR_UPD **Current NCO Loop Update Step** **R [15:0]**
This value indicates the current NCO loop update step. It differs from the programmed update step if autoacquisition is enabled. The registers are read-only. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.15 Register 40

FIFO_FULL **FIFO Fullness Indicator** **R [7:0]**
This value is a sign representation of the virtual FIFO fullness used for the NCO loop regulation. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0.

4.2.16 Register 41

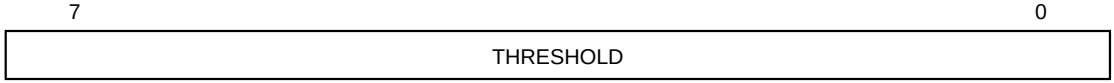


PH_GAIN **Phase Regulation Gain** **R/W [7:0]**
This value sets the gain used during phase regulation. The real value applied is multiplied by four. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0b0001 0000.

4.2.17 Register 42

EXT_GAP **Gap Bytes** **R/W [7:0]**
This value indicates the number of gap bytes applied to the TS input. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0b0100 0110.

4.2.18 Register 43



THRESHOLD **FIFO Measurement Threshold** **R/W [7:0]**
This value sets the threshold for the virtual FIFO measurement, which is used as the initial value for the autoacquisition. These are NCO-related register fields; they are used only in PLL Mode 2. The reset value is 0b0111 0011

Table 4.2 shows the reset values for all register fields.

Table 4.2 Reset Values for Register Fields

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1
0	1	1	0	0	0	0	0	2
0	0	0	0	0	0	0	0	3
1	0	1	1	1	0	1	1	4
0	1	0	0	0	1	1	1	5
1	0	1	0	0	0	0	1	6
0	0	0	0	1	0	0	0	7
0	0	0	0	0	0	0	0	8
0	0	0	0	0	0	1	0	9
0	0	0	0	0	0	0	0	10
0	0	0	1	0	0	0	0	11

Table 4.2 Reset Values for Register Fields (Cont.)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A
0	0	0	0	0	0	0	0	12
0	0	0	0	0	1	1	1	13
0	0	0	0	0	0	0	0	14
0	0	0	0	0	0	0	0	15
1	1	1	1	1	1	1	1	16
1	1	1	1	1	1	1	0	17
0	1	1	1	1	1	1	1	18
0	0	0	0	0	0	0	0	19
0	0	0	0	0	0	0	1	20
0	0	0	0	0	0	0	1	21
0	0	0	0	0	0	0	0	22
0	0	0	0	0	0	0	0	23
0	0	0	0	0	0	0	0	24
0	0	0	0	0	0	0	0	25
0	0	0	0	0	0	0	0	26
0	0	0	0	0	0	0	0	27
0	0	0	0	0	0	0	0	28
0	0	0	0	0	0	0	0	29
0	0	0	0	0	0	0	0	30
0	0	0	0	0	0	0	0	31
0	0	0	0	0	0	0	0	32
0	0	0	0	0	0	0	0	33
0	0	0	0	0	0	0	0	34
0	0	0	0	0	0	0	0	35
0	0	0	0	0	0	0	0	36
0	0	0	0	0	0	0	0	37
0	0	0	0	0	0	0	0	38
0	0	0	0	0	0	0	0	39
0	0	0	0	0	0	0	0	40
0	0	0	1	0	0	0	0	41
0	1	0	0	0	1	1	0	42
0	1	1	1	0	0	1	1	43

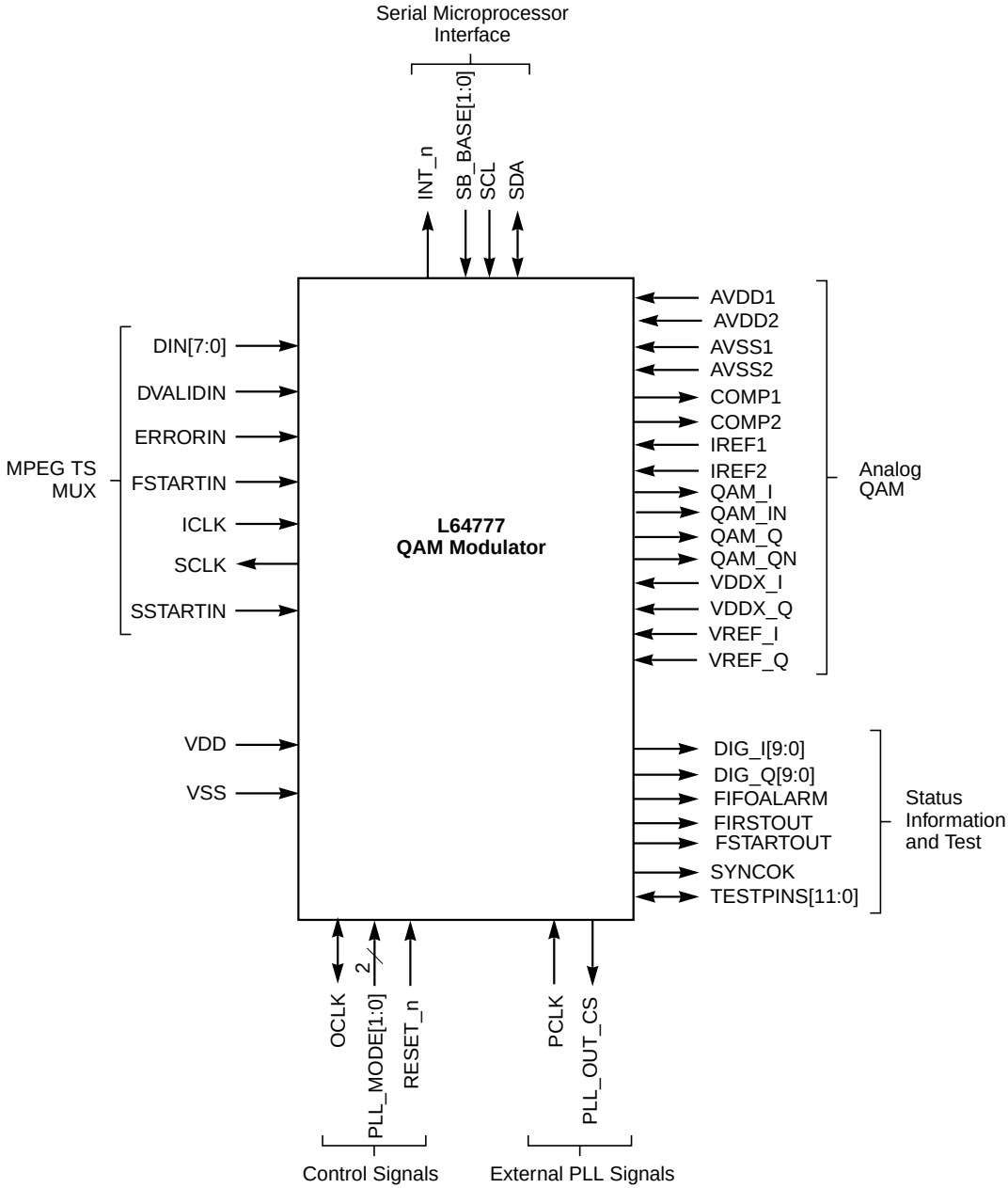
Chapter 5
Signals

This chapter defines the signals for the L64777. It consists of the following sections:

5.1 Overview

Figure 5.1 shows the L64777 interface signals in their respective groupings. Within each category, the signals are described in alphabetical order by signal mnemonic.

Figure 5.1 Logic Symbol for the L64777



5.2 MPEG Transport Stream Multiplexer Signals

DIN[7:0] **QAM Modulator Parallel/Serial Data In** **Input**
Serial data enters the L64777 on DIN[0]; parallel data enters on DIN[7:0]. The modulator samples DIN[7:0] at the positive edge of ICLK. The DIN[7:0] input accepts data with any number of invalid bits in between. The modulator disregards invalid bits or bytes and does not take them into the input FIFO.

DVALIDIN **Clock Enable Input** **Input**
When DVALIDIN is active (HIGH), the L64777 accepts data from DIN[7:0] on a continuous basis. When DVALIDIN is LOW, data input to the internal FIFO and internal data processing stops, and the encoder does not accept new input from the DIN[7:0] pins. DVALIDIN functions independently of the modulator.

ERRORIN **Error Detection Flag** **Input**
The ERRORIN pin is asserted to flag uncorrectable errors. The L64777 checks the ERRORIN status at the first bit of a frame; then, if required (HIGH = set error bit), it copies the value of that bit to the MPEG error-indication bit.

FSTARTIN **External Sync Input** **Input**
The FSTARTIN pin is asserted to mark the beginning of an MPEG transport packet by a hardwired signal. If the incoming bitstream contains no unique sync words, this pulse must be applied to the L64777. The L64777 forces synchronization with FSTARTIN pulses into the chip; it does not flywheel-stabilize synchronization as in the sync word detection mode. In the sync insertion mode, the L64777 regenerates the DVB-defined sync information and inserts it into the QAM Modulator.

ICLK **QAM Modulator Input Clock** **Input**
ICLK is a positive-edge-triggered clock. The L64777 clocks DIN[7:0], DVALIDIN, ERRORIN, FSTARTIN and SSTARTIN on the rising edge of ICLK. ICLK is either a byte clock or a bit clock, depending on the control register (Register 1) setup for parallel/serial mode.

SCLK **Modulator Symbol Clock Output** **Output**
SCLK is a clock output synchronous to internally processed symbols and bytes; it is identical to OCLK/4. The L64777 uses SCLK to determine the phase of the Nyquist filter output. The rising edge of SCLK is followed by Phase 0. The falling edge is the transition of Phase 1 to Phase 2 in 4-fold oversampling mode.

SSTARTIN **Sync Sequence Start** **Input**
The SSTARTIN pin is asserted to mark the beginning of a new, fully reset sequence by a hardwired signal. The L64777 evaluates the SSTARTIN negative slope and restarts all internal sequences at the next Block/Frame start following the negative SSTARTIN slope. If no SSTARTIN is applied, all internal sequences run free after the reset.

5.3 Status Information Signals

DIG_I[9:0] **Digital I Component** **Output**
This port provides modulator I-component output in digital format. Depending on the PLL mode, either OCLK or PCLK is the related clock.

DIG_Q[9:0] **Digital Q Component** **Output**
This port provides modulator Q-component output in digital format. Depending on the PLL mode, either OCLK or PCLK is the related clock.

FIFOALARM **FIFO Collision Detected** **Output**
If this alarm occurs, the FIFO control has detected equal pointers for read and write access. A detected collision most probably indicates unlocked external PLL-VCO circuitry. The L64777 synchronizes this signal with SCLK-driven flip-flops for the output.

FIRSTOUT **First Block of New Sequence Out** **Output**
FIRSTOUT occurs together with FSTARTOUT and indicates the head of a sync block that has just-reset sequences, as controlled by SSTARTIN. FIRSTOUT is the acceptance of a SSTARTIN negative slope delayed by all internal processing modules.

FSTARTOUT **Frame Start Output** **Output**
FSTARTOUT is asserted during the first symbol in every sync frame. The width of FSTARTOUT reflects the number of bytes that the gap parameter inserts. A one-cycle width indicates no inserted gaps; a width of 17 means 16 inserted bytes as an Reed-Solomon gap. FSTARTOUT is applied only in sync word detection mode. If FSTARTIN pulses force synchronization, FSTARTOUT is constantly LOW.

SYNCOK **SYNC Detection/Phase Monitoring** **Output**
In internal sync mode, this pin indicates undisturbed synchronization status when HIGH. This signal is asserted when the number of track steps required for synchronization is fulfilled. If FSTARTIN pulses force synchronization, SYNCOK is constantly LOW.

5.4 Test Signals

FTMODE[2:0] **Functional Test Bus** **Input**
These must be tied to 0.

IDDTN[3] **IDD Test Mode** **Input**
IDDTN is a production test pin.

NT_OUT[4] **Nand Tree Output** **Output**
NT_OUT is a production test pin.

SCAN_ENABLE[5]
Scan Enable **Input**
This pin enables scan chain shift.

TNn[11] **Test Output Enable** **Input**
TNn switches all 3-state buffers to high-impedance mode for testing.

TRSTn[10] **Test Reset** **Input**
Reset for the JTAG unit.

TMS[9] **Test Mode Select** **Input**
TMS selects the JTAG unit test mode.

TDO[8] **Test Data Output** **Output**
TDO is the JTAG unit data output.

TDI[7] **Test Data Input** **Input**
TDI is the JTAG unit data input.

TCK[6] **Test Mode Clock** **Input**
TCK is the JTAG test mode clock.

5.5 Control Signals

OCLK **Encoder Out/Processing Clock In** **Bidirectional**
OCLK is a positive-edge-triggered clock. The L64777 internally processes data based on a fraction of OCLK (for example: scrambler, interleaver, Reed-Solomon encoder) and references data outputs (I, Q, FSTARTOUT) to OCLK.

PLL_MODE[1:0]
Select PLL Mode **Input**
To select the PLL mode:

0b00 or 0b01 for external PLL usage
0b11 for NCO usage

RESET_n **Reset** **Input**
This pin resets all internal data paths. Reset timing is asynchronous to the device clocks. Reset affects all the configuration registers and the filter coefficients, which must be downloaded again after reset.

5.6 External PLL Signals

PCLK **Processing Clock: PLL Mode 2** **Input**
The PCLK output of the L64724 provides this clock, which drives the digital signal processing of interpolation and the NCO. When using Mode 1, leave this pin open.

PLL_OUT_CS **PLL Current Source** **3-State Output**
This pin is a charge pump for an external PLL low pass to control frequency. The comparator is frequency- and phase-sensitive. The pin is normally on 3-state Z level and drives positive and negative current, as required. Depending on the configuration, the current source can be inverted.

5.7 Analog QAM Signals

AVDD1 **Analog VDD Input: I Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

AVDD2 **Analog VDD Input: Q Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

AVSS1 **Analog VSS Input: I Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

AVSS2 **Analog VSS Input: Q Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

COMP1 **Compensation Output: I Comp. DAC Analog Output**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

COMP2 **Compensation Output: Q Comp. DAC Analog Output**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

IREF1 **Reference Current: I Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

IREF2 **Reference Current: Q Component DAC Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

QAM_I **Symbol I Modulation Analog Output**
QAM_I is the positive differential analog in-phase output signal of the modulator.

QAM_IN **Symbol I Modulation Inverted** **Analog Output**
QAM_IN is the corresponding inverted differential part to QAM_I.

QAM_Q **Symbol Q Modulation** **Analog Output**
QAM_Q is the positive differential analog quadrature output signal of the modulator.

QAM_QN **Inverted Differential of QAM_Q** **Analog Output**
QAM_QN is the corresponding inverted differential part to QAM_Q.

VDDX_I **Isolated Power: Digital-to-Analog Converter, I Channel**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

VDDX_Q **Isolated Power: Digital-to-Analalog Converter, Q Channel**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

VREF_I **Reference Voltage Input: I** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

VREF_Q **Reference Voltage Input: Q** **Analog Input**
For usage and value, see the LSI Logic datasheet *G10®-p CW900100 10-bit Direct Digital Synthesis Digital-to-Analog Converter* (September 1998).

5.8 Serial Microprocessor Interface Signals

INT_n **Interrupt Request** **Output**
The L64777 asserts INT_n LOW when the interrupt is enabled and an interrupt condition occurs. INT_n is an open drain output that requires an external pull-up resistor for operation.

SB_BASE[1:0]

Serial Bus Base Address **Input**

The external microprocessor must apply these two signals as static signals to the device because they determine the two LSBs of the serial bus base address.

SCL **Serial Clock Line** **Input**

In conjunction with SDA, SCL controls the microprocessor interface according to the protocol described in Appendix A.

SDA **Serial Data Access** **Bidirectional**

In conjunction with SCL, SDA controls the microprocessor interface according to the protocol described in Appendix A.

Chapter 6
Specifications

This chapter provides information about the electrical ratings, pins, and packaging for the L64777. It consists of the following sections:

6.1 AC/DC Specifications

This section lists the electrical requirements, provides the AC timing characteristics, shows the AC timing diagrams, and lists the AC timing values for the L64777 decoder.

6.1.1 Electrical Ratings

The tables in this section specify the electrical requirements for the L64777 decoder. Table 6.1 provides the L64777 absolute maximum electrical and temperature ratings. Table 6.2 provides the L64777 recommended operating conditions. Table 6.3 lists the DC characteristics for the L64777.

Table 6.1 L64777 Absolute Maximum Ratings

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply	–0.3 to 3.9	V
V_{IN}	LVTTL Input Voltage	–1.0 to V_{DD} + 0.3	V
V_{IN}	5 V Compatible Inputs	–1.0 to 6.5	V
I_{IN}	DC Input Current	10	mA
T_{STG}	Storage Temperature Range (Plastic)	–40 to +150	°C
T_J	Operating Junction Temperature Range	0 to +125	°C

Table 6.2 L64777 Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{DD}	DC Supply	+ 3.14 to + 3.45	V
T_A	Ambient Temperature	0 to + 70	°C

When studying the values in Table 6.3, note that the L64777 follows the LSI Logic G10-p process, which is characterized by a 0.35-micron gate length.

Table 6.3 L64777 DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
V_{DD}	Supply Voltage		3.14	3.3	3.45	V
V_{IL}	Input Voltage LOW		Vss – 0.5		0.8	V
V_{IH}	Input Voltage HIGH		2.0		V_{DD} + 0.3	V
V_{OH}	Output Voltage HIGH	I_{OH} = –4.0 mA	2.4		V_{DD}	V
V_{OL}	Output Voltage LOW	I_{OL} = 4.0 mA		0.2	0.4	V
I_{OZ}	Current 3-State Leakage w/Pulldown	V_{DD} = Max, V_{OUT} = V_{SS} or V_{DD}	–10	± 1	10	µA

Table 6.3 L64777 DC Characteristics (Cont.)

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
I_{IN}	Input Current Leakage	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	–10	± 1	10	mA
I_{IN}	Input Current Leakage w/Pullup	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	–62	–215	–384	mA
I_{IN}	Input Current Leakage w/Pulldown	V_{DD} = Max, V_{IN} = V_{DD} or V_{SS}	–62	–215	–384	mA
I_{DD}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS}			2	mA
I_{CC}	Dynamic Supply Current	ICLK = 54 MHz max, PLL MODE 2 PCLK 90 MHz VDD = Max		50		mA

1. Specified at V_{DD} = 3.3 V ± 5% at ambient temperature over the specified range.

6.1.2 AC Timing Diagrams for L64777

Figure 6.1 illustrates the TS input timing.

Figure 6.1 TS Input Timing

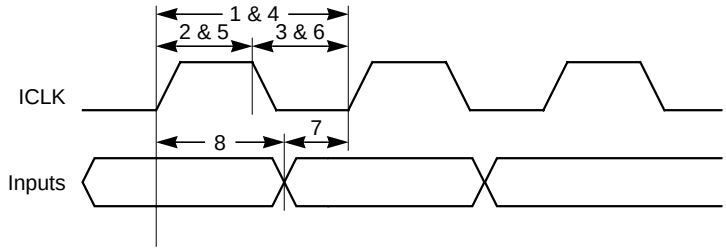


Figure 6.2 illustrates the reset timing of the L64777.

Figure 6.2 L64777 RESET Timing Diagram

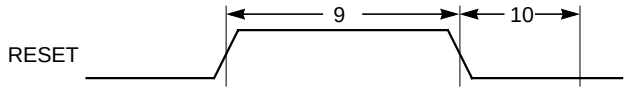
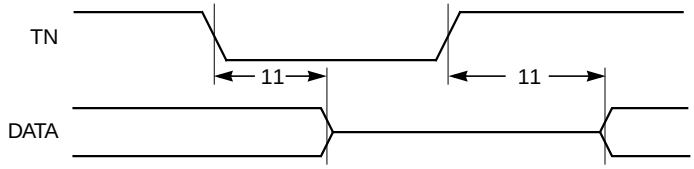


Figure 6.3 illustrates the 3-state delay timing of the L64777 bus.

Figure 6.3 L64777 Bus 3-state Delay Timing



The numbers in column 1 of Table 6.4 refer to the timing parameters in the preceding figures. All parameters in this table apply for T_A = 0 °C to 85 °C, V_{DD} = 3.1 V to 3.6 V, and an output load of 50 pF.

Table 6.4 L64777 Preliminary Timing Parameters

No.	Parameter	Description	Min	Max	Unit
1	tCYCLE	Clock Cycle OCLK	32	–	ns
2	tPWH	Clock Pulse Width HIGH OCLK	7	–	ns
3	tPWL	Clock Pulse Width LOW OCLK	7	–	ns
4	tI_CYCLE	Clock Cycle ICLK	18.5	–	ns
5	tI_PWH	Clock Pulse Width HIGH ICLK	9	–	ns
6	tI_PWL	Clock Pulse Width LOW ICLK	9	–	ns
7	tI_S	Input Setup Time to ICLK	6	–	ns
8	tI_H	Input Hold to ICLK	2	–	ns
9	tRWH	Reset Pulse Width HIGH	50	–	ns
10	tWK	Wake-up Time after RESET (used for RAM initialization during microprocessor configuration access)	1280 2560	– –	ICLK cycles with DVALIDIN = HIGH OCLK cycles
11	tTDLY	Delay from TN	–	20	ns

6.2 Pin Descriptions and Lists

The following subsections provide descriptions for the electrical pins, as well as numerical and alphabetic listings of all L64777 pins.

6.2.1 L64777 Electrical Pin Descriptions

Table 6.5 summarizes the electrical properties of the pins on the L64777. The table provides the signal types for both output and input pins, and the drive capacity for outputs.

Table 6.5 L64777 Pin Description Summary

Mnemonic	Description	Type	Drive (mA)	Active
AVDD1	Supply for DAC	Analog Input	–	–
AVDD2	Supply for DAC	Analog Input	–	–
AVSS1	Analog Supply for DAC	Analog Input	–	–
AVSS2	Supply for DAC	Analog Input	–	–
COMP1	Compensation Output for DAC	Analog Output	–	–
COMP2	Compensation Output for DAC	Analog Output	–	–
DIG_I[9:0]	Digital I Output	Output	4	HIGH
DIG_Q[9:0]	Digital Q Output	Output	4	HIGH
DIN[7:0]	Data Input	TTL Input	–	HIGH
DVALIDIN	Data Enable Input	TTL Input	–	HIGH
ERRORIN	Error Flag Input	TTL Input	–	LOW
FIFOALARM	FIFO Alarm Output	Output	4	HIGH
FIRSTOUT	Beginning of Sequence	Output	4	HIGH
FSTARTIN	Frame Start Input	TTL Input	–	HIGH
FSTARTOUT	Frame Start Output	Output	4	HIGH

Table 6.5 L64777 Pin Description Summary (Cont.)

Mnemonic	Description	Type	Drive (mA)	Active
FTMODE[2:0]	Functional Test Mode	Input w/Pulldown	–	HIGH
GND	Ground	Analog	–	–
ICLK	Input Clock	TTL Input	–	LOW/ HIGH
IDDTN	IDD Test	TTL Input w/Pullup	–	LOW
INT_n	Interrupt Request	Open Drain, Driving Low	4	LOW
IREF1	Reference Current Input	Analog Input	–	–
IREF2	Reference Current Input	Analog Input	–	–
NT_OUT	Nand Tree	Output	4	HIGH
OCLK	VCO Clock Output or External Clock Input	Bidirectional	–	LOW/ HIGH
PCLK	Clock Input for PLL Mode 2	TTL input	–	HIGH
PLL_MODE[1:0]	Select PLL Mode	Input w/Pulldown	–	HIGH
PLL_OUT_CS	PLL Current Source	3-state Current Source	4	3-state
QAM_I	Positive DAC Output I Channel	Analog Output	–	–
QAM_In	Negative DAC Output I Channel	Analog Output	–	–
QAM_Q	Positive DAC Output Q Channel	Analog Output	–	–
QAM_QN	Negative DAC Output Q Channel	Analog Output	–	–
RESET_n	Chip Reset	TTL Input	–	LOW
SB_BASE[1:0]	Serial Bus Base Address Selector	Input w/Pulldown	–	HIGH

Table 6.5 L64777 Pin Description Summary (Cont.)

Mnemonic	Description	Type	Drive (mA)	Active
SCAN_ENABLE	Scan Enable	TTL Input w/Pulldown	–	HIGH
SCL	Serial Control Line	Input (5 V-tolerant)	4	HIGH
SCLK	Symbol Clock Output	Output	4	LOW/ HIGH
SDA	Serial Data Access	Bidirectional (5 V-tolerant)	4	Open-drain
SSTARTIN	Sequence Start Input	TTL Input	–	HIGH
SYNCOK	Sync Detection Flag	Output	4	HIGH
TCK	JTAG Test Clock	TTL Input w/Pulldown	–	+[1]
TDI	JTAG Test Data In	TTL Input w/Pulldown	–	HIGH
TDO	JTAG Test Data Out	Output	4	HIGH
TMS	JTAG Test Mode Select	TTL Input w/Pulldown	–	HIGH
TNn	3-State Mode	TTL Input w/Pullup	–	LOW
TRSTn	JTAG Test Reset	TTL Input w/Pulldown	–	LOW
VDDX_I	Supply for Digital DAC Part	Analog Input	–	–
VDDX_Q	Supply for Digital DAC Part	Analog Input	–	–
VREF_I	Voltage Reference	Analog	–	–
VREF_Q	Voltage Reference	Analog	–	–

1. Also 5 V compatible.

6.2.2 Numerical Pin List for the L64777

Table 6.6 L64777 Numerical Pin List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VDD	1	PLL_MODE.0	31	TRSTN	61	VDD	91
VSS	2	PLL_MODE.1	32	VDD	62	VSS	92
QAM_I	3	IDDTN	33	TDO	63	NT_OUT	93
QAM_IN	4	TN	34	INT_N	64	VSS	94
AVDD1	5	RESET_N	35	VSS	65	SCAN_ENABLE	95
IREF1	6	VSS	36	VDD	66	FTMODE.0	96
COMP1	7	DIG_Q.0	37	FIFOALARM	67	FTMODE.1	97
VREF_I	8	DIG_Q.1	38	FIRSTOUT	68	FTMODE.2	98
AVSS	9	DIG_Q.2	39	SYNCOK	69	SB_BASE.0	99
VDDX_I	10	DIG_Q.3	40	FSTARTOUT	70	SB+BASE.1	100
VDDX_Q	11	DIG_Q.4	41	VSS	71	VSS	101
AVSS2	12	VSS	42	VDD	72	PCLK	102
VREF_Q	13	VDD	43	DIN.7	73	VSS	103
COMP2	14	DIG_Q.5	44	DIN.6	74	VDD	104
IREF2	15	DIG_Q.6	45	DIN.5	75	SCLK	105
AVDD2	16	DIG_Q.7	46	DIN.4	76	DIG_I.0	106
QAM_QN	17	DIG_Q.8	47	VDD	77	DIG_I.1	107
QAM_Q	18	DIG_Q.9	48	VSS	78	DIG_I.2	108
NC	19	VSS	49	VSS	79	DIG_I.3	109
GND	20	VSS	50	ICLK	80	DIG_I.4	110
NC	21	VDD	51	DIN.3	81	VDD	111
NC	22	OCLK	52	DIN.2	82	DIG_I.5	112
NC	23	VDD	53	DIN.1	83	DIG_I.6	113
NC	24	VSS	54	DIN.0	84	DIG_I.7	114
NC	25	VSS	55	VSS	85	DIG_I.8	115
VSS	26	TCK	56	VDD	86	DIG_I.9	116
PLL_OUT_CS	27	TDI	57	DVALIDIN	87	VDD	117
VDD	28	TMS	58	ERRORIN	88	VSS	118
VDD	29	VSS	59	FSTARTIN	89	SCL	119
NC	30	VDD	60	SSTARTIN	90	SDA	120

1. *NC* pins are not connected.

6.2.3 Alphabetic Pin List for the L64777

Table 6.7 L64777 Alphabetical Pin List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AVDD1	5	DIN.4	76	PLL_MODE.132		VDD77	
AVDD2	16	DIN.5	75	PLL_OUT_CS	27	VDD86	
AVSS	9	DIN.6	74	QAM_I	3	VDD91	
AVSS2	12	DIN.7	73	QAM_IN	4	VDD	104
COMP1	7	DVALIDIN	87	QAM_Q	18	VDD	111
COMP2	14	ERRORIN	88	QAM_QN	17	VDD	117
DIG_I.0	106	FIFOALARM	67	RESET_N	35	VDD	62
DIG_I.1	107	FIRSTOUT	68	SB+BASE.1	100	VDDX_I	10
DIG_I.2	108	FSTARTIN	89	SB_BASE.0	99	VDDX_Q	11
DIG_I.3	109	FSTARTOUT	70	SCAN_ENABLE	95	VREF_I	8
DIG_I.4	110	FTMODE.0	96	SCL	119	VREF_Q	13
DIG_I.5	112	FTMODE.1	97	SCLK	105	VSS	2
DIG_I.6	113	FTMODE.2	98	SDA	120	VSS	26
DIG_I.7	114	GND	20	SSTARTIN	90	VSS	36
DIG_I.8	115	ICLK	80	SYNCOK	69	VSS	42
DIG_I.9	116	IDDTN	33	TCK	56	VSS	49
DIG_Q.0	37	INT_N	64	TDI	57	VSS	50
DIG_Q.1	38	IREF1	6	TDO	63	VSS	54
DIG_Q.2	39	IREF2	15	TMS	58	VSS	55
DIG_Q.3	40	NC	22	TN	34	VSS	59
DIG_Q.4	41	NC	30	TRSTN	61	VSS	65
DIG_Q.5	44	NC	21	VDD	1	VSS	71
DIG_Q.6	45	NC	19	VDD	28	VSS	78
DIG_Q.7	46	NC	23	VDD	29	VSS	79
DIG_Q.8	47	NC	24	VDD	43	VSS	85
DIG_Q.9	48	NC	25	VDD	51	VSS	92
DIN.0	84	NT_OUT	93	VDD	53	VSS	94
DIN.1	83	OCLK	52	VDD	60	VSS	101
DIN.2	82	PCLK	102	VDD	66	VSS	103
DIN.3	81	PLL_MODE.0	31	VDD	72	VSS	118

1. *NC* pins are not connected.

6.3 Package Pinout

Figure 6.4 Package 120-Pin PQFP Pinout

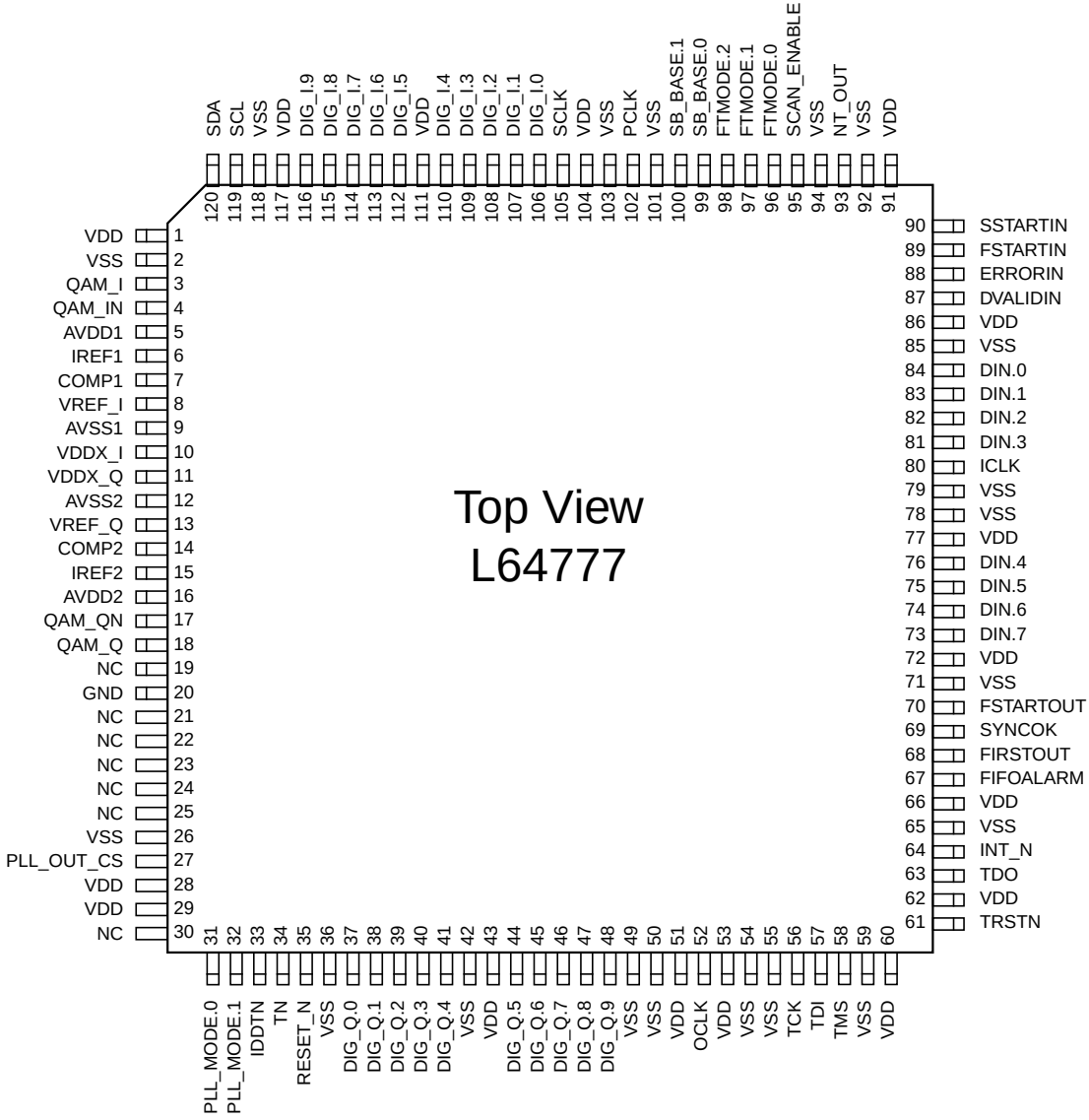
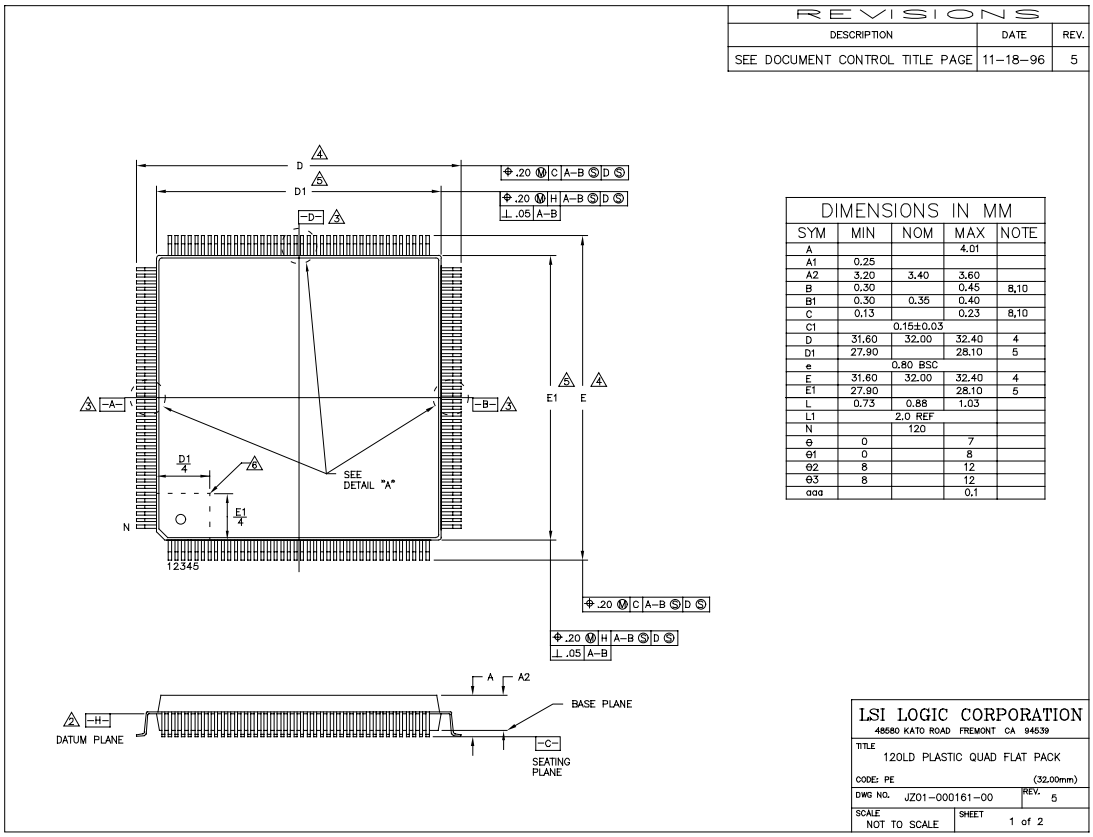


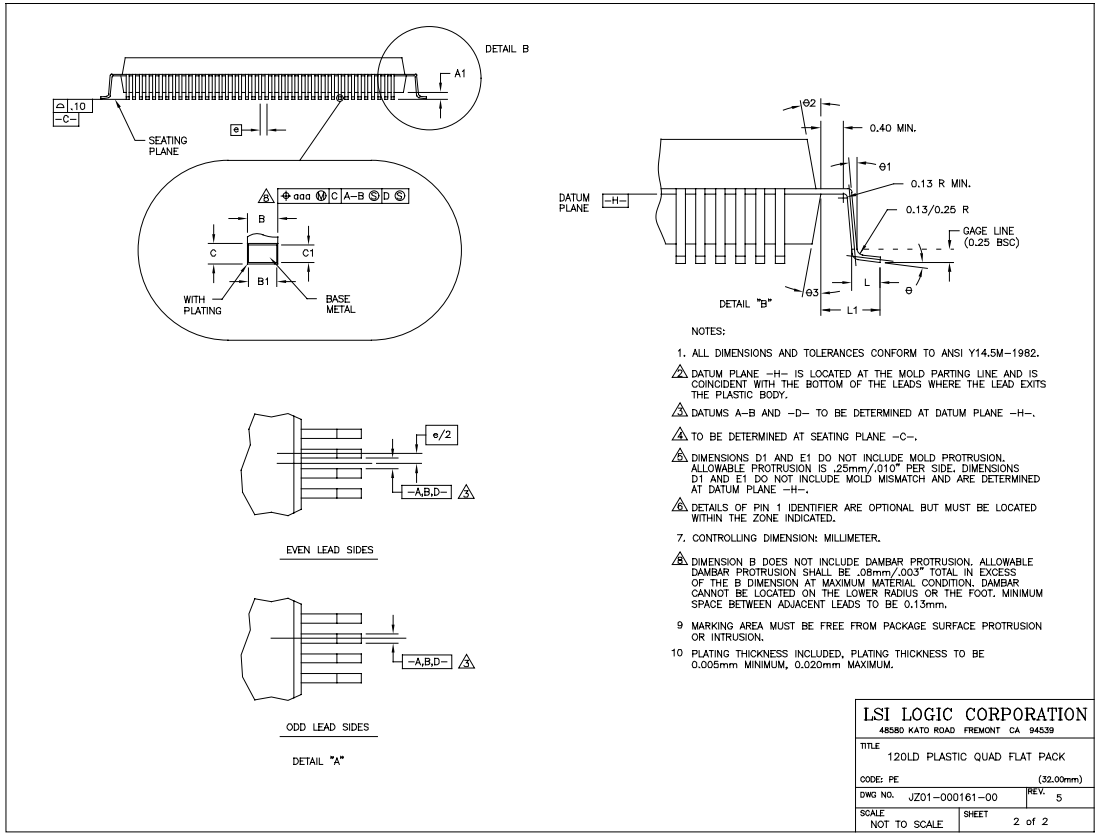
Figure 6.5 provides a mechanical drawing of the 120-pin PQFP for the L64777.

Figure 6.5 120-Pin PQFP (PE) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PE.**

Figure 6.5 120-Pin PQFP (PE) Mechanical Drawing (Cont.)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PE.**

Appendix A
Programming the L64777 in Serial Host Interface Mode

This appendix discusses how to program the L64777 internal registers and data tables in serial host interface mode. This chapter is intended primarily for system programmers who are developing software drivers using the serial bus.

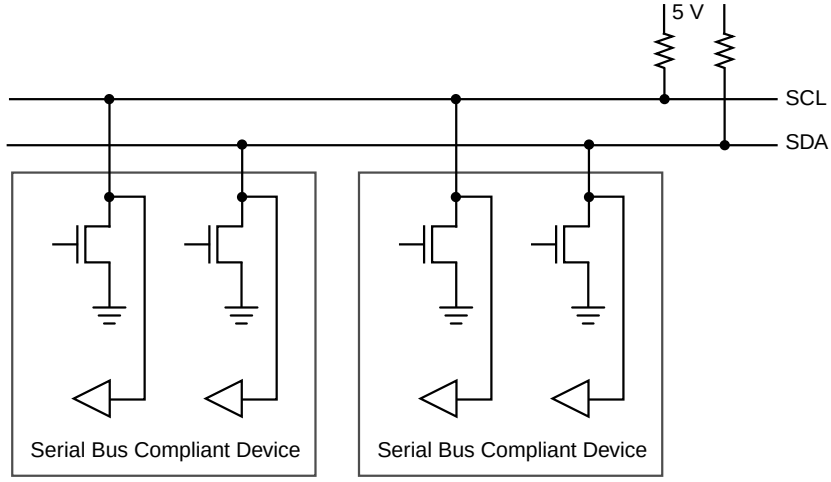
This appendix contains the following sections:

- Section A.1, “Serial Bus Protocol Overview,” page A-1, provides a high-level overview of the serial bus protocol.
- Section A.2, “Programming the Slave Address Using the Serial Bus Interface,” page A-4, shows how the slave address is formed and transmitted.
- Section A.3, “Write Cycle Using the Serial Bus Interface,” page A-4, shows an example of a serial bus write cycle.
- Section A.4, “Read Cycle Using the Serial Bus Interface,” page A-5, shows an example of a serial bus read cycle.
- Section A.5, “Limitations,” page A-7, shows the limitations of the L64777

A.1 Serial Bus Protocol Overview

The multimaster serial bus interface has two 1-bit lines—SDA (Serial Data) and SCL (Serial Clock)—that are connected to the bus as shown in Figure A.1. External pullup resistors hold the bus at a logic 1 value when the bus is not in operation.

Figure A.1 Quick Overview of the Serial Bus



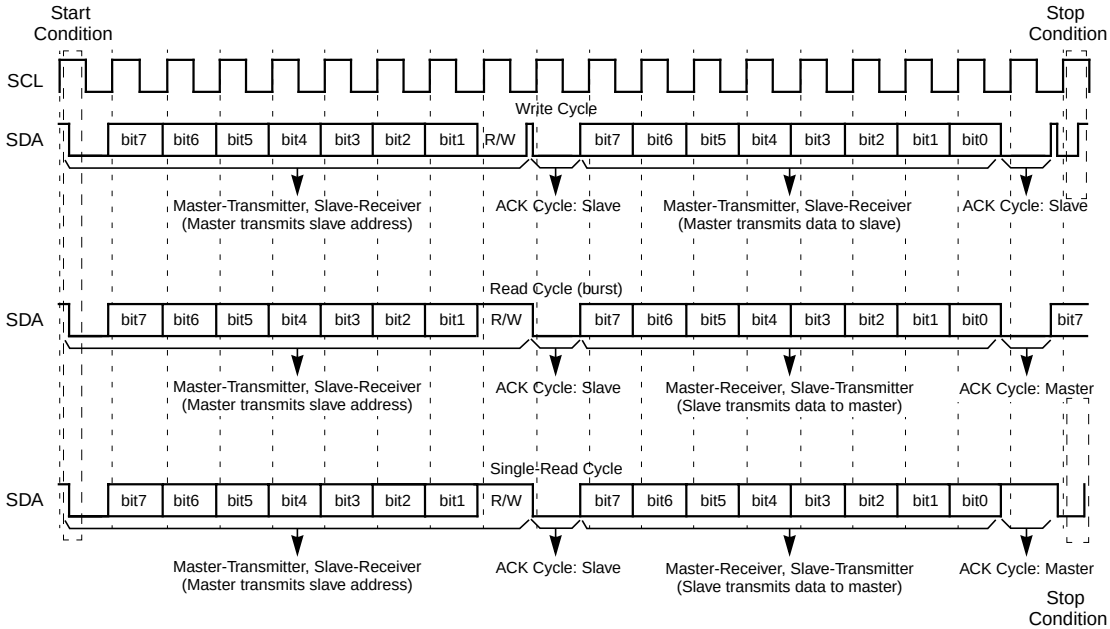
At the serial interface, data transfers on the SDA pin are synchronized to a serial clock input on the SCL line. The serial data clock can have a maximum frequency of 400 kHz. The pins SB_BASE[1:0] input the two LSB's of the slave address required by the serial bus protocol. The slave address definition is shown below:

7-Bit Slave Address for L64777 Serial Bus

1	1	0	1	0	SB_BASE1	SB_BASE0

The bus master always generates the clock and cycle start and stop conditions. Figure A.2 gives an overview of the read and write cycles using the serial bus protocol.

Figure A.2 Serial Bus Write/Read Cycle



Start Condition: The master (which drives the SCL) indicates the start of a cycle by pulling SDA to LOW when SCL is HIGH.

Stop Condition: The master (which drives the SCL) indicates the end of a cycle by releasing SDA to HIGH when SCL is HIGH.

Data Transfer: All data changes on the SDA line happen only when clock is LOW, except for the special cases outlined above to indicate cycle Start/Stop.

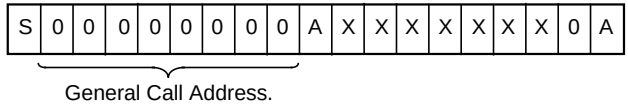
Acknowledge: The receiver always generates the acknowledge. In the case of a single read, the master-receiver does not generate an ACK so that it can generate the Stop condition (as indicated above).

A.2 Programming the Slave Address Using the Serial Bus Interface

A general call (master does a start condition followed by eight 0's) address is used to address every device on the serial bus. Any device that requires information to be supplied through this general call structure must acknowledge the cycle. The second byte has the following meaning when its LSB is 0 (see Figure A.3):

– 0b0000 0110 (0x6): Reset and write the programmable part of the slave address by hardware from the SB_BASE pins.

Figure A.3 General Call Structure



S: Start Condition
A: Acknowledge Cycle

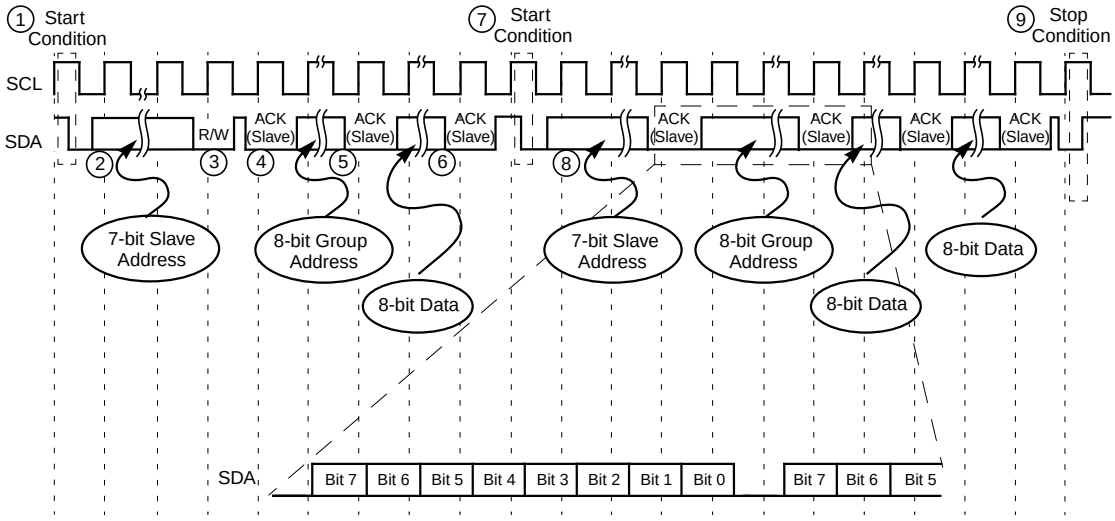
A.3 Write Cycle Using the Serial Bus Interface

Figure A.4 shows the timing for a burst, or a single-write cycle. The following cycles must take place for a write cycle:

1. The master starts the cycle with the start condition.
2. The master transmits the 7-bit slave address.
3. The master transmits an 8th bit (the R/W bit) = 0 to indicate a write cycle.
4. The addressed slave acknowledges the reception of the slave address by driving SDA low in the ACK cycle.
5. The master sends the 8-bit Group 0 address (0x0) to indicate that the Address Programming register (APR) is to be loaded. (The master accesses Group 0 only to load the APR.)
6. The master then sends the 8-bit data, which initializes the address pointer register (APR0).

7. The master generates another start condition.
8. The master repeats steps 2–7 to address the appropriate group and write 1 or more data bytes.
9. The master terminates the cycle by issuing a stop condition.

Figure A.4 Burst Write to Slave (Master-Transmitter, Slave-Receiver)



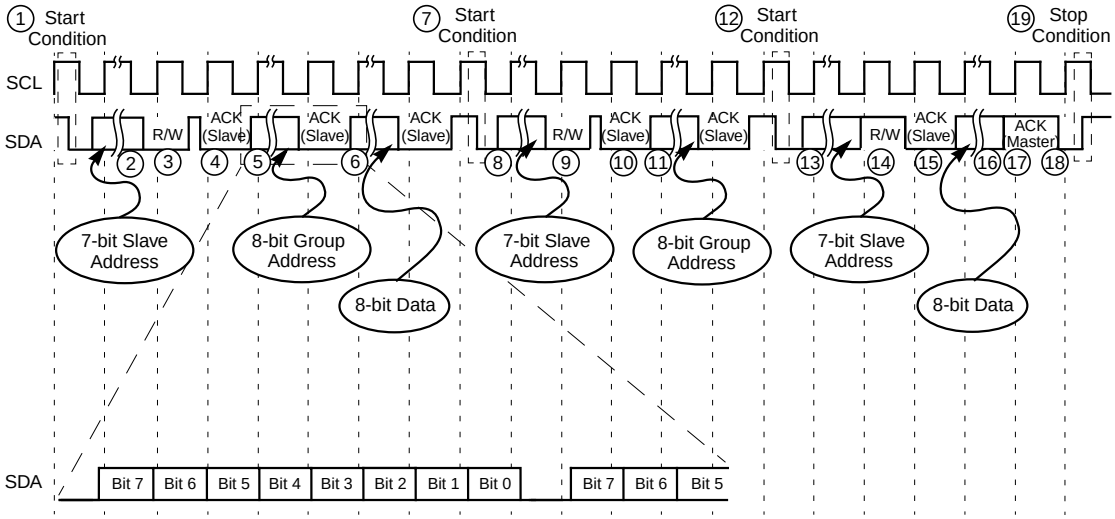
A.4 Read Cycle Using the Serial Bus Interface

Figure A.5 shows the timing for a burst, or a single read cycle. The following cycles must take place for a read cycle:

1. The master starts the cycle by issuing a start condition.
2. The master transmits the 7-bit slave address.
3. The master sets the R/W bit = 0 to indicate a write cycle.
4. The addressed slave acknowledges the reception of the slave address by driving SDA low in the ACK cycle.
5. The master sends the 8-bit Group 0 address (0x0) to indicate that the APR is to be loaded. (The master accesses Group 0 only to load the APR.)

6. The master then sends the 8-bit data, which initializes the base pointer (APR0/1).
7. The master repeats the start condition.
8. The master transmits the 7-bit slave address.
9. The master sets the R/W bit = 0 to indicate a write cycle.
10. The addressed slave acknowledges the reception by driving SDA LOW in the ACK cycle.
11. The master transmits the number of the group that it wishes to read, which the slave acknowledges.
12. The master issues another start condition.
13. The master transmits the 7-bit slave address.
14. The master sets the R/W bit = 1 to indicate a read cycle.
15. The slave drives SDA LOW to acknowledge.
16. The slave starts transmitting the data, MSB first.
17. The master has to provide the acknowledge by driving SDA LOW during the ACK cycle.
18. In the case of a single read, the master does not drive SDA LOW during the ACK cycle after reception of the first byte. The slave responds to this by relinquishing control of the bus and waiting for the master to issue a stop condition. For burst reads, the master drives SDA LOW for each byte it receives during the ACK cycle, except for the last byte.
19. The master terminates the cycle by issuing a stop condition.

Figure A.5 Single Read from Slave



A.5 Limitations

You can access the internal registers either in bursts or single-byte operation. You must access the status registers 12 and 13 as single-byte read or write.

After a stop condition, the user must program the APR to the desired next access address. Do not rely on the expected location after the last access.

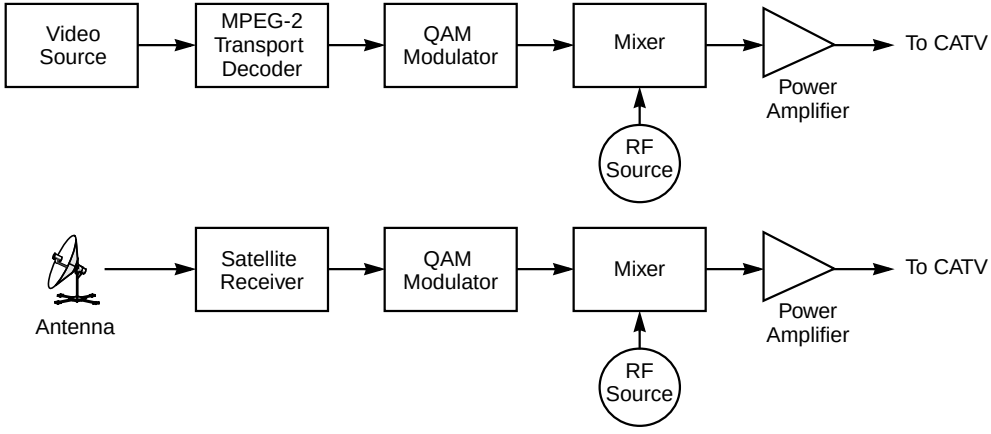
Appendix B
PLL Divider Settings and L64724/34 Connection

This appendix lists the PLL divider settings for typical applications. It also describes the L64777 connection to the L64724 and contains the following sections:

B.1 Overview

The QAM modulator is the last stage in a digital CATV transmitter system. Figure B.1 shows a block diagram of a typical CATV transmitter.

Figure B.1 CATV Block Diagram



The QAM modulator is programmed for its configuration and operational modes through the Serial Microprocessor interface. The L64777 synchronizes with the input data, derives the operating clock (based on the operational mode), carries out clock conversion with appropriate FIFO management, inserts the sync and error flags, and performs scrambling, RS encoding, and convolutional interleaving.

Signal frequencies at the symbol clock (SCLK) and operating clock (OCLK) outputs of the L64777 indicate appropriate locking of the internal timing system with respect to the incoming data rates when the input is from an MPEG source or the L64724 satellite receiver. The relationship among the SCLK, OCLK, and input data rate is described in the following subsections. If the same serial host controls both the L64724 and the L64777, hold the L64777 in reset until the L64724 PLL has been programmed.

B.2 PLL Driver Settings for Typical Applications

Table B.1 lists the L64777's PLL driver settings for Mode 1.

Table B.1 Typical Settings of CNT_I and CNT_O

ICLK in MHz	QAM mode	TS rate in Mbyte/s /Mbit/s	CNT_I (decimal)	CNT_O (decimal)	Frequency at Phase Comparator in MHz	OCLK in MHz
7.32	256	6.75/54.0	8	32	0.92	29.30
5.17	64	4.76/38.1	6	32	0.87	27.56
4.33	32	3.99/31.9	5	32	0.87	27.69
3.42	16	3.15/25.2	4	32	0.86	27.34

Note that the above settings assume a block length of 204 bytes with 16 invalid bytes and TS is the effective input rate attained, considering the number of cycles with valid data.

B.3 Connecting the L64777 to the LSI Logic L64724

The L64777 can be connected to the satellite receiver device L64724. The L64724 uses an interpolation-based digital receiver. Thus, it outputs a transport-rate byte clock with the granularity of the L64724 internal processing clock, PCLK. See the LSI Logic *L64724 Satellite Receiver Technical Manual* (April 2000).

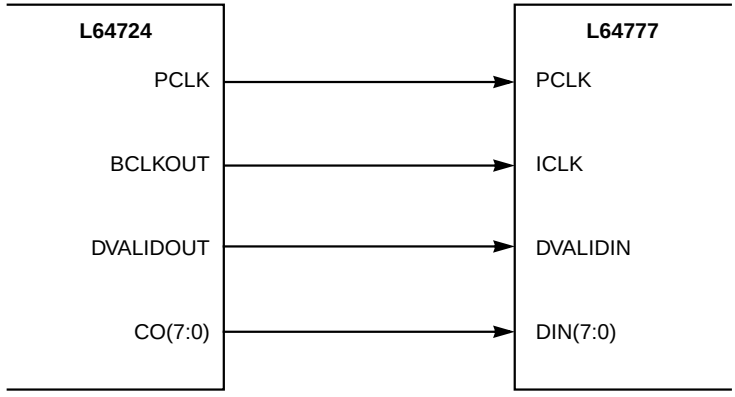
A digital NCO generates this byte clock, which consists of clock cycles having a length of k or k + 1 PCLK cycles. Usually, the rate of the byte clock is exactly that of the received transport stream rate.

To ease interfacing, the L64724 supports two modes of byte-clock generation. Mode 2 of the synchronous parallel interface (SPI) is best suited for interconnection with L64777. In this mode, the L64724 outputs 204-byte clock cycles, together with an indication for the 188 valid data bytes. Connect the byte clock to the ICLK input of the L64777, as a reference for generating the output sampling rate (OCLK); and connect the PCLK output of the L64724 to the PCLK input of L64777.

To keep the loop bandwidth as low as possible, L64777 provides a digital interpolation scheme and an NCO to lock to the byte clock in PLL mode 2.

Figure B.2 provides a simplified illustration of the signals between the L64724 and the L64777.

Figure B.2 Signals between the L64724 and L64777



When the input to the L64777 is from the L64724 for a satellite of selected center frequency and baud rate, the parameters to be programmed into the L64777 for 64 QAM are:

Operational Mode = NCO mode (Mode 2)

Block Length = 188 bytes

GAP = 16 bytes

I-Counter = 6 (0x6)

O-Counter = 32 (0x20)

After synchronization:

OCLK = Baud rate x 2 x 3/4 x oversampling x 1/(symbol size)

SCLK = OCLK/4

where:

oversampling = 4

symbol size = 6 for QAM mode of 64 (log of QAM level to base 2)

Note that the PLL_SET bit (Register 1) must be set before downloading any counter parameters, and it must be cleared after completion. This applies to Mode 2 programming.

Appendix C
Monitoring Device Internal Signals

The programming of the test register (14) allows monitoring of the device's internal signals. Depending on the programming of the test register bits (Register 15), the following signals are observable on the DIG_Q[9:0] pins:

TEST[3:0]

0b0000: Nyquist filter output or interpolator output (normal operation)
0b0001: FIFO output
0b0010: Scrambler output
0b0011: RS encoder output

0b0100: Interleaver output
0b0101: M-tuple output
0b0110: Mapper output
0b0111: N/A

0b1000: Interpolator control
0b1001: NCO step bit [23:16] on DIG_Q[7:0]
0b1010: NCO step bit [15:8] on DIG_Q[7:0]
0b1011: NCO step bit [7:0] on DIG_Q[7:0]

0b1100: Virtual FIFO content
0b1101: Value reserved; do not program
0b1110: Value reserved; do not program
0b1111: Value reserved; do not program

test.4: Set to 1 for power-down mode; after reset, this is 0
test.5: Set to 1 for power-down mode; after reset, this is 0
test.6: Set to 1 for power-down mode; after reset, this is 0

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