LSI LOGIC

Full Duplex

84C24

Quad 10Base-T Ethernet Media Interface Adapter

96200

Features

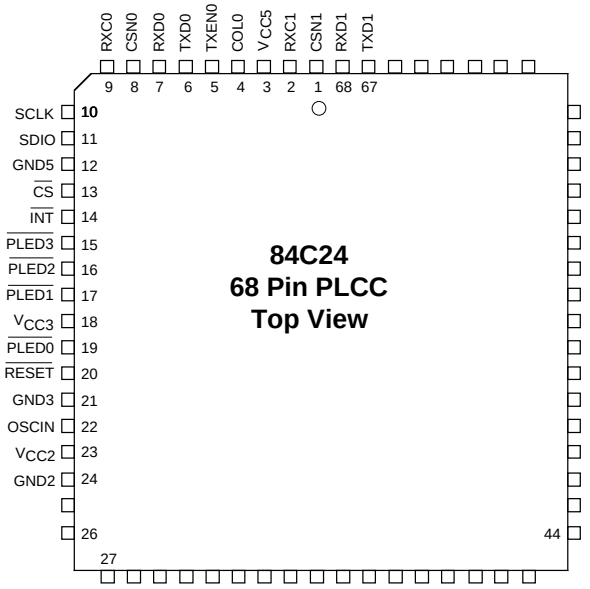
- Single Chip Interface Between Ethernet Controller And Twisted Pair Wire
- Four Independent Channels In One IC
- On Chip Wave Shaping And Filters - No External Filters Required
- Few External Components
- Meets All Applicable IEEE 802.3 and 10Base-T Standards
- Direct Interface To SEEQ, Intel, AMD, NSC Controllers
- Full/Half Duplex AutoNegotiation Per IEEE 802.3 Clause 28
- Many User Features And Options
  - Half/Full Duplex AutoNegotiation
  - Universal Controller Interface
  - Autopolarity
  - Smart Squelch
  - Transmit Level Adjust
  - Receive Level Adjust
  - 100/150 Ohm Cable
  - Powerdown
  - SQE Disable
  - Link Disable
  - Jabber Disable
  - Transmit Disable
  - Programmable LED Output
  - Loopback
- Status Outputs
  - Link
  - Polarity
  - Jabber
  - Full Duplex
  - AutoNegotiation
  - Interrupt
- LED Outputs
  - Link
  - Full Duplex
  - User Programmable
- Serial Port For Configuration And Status
- 68L PLCC

Note: Check for latest Data Sheet revision before starting any designs.

SEEQ Data Sheets are now on the Web, at www.lsilogic.com.

This document is an LSI Logic document. Any reference to SEEQ Technology should be considered LSI Logic.

Pin Configuration



84C24 Table of Contents

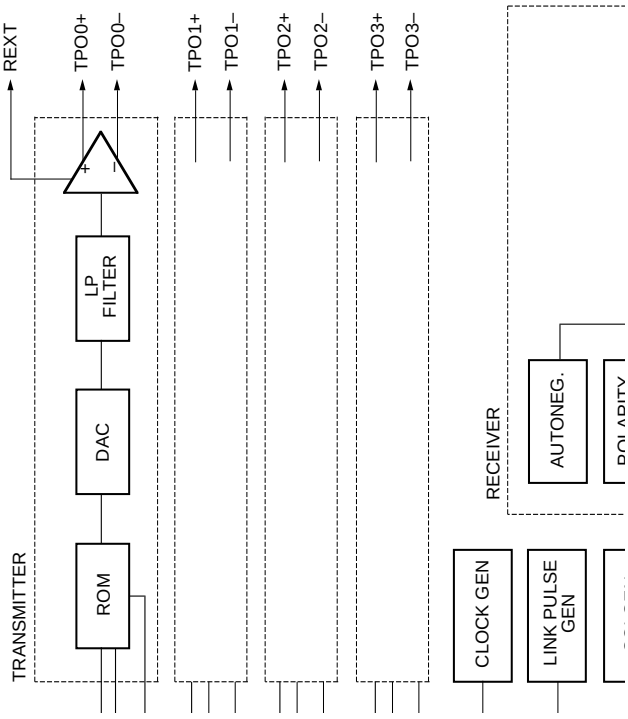
1.0 Pin Description

Pin	Pin Name	I/O	Description
45 47 59 3 55 18 23 25	V_{CC} 8 V_{CC} 7 V_{CC} 6 V_{CC} 5 V_{CC} 4 V_{CC} 3 V_{CC} 2 V_{CC} 1	—	**Positive Supply.** 5V ± 5%.
44 46 60 12 64 21 24 26	GND 8 GND 7 GND 6 GND 5 GND 4 GND 3 GND 2 GND 1	—	**Ground.** 0 Volts.
42 38 33 29	TPO 3+ TPO 2+ TPO 1+ TPO 0+	O	**Twisted Pair Transmit Output, Positive.**
43 39 34 30	TPO 3– TPO 2– TPO 1– TPO 0–	O	**Twisted Pair Transmit Output, Negative.**
40 36 31 27	TPI 3+ TPI 2+ TPI 1+ TPI 0+	I	**Twisted Pair Transmit Input, Positive.**
41 37 32 28	TPI 3 – TPI 2 – TPI 1 – TPI 0 –	I	**Twisted Pair Transmit Input, Negative.**
35	REXT	O	**Transmit Current Set.** An external resistor connected between this pin and GND will set the output current supplied on TPO[3:0]±.
51	TXC	O	**Transmit Clock Output.** This controller interface output provides a 10 Mhz clock to the controller. Transmit data from the controller on TXD is clocked in on edges of TXC and OSCIN.
49 57 66 5	TXEN 3 TXEN 2 TXEN 1 TXEN 0	I	**Transmit Enable Input.** This controller interface input has to be asserted when data on TXD is valid.
50 58 67 6	TXD 3 TXD 2 TXD 1 TXD 0	I	**Transmit Data Input.** This controller interface input contains data to be transmitted on the TP transmit output and is clocked in on edges of TXC and OSCIN.

Pin Description (continued)

Pin	Pin Name	I/O	Description
54 63 2 9	RXC 3 RXC 2 RXC 1 RXC 0	O	**Receive Clock Output.** This controller interface output provides a 10 Mhz clock to the controller. Receive data on RXD is clocked out to the controller on edges of RXC.
53 62 1 8	CSN 3 CSN 2 CSN 1 CSN 0	O	**Carrier Sense Output.** This controller interface output is asserted when valid data is present on the RXD output.
52 61 68 7	RXD 3 RXD 2 RXD 1 RXD 0	O	**Receive Data Output.** This controller interface output contains receive data from the TP input and is clocked out on edges of RXC.
48 56 65 4	COL 3 COL 2 COL 1 COL 0	O	**Collision Output.** This controller interface output is asserted when collision between transmit and receive data occurs.
22	OSCIN	I	**Clock Oscillator Input.** There must be either a 10 Mhz crystal or a 10 Mhz clock tied between this pin and GND. TXC output is generated from this input.
15 16 17 19	$\overline{\text{PLED}}$ 3 (SA3) $\overline{\text{PLED}}$ 2 (SA2) $\overline{\text{PLED}}$ 1 (SA1) $\overline{\text{PLED}}$ 0 (SA0)	I/O Open Drain Pullup	**Programmable LED Outputs/Serial Port Address Inputs.** These pins are normally outputs and can be programmed through the serial port to be either a Link Pulse Detect Ouput, Full Duplex Detect Output, or user select output. These pins can drive an LED from V_{CC}. During powerup or reset, these are inputs and the value on these pins is latched in and used as the serial port device address.
13	$\overline{\text{CS}}$	I	**Serial Port Chip Select Input.** This pin enables the serial port for I/O operation.
10	SCLK	I	**Serial Port Clock Input.** This clock shifts serial port data into SDIO on falling edges and out of SDIO on falling edges.
11	SDIO	I/O	**Serial Port I/O Data.** This bidirectional pin contains serial port data that is clocked in and out on falling edges of SCLK.
14	$\overline{\text{INT}}$	O Open Drain Pullup	**Serial Port Interrupt Output.** This output is asserted whenever there is a change in certain serial port read bits, and deasserted after these bits are read. This pin consists of an open drain output transistor with a resistor pullup.
20	$\overline{\text{RESET}}$	I Pullup	**Reset Input.** 1 = Normal 0 = Device In Reset State

2.0 Block Diagram



3.0 Functional Description

3.1 INTRODUCTION

The 84C24 is a highly integrated analog interface IC's for twisted pair Ethernet applications (10Base-T).

The 84C24 consists of four (4) separate and independent channels, each consisting of: Manchester encoder, twisted pair transmitter with wave shaping and on chip filters, twisted pair transmit output driver, twisted pair receiver with on chip filters, Manchester decoder, and controller interface. The 84C24 also has a serial port to set configuration inputs and read status outputs for each channel.

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters and common mode chokes normally required in 10Base-T applications.

The 84C24 is ideal as a media interface for 10Base-T switching hubs, routers, bridges, servers, and other multiport devices.

3.2 GENERAL

The 84C24 has four independent 10Base-T Media Interface Adapter channels. Each channel has six main sections: controller interface, Manchester encoder, Manchester decoder, twisted pair transmitter, twisted pair receiver, and collision sense. There is also a serial port and a crystal oscillator that is common to all four channels.

On the transmit side, NRZ data is received on the controller interface from an external controller. The data is then sent to the Manchester encoder for formatting. The Manchester encoded data is then sent to the TP transmitter. The TP transmitter is composed of a waveform generator that preshapes the output, a filter to remove high frequency components, and an output driver to drive the 100 ohm twisted pair cable. In addition, the transmitter generates link pulses, start of idle (SOI) pulses, and detects the jabber condition.

On the receive side, the twisted pair receiver receives incoming Manchester encoded data from the twisted pair cable, removes high frequency noise from the input, determines if the input signal is a valid packet, and then converts the data from twisted pair levels to internal digital levels. The twisted pair receiver also detects link pulses, detects start of idle (SOI) pulses, detects and corrects for reverse polarity on the twisted pair inputs, implements a squelch algorithm to reject invalid signals, and detects and enables Full Duplex operation. The output of the twisted pair receiver then goes to the Manchester encoder which recovers a clock from the TP data stream, recovers the data, and converts the data back to NRZ. The NRZ data is then transmitted to an external controller through the controller interface.

The crystal oscillator generates a master clock for the device. The serial port is a bidirectional port through which configuration inputs can be set and status outputs can be read out.

Each block plus the operating modes are described in more detail in the following sections. A block diagram of the 84C24 is shown in Figure 1.

3.3 CONTROLLER INTERFACE

The 84C24 can directly connect, without any external logic, to Ethernet controllers manufactured by SEEQ, Intel, NSC, and AMD. The selection of controller interface type is done by setting the controller interface select bits in the serial port Global Configuration register.

The controller interface signal pins are transmit data (TXD), transmit clock (TXC), transmit enable (TXEN), receive data (RXD), receive clock (RXC), carrier sense (CSN), collision (COL).

On the transmit side, when TXEN is deasserted, no data is transmitted. When TXEN is asserted, data on TXD is clocked into the device on the edges of the TXC output clock. Since OSCIN input clock generates the TXC output clock, TXD data is also clocked in on edges of OSCIN.

On the receive side, when invalid data is sensed on the TP inputs, the receiver is idle. During idle, CSN is deasserted, RXD is held either low (SEEQ, NSC) or high (Intel, AMD), and RXC either follows TXC (Seeq) or is held low (Intel, AMD, NSC). When a valid packet is detected on the TP receive inputs, CSN is asserted and the clock recovery process starts on the incoming data. After the receive clock has been recovered from the data, RXC is either switched from TXC to the recovered data clock (SEEQ mode) or RXC is switched from low to the recovered data clock (Intel, AMD, NSC). The recovered NRZ data is clocked out on RXD on edges of the RXC clock. When the end of packet is detected on the TP input, CSN is deasserted. After CSN deassertion, RXC is either switched over to TXC (SEEQ) or held low (Intel, AMD, NSC).

The collision output, COL, is asserted whenever the collision condition is detected.

The output pin $\overline{PLED}$ can be configured to be a Full Duplex output by appropriately setting the programmable LED output select bits in the serial port Global Configuration register. A Full Duplex Detect status bit is also available in the serial port Channel Status register.

3.4 MANCHESTER ENCODER

Manchester encoding is the process of combining the clock and data together into one serial stream to be transmitted onto the twisted pair wire. To Manchester encode data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. This guarantees that a transition always occurs in the middle of the bit cell. Manchester encoding of the data from TXD occurs only when TXEN is asserted.

3.5 MANCHESTER DECODER

Manchester decoding is the process of extracting clock and data from a Manchester encoded data stream. In Manchester encoded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data.

Clock recovery is done with a PLL. When valid data is not detected on the receive input, the 10 MHz TXC clock is applied to the input of the PLL. When valid data is detected on the TP receive input, the PLL input is switched to the incoming data. The PLL then recovers the clock by locking onto zero crossings of the incoming signal from the twisted pair wire. The recovered RXC clock frequency is 10 MHz. The PLL can lock onto the preamble signal in less than 12 transitions (bit times) and can reliably perform the data recovery process with up to ±13.5 nS of jitter on the TP input. While the PLL is in the process of locking onto the preamble signal, some of the preamble data symbols are lost. The clock recovery process recovers enough preamble data symbols to pass at least 5 bytes of preamble to the receive controller interface.

Data recovery is done by latching in data from the receiver with the recovered clock extracted by the PLL.

3.6 TWISTED PAIR TRANSMITTER

3.6.1 Transmitter

The transmitter consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM outputs; the ROM outputs are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Section 14 and also shown in Figure 2. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the preshaped and smoothed waveform to a current output that can drive 0-100 meters of 100 ohm UTP or 150 ohm STP twisted pair cable tied directly to pins TPO± without any external filters. During the idle period, no output signal is transmitted on TPO± (except link pulse).

3.6.2 Transmit Level Adjust

The transmit level can be adjusted with three transmit level adjust bits in the serial port Global Configuration register as shown in Table 1. The adjustment range is -18% to +24% in 6% steps.

The 84C24 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications.

3.6.3 Transmit Disable

The TP transmitter can be disable by setting the transmit disable bit in the serial port Channel Configuration register. When disabled, the TP transmitter is forced into the idle state with link pulses not transmitted, even if TXEN is asserted.

Table 1. Transmit Level Adjust

TLVL3-1	Gain
000	1.24
001	1.18
010	1.12
011	1.06
100	1.00
101	0.94
110	0.88
111	0.82

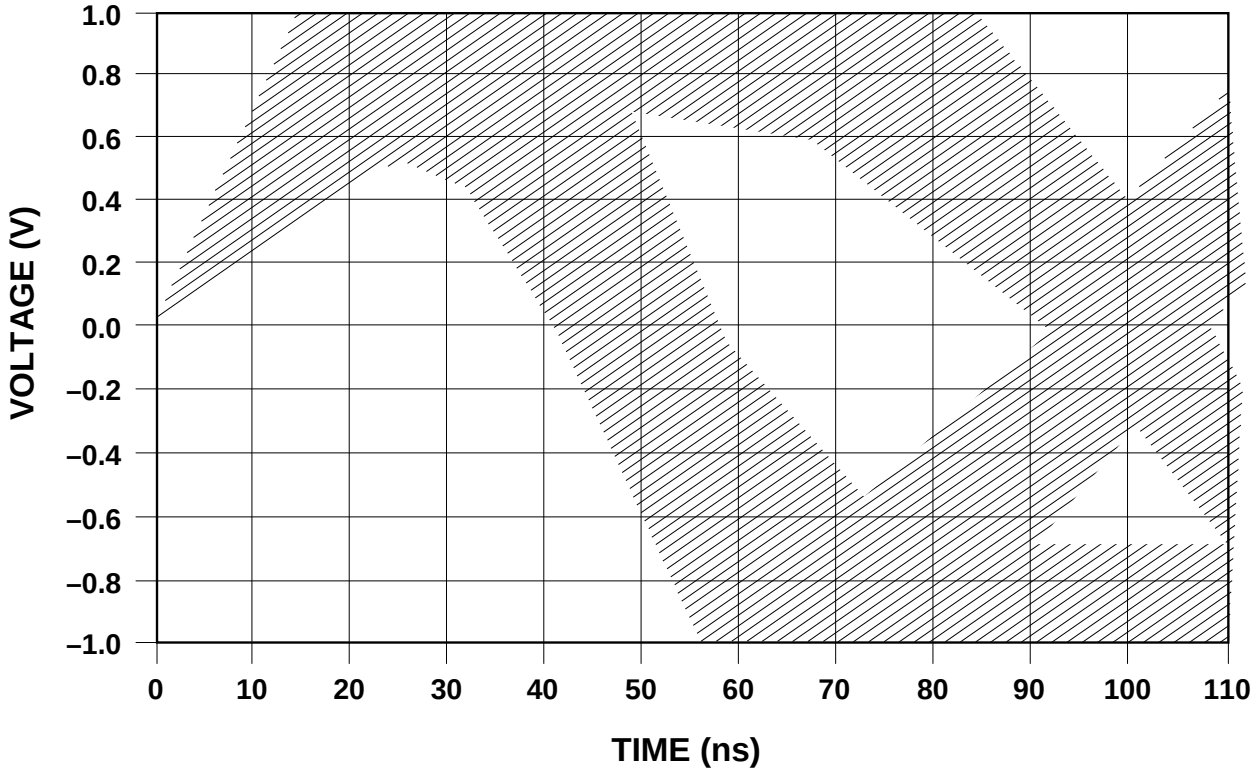


Figure 2. TP Differential Output Voltage Template

3.6.4 STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 ohm shielded twisted pair (STP) cable. When STP mode is enabled, the output current is reduced by the ratio of 100/150 in order to keep the amplitude of the transmit signal unchanged from the specified transmit levels and template. The STP mode can be selected through the cable type select bit in the serial port Global Configuration register.

3.7 TWISTED PAIR RECEIVER

3.7.1 Receiver

The TP receiver is able to detect input signals from the twisted pair cable that are within the template shown in Figure 3.

The TPI± inputs are internally biased to V_{CC}/3 by internal bias resistors. The TPI± inputs pass through a low pass filter designed to eliminate high frequency noise on the input.

The receive filter output then goes to two different types of receive comparators, threshold and zero crossing. The threshold comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid data. The output of the threshold comparator is used for squelch, link pulse detect, SOI detect, reverse polarity detect, and Full Duplex detect. The output of the zero crossing comparator is used for data recovery.

3.7.2 Squelch

The threshold comparator compares the TPI± inputs against fixed positive and negative thresholds, called squelch levels. If the input voltage to the threshold comparator exceeds the squelch levels for three bit times with alternating polarity within a 100-250 ns interval, the data is considered to be valid and the receiver now enters into the unsquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. While in the unsquelch state, the receive squelch circuit looks for SOI (Start Of Idle) pulse at the end of a packet. When the SOI signal is detected, the receive squelch is turned on again. The receiver meets the squelch requirements defined in IEEE 802.3 Section 14.

3.7.3 Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the serial port Channel Configuration register. By setting this bit, the device can support cable lengths exceeding 100 meters.

3.8 SOI (Start of Idle)

The SOI pulse is a positive pulse inserted at the end of every transmitted packet on the twisted pair wire to indicate the end of transmission and the start of idle.

The TP transmitter generates an SOI pulse at the end of data transmission when TXEN is deasserted. The TP transmitted SOI output pulse is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Section 14 and shown in Figure 4.

The TP receiver detects the SOI pulse by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CSN is deasserted.

3.9 LINK INTEGRITY & AUTONEGOTIATION

3.9.1 General

The 84C24 can be configured to implement either the IEEE 802.3 Clause 14 10Base-T link algorithm for link integrity or the IEEE 802.3 Clause 28 Link Signaling algorithm for both link integrity and AutoNegotiation of Full or Half Duplex operation with a remote device. The choice of either standard 10Base-T link algorithm or AutoNegotiation link algorithm is made by setting the AutoNegotiation enable bit in serial port Global Configuration register. Per the IEEE specification, the 84C24 can interoperate with a remote device that does not implement the IEEE 802.3 Clause 28 AutoNegotiation algorithm as long as the remote device has the 10Base-T link integrity algorithm.

3.9.2 10Base-T Link Integrity Algorithm

The transmit and receive 10Base-T algorithms are the same as defined in IEEE 802.3 Clause 14. The 10Base-T algorithm uses normal link pulses, or NPL's to establish link integrity. The transmit link pulse meets the template defined in IEEE 802.3 Clause 14 and shown in Figure 5. Refer to the IEEE 802.3 Clause 14 section on Link Integrity for more details.

3.9.3 AutoNegotiation Algorithm

The transmit and receive AutoNegotiation algorithms are the same as defined in IEEE 802.3 Clause 28. The AutoNegotiation algorithm uses a burst of link pulses, called fast link pulses (FLP), to pass up to 16 bits of signaling data back and forth between the 84C24 and a remote device. The transmit FLP's meet the template defined in IEEE 802.3 Clause 14 and shown in Figure 5. A timing diagram contrasting NLP's and FLP's is shown in Figure 6. Each of the four channels on the 84C24 has an independent and separate AutoNegotiation state machine.

In the 84C24 the FLP's are used to advertise either Full or Half Duplex capability to a remote device. The 84C24 Full and Half Duplex advertisement capabilities are programmed by setting the duplex select bits in the serial port Channel Configuration registers.

The AutoNegotiation algorithm is initiated when any of the following events occurs: (1) Powerup, (2) device reset, (3) AutoNegotiation reset, (4) device enters Link Fail State, or (5) AutoNegotiation enable bit is set. Once the negotiation process is completed, the 84C24 configures itself for either Full or Half Duplex Operation, depending on the outcome of the AutoNegotiation. The result of the AutoNegotiation process for each channel is stored in the duplex detect bits in the serial port Channel Status Registers. When the AutoNegotiation process is completed, the 84C24 switches back to the 10Base-T link integrity algorithm with NLP's.

The status of the negotiation process for each channel can be viewed by reading the AutoNegotiation status bits in the serial port Channel Status registers.

The AutoNegotiation algorithm embedded inside the 84C24 is more complicated than stated above. If more details are needed, refer to IEEE 802.3 Clause 28.

3.9.4 Link Indication

The receive link detect status is available as a bit in serial port Channel Status register and it can also be programmed to appear on the PLED[3:0] pins if the programmable LED output select bits are set appropriately in the Global Configuration register. When PLED[3:0] pins are programmed as link pulse detect outputs, they are individually asserted low when that channel is in the Link Pass State. The PLED[3:0] outputs are open drain with resistor pullups and can drive and LED from V_{CC} or can drive another digital input.

3.9.5 Link Disable

The link pulse function can be disabled for each channel by setting the link disable bit in the serial port Channel Configuration registers. When the link pulse function is disabled for that channel, the device ignores the reception of link pulses, stays in the Link Pass State, continues to transmit NLP's and configures itself for Full or Half Duplex based on the value of the duplex select bits in the serial port Channel Configuration registers.

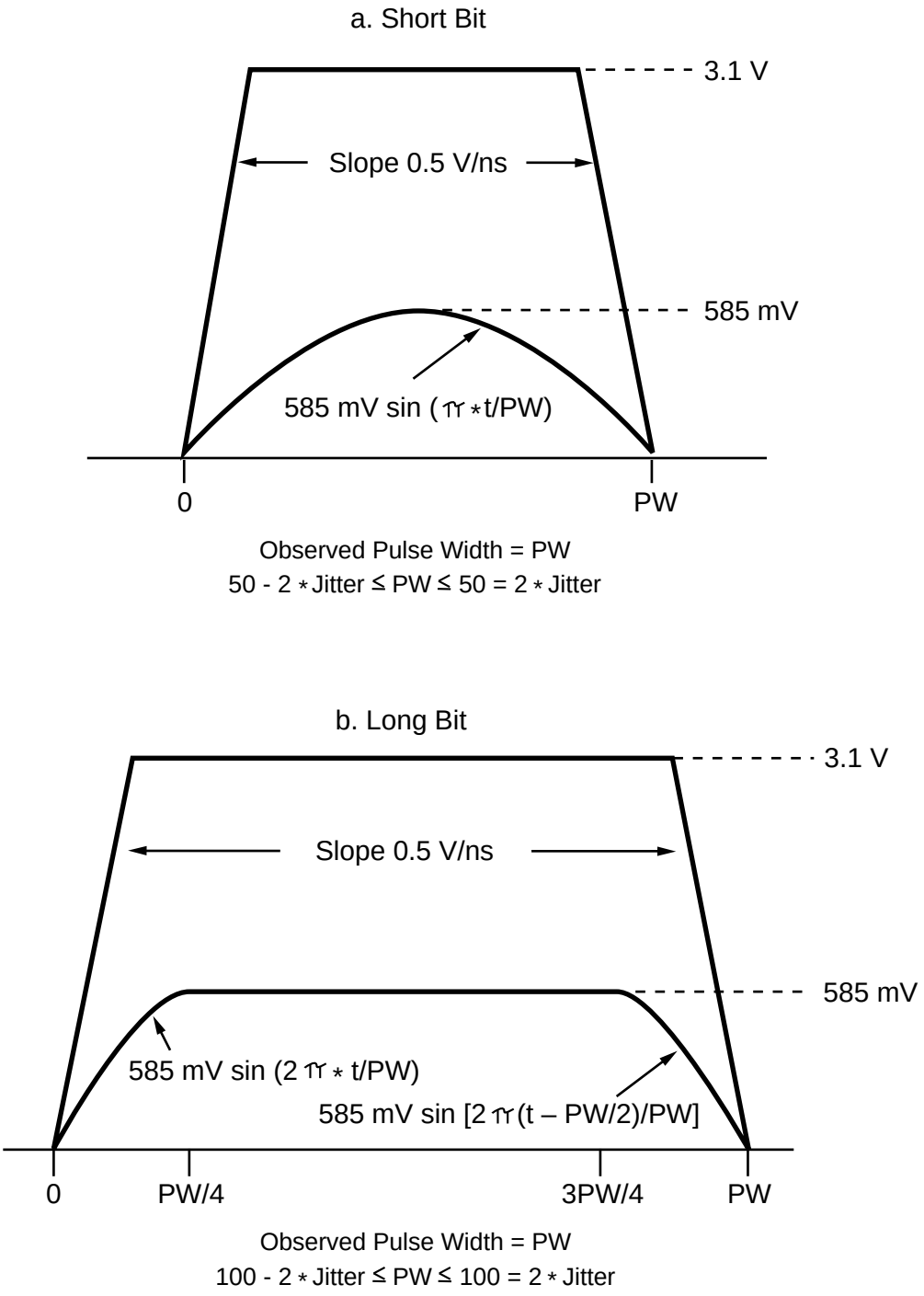


Figure 3. Receive Differential Input Voltage Template

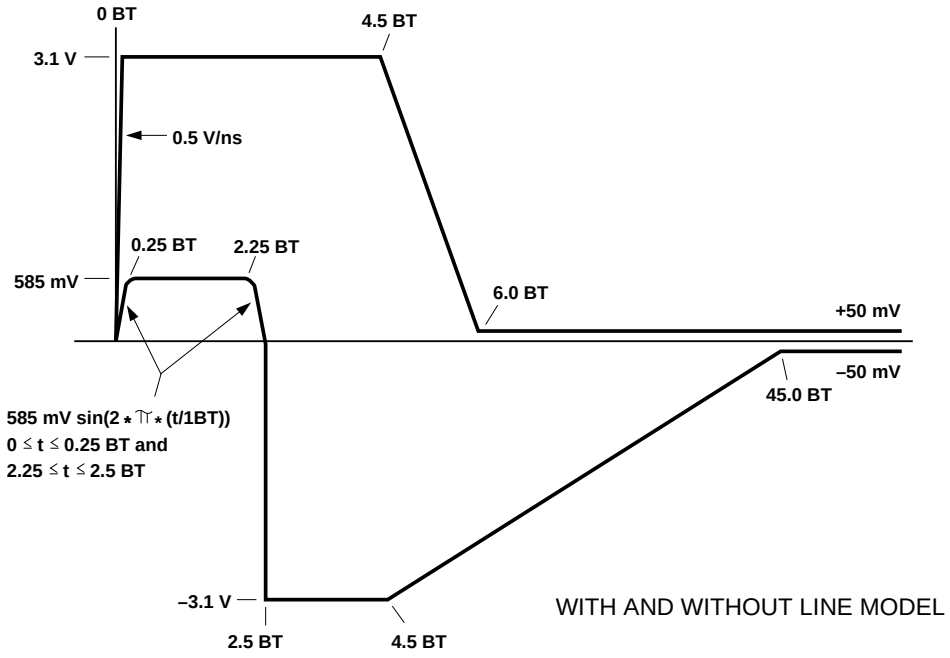


Figure 4. SOI Output Voltage Template

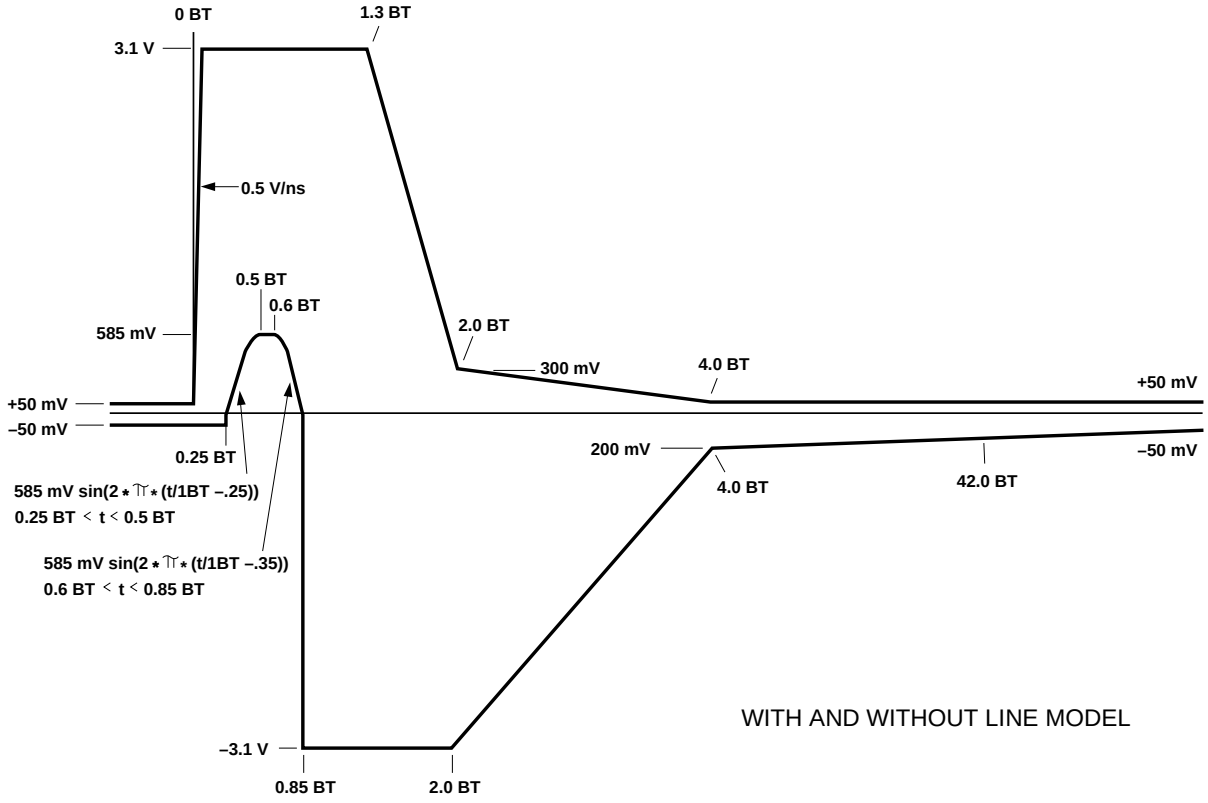


Figure 5. Link Pulse Output Voltage Template

3.10 COLLISION

Collision occurs whenever transmit and receive occur simultaneously on TPO± outputs and TPI± inputs. COL is asserted when collision occurs. COL is also asserted when the jabber condition has been detected and when the SQE test is performed. Collision function is disabled if the device is in the Link Fail State or Full Duplex mode.

3.11 SIGNAL QUALITY ERROR (SQE)

The controller interface connection is continually tested by transmitting a 1 µs collision pulse on the collision output, COL, after each transmit packet. This is known as the signal quality error (SQE) test.

The SQE test is disabled when the device is in the Link Fail state or when jabber is detected. SQE test can also be enabled by setting the SQE enable bit in the serial port Global Configuration register. See the Serial port section for more details.

3.12 JABBER

Jabber condition occurs when the transmit packet exceeds its maximum allowable length. When jabber is detected, the transmit outputs on TPO± are forced to the idle state, collision is asserted, and the jabber detect bit is set in the serial port Channel Status register. In addition, jabber function can be disabled by setting a jabber disable bit in the serial port Global Configuration register.

3.13 RECEIVE POLARITY CORRECTION

The polarity of the signal on the receive input twisted pair pins , TPI±, is continuously monitored. If either 3 consecutive SOI or 3 consecutive link pulses indicate incorrect polarity on TPI±, the polarity is internally determined to be incorrect. If reverse polarity is detected, the reverse polarity detect bit is set in the serial port Channel Status register.

The 84C24 will automatically correct for the reverse polarity condition with the autopolarity feature. Autopolarity can be disabled by setting the autopolarity disable bit in the serial port Global Configuration register.

3.14 FULL DUPLEX MODE

Full Duplex mode allows transmission and reception to occur simultaneously. When Full Duplex mode is enabled, collision is disabled, internal loopback is disabled, and SQE pulse is disabled.

The device can be forced into the Half or Full Duplex mode, or the device also can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

The device can be forced into the Full or Half Duplex modes by setting the duplex bits in the serial port Channel Configuration register.

The device can automatically configure itself for Full or Half Duplex modes by using the AutoNegotiation scheme to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. All of this is described in gruesome detail in the Link Integrity And AutoNegotiation section. AutoNegotiation can be enabled by setting the AutoNegotiation enable bit in the serial port Global Configuration register.

Full Duplex detect status output bit is available in the serial port Channel Status register and it can also be programmed to appear on the $\overline{PLED[3:0]}$ pin by setting the programmable LED output select bits in the serial port Global Configuration register. When $\overline{PLED[3:0]}$ is programmed as Full Duplex detect output, it is asserted low when the device is in the Full Duplex mode, either forced or autodetected. The $\overline{PLED[3:0]}$ output is open drain with resistor pullup and can drive an LED from V_{CC} or can drive another digital input.

3.15 LOOPBACK

In order to emulate coax Ethernet behavior, transmitted data on TPO± is normally internally looped back onto the receive section and sent out on the receive controller pins RXD, CSN, and RXC as if it was a regular received packet. The loopback function is disabled if the device is in the Link Fail State, jabber condition, or in Full Duplex mode.

Diagnostic loopback can be implemented by disabling the transmitter and sending a transmit packet. The transmitter can be disabled by setting the transmit disable bit in the serial port Channel Configuration register.

3.16 RESET

The 84C24 can be reset by setting the reset bit in the serial port Global Configuration register, by asserting the $\overline{RESET}$ pin active low, or by applying V_{CC} to the device.

When the reset bit is set, an internal powerup reset pulse is generated which resets all internal timers and state machines and forces the serial port bits to their default values. After the powerup reset pulse has finished, the reset bit in the serial port Global Configuration register is cleared.

When the reset pin $\overline{RESET}$ is forced low, all internal timers and state machines are reset and the serial port bits are forced to their default values. After the $\overline{RESET}$ pin is let go or forced high, the device returns to normal operation.

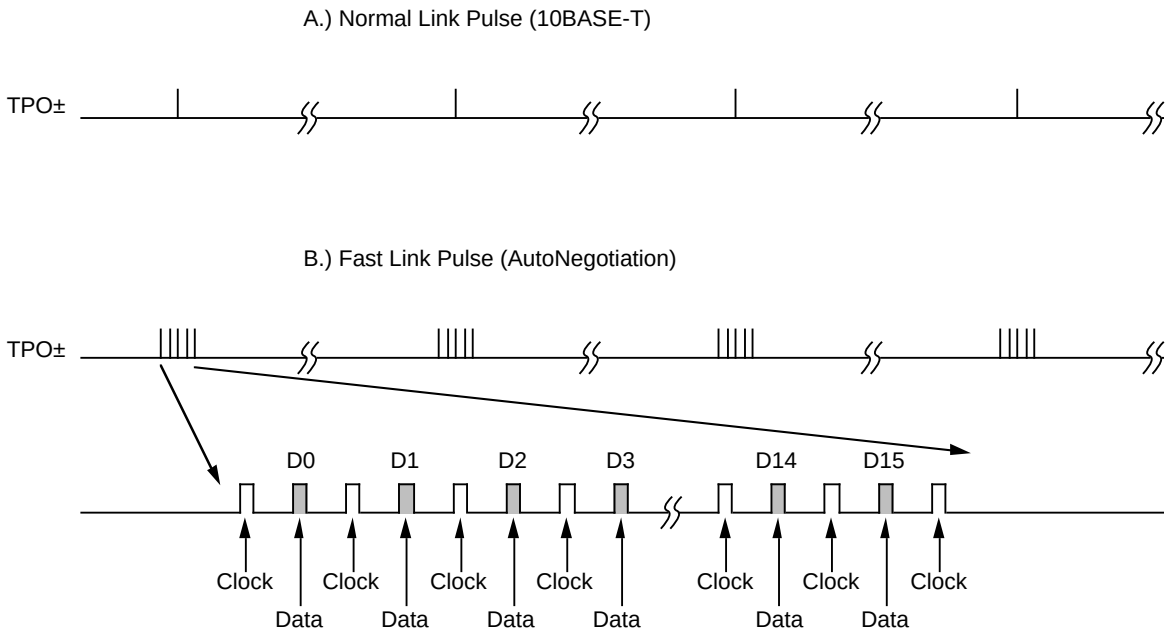


Figure 6. NLP vs. FLP Link Pulse

3.17 POWERDOWN

The 84C24 can be powered down by setting the power-down enable bit in the serial port Global Configuration register. In powerdown mode, the outputs are tristated and the power consumption is reduced to less than 0.5 mW.

3.18 OSCILLATOR

The 84C24 requires a 10 Mhz reference frequency for internal signal generation. This 10Mhz reference frequency is generated by either connecting an external crystal between OSCIN and GND or an external 10 MHz clock to OSCIN. TXC output is synchronized to the OSCIN clock Input.

3.19 LED DRIVERS

The $\overline{PLED[3:0]}$ pins contain an open drain output transistor with a resistor pullup. These outputs can drive LED's tied to V_{CC} or other digital inputs.

The $\overline{PLED[3:0]}$ pins can be programmed to perform one of five different functions: (1) Link Detect, (2) Full Duplex Detect, (3) On, (4) Off, or (5) Blink.

The $\overline{PLED[3:0]}$ pins can be programmed for one of these 5 functions by appropriately setting the LED output select bits in the Global Configuration and Channel Configuration registers. When the $\overline{PLED[3:0]}$ pins are programmed to indicate Link or Full Duplex, the LED output drivers are controlled by the internal logic as described in the Link Integrity and Full Duplex section. When $\overline{PLED[3:0]}$ are programmed to be On, the LED output goes low, thus turning on the LED. When PLED[3:0] is programmed to be Off, the LED output driver turn off, thus turning off the LED. When $\overline{PLED[3:0]}$ is programmed to Blink, the LED output driver will continuously turn on and turn off at a rate of 100 ms on, 100 ms off.

3.20 SERIAL PORT

3.20.1 Signal Description

The serial port has eight pins: SCLK, SDIO $\overline{INT}$, $\overline{CS}$ and SA[3:0]. SCLK is the serial shift clock input. SDIO is a bidirectional data I/O pin. $\overline{INT}$ is an interrupt output. $\overline{CS}$ is a serial port select input. SA[3:0] are address pins for the serial port.

SA[3:0] share the same pins as the $\overline{PLED[3:0]}$ output, drivers respectively. At powerup or reset, the output drivers are tristated for an interval called the power-on reset time. During the power-on reset interval, the value on these pins is latched into the device and used as the serial port address.

3.20.2 Timing and Multiple Register Access

The serial port is idle when $\overline{CS}$=1. During idle, SDIO is in the high impedance state. When $\overline{CS}$ goes low, a serial shift cycle is initiated. Data on SDIO is then shifted in on the first 16 falling edges of SCLK (SDIO is high impedance). On the next 16 falling edges of SCLK, data is either shifted in or out on SDIO, depending on whether a write cycle or read cycle was selected with the bit R/$\overline{W}$. After the first 32 SCLK clock cycles have been completed, one complete register has been read/written. If $\overline{CS}$ is still kept low for an additional 16 SCLK clock cycles, the next register number in numerical order is accessed and read/written. This multiple register access can continue on as many registers as desired as long as $\overline{CS}$ continues to stay low and groups of 16 SCLK clocks are present. When $\overline{CS}$ goes high or when all registers have been accessed in a multiple register access cycle, the serial shifting process is halted, the data is latched into the device, and SDIO goes into the high impedance state.

$\overline{INT}$ is an output pin that goes low whenever any one of the interrupt bits changes state in the serial port Channel Status registers. After the serial port bit that set the interrupt is read out, $\overline{INT}$ is reset back to a high. Refer to the Interrupt section for more details.

3.20.3 Frame Structure

The structure of the serial port frame is shown in Table 3. Each serial port access cycle consists of 32 bits, minimum. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16+ bits are from one or more of the ten internal registers.

The first bit in the serial port frame is a start bit and needs to be written as a 0 for the serial port cycle to continue. The next bit is a read/write bit which determines if the accessed register(s) bits will be read or write. The next 8 bits are device addresses, and PHYAD[7:4] must be 1111 and PHYAD[3:0] must match the values on pins SA[3:0] for the serial port access to continue. The next 4 bits are register address select bits which select one of the ten data registers for access. The next 2 bits are turnaround bits which are not actual register bits but extra time for SDIO to switch from write to read if necessary. The final 16+ bits of the serial port cycle come from one or more registers designated by the register address bits.

3.20.4 Bit Types

Since the serial port is bidirectional, there are many different type of bits. Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle.Read/Write bits (R/W) are actually write bits which can be read out during a read cycle.

R/WSC bits are R/W bits that clear themselves after a set period of time or after a specific event has completed. R/LT are read bits that latch on transition, and they stay latched until they are read. After they are read, they are updated to their current value. R/LT bits can also be programmed to assert the interrupt function as described in the Interrupt section. The bit type definitions are summarized in Table 2.

Table 2. Serial Port Register Bit Type Definition

Sym	Name	Definition	
		Write Cycle	**Read Cycle**
W	Write	Input	No Operation, Hi Z
R	Read	No Operation, Hi Z	Output
R/W	Read/Write	Input	Ouput
R/W SC	Read/Write, Self Clearing	Input Clears Itself After Operation Completed	Output
R/LT	Read, Latching On Transition	No Operation, Hi Z	Output When Bit Transitions, Bit Latched And Interrupt Set. When Bit Is Read, Interrupt Cleared And Bit Updated.

3.20.5 Interrupt

The 84C24 has a hardware and software interrupt capability for serial port status outputs.

As stated previously, R/LT are read bits that latch on transition. R/LT bits are also called interrupt bits if they are not masked out with the Global Mask register bits. Interrupt bits automatically latch themselves into their register locations and assert the interrupt pin $\overline{INT}$ low and interrupt bits INT and INT_GLBL high when they change state. Interrupt bits stay latched until they are read. When interrupt bits are read, the interrupt register bit INT is cleared for that register and the interrupt bit is updated to its current value. When all interrupt register bits are cleared in all four of the Channel Status registers, the $\overline{INT}$ pin is deasserted and the global interrupt bit INT_GLBL in the Channel Status registers is cleared. Each interrupt bit can be individually masked and subsequently be removed as an interrupt bit by setting the appropriate mask register bits in the Global Mask register.

As stated previously, interrupt is asserted if one or more of the interrupt bits has changed since the last serial read operation. A quick way to find the bit(s) that have changed since the last interrupt clear is to set register address bits REGAD[3:0] = 1111. If REGAD[3:0] = 1111, the accessed register is not determined by REGAD[3:0]. Instead, the register accessed is the one from the Channel Status registers where the interrupt bit has changed. After this "interrupted" register is read out, the interrupt register bit INT for that channel is cleared. If more than one INT register bit is set and REGAD[3:0] = 1111 is used to access them, the channel registers are accessed in numerical order on each read cycle. After all INT bits have been cleared in each Channel Status register, the $\overline{INT}$ pin is deasserted and the INT_GLBL bits in the Channel Status registers are cleared.

3.20.6 Register Structure

The 84C24 has ten internal 16 bit registers. A map of the registers is shown in Table 3. The ten internal registers consist of one Global Configuration register for setting configurations for all four channels, four Channel Configuration registers (one for each channel), four Channel Status registers (one for each channel), and one Global Mask register for interrupt masking of all four Channel Status registers.

The structure and bit definition of the Global Configuration register is shown in Table 5.

The structure and bit definitions for the Channel Configuration registers is shown in Table 6. Since the channel registers are identical in structure, the designator [m] is used where m = 1, 2, 3, and 4 depending on which channel register is accessed.

The structure and bit definitions for the Channel Status register is shown in Table 7. Since the channel registers are identical in structure, the designator [n] is used where n = 5, 6, 7, or 8 depending on which channel register is accessed.

The structure and bit definitions for the Global Mask register is shown in Table 8. This register allows each R/LT bit in the Channel Status register to be masked out or removed as a bit that will set interrupt.

4.0 Register Description

Table 3. Serial Port Frame Structure

<0>	<Read/Write>	<PHY Addr.>	<Reg. Addr.>	<Turnaround>	<Data> .....
ST	R/$\overline{W}$	PHYAD[7:0]	REGAD[3:0]	TA[1:0]	D[15:0] .....

Register 0	Global Configuration
Register 1	Channel 1 Configuration
Register 2	Channel 2 Configuration
Register 3	Channel 3 Configuration
Register 4	Channel 4 Configuration
Register 5	Channel 1 Status
Register 6	Channel 2 Status
Register 7	Channel 3 Status
Register 8	Channel 4 Status
Register 9	Global Mask

Symbol	Name	Definition	R/W
ST		Must Be Written As 0 For Serial Port Cycle To Continue	W
R/$\overline{W}$	Read/Write Select	1 = Read Cycle 0 = Write Cycle	W
PHYAD[7:0]	Physical Device Address	When PHYAD[7:4] = 1111 and PHYAD[3:0] = SA[3:0] Address Pins, The Serial Port Is Selected For Operation.	W
REGAD[3:0]	Register Address	1111 = Go To Channel Register That Has Interrupt 1001 = Global Mask Register 1000 = Channel 4 Status Register 0111 = Channel 3 Status Register 0110 = Channel 2 Status Register 0101 = Channel 1 Status Register 0100 = Channel 4 Configuration Register 0011 = Channel 3 Configuration Register 0010 = Channel 2 Configuration Register 0001 = Channel 1 Configuration Register 0000 = Global Configuration Register	W
TA1 TA0	Turnaround Time	These Bits Provide Some Turnaround Time For SDIO To Go From High Impedance To Active And Are Always High Impedance.	W
D[15:0]	Data	These 16 Bits Contain Data To/From One Of The Ten Registers Selected By Register Address Bits REGAD[3:0].	Any

ST is shifted in first

t Register Map

	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
)	PLED_SEL1	PLED_SEL0	TLVL3	TLVL2	TLVL1	JAB_DIS	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	1	0	0	0	0	0
IS								
IS								
IS								
IS								
/								
ET1	DPLX_DET0	LNK_FAIL	RPOL	JAB				
ET1	DPLX_DET0	LNK_FAIL	RPOL	JAB				
ET1	DPLX_DET0	LNK_FAIL	RPOL	JAB				
ET1	DPLX_DET0	LNK_FAIL	RPOL	JAB				
	R/LT	R/LT	R/LT	R/LT				
	1	1	0	0				

Table 5. Register 0 (Global Configuration) Structure And Bit Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
RST	PDN	ANEG_EN	APOL_DIS	SQE_EN	STP/$\overline{\text{UTP}}$	CIS1	CIS0
R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W

0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
PLED_SEL1	PLED_SEL0	TLVL3	TLVL2	TLVL1	JAB_DIS	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Symbol	Name	Definition	R/W	Def.
0.15	RST	Reset	1 = Reset, Clear After Reset Done 0 = Normal	R/W SC	1
0.14	PDN	Powerdown Enable	1 = Powerdown 0 = Normal	R/W	0
0.13	ANEG_EN	AutoNegotiation Enable	1 = AutoNegotiation Enabled 0 = Normal	R/W	0
0.12	APOL_DIS	Auto Polarity Disable	1 = Auto Polarity Correction Function Disabled 0 = Normal	R/W	0
0.11	SQE_EN	SQE Test Enable	1 = SQE Enabled 0 = Disabled	R/W	0
0.10	STP/$\overline{\text{UTP}}$	STP/UTP Cable Type Select	1 = STP (150 ohm) 0 = UTP (100 ohm)	R/W	0
0.9 0.8	CIS1 CIS0	Controller Interface Select	11 = AMD 10 = NSC 01 = Intel 00 = SEEQ	R/W	0 0
0.7 0.6	PLED_SEL1 PLED_SEL0	Programmable LED Output Pin Select	11 = $\overline{\text{PLED[3:0]}}$ Pin Is Determined By PLED Bit (m.11) In Channel Configuration Registers. If m.11 = 1, $\overline{\text{PLED}}$ Blinks 104 ms On/Off If m.11 = 0, $\overline{\text{PLED}}$ Off 10 = $\overline{\text{PLED[3:0]}}$ Pin Is Determined By PLED Bit (m.11) In Channel Configuration Registers 01 = $\overline{\text{PLED[3:0]}}$ Pin Is Full Duplex Detect Output 00 = $\overline{\text{PLED[3:0]}}$ Pin Is Link Pulse Detect Output	R/W	0 0
0.5 0.4 0.3	TLVL3 TLVL2 TLVL1	Transmit Output Level Adjust	See Table 1	R/W	1 0 0
0.2	JAB _DIS	Jabber Disable	1 = Jabber Function Disabled 0 = Normal	R/W	0
0.1			Reserved for factory use, must be 0	R/W	0
0.0			Reserved for factory use, must be 0	R/W	0

x.15 Bit Is Shifted First

Table 6. Registers 1-4 (Channel Configuration) Structure And Bit Definition

m.15	m.14	m.13	m.12	m.11	m.10	m.9	m.8
ANEG_RST	ANEG_RF_A	DPLX_SEL1	DPLX_SEL0	PLED	XMT_DIS	RLVL0	LNK_DIS
R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W

m.7	m.6	m.5	m.4	m.3	m.2	m.1	m.0

Bit	Symbol	Name	Definition	R/W	Def.
m.15	ANEG_RST	AutoNegotiation Reset	1 = Halt Xmt Link Pulse, then Restart AutoNegotiation Process 0 = Normal	R/W SC	0
m.14	ANEG_RF_A	AutoNegotiation Remote Fault Advertise Enable	1 = Remote Fault Advertise 0 = No Advertise	R/W	0
m.13 m.12	DPLX_SEL1 DPLX_SEL0	Duplex Select	If ANEG_EN=1: 11 = Full And Half Advertise During AutoNegotiation 10 = Full Duplex Advertise During AutoNegotiation 01 = Half Duplex Advertise During AutoNegotiation 00 = None Advertise During AutoNegotiation If ANEG_EN=0: 11 = Full Duplex 10 = Full Duplex 01 = Half Duplex 00 = None	R/W	0 1
m.11	PLED	Programmable LED Output Select	1 = LED On ($\overline{\text{PLED}}$ [m] Pin Is Low) 0 = LED Off ($\overline{\text{PLED}}$ [m] Pin Is High)	R/W	0
m.10	XMT_DIS	TP Transmit Disable	1 = TP Transmitter Disabled, Both Data And Link 0 = Normal	R/W	0
m.9	RLVL0	Receive Level Adjust	1 = Receive Squelch Levels Reduced by 4.5dB 0 = Normal	R/W	0
m.8	LNK_DIS	Link Pulse Disable	1 = Receive Link Pulse Detect Function Disabled 0 = Normal	R/W	0
m.7 thru m.0					

x.15 Bit Is Shifted First
m=Channel Configuration Register Number: 1, 2, 3, or 4

Table 7. Registers 5-8 (Channel Status) Structure And Bit Definition

n.15	n.14	n.13	n.12	n.11	n.10	n.9	n.8
INT_GLBL	INT	A1	A0	ANEG_DET1	ANEG_DET0	ANEG_RF_R	DPLX_DET1
R	R	R	R/LT	R/LT	R/LT	R/LT	R/LT

n.7	n.6	n.5	n.4	n.3	n.2	n.1	n.0
DPLX_DET0	LNK_FAIL	RPOL	JAB				
R/LT	R/LT	R/LT	R/LT				

Bit	Symbol	Name	Definition	R/W	Def.
n.15	INT_GLBL	Global Interrupt Detect	1 = R/LT Bit In Registers 5-8 Has Changed State Since Last Read 0 = No Interrupt	R	0
n.14	INT	Local Interrupt Detect	1 = R/LT Bit In Register [n] Has Changed State Since Last Read 0 = No Interrupt	R	0
n.13 n.12	A1 A0	Register Address Identification	11 = This Register Is Channel 4 Status, n=8 10 = This Register Is Channel 3 Status, n=7 01 = This Register Is Channel 2 Status, n=6 00 = This Register Is Channel 1 Status, n=5	R	11 10 01 00
n.11 n.10	ANEG_DET1 ANEG_DET0	AutoNegotiation Status	11 = AutoNegotiation Detected, Negotiation Started 10 = AutoNegotiation Detected, Negotiation Stuck 01 = AutoNegotiation Detected, Negotiation Done 00 = AutoNegotiation Not Detected	R/LT	00
n.9	ANEG_RF_R	AutoNegotiation Remote Fault Detect	1 = Remote Fault Detected From Remote End 0 = Normal	R/LT	0
n.8 n.7	DPLX_DET1 DPLX_DET0	Duplex Detect	11 = Invalid 10 = Device In Full Duplex 01 = Device In Half Duplex 00 = Device in Neither Half Or Full Duplex	R/LT	01
n.6	LNK_FAIL	Link Fail Detect	1 = No Link Pulse Detected On Receive TP Input 0 = Normal	R/LT	1
n.5	RPOL	Reverse Polarity Detect	1 = Reverse Polarity Detected On Receive TP Input 0 = Normal	R/LT	0
n.4	JAB	Jabber Detect	1 = Jabber Detected 0 = Normal	R/LT	0
n.3 thru n.0					

x.15 Bit Is Shifted First
n= Channel Status Register Number: 5, 6, 7, or 8

Table 8. Register 9 (Global Mask) Structure And Bit Definition

9.15	9.14	9.13	9.12	9.11	9.10	9.9	9.8
	MASK_ INT			MASK_ ANEG_DET1	MASK_ ANEG_DET0	MASK_ ANEG_RF_R	MASK_ DPLX_DET1
R/W						R/W	R/W

9.7	9.6	9.5	9.4	9.3	9.2	9.1	9.0
MASK_ DPLX_DET0	MASK_ LNK_FAIL	MASK_ RPOL	MASK_ JAB	0	1		
R/W	R/W	R/W	R/W	R/W	R/W		

Bit	Symbol	Name	Definition	R/W	Def.
9.15					
9.14	MASK_ INT	Interrupt Mask - Interrupt Detect	1 = Mask Interrupt For INT In Register 0, n, And INT Pin 0 = No Mask	R/W	1
9.13 9.12					
9.11	MASK_ ANEG_DET1	Interrupt Mask - NWay Detect	1 = Mask Interrupt For ANEG_DET1 In Register n 0 = No Mask	R/W	1
9.10	MASK_ ANEG_DET0	Interrupt Mask - NWay Detect	1 = Mask Interrupt For ANEG_DET0 In Register n 0 = No Mask	R/W	1
9.9	MASK_ ANEG_RF_R	Interrupt Mask - NWay Remote Fault Detect	1 = Mask Interrupt For ANEG_RF_R In Register n 0 = No Mask	R/W	1
9.8	MASK_ DPLX_DET1	Interrupt Mask - Duplex Detect	1 = Mask Interrupt For DPLX_DET1 In Register n 0 = No Mask	R/W	1
9.7	MASK_ DPLX_DET0	Interrupt Mask - Duplex Detect	1 = Mask Interrupt For DPLX_DET0 In Register n 0 = No Mask	R/W	1
9.6	MASK_ LNK_FAIL	Interrupt Mask - Link Fail Detect	1 = Mask Interrupt For LNK_FAIL In Register n 0 = No Mask	R/W	1
9.5	MASK_ RPOL	Interrupt Mask - Reverse Polarity Detect	1 = Mask Interrupt For RPOL In Register n 0 = No Mask	R/W	1
9.4	MASK_ JAB	Interrupt Mask - Jabber Detect	1 = Mask Interrupt For JAB In Register n 0 = No Mask	R/W	1
9.3			Reserved for Factory use, must be 0.	R/W	0
9.2			Reserved for Factory use, must be 1.	R/W	1
9.1 9.0					

x.15 Shifted First
n= Channel Status Register Number: 5, 6, 7, or 8

5.0 Application Information

5.1 EXAMPLE SCHEMATICS

Typical examples of the 84C24 used in a switching hub applications are shown in the schematics in Figures 7 and 8.

5.2 TP TRANSMIT INTERFACE

The interface between the TP outputs on TPO± and the twisted pair cable requires a transformer and two resistors for each channel as shown in Figure 7 and 8.

The transmit transformer specifications are shown in Table 9. Sources for the transformer are listed in Table 10.

Table 9. Transformer Specification

Parameter	Specification	
	Transmit	Receive
Turns Ratio	2 √2:1 CT	1:1
Inductance (µH Min)	200	200
Leakage Inductance (µH Max)	0.4	0.2
Capacitance (pF Max)	10	10
DC Resistance (Ohms Max)	0.25	0.25

Two external 400 ohm 1% resistors are needed on TPO± to provide a 100 ohm termination impedance when looking back through the transformer from the twisted pair cable, as shown in the Figure 7 and 8 schematic.

The 84C24 has special circuitry to reduce common mode noise on the twisted pair output. However, common mode chokes may be needed to meet emissions requirements. Common mode chokes are not illustrated in the application schematics in Figures 7 and 8.

To minimize noise pickup, the loading on TPO± should be minimized and both outputs should always be loaded equally.

Table 10. Transformer Sources

Vendor	Part Number
Valor	ST4178
NanoPulse	NP6098-30
PCA	EPE6130S
Belfuse	S553-1084-02
Pulse Engr	PE68042

5.3 TP RECEIVE INTERFACE

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with an external resistor as shown in Figure 7 and 8.

The receive transformer specification is shown in Table 9. Sources for the transformer are listed in Table 10.

The receive input needs to be terminated with 98 ohms in order to meet input impedance requirements of IEEE 802.3 Section 14. Notice that in Figure 7 and 8, the receive input has this input termination resistor broken up into two 49 ohm 1% resistors with a 0.1µF capacitor tied between the center points and GND. This capacitor attenuates common mode input noise. The 0.1µF capacitor is optional and is only needed if the device is required to meet the receive common mode input AC voltage specification in IEEE 802.3 Section 14. If the capacitor is not needed, then the two termination resistors can be lumped into one 98 ohm 1% resistor across TPI±.

In order to minimize noise pickup into the receive path, loading on TPI± should be minimized and both inputs should be loaded equally.

5.4 TP TRANSMIT OUTPUT CURRENT SET

The TPO± output current level is set by an external resistor tied between REXT and GND. The output current is determined by the following equation where R is the value of REXT:

$$I_{out} = (R/10K) * 50mA$$

REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels.

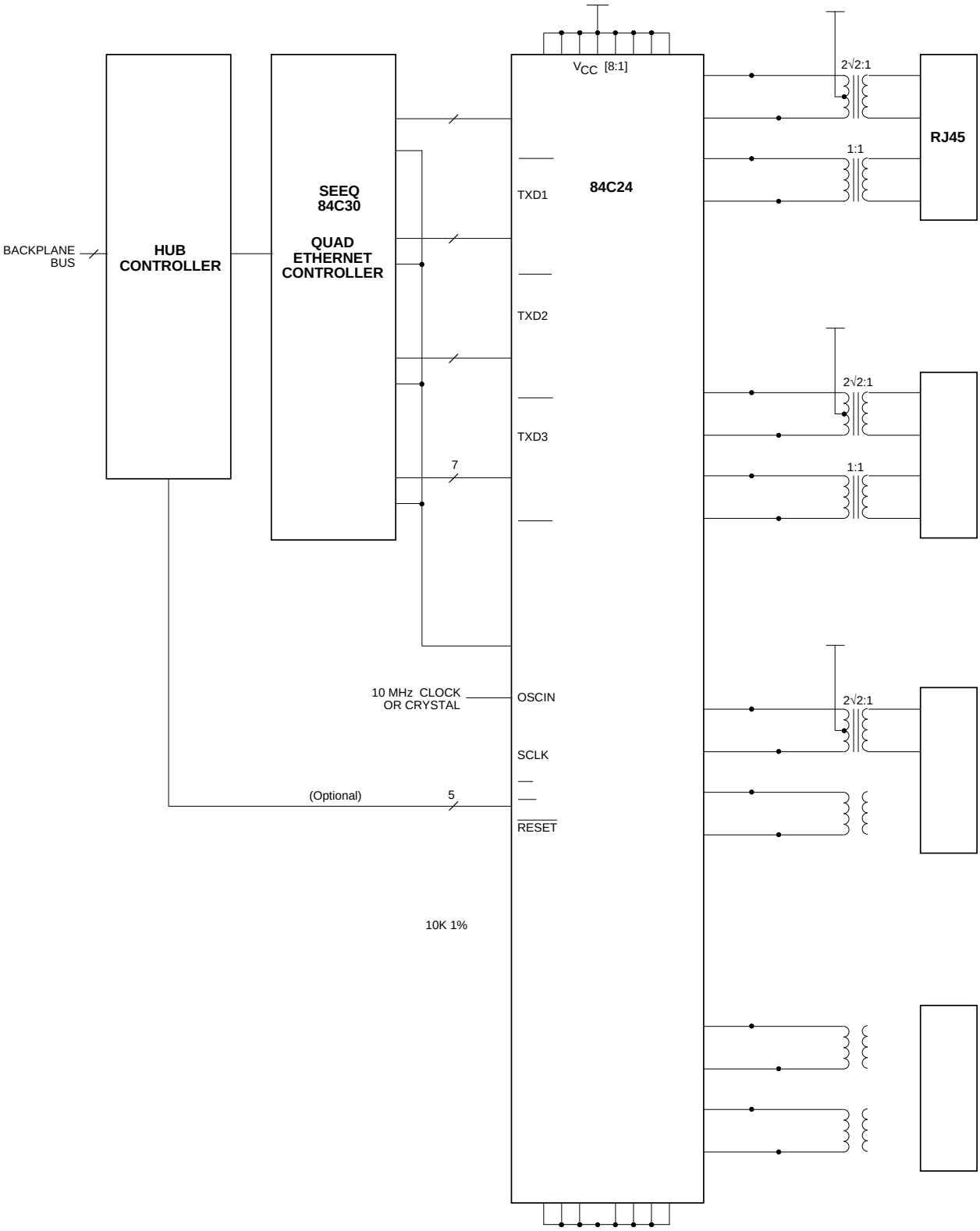


Figure 7. Typical Switching Hub Schematic Using 84C24

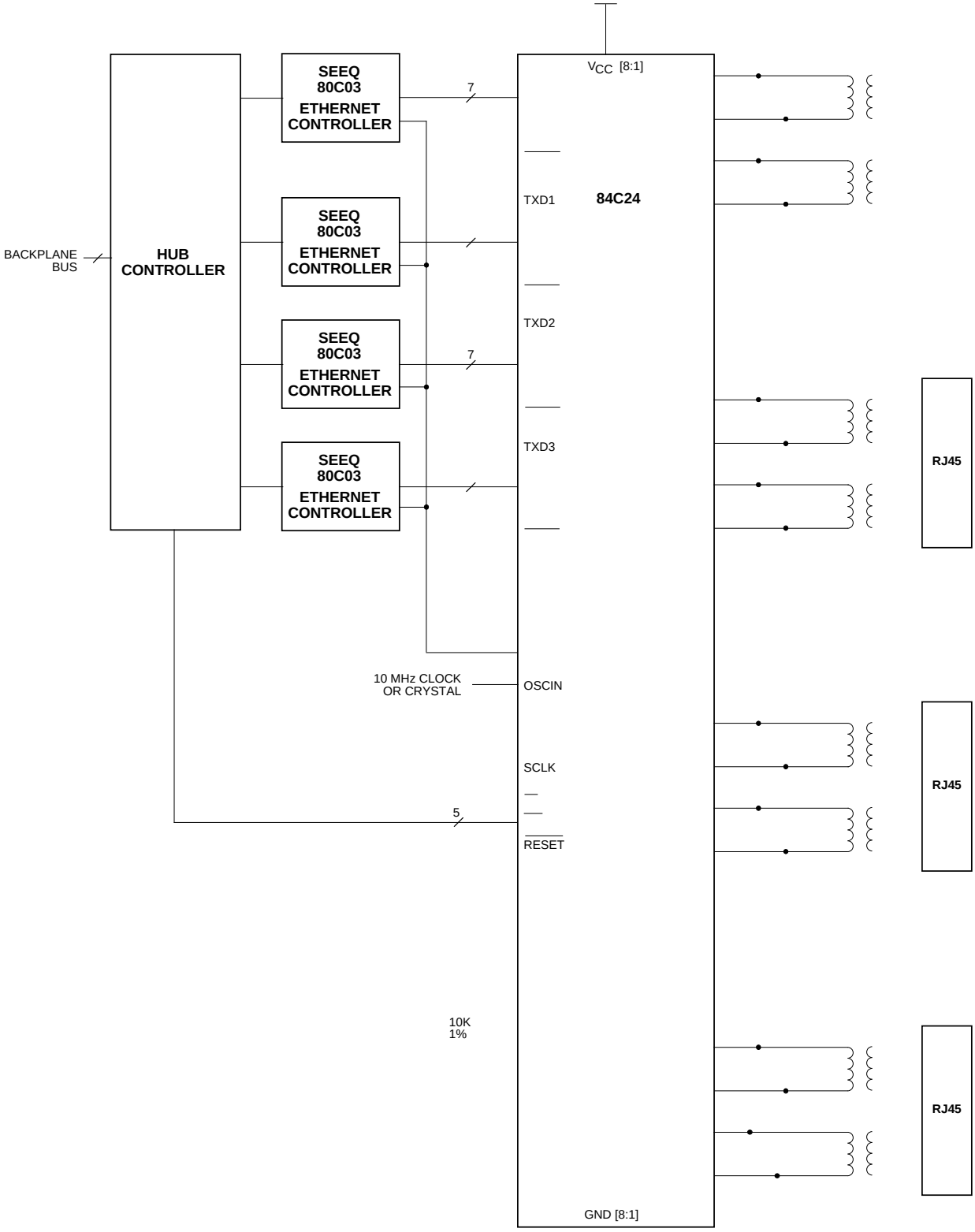


Figure 8. Typical Switching Hub Schematic Using 84C24

Keep the external resistor close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

Since the TPO± output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it might be necessary to adjust the value of the output current to compensate for external loading. One way to adjust the TPO± output level is to change the value of the external resistor tied to REXT as discussed in the previous paragraphs. A better way to adjust the TPO± output level is to use the transmit level adjust register bits accessed through the serial port. These four bits can adjust the output level by -18% to +24% in 6% steps as described in Table 1.

5.5 CONTROLLER INTERFACE

The controller interface will connect to any of the following Ethernet controllers, without any glue logic, as shown in Figure 7 and 8.

Standard Ethernet controllers use TXC to clock data on TXD. TXC is specified on standard Ethernet controllers to be an output. If a nonstandard controller is used, there might be a need to clock TXD into the 84C24 on the edges of an external master clock. The master clock, in this case, would be an input to the 84C24. This can be done by using OSCIN as the master clock input. OSCIN generates TXC inside the 84C24; thus, TXD data can be clocked into the 84C24 on edges of output clock TXC or input clock OSCIN. In the case where OSCIN is used as the input clock, a crystal is no longer needed on OSCIN, and TXC can be left open or used for some other purpose.

5.6 SERIAL PORT

5.6.1 General

The 84C24 has a serial port to set all of the device's configuration inputs and read out the status outputs. Most microcontrollers can easily interface to the serial port without any extra logic, as shown in Figure 7 and 8.

As described earlier, the serial port consists of 8 lines: SCLK, SDIO, $\overline{INT}$, $\overline{CS}$, and SA[3:0]. However, only three lines, SCLK, SDIO, and $\overline{CS}$ are needed to shift data in and out. $\overline{INT}$ is provided for convenience only and SA[3:0] are usually pinstrapped to the correct device address.

The $\overline{CS}$ signal can be extended such that multiple registers can be read out in a single serial port read cycle.

5.6.2 Polling vs. Interrupt

The status output status bits can be monitored by either polling the serial port or with interrupt.

If polling is used, the registers can be read by an external device at regular intervals and the status bits can be checked against their previous values to determine any changes. To make polling simpler, multiple registers can be accessed on a single read cycle by extending $\overline{CS}$. This eliminated the need to poll registers individually.

The interrupt feature offers the ability to detect changes in the status output bits without constant register polling. Assertion of the $\overline{INT}$ pin or INT and INT_GLBL serial port bits indicates that one or more of the status output bits has changed since the last read cycle. Thus, any of these interrupt signals can be used by an external device to initiate a read cycle. Then the individual registers (or multiple registers) can be read out and status bits compared against their previous values to determine any changes. If the register address REGAD[3:0] = 1111 is selected, the serial port will automatically go to the register that has the "interrupted bit", thus eliminating the need to read all four Channel Status registers in response to a single interrupt. If multiple bits asserted the interrupt and REGAD[3:0] = 1111 is used to access them, the interrupted registers are accessed in numerical order on each read cycle. After all the interrupt bits have been read out, the interrupt signals are deasserted. A mask register bit for every status output bit exists in the Global Mask register so that the interrupt bits can be individually programmed for each application.

5.6.3 Serial Port Addressing

The device address for the serial port is selected by tying the SA[3:0] pins to the desired value. SA[3:0] share the same pins as the $\overline{PLED}$[3:0] outputs, respectively, as shown in Figure 9a. At powerup or reset, the output drivers are tristated for an interval called the power-on reset time. During the power-on reset interval, the value on these pins is latched into the device and used as the serial port address. The LED outputs are open drain with internal resistor pullup to V_{CC}.

If an LED is desired on the LED outputs, then an LED and resistor are tied to V_{CC} as shown in Figures 9b. If a high address is desired, then the LED to V_{CC} automatically makes the latched address value a high. If a low value for the address is desired, then a 50K resistor to GND must be added as shown in Figure 9b.

If no LED's are needed on the LED outputs, the selection of addresses can be done without any external components as shown in Figure 9c. If a high address is desired, the pin should be left floating and the internal pullup will pull the pin high during power-on reset and latch in a high address value. If a low address is desired, then the output pin can either be tied directly to GND or tied to GND through an optional 33K resistor as shown in Figure 9C. The optional 33K resistor allows the pin to be used as a digital output under normal conditions. Notice that the default address in the serial port is SA[3:0] = 1111.

There are 8 serial port device address bits (PHYAD[7:0]) even though there are only 4 address inputs (SA[3:0]). The upper 4 serial port device address bits on PHYAD[7:4] are not used and the device always looks for them to be 1's. Thus, these can be used to decode the serial port by writing one or more 0's into these bits.

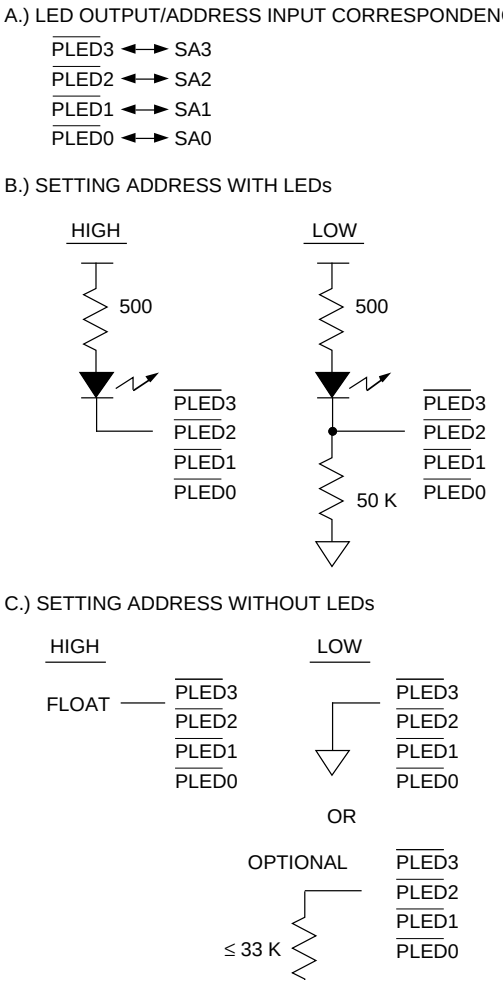


Figure 9. Serial Port Device Address Selection

Table 11. Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	10 Mhz +/- 0.01%
Equivelent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1mW max

5.7 RESET

The reset function in the 84C24 resets all the internal timers and sets all the input configuration bits in the serial port to their default values. Reset can be initiated internally or externally.

An internal reset automatically occurs when V_{CC} is applied to the 84C24.

An external reset can be initiated in two ways. The first way to cause an external reset is to set the reset bit in the serial port Global Configuration register. Setting this bit will create an internal reset pulse which will clear the bit when the reset pulse has completed. The second way to do reset is to force an active low reset signal on the RESET pin. Typically this reset signal would come from a microprocessor or some other digital device.

It is not necessary to use the reset function in normal operation; it is available if external control of reset is desired.

5.8 DIAGNOSTIC LOOPBACK

As described in the earlier Loopback section, the 84C24 automatically loops back transmit data back into the receive path on every transmitted packet. However, it might be necessary to provide a diagnostic loopback in which transmit data is returned through the receive path but transmit data is not actually sent out on TPO±. This can be performed with the 84C24 by first disabling the transmitter with the transmit disable bit in the serial port Channel Configuration register and then transmitting a packet. This internal loopback function will force the transmit data back onto the receive controller interface while not actually sending out the data on the twisted pair interface.

5.9 OSCILLATOR

The 84C24 requires a 10 Mhz reference frequency for internal signal generation. This 10Mhz reference frequency can be generated by either connecting an external crystal or an external clock between OSCIN and GND.

If the crystal oscillator is used, it needs only an external crystal, and no other external capacitors or other components are required. The crystal must have the characteristics shown in Table 11. The crystal must be placed as close as possible to OSCIN and GND so that parasitics on OSCIN are kept to a minimum.

5.10 LED DRIVERS

The $\overline{\text{PLED}}[3:0]$ outputs can all drive LED's tied to V_{CC}. The $\overline{\text{PLED}}[3:0]$ outputs can be programmed through the serial port to do one of 5 different functions: (1) Link Detect Indication, (2) Full Duplex Indication, (3) On, (4) Off, or (5) Blink. The $\overline{\text{PLED}}[3:0]$ pins can be programmed for one of these 5 functions by appropriately setting the LED output select bits in the Global Configuration and Channel Configuration registers. When the $\overline{\text{PLED}}[3:0]$ pins are programmed to indicate Link or Full Duplex, the LED output drivers are controlled by internal logic described in the Link Integrity and Full Duplex section. When $\overline{\text{PLED}}[3:0]$ is programmed to be On, the LED output driver goes low, thus turning on the LED under user control. When $\overline{\text{PLED}}[3:0]$ is programmed to be Off, the LED output driver turn off, thus turning off the LED under user control. When $\overline{\text{PLED}}[3:0]$ is programmed to Blink, the LED output driver will continuously blink at a rate of 100 ms on, 100 ms off.

The On and Off functions allow the LED driver to be controlled directly through the serial port to indicate any function that is desired under external control. The Blink function allows the same external control of the LED driver and also offers the provision to blink the LED without the need for any external timers.

The $\overline{\text{PLED}}[3:0]$ outputs can also drive other digital inputs and can be user defined and controlled through the serial port.

5.11 POWER SUPPLY DECOUPLING

There are eight V_{CC}'s on the 84C24 ($V_{CC}[8:1]$) and eight GND's (GND[8:1]).

All eight V_{CC}'s should be connected together as close as possible to the device with a large V_{CC} plane. If the V_{CC}'s vary in potential by even a small amount, noise and latchup can result.

All eight GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result.

A 0.01-0.1uF decoupling capacitor should be connected between each V_{CC}/GND set as close as possible to the device pins, preferably within 0.5".

The V_{CC} connection to the transmit transformer center tap shown in Figures 7 and 8 has to be well decoupled in order to minimize common mode noise injection from V_{CC} onto the TP inputs and outputs. It is recommended that a 0.01µF decoupling capacitor be placed between the center tap V_{CC} to the 84C24 GND plane. This decoupling capacitor should be physically placed within 0.5" of the transformer center tap.

The PCB layout and power supply decoupling should keep any AC ripple and noise voltage across each VCC-GND pin combination to less than 100 mVpp, and preferably less than 50 mVpp. In addition, the VCC's should all be within 25 mV of each other, and the GND's should be within 25mV of each other, when measured at the device.

6.0 Specifications

Absolute Maximum Ratings

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, GND unless otherwise specified.

V_{CC} Supply Voltage ..... -0.3V to 7V
All Inputs and Outputs ..... -0.3V to V_{CC}+0.3V
Input Latchup Current ..... +/-25 mA
Package Power Dissipation ..... 3 Watt @ 25°C
Storage Temperature ..... -65 to +150°C
Operating Temperature ..... -65 to +85°C
Lead Temperature (Soldering, 10 Sec) ..... 250°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70°C
2. VCC = 5V +/-5%
3. 10 Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
VIL	Input Low Voltage			0.8	Volt	All except OSCIN, SA[3:0]
				V_{CC} -1.4	Volt	SA[3:0]
				1.5	Volt	OSCIN
VIH	Input High Voltage	2			Volt	All except OSCIN, SA[3:0]
		V_{CC} - 0.3			Volt	SA[3:0]
		3.5			Volt	OSCIN
IIL	Input Low Current			-1	µA	VIN = GND All Except SA[3:0], $\overline{\text{RESET}}$, OSCIN, TPI±
		-4		-50	µA	VIN = GND SA[3:0], $\overline{\text{RESET}}$
				-150	µA	OSCIN
IIH	Input High Current			1	µA	VIN = V_{CC} All Except OSCIN, TPI±
				150	µA	VIN = V_{CC} OSCIN
VOL	Output Low Voltage			0.4	Volt	IOL = -2mA All except $\overline{\text{PLED[3:0]}}$
				1	Volt	IOL = -20mA $\overline{\text{PLED[3:0]}}$
VOH	Output High Voltage	4			Volt	IOL = 2mA All except $\overline{\text{PLED[3:0]}}$, $\overline{\text{INT}}$
		2.4			Volt	IOL = 4µA $\overline{\text{PLED[3:0]}}$, $\overline{\text{INT}}$
CIN	Input Capacitance		5		pF	
ICC	VCC Supply Current			275	mA	Transmitting, Current into all VCC Pins
				0.1	mA	Powerdown Mode

TWISTED PAIR CHARACTERISTICS, TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70° C
2. V_{CC} = 5V +/-5%
3. 10 Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. TPO ± Load in Figure 8 or equivalent.

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
TOV	TPO± Differential Output Voltage	2.2 * 2√2	2.5 * 2√2	2.8 * 2√2	V pk	Primary Side of XFMR in Figure 8
		2.2	2.5	2.8	V pk	Secondary Side of XFMR in Figure 8
TOVT	TPO± Differential Output Voltage Template	See Figure 2				
TSOI	TPO± SOI Output Voltage Template	See Figure 4				
TLPT	TPO± Link Pulse Output Voltage Template	See Figure 5				
TOIV	TPO± Differential Output Idle Voltage			+/- 50	mV	Measured on Secondary Side of XFMR on Figure 8
TOIA	TPO± Output Current	44/√2	50/√2	56/√2	mA pk	
		29/√2	33/√2	37/√2	mA pk	STP Cable Mode
TOIR	TPO± Output Current Adjustment Range	0.80		1.25		V_{CC} = 5V, Adjustable With REXT Relative to Value at REXT = 10 K
		0.82		1.24		V_{CC} = 5V, Adjustable With TLVL3-0, Relative To Value At TLVL3-0=0111
TORA	TPO± Output Current TLVL Step Accuracy			+/-50	% of Step	Relative To Ideal Values In Table 1, Table 1 Values Relative to Value with TLVL3-0 = 0111
THD	TPO± Harmonic Distortion			-27	dB	All 1's output
TOR	TPO± Output Resistance		10K		Ohm	
TOC	TPO± Output Capacitance		15		pF	

TWISTED PAIR CHARACTERISTICS, RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70° C
2. V_{CC} = 5V +/-5%
3. 10 Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. 10 MHz sinewave on TPI±

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
RST	TPI± Squelch Threshold	310		540	mV pk	
		190		330	mV pk	RLVL=1
RUT	TPI± Unsquelch Threshold	190		330	mV pk	
		115		200	mV pk	RLVL=1
ROCV	TPI± Input Open Circuit Voltage		$V_{CC}/3$		Volt	
RCMR	TPI± Input Common Mode Voltage Range		$V_{CC}/3$ ±1.0		Volt	
RDR	TPI± Input Differential Voltage Range	GND		V_{CC}	Volt	
RIR	TPI± Input Resistance	5K			ohm	
RIC	TPI± Input Capacitance		10		pF	

AC TEST TIMING CONDITIONS

Unless otherwise noted, all test conditions are as follows:

1. T_A = 0 to +70°C
2. V_{CC} = 5V +/-5%
3. 10 Mhz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. Input conditions:
   - All Inputs: tr,tf<=10ns, 20-80%
6. Output Loading
   - TPO±: As shown in Figure 8 or equivalent
   - TXC: 100pF
   - PLED[3:0], $\overline{INT}$: 1K Pullup, 50pF
   - All Other Digital Outputs: 50pF
7. Measurement Points:
   - TPO±, TPI±: 0v During Data, +0.3V at start/end of packet
   - All other inputs and outputs: 1.5 Volts

10 MHz INPUT CLOCK TIMING CHARATERISTICS

Refer to Figure 10 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	OSCIN Cycle Time	99.99		100.01	ns	
t_2	OSCIN High Time	40			ns	
t_3	OSCIN Low Time	40			ns	
t_4	TXC Delay Time			10	ns	TXC Rising and Falling Edge

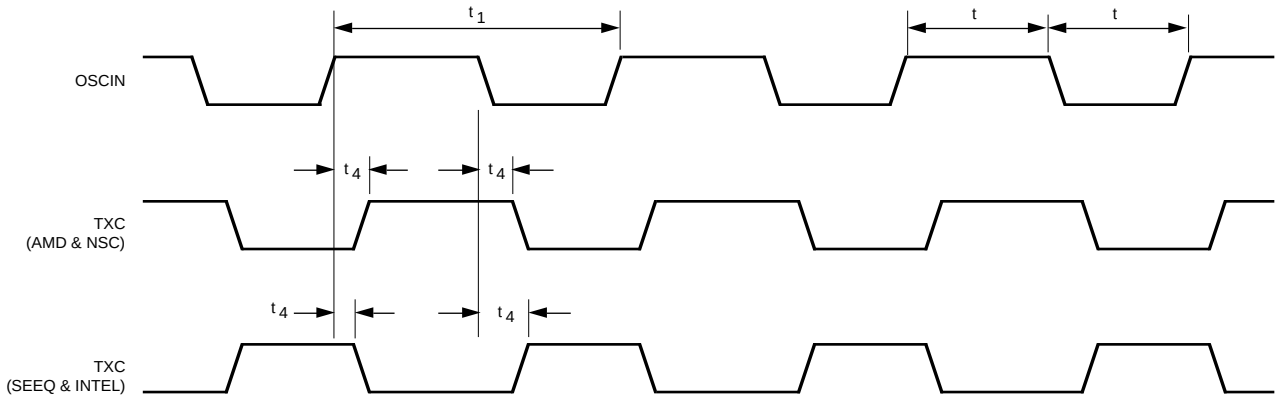
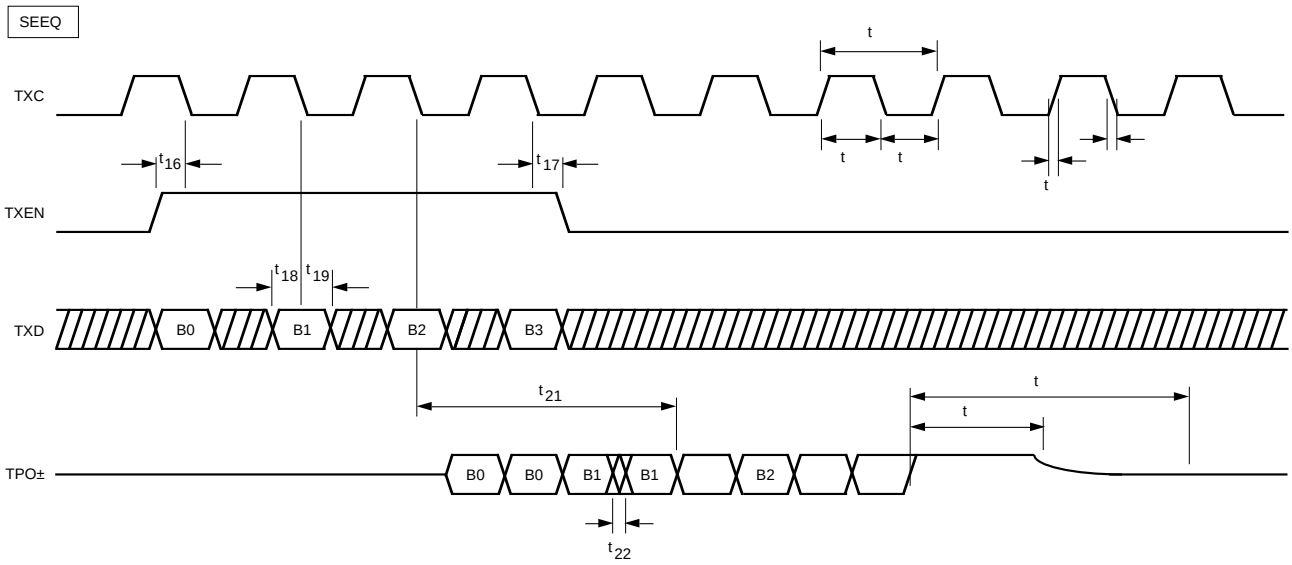


Figure 10. 10 MHz Clock Input Timing

TRANSMIT TIMING CHARACTERISTICS

Refer To Figure 11 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{11}	TXC Cycle Time	99.99	100	100.01	ns	
t_{12}	TXC High Time	40		60	ns	
t_{13}	TXC Low Time	40		60	ns	
t_{14}	TXC Rise and Fall Time			7	ns	
t_{16}	TXEN Setup Time	25			ns	
t_{17}	TXEN Hold Time	0			ns	
t_{18}	TXD Setup Time	25			ns	
t_{19}	TXD Hold Time	0			ns	
t_{20}	Transmit Bit Loss			2	Bits	
t_{21}	Transmit Propagation Delay			200	ns	
t_{22}	Transmit Output Jitter			+/-5.5	ns	
t_{23}	Transmit SOI Pulse Width To 0.3V	250			ns	Measure TPO± from last zero cross to 0.3V point.
t_{24}	Transmit SOI Pulse Width to 40 mV			4500	ns	Measure TPO± from last zero cross to 40 mV point.



NSC, AMD — SAME AS SEEQ EXCEPT TXC IS INVERTED (RISING EDGE TRIGGERED).

INTEL — SAME AS SEEQ EXCEPT TXEN IS INVERTED (ACTIVE LOW).

Figure 11. Transmit Timing

RECEIVE TIMING CHARACTERISTICS

Refer To Figures 12 and 13 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{31}	CSN Assert Delay Time			600	ns	
t_{32}	CSN Setup Time	30			ns	
t_{33}	CSN Hold Time	10		40	ns	NSC Has 5 Extra RXC Clocks After CSN Goes Low
t_{34}	CSN Deassert Delay Time	2000			ns	
t_{35}	RXD Setup Time	40			ns	
t_{36}	RXD Hold Time	30			ns	
t_{37}	RXD Propagation Delay			300	ns	
t_{38}	RXC High Time	40		200	ns	SEEQ, NSC, AMD
		40		60	ns	Intel
t_{39}	RXC Low Time	40		60	ns	SEEQ, NSC, AMD
		40		200	ns	Intel
t_{40}	CSN Assert To RXC Switchover From TX Clock To RX Clock			1200	ns	
t_{41}	CSN Deassert To RXC Switchover From RX Clock To TX Clock			250	ns	
t_{42}	SOI Pulse Width Required For Idle Detection	125		200	ns	Measure TPI± from last zero cross to 0.3V point.
t_{43}	Receive Input Jitter			±13.5	ns	Data
				±8.5	ns	Preamble
t_{44}	RXC, RXD, CSN Output Rise And Fall Times			10	ns	

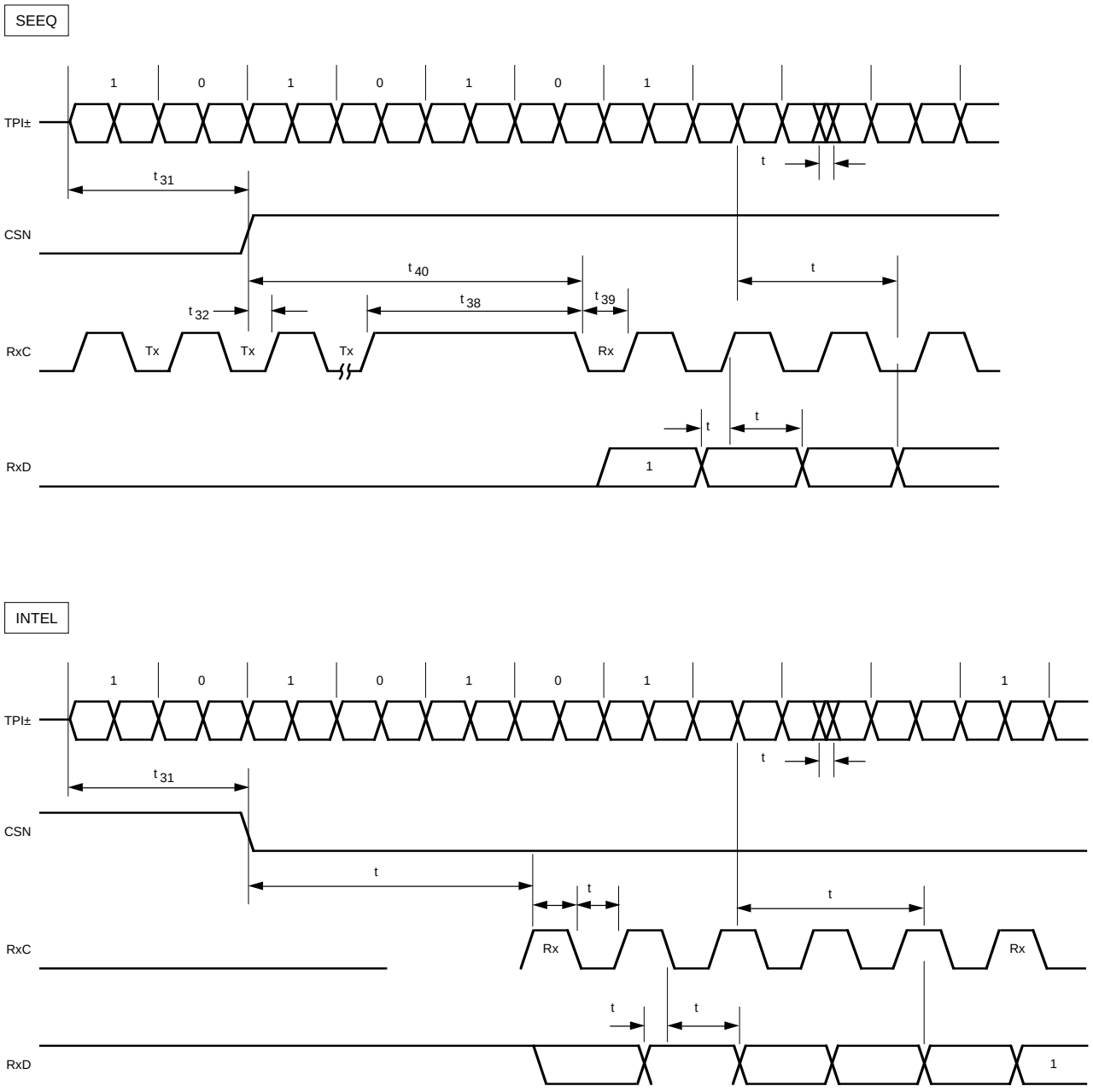
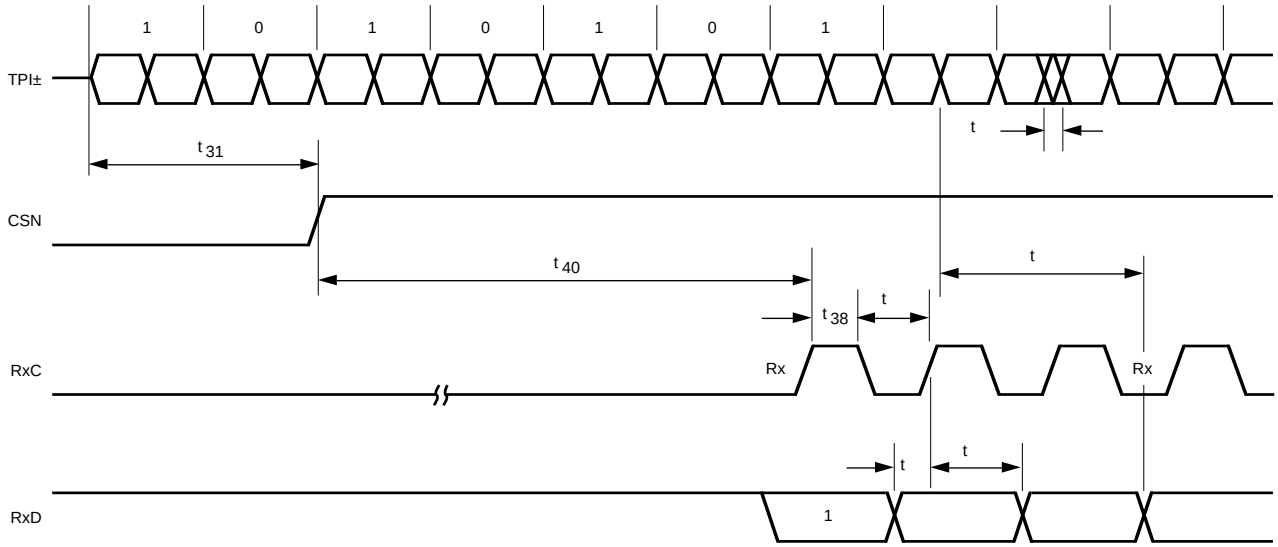


Figure 12. Receive Timing, Start of Packet

AMD



NSC SAME AS AMD EXCEPT RXD LOW DURING IDLE

Figure 12. Receive Timing, Start of Packet (continued)

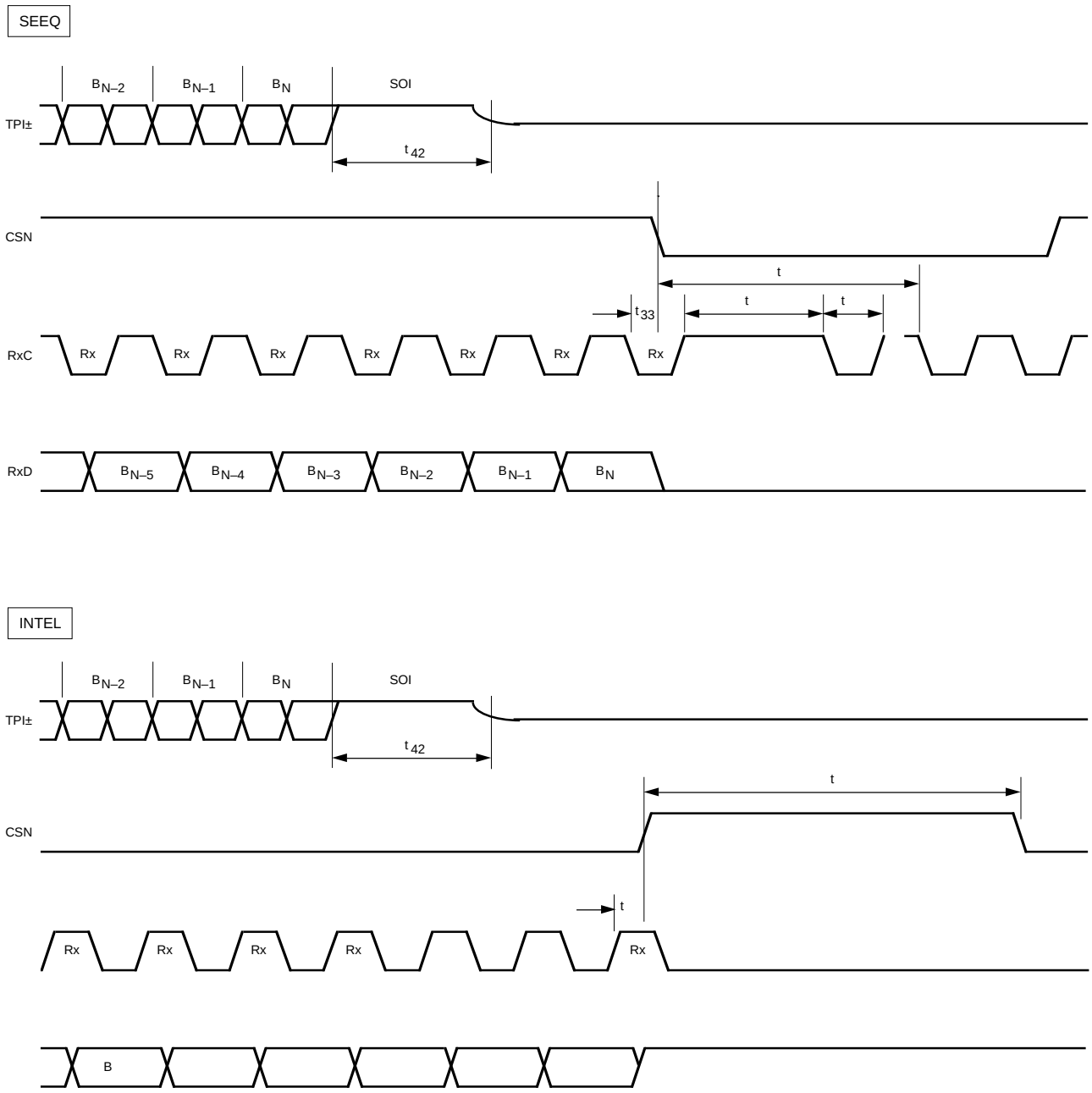


Figure 13. Receive Timing, End of Packet

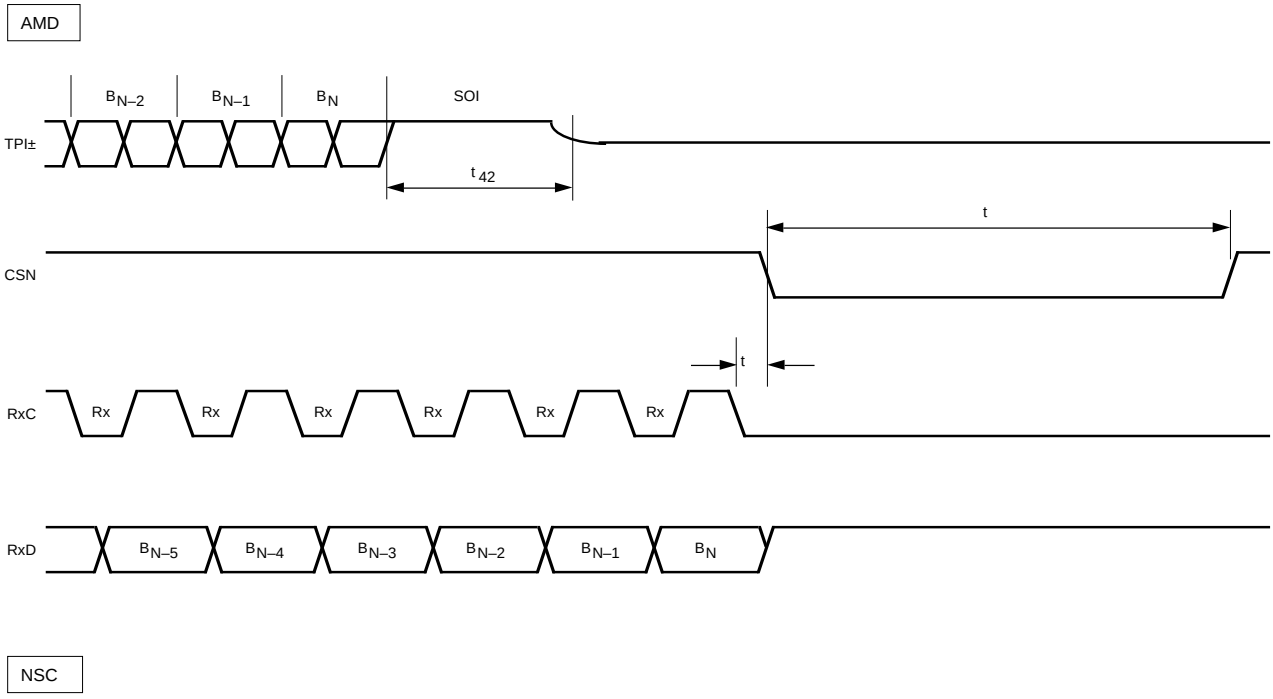
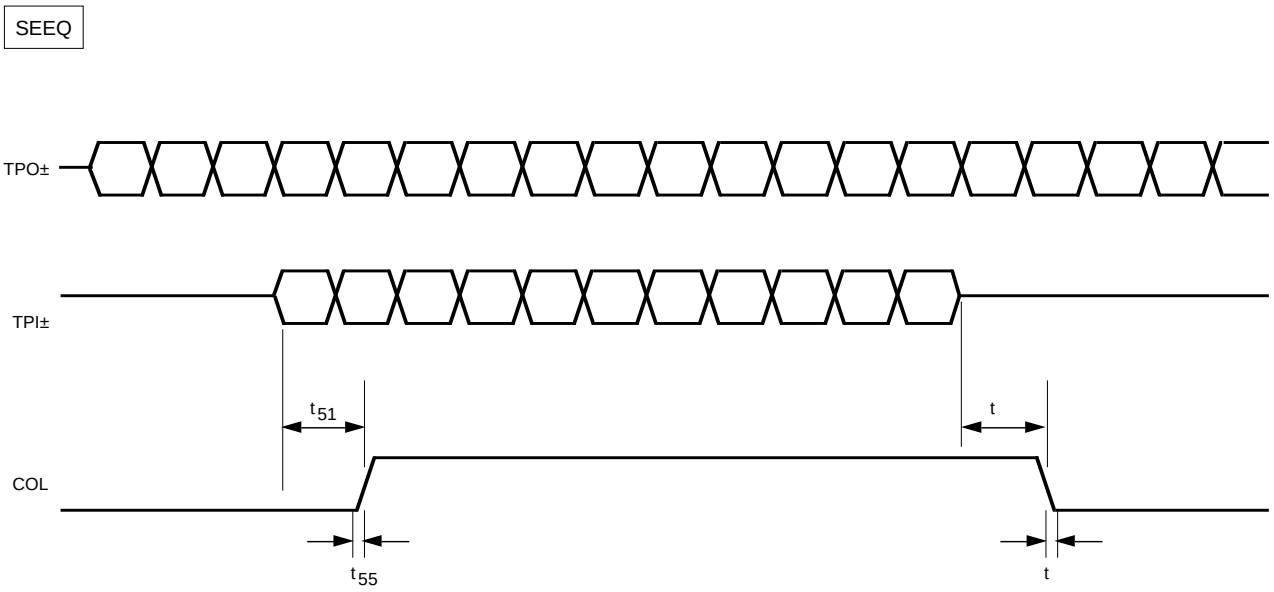


Figure 13. Receive Timing, End of Packet (continued)

COLLISION TIMING CHARACTERISTICS

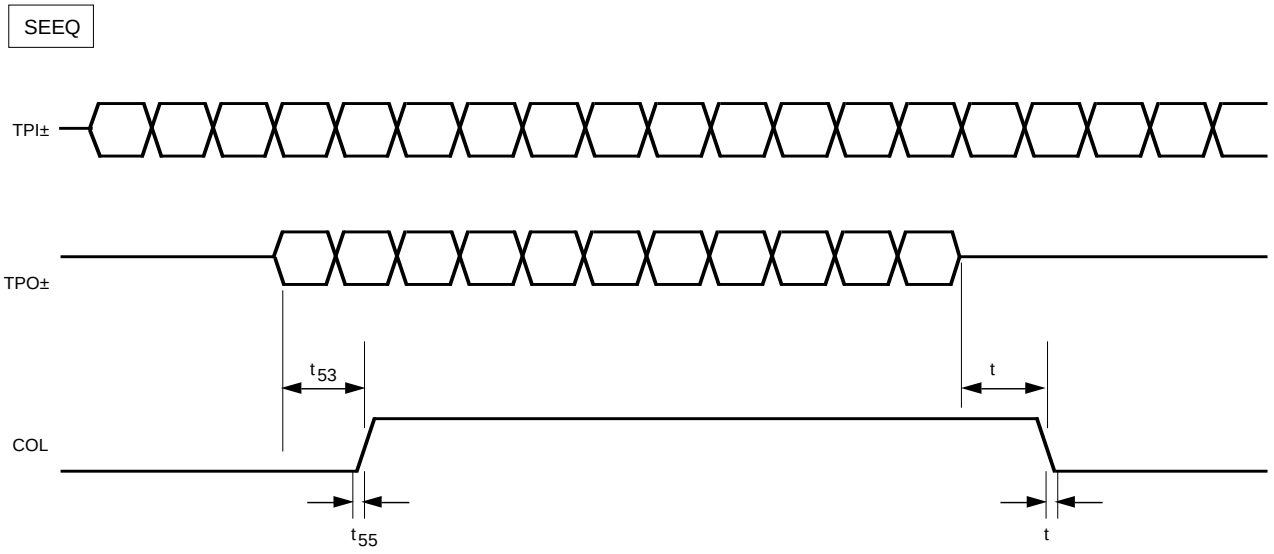
Refer To Figures 14 and 15 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	COL Assert Delay Time - Rcv after Xmit			500	ns	
t_{52}	COL Deassert Delay Time - Rcv After Rcv			300	ns	
t_{53}	COL Deassert Delay Time - Xmit After Rcv			300	ns	
t_{54}	COL Deassert Delay Time - Xmit After Rcv			300	ns	
t_{55}	COL Rise and Fall Time			10	ns	



NSC	SAME AS SEEQ
INTEL	SAME AS SEEQ EXCEPT COL IS INVERTED (ACTIVE LOW)
AMD	SAME AS SEEQ

Figure 14. Collision Timing, Receive After Transmit



NSC	SAME AS SEEQ
INTEL	SAME AS SEEQ EXCEPT COL IS INVERTED (ACTIVE LOW)
AMD	SAME AS SEEQ

Figure 15. Collision Timing, Transmit After Receive

LINK PULSE TIMING CHARACTERISTICS

Refer To Figures 16 and 17 For Timing Diagram

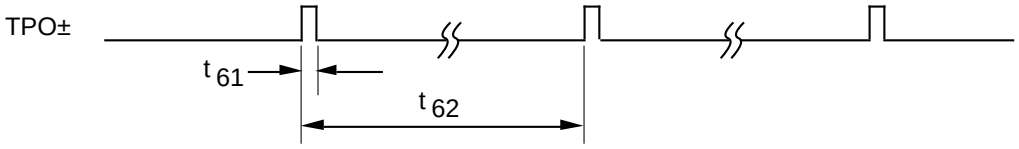
SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{61}	NLP Transmit Link Pulse Width	See Figure 5			ns	
t_{62}	NLP Transmit Link Pulse Period	8		24	ms	
t_{63}	NLP Receive Link Pulse Width Required For Detection	50			ns	
t_{64}	NLP Receive Link Pulse Minimum Period Required For Detection	3		5	ms	link_test_min
t_{65}	NLP Receive Link Pulse Maximum Period Required For Detection	50		150	ms	link_test_max link_loss
t_{66}	NLP Receive Link Pulses Required To Exit Link Fail State	3	3	3	Link Pulses	lc_max
t_{67}	FLP Transmit Link Pulse Width	See Figure 5			ns	
t_{68}	FLP Transmit Clock Pulse To Data Pulse Period	55.5	62.5	69.5	µs	
t_{69}	FLP Transmit Clock Pulse To Clock Pulse Period	111	125	139	µs	
t_{70}	FLP Transmit Link Pulse Burst Period	8		22	ms	
t_{71}	FLP Receive Link Pulse Width Required For Detection	50			ns	
t_{72}	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	5		25	µs	
t_{73}	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	µs	
t_{74}	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	µs	

LINK PULSE TIMING CHARACTERISTICS (continued)

Refer To Figures 16 and 17 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{75}	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	µs	
t_{76}	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t_{77}	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	ms	
t_{78}	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	ms	
t_{79}	FLP Receive Link Pulses Bursts Required To Detect NWay Capability	3	3	3	Link Pulse Bursts	
t_{80}	FLP Receive Acknowledge Fail Period	1200		1500	ms	
t_{81}	FLP Transmit Renegotiate Link Fail Period	1200		1500	ms	
t_{82}	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotation Has Completed	1200		1500	ms	

A.) Transmit NLP



B.) Receive NLP

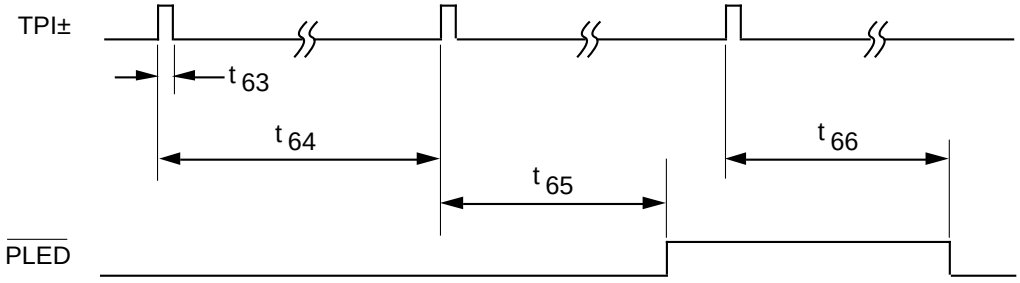
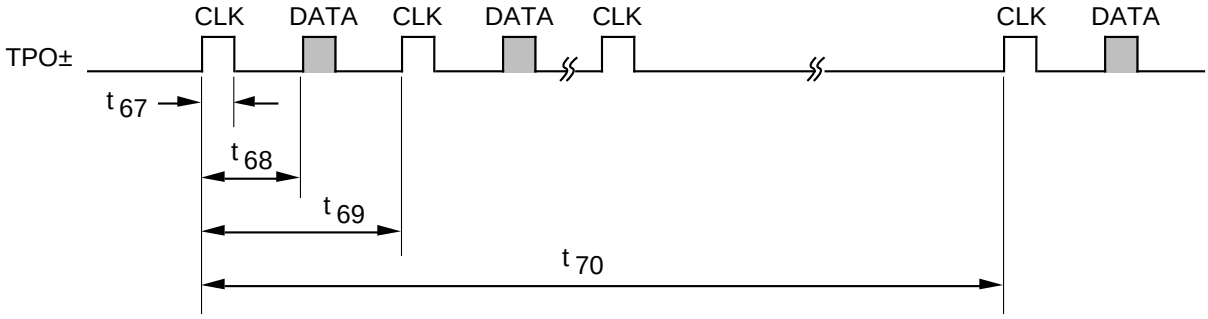
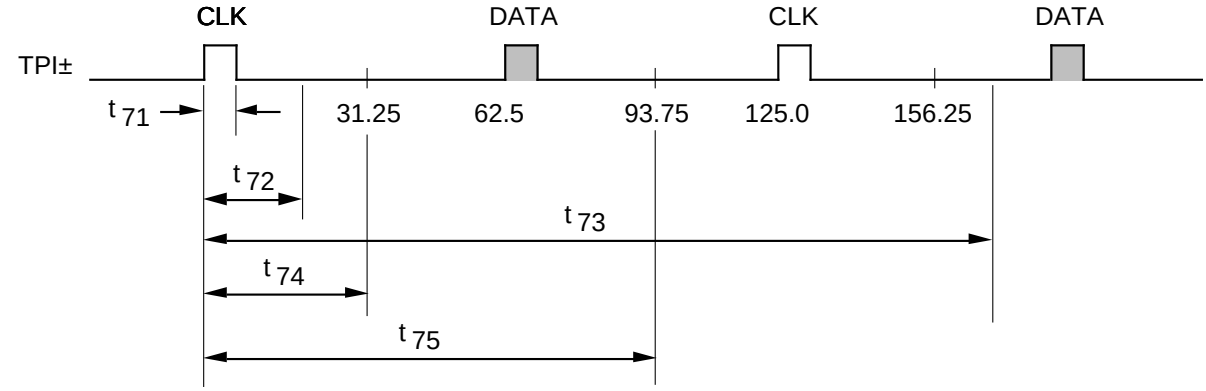


Figure 16. NLP Link Pulse Timing

A.) Transmit FLP and FLP Burst



B.) Receive FLP



C.) Receive FLP Burst

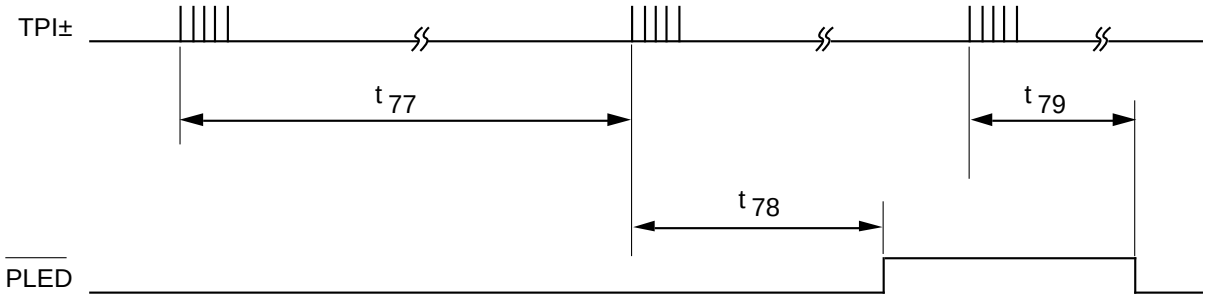


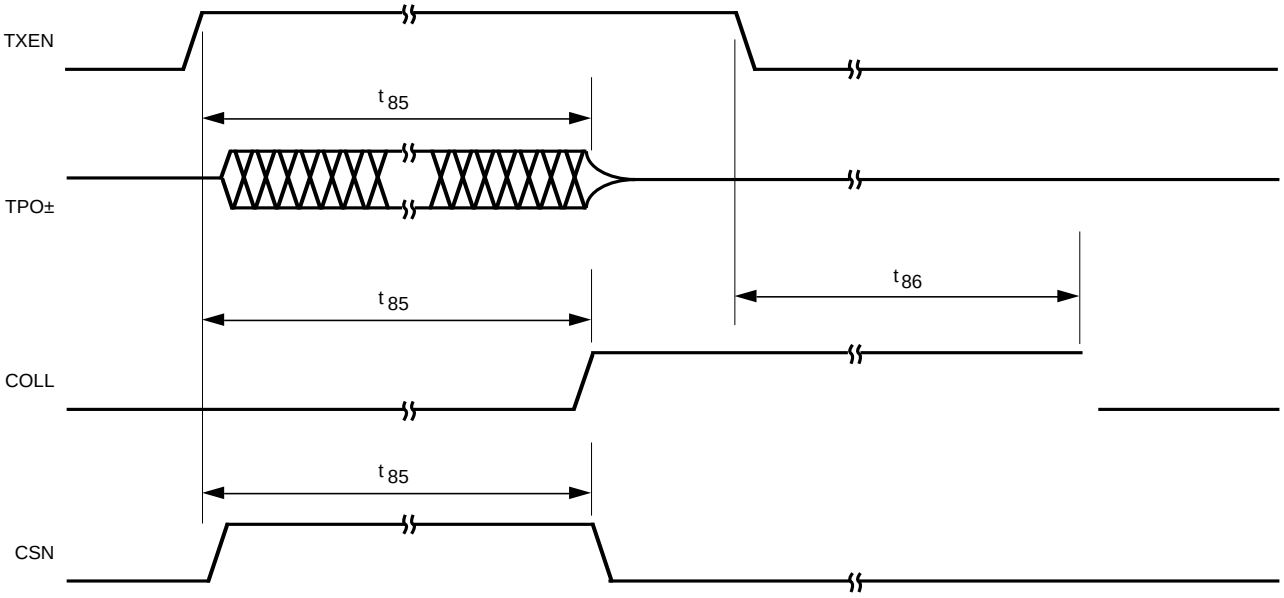
Figure 17. FLP Link Pulse Timing

JABBER TIMING CHARACTERISTICS

Refer To Figure 18 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{85}	Jabber Activation Delay Time	20		150	ms	
t_{86}	Jabber Deactivation Delay Time	250		750	ms	

SEEQ



NSC SAME AS SEEQ

INTEL SAME AS SEEQ EXCEPT COL IS INVERTED (ACTIVE LOW), CSN IS INVERTED (ACTIVE LOW), AND TXEN IS INVERTED (ACTIVE LOW)

AMD SAME AS SEEQ

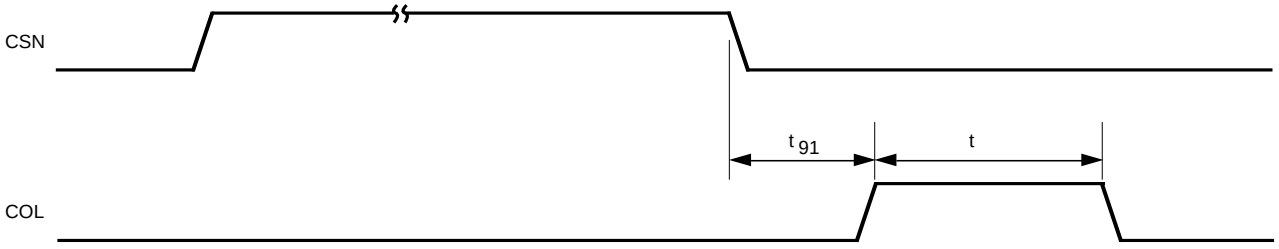
Figure 18. Jabber Timing

SQE TIMING CHARACTERISTICS

Refer To Figure 19 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{91}	SQE Pulse Delay	600		1600	ns	
t_{92}	SQE Pulse Width	900		1100	ns	

SEEQ



NSC SAME AS SEEQ

INTEL SAME AS SEEQ EXCEPT CSN IS INVERTED (ACTIVE LOW), COL IS INVERTED (ACTIVE LOW)

AMD SAME AS SEEQ

Figure 19. SQE Timing

LED DRIVER TIMING CHARACTERISTICS

Refer To Figure 20 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{96}	$\overline{\text{PLED[3:0]}}$ On Time	100		108	ms	
t_{97}	$\overline{\text{PLED[3:0]}}$ Off Time	100		108	ms	

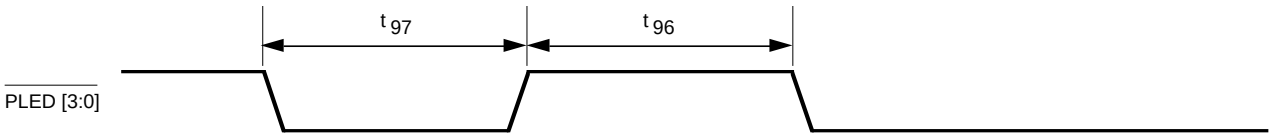


Figure 20. LED Driver Timing

SERIAL PORT TIMING CHARACTERISTICS

Refer To Figure 21 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{101}	SCLK Low Time	50			ns	
t_{102}	SCLK High Time	50			ns	
t_{103}	$\overline{CS}$ To SCLK Setup Time	25			ns	
t_{104}	$\overline{CS}$ To SCLK Hold Time	25			ns	
t_{105}	$\overline{CS}$ High Time	100			ns	
t_{106}	SDIO Setup Time	0			ns	Write Bits
t_{107}	SDIO Hold Time	25			ns	Write Bits
t_{108}	SCLK To SDIO Delay			25	ns	Read Bits
t_{109}	SDIO Hi-z To Active Delay			25	ns	Write-Read Transition
t_{110}	SDIO Active To Hi-z Delay			20	ns	Read-High Impedance Transition
t_{111}	$\overline{CS}$ Deassert To $\overline{INT}$ Transition			100	ns	

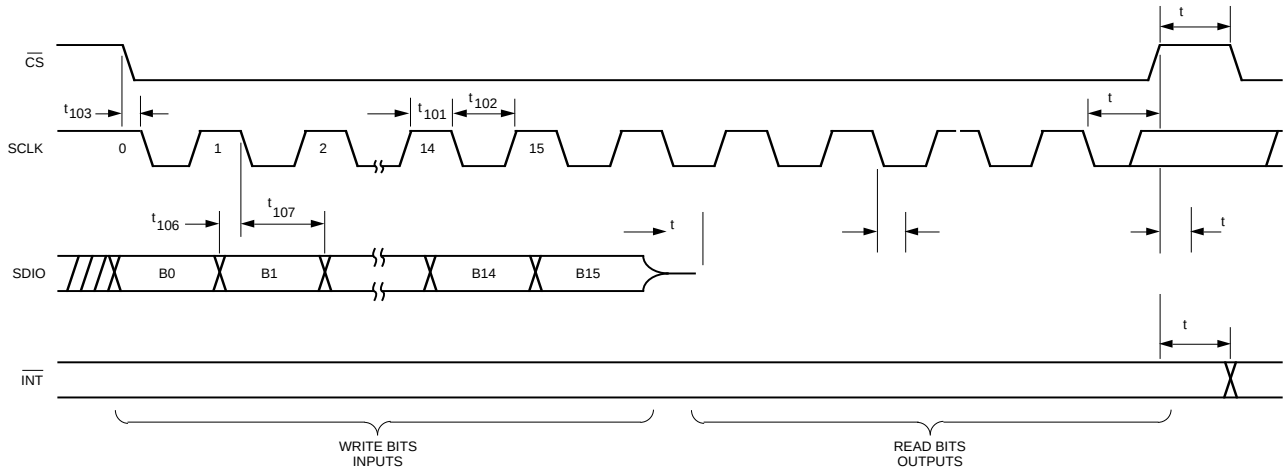
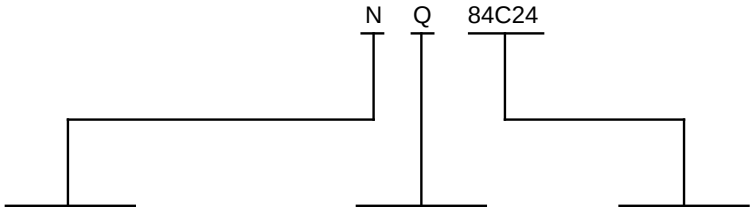


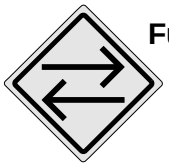
Figure 20. Serial Port Timing

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE
N = Plastic Leaded Chip Carrier	Q – 0°C to +70°C	4-Port ENDEC 10Base-T Transceiver

SEEQ Full Duplex Designation



Full Duplex

Symbol identifies product as Full Duplex device.

Revision History

6/18/96

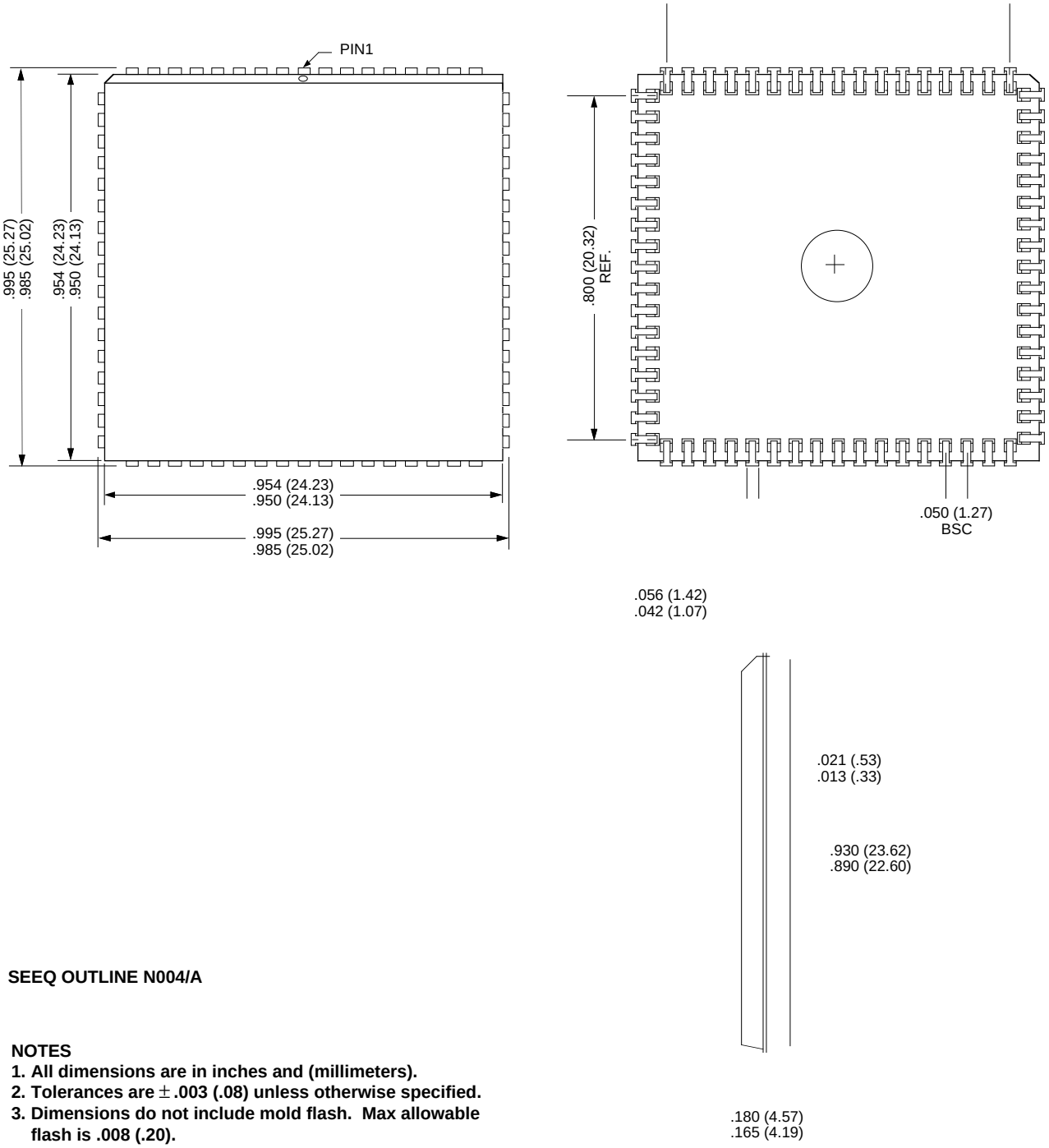
- Page 3, Pin Description: Pin (40, 36, 31, 27) I/O changed from O to I,
  : Pin (41, 37, 32, 28) I/O changed from O to I.
- Page 4, Pin Description: Pin (15, 16, 17, 19) I/O clarified,
  : Pin (14) I/O clarified.
- Page 22, Paragraph starting 'The 84C24 has special circuitry to reduce...' has been replaced with new copy.
- Page 26, Paragraph starting 'If no LED's are needed...' new copy has been added.
- Page 26, Figure 9 Serial Port Device Address Selection has been changed.
- Page 28, DC Electrical Characteristics: Test conditions 1. T_A = 0 to 70°C,
  : Input Low Voltage: (max) changed from V_{CC} –1.0 to V_{CC} –1.4,
  : Input Low Current (min) changed from –10 to –4,
  : Input Low Current (typ) deleted,
  : Output High Voltage, Conditions changed from IOL = 50µA to IOL = 4µA,
  : V_{CC} Supply Current (max) deleted,
  : V_{CC} Supply Current (typ) now 275,
  : V_{CC} Supply Current, Conditions now read, 'Transmitting, Current Into all V_{CC} Pins',
  : Input Low Current, Conditions clarified,
  : Input High Current Conditions clarified.
- Page 29, Twisted Pair Characteristics Transmit: Test conditions 1. T_A = 0 to 70° C,
  : TOIR (min) changed from 0.70 to 0.80,
  : TOIR (max) changed from 1.40 to 1.25,
  : TORA (max) changed from ± 25 to ± 50,
  : TORA (unit) is now % of Step,
  : TORA Conditions have been clarified,
  : TCMA deleted.

Revision History continued

- Page 30, Twisted pair Characteristics Receive: Test conditions 1. T_A = 0 to 70°C,
  : ROCV (min and max) has been deleted,
  : RCMR (min and max) has been deleted,
  : RCMR (typ) is now V_{CC} /3 ± 1.0,
  : RCRR (typ) is now -20,
  : RCRR (max) has been deleted.
- Page 31, AC Test Timing Conditions: Test Conditions 1. T_A = 0 to 70°C,
- Page 33, Receive Timing Characteristics: t_{41} (max) changed from 200 to 250,
  : t_{42} (min) changed from 150 to 125,
  : t_{42} (max) is now 200.
- Page 41, Link Pulse Timing Characteristics: t_{67} (min, typ, max) changed to see Figure 5.
- Page 48, Serial Port Timing Characteristics: t_{101} (min) changed from 40 to 50,
  : t_{102} (min) changed from 40 to 50,
  : t_{103} (min) changed from 20 to 25,
  : t_{104} (min) changed from 20 to 25,
  : t_{107} (min) changed from 20 to 25,
  : t_{108} (max) changed from 20 to 25,
  : t_{109} (max) changed from 20 to 25.

SURFACE MOUNT PACKAGES

68 PIN PLASTIC LEADED CHIP CARRIER TYPE N



SEEQ OUTLINE N004/A

NOTES
1. **All dimensions are in inches and (millimeters).**
2. **Tolerances are ± .003 (.08) unless otherwise specified.**
3. **Dimensions do not include mold flash. Max allowable flash is .008 (.20).**