Ultra-Low Power RS485 Transceiver with Shutdown

FEATURES

- **Low Power: I_{CC} = 120μA Max with Driver Disabled**
- I_{CC} = 500μA Max with Driver Enabled, No Load
- **Drivers/Receivers Have ±10kV ESD Protection**
- **1μA Quiescent Current in Shutdown Mode**
- **High Speed: Up to 2.5Mbits/s Data Rate**
- Single 5V Supply
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Up to 32 Transceivers on the Bus
- 30ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

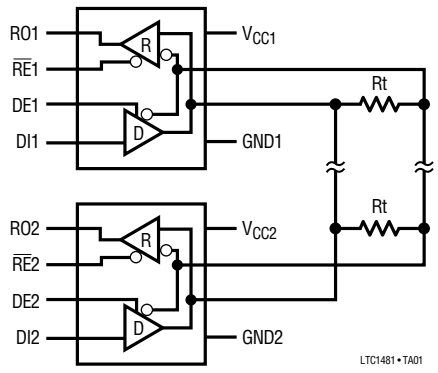
DESCRIPTION

The LTC®1481 is an ultra-low power differential line transceiver designed for data transmission standard RS485 applications. It will also meet the requirements of RS422. The CMOS design offers significant power savings over its bipolar counterparts without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 80μA while operating and less than 1μA in shutdown.

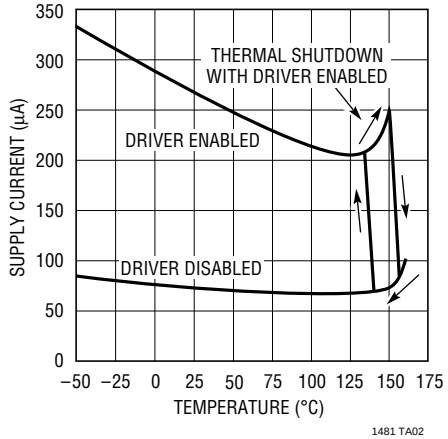
The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

The LTC1481 is fully specified over the commercial and extended industrial temperature range and is available in 8-pin DIP and SO packages.

TYPICAL APPLICATION



Supply Current vs Temperature

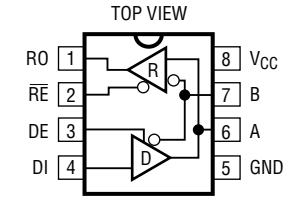


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range
LTC1481C ..... $0°C \le T_A \le 70°C$
LTC1481I ..... $-40°C \le T_A \le 85°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N8)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S8)

ORDER PART NUMBER
LTC1481CN8 LTC1481IN8 LTC1481CS8 LTC1481IS8
S8 PART MARKING
1481 1481I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485), Figure 1	● ●	2.0 1.5		 5	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = 12V DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = −7V	● ●			1.0 −0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V	●		45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, V_{ID} = 200mV	●	3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12			kΩ
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●		300 80	500 120	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

SWITCHING CHARACTERISTICS

V_{CC} = 5V (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 5)	●	10	30	60	ns
t_{PHL}	Driver Input to Output		●	10	30	60	ns
t_{SKEW}	Driver Output to Output		●		5	10	ns
t_r, t_f	Driver Rise or Fall Time		●	3	15	40	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●		40	70	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4, 6), S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4, 6), S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 7)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output		●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
f_{MAX}	Maximum Data Rate		●	2.5			Mbits/s
t_{SHDN}	Time to Shutdown	DE = 0, $\overline{RE}$ = ⊥	●	50	200	600	ns
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●		40	100	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●		40	100	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 2, 8), S2 Closed	●			3500	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 2, 8), S1 Closed	●			3500	ns

The ● denotes specifications which apply over the full operating temperature range.

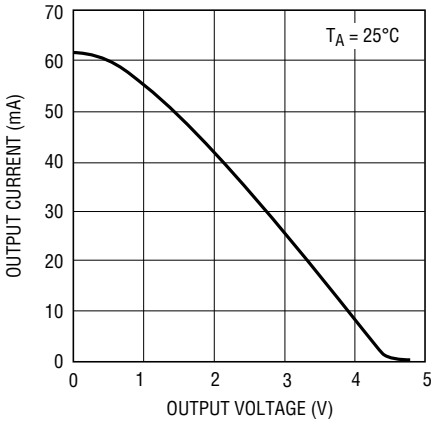
Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

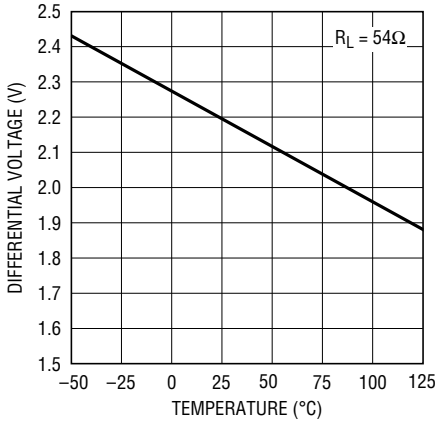
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

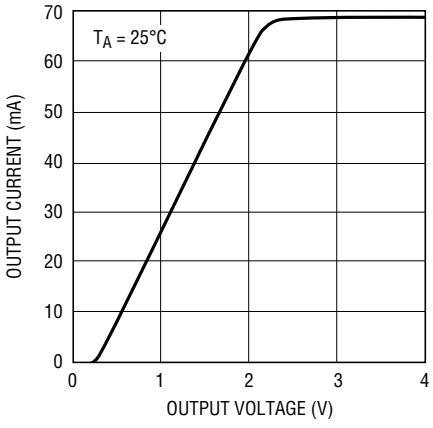
Driver Differential Output Voltage vs Output Current



Driver Differential Output Voltage vs Temperature

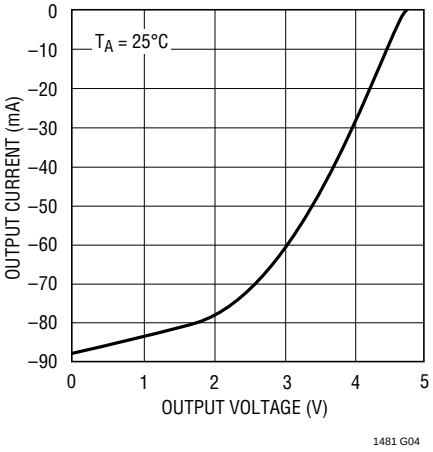


Driver Output Low Voltage vs Output Current



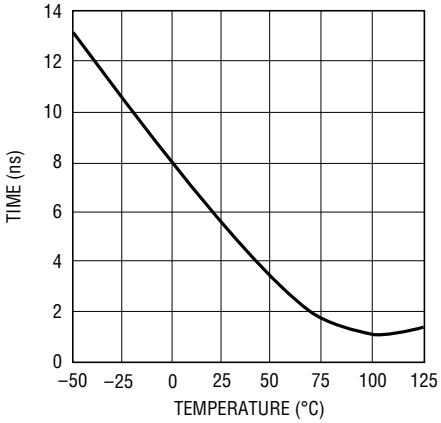
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output High Voltage vs Output Current



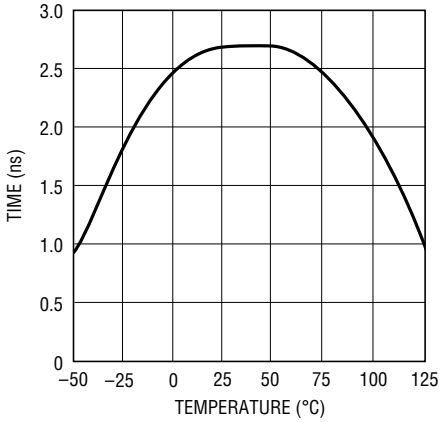
1481 G04

Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



1481 G05

Driver Skew vs Temperature



1481 G05

PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A high on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is low, the part will enter a low power (1μA) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE high) then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 4.75V < V_{CC} < 5.25V.

FUNCTION TABLES

LTC1481 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode for LTC1481

LTC1481 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode for LTC1481

TEST CIRCUITS

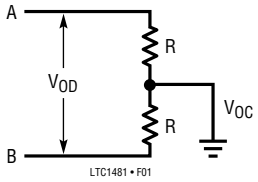


Figure 1. Driver DC Test Load

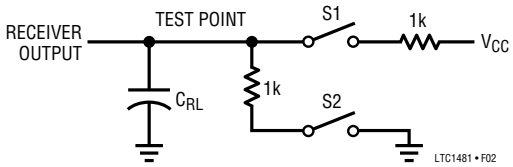


Figure 2. Receiver Timing Test Load

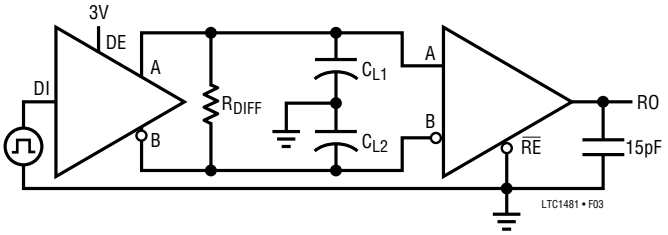


Figure 3. Driver/Receiver Timing Test Circuit

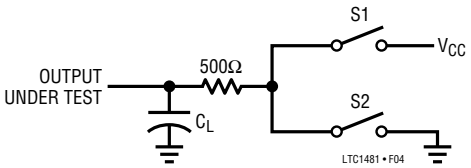


Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

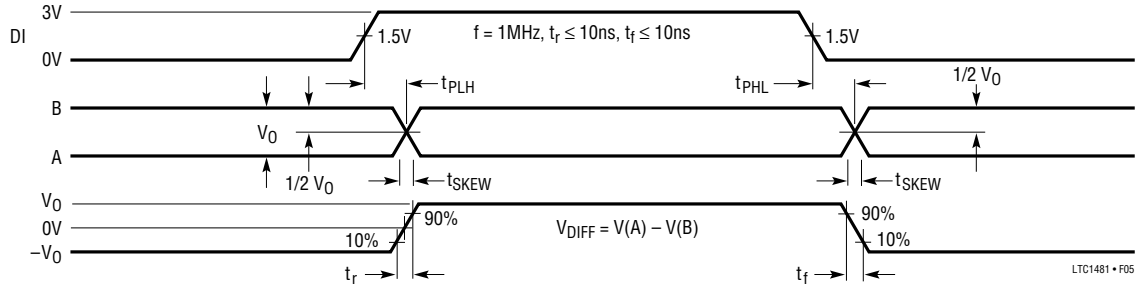


Figure 5. Driver Propagation Delays

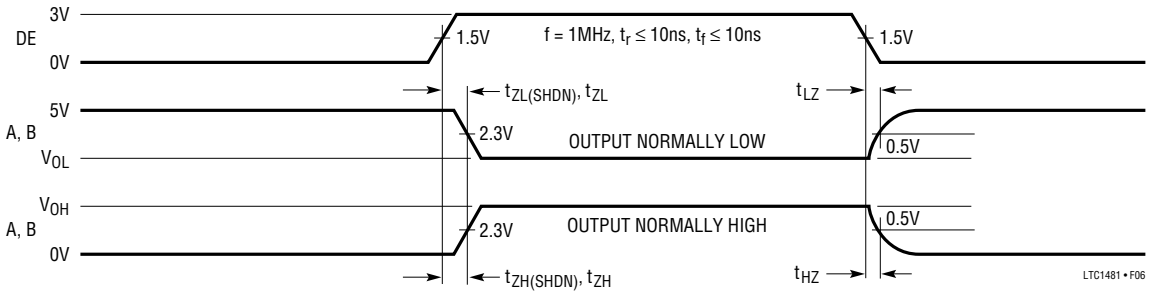


Figure 6. Driver Enable and Disable Times

SWITCHING TIME WAVEFORMS

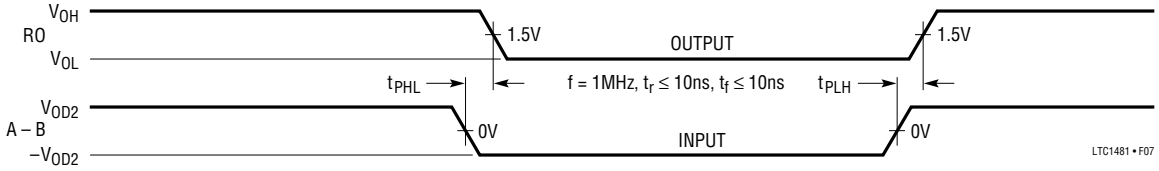


Figure 7. Receiver Propagation Delays

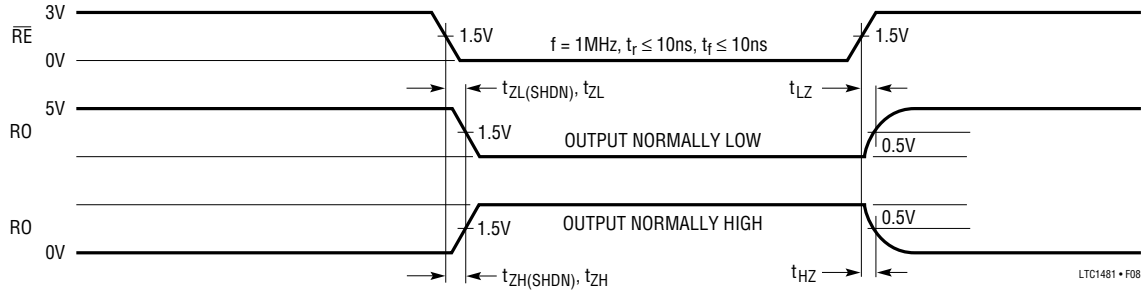


Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Basic Theory of Operation

Traditionally, RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latch-up. Unfortunately, most bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC1481 is a CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latch-up immunity.

The LTC1481 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latch-up and providing excellent ESD protection. Figure 9 shows the LTC1481 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode (D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well-known CMOS latch-up condition, which could destroy the device.

The LTC1481 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diode D1 or D2 still turns on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latch-up is virtually eliminated under power-up or power-down conditions.

APPLICATIONS INFORMATION

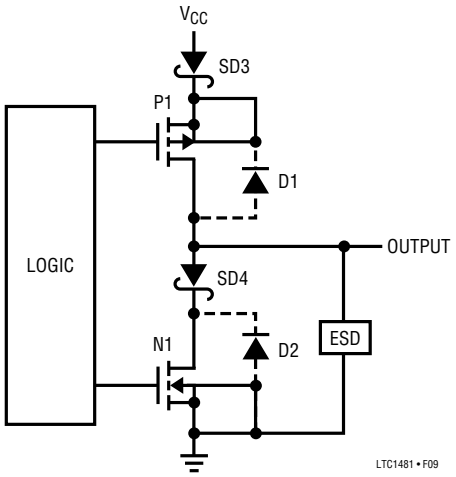


Figure 9. LTC1481 Output Stage

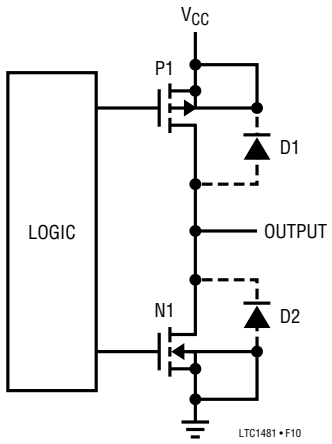


Figure 10. Conventional CMOS Output Stage

The LTC1481 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is well beyond the RS485 operating range. Because the ESD injected current in the N-well or substrate consists of majority carriers, latch-up is prevented by careful layout techniques. An ESD cell protects output against multiple 10kV human body model ESD strikes.

Low Power Operation

The LTC1481 is designed to operate with a quiescent current of 120µA max. With the driver in three-state, I_{CC} will drop to this 120µA level. With the driver enabled there will be additional current drawn by the internal 12k resistor. Under normal operating conditions this additional current is overshadowed by the current drawn by the external bus impedance.

Shutdown Mode

Both the receiver output (RO) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ high and DE low respectively. In addition, the LTC1481 will enter shutdown mode when $\overline{RE}$ is high and DE is low.

In shutdown the LTC1481 typically draws only 1µA of supply current. In order to guarantee that the part goes into shutdown, DE must be low and $\overline{RE}$ must be high for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode. Toggling either $\overline{RE}$ or DE will wake the LTC1481 back up within 3.5µs.

Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and receiver. Figure 11 shows the test circuit for the LTC1481 propagation delay.

The receiver delay times are:

$|t_{PLH} - t_{PHL}|$ = 13ns Typ, V_{CC} = 5V

The drivers skew times are:

Skew = 5ns Typ, V_{CC} = 5V

10ns Max, V_{CC} = 5V, T_A = –40°C to 85°C

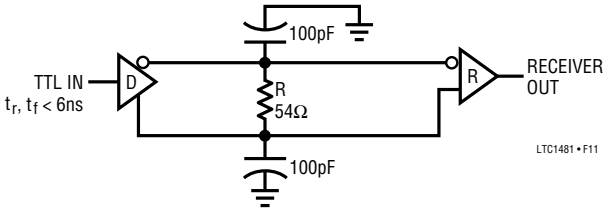
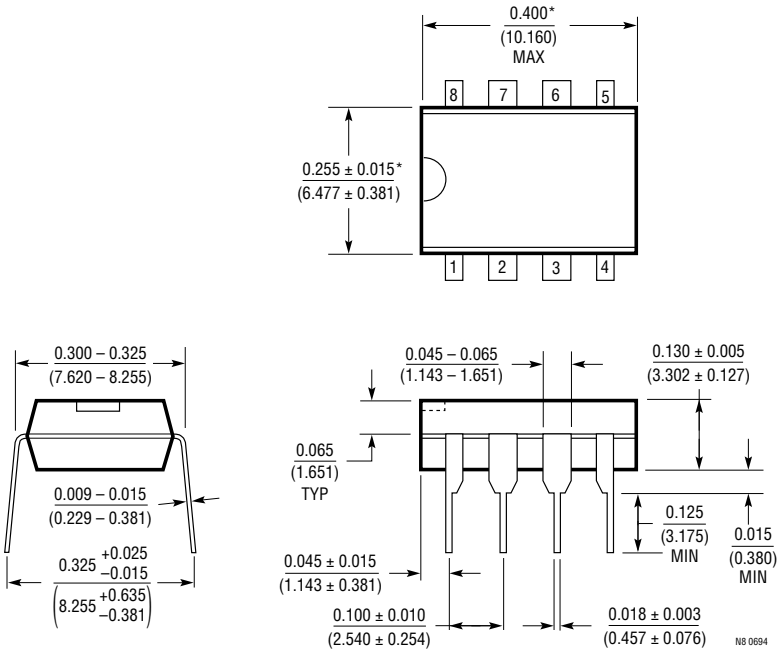


Figure 11. Receiver Propagation Delay Test Circuit

PACKAGE DESCRIPTION

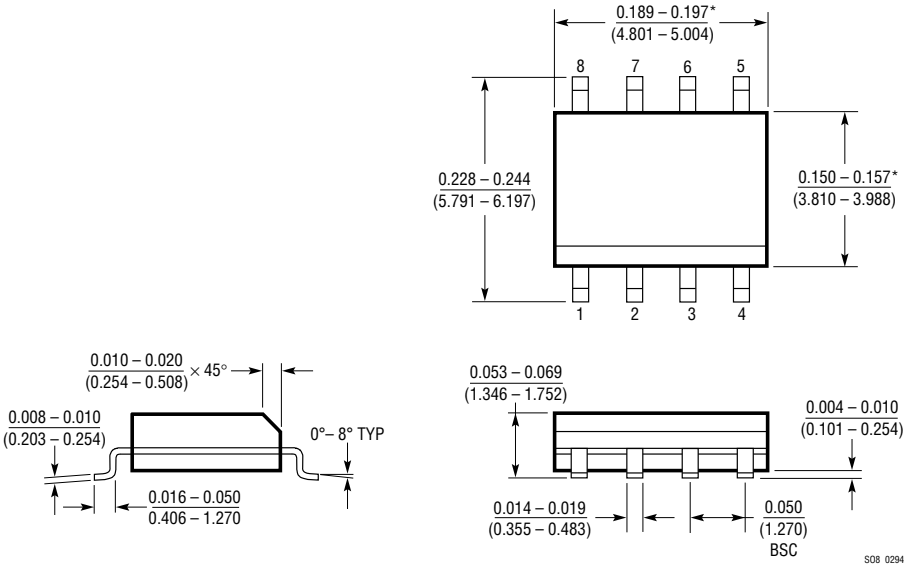
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTURSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

S8 Package
8-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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