ORCA® ORLI10G

Quad 2.5Gbps, 10Gbps
Quad 3.125Gbps, 12.5Gbps Line Interface FPSC

February 2003 **Data Sheet**

Introduction

Lattice has developed a new *ORCA* Series 4-based FPSC which combines a high-speed line interface with a flexible FPGA logic core. Built on the Series 4 reconfigurable embedded System-on-a-Chip (SoC) architecture, the ORLI10G consists of an OIF standard compliant (OIF-SFI4-01.0) SFI-4.1 or *IEEE*® 802.3ae compliant XSBI, 10 Gbits/s or 12.5 Gbits/s transmit and 10 Gbits/s or 12.5 Gbits/s receive line interface.

Both transmit and receive interfaces consist of 16-bit LVDS data at up to 850 Mbits/s, integrated transmit and receive programmable PLLs for data rate conversions between the line-side and system-side data rates, and a programmable logic interface at the system end for use with SONET/SDH, Ethernet, or OTN/digital wrapper with strong FEC system device data standards. In addition to the embedded functionality, the device includes over 400k of usable FPGA gates. The line interface includes logic to divide the data rate down to 212 MHz or less (1/4 line rate) or 106 MHz or less (1/8 line rate) for transfer to the FPGA logic. The ORLI10G is designed to connect to a plethora of industry standard devices on the line side. The programmable logic interface on the system side allows direct connection to a 10 Gbits/s Ethernet MAC, a 10 Gbits/s SONET/SDH framer/data engine, or a 10 Gbits/s/12.5 Gbits/s digital wrapper/FEC framer/data engine.

For 10 Gbits/s Ethernet, the ORLI10G supports the Physical Coding Sublayer (PCS), interfaces to the Physical Media Attachment (PMA), and connects to the system interface (host or switch) for the proposed *IEEE* 802.3ae 10 Gbits/s serial LAN PHY.

The ORLI10G FPSC is a high-speed programmable device for 10 Gbits/s data solutions. It can be used as the interface between the line interface and the system interface in a variety of emerging networks, including 10 Gbits/s SONET/SDH (OC-192/STM-48), 10 Gbits/s Optical Transport Networks (OTN) using digital wrapper and strong FEC, or 10 Gbits/s Ethernet. Other functions include use in quad OC-48/ STM-16 SONET/SDH systems, interfaces between quad OC-48/STM-16 and OC-192/STM-64 components, and use as a generic data transfer mechanism between two devices at 10 Gbits/s rates. Data is received at the line interface and then sent to either a 4-bit or 8-bit serial-to-parallel converter. On the transmit interface, either a 4-bit or 8-bit parallel-to-serial converter is used. Thus, the data rate at the internal FPGA interface is either 1/4 or 1/8 the line rate.

The programmable PLLs on the ORLI10G provide for great flexibility in handling clock rate conversion due to differing amounts of overhead bits in various system data standards. For example, the ORLI10G can divide down the STS-192/STM-64 SONET/SDH data line rate of 622 MHz by 4 to synchronize with a 155 MHz system clock, or the 12.5 Gbits/s Super-FEC data line rate of 781 MHz can be divided by 8 MHz to 98 MHz system clock or by 8 x 4/5 to provide a 78 MHz system data rate.

Table 1. ORCA ORLI10G–Available FPGA Logic (equivalent to ORCA OR4E04)

Device	PFU Rows	PFU Columns	Total PFUs	FPGA Max. User I/Os*	LUTs	EBR Blocks	EBR Bits (k)	FPGA System Gates (k)
ORLI10G	36	36	1,296	316	10,368	12	111	333—643

* 316 are available in the 680 PBGAM package.

Note: The embedded core, embedded system bus, FPGA interface and MPI are not included in the above gate counts. The System Gate ranges are derived from the following: minimum system gates assumes 100% of the PFUs are used for logic only (no PFU RAM) with 40% EBR usage and 2 PLLs. Maximum system gates assumes 80% of the PFUs are for logic, 20% are used for PFU RAM, with 80% EBR usage and 6 PLLs.

Embedded Function Features

- Provides a line-interface to system-interface with various system standards such as OC-192/STM-64 SONET/SDH, quad OC-48/STM-16 10 Gbits/s Ethernet, and 10 Gbits/s OTN (digital wrapper/strong FEC) or 12.5 Gbits/s SuperFEC.
- Embedded PLLs with programmable M/N multiplication/division values provide flexible data rate conversion between line side and system side.
- Line-side supports 16-bit LVDS data with multiple line frequencies supported up to 850 MHz, depending on system standard.
- Line-side interface, including timing and jitter specifications, compliant to OIF 99.102.5 standard.
- Receive-side interface can be split into four separate asynchronous 2.5 Gbits/s interfaces (4-bit LVDS data interface for each) with a separate clock for each for transfer to the FPGA logic.
- Data and clock rates divided by 4 or 8 for use in FPGA logic.
- LVDS I/Os compliant with *EIA*®-644 support hot insertion. All embedded LVDS I/Os include both input and output on-board termination to allow high-speed operation.
- Low-power LVDS buffers.

Intellectual Property Features

Programmable logic provides a variety of yet-to-be standardized interface functions, including the following IP core functions:

- 10 Gbits/s Ethernet Physical Coding Sublayer (PCS), as defined by *IEEE* 802.3ae:
  - XGMII for interfacing to 10 Gbits/s Ethernet MACs. XGMII is a 156 MHz double data rate parallel short-reach (typically less than 3 in.) interconnect interface.
  - Elastic store buffers for clock domain transfer to/from the XGMII interface.
  - $X^{59} + X^{39} + X^{1}$ scrambler/descrambler for 10 Gbits/s Ethernet.
  - 64b/66b encoders/decoders for 10 Gbits/s Ethernet.
  - Idle insertion and deletion.
  - SMI interface for control and status.
- Quad 2.5 Gbits/s SONET/SDH to 10 Gbits/s SONET/SDH MUX/deMUX functions.

Programmable Features

- High-performance programmable logic:
  - 0.16 µm 7-level metal technology.
  - Internal performance of >250 MHz.
  - Over 400k usable FPGA system gates.
  - Meets multiple I/O interface standards.
  - 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - LVTTL (3.3 V) and LVCMOS (2.5 V, and 1.8 V) I/Os.
  - Per pin selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - Individually programmable drive capability:
    24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - Two slew rates supported (fast and slew limited).
  - Fast-capture input latch and input Flip-Flop latch for reduced input setup time and zero hold time.
  - Fast open-drain drive capability.
  - Capability to register 3-state enable signal.
  - Off-chip clock drive capability.
  - Two input function generator in output path.

- New programmable high-speed I/O:
  - Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - Double-ended: LVDS, bused-LVDS, LVPECL. Programmable (on/off) internal parallel termination (100 Ω) also supported for these I/Os.
- New capability to (de)multiplex I/O signals:
  - New DDR on both input and output at rates up to 350 MHz (700 MHz effective rate).
  - New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-quad Programmable Function Unit (PFU):
  - Eight 16-bit Look-Up Tables (LUTs) per PFU.
  - Nine user registers per PFU, one following each LUT, organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 : 1 MUX, new 8 : 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - Soft-Wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing, which reduces routing congestion and improves speed.
  - Flexible fast access to PFU inputs from routing.
  - Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-stable buffers, up to a 10-bit decoder, and *PAL*™-like AND-OR-INVERT (AOI) in each programmable logic cell.
- New 200 MHz embedded quad-port RAM blocks, two read ports, two write ports, and two sets of byte lane enables. Each embedded RAM block can be configured as:
  - 1—512 x 18 (quad-port, two read/two write) with optional built-in arbitration.
  - 1—256 x 36 (dual-port, one read/one write).
  - 1—1k x 9 (dual-port, one read/one write).
  - 2—512 x 9 (dual-port, one read/one write for each).
  - 2 RAMs with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - Supports joining of RAM blocks.
  - Two 16 x 8-bit Content Addressable Memory (CAM) support.
  - FIFO 512 x 18, 256 x 36, 1k x 9, or dual 512 x 9.
  - Constant multiply (8 x 16 or 16 x 8).
  - Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, MicroProcessor Interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - Full boundary scan (*IEEE* 1149.1 and draft 1149.2 JTAG) for the programmable I/Os only.
  - Programming and readback through boundary-scan port compliant to *IEEE* Draft 1532:D1.7.
  - TS_ALL testability function to 3-state all I/O pins.
  - New temperature-sensing diode.
- Improved built-in clock management with Programmable Phase-Locked Loops (PPLLs) provides optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to

420 MHz. Multiplication of input frequency up to 64x and division of input frequency down to 1/64x is possible.

- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also supports compliance with many setup/hold and clock-to-out I/O specifications, and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC*®/PowerQUICC 860, and *PowerPC*/PowerQUICC II MPC8260 high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard-cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space is provided.
- New embedded *AMBA*™ specification 2.0 AHB system bus (*ARM*® processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard cell blocks.
- Variable-size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E04).
- New local clock routing structures allow creation of localized clock trees.
- Two new edge clock structures allow up to six highspeed clocks on each edge of the device for improved setup/hold and clock-to-out performance.
- New Double-Data Rate (DDR) and Zero-Bus Turn-around (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced-speed internal logic.
- ispLEVER development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets Universal Test and Operations PHY Interface for ATM (UTOPIA) Levels 1, 2, and 3 as well as POS-PHY3. Also meets proposed specifications for UTOPIA Level 4 and POS-PHY4 for 10 Gbits/s interfaces.
- Meets POS-PHY3 (2.5 Gbits/s) and POS-PHY4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.

Description

FPSC Definition

FPSCs, or Field-Programmable System Chips, are devices that combine field-programmable logic with ASIC, or mask-programmed logic, on a single device. FPSCs provide the time to market and the flexibility of FPGAs, the design effort savings of using soft intellectual property (IP) cores, and the speed, design density, and economy of ASICs.

FPSC Overview

Lattice's Series 4 FPSCs are created from Series 4 *ORCA* FPGAs. To create a Series 4 FPSC, several columns of programmable logic cells (see FPGA Logic Overview section for FPGA logic details) are added to an embedded logic core. Other than replacing some FPGA gates with ASIC gates, at greater than 10:1 efficiency, none of the FPGA functionality is changed; all of the Series 4 FPGA capability is retained: embedded block RAMs, MPI, PCMs, boundary scan, etc. Columns of programmable logic are replaced on one side of the device, allowing pins from the replaced columns to be used as I/O pins for the embedded core. The remainder of the device pins retain their FPGA functionality.

FPSC Gate Counting

The total gate count for an FPSC is the sum of its embedded core (standard-cell/ASIC gates) and its FPGA gates. Because FPGA gates are generally expressed as a usable range with a nominal value, the total FPSC gate count is sometimes expressed in the same manner. Standard-cell ASIC gates are, however, 10 to 25 times more silicon-area efficient than FPGA gates. Therefore, an FPSC with an embedded function is gate equivalent to an FPGA with a much larger gate count.

FPGA/Embedded Core Interface

The interface between the FPGA logic and the embedded core has been enhanced to provide a greater number of interface signals than on previous FPSC architectures. Compared to bringing embedded core signals off-chip, this on-chip interface is much faster and requires less power. All of the delays for the interface are precharacterized and accounted for in the ispLEVER Development System.

Series 4-based FPSCs expand this interface by providing a link between the embedded block and the multimaster 32-bit system bus in the FPGA logic. This system bus allows the core easy access to many of the FPGA logic functions, including the embedded block RAMs and the microprocessor interface.

Clock spines also can pass across the FPGA/embedded core boundary. This allows fast, low-skew clocking between the FPGA and the embedded core. Many of the special signals from the FPGA, such as DONE and global set/reset, are also available to the embedded core, making it possible to fully integrate the embedded core with the FPGA as a system.

For even greater system flexibility, FPGA configuration RAMs are available for use by the embedded core. This supports user-programmable options in the embedded core, in turn allowing greater flexibility. Multiple embedded core configurations may be designed into a single device with user-programmable control over which configurations are implemented, as well as the capability to change core functionality simply by reconfiguring the device.

ispLEVER Development System

The ispLEVER development system is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture and then place and route it using ispLEVER's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The ispLEVER development system interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow, the design entry and the bit stream generation stage. Recent improvements in ispLEVER allow the user to provide

timing requirement information through logical preferences only; thus, the designer is not required to have physical knowledge of the implementation.

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. A floor planner is available for layout feedback and control. A static timing analysis tool is provided to determine design speed, and a back-annotated netlist can be created to allow simulation and timing.

Timing and simulation output files from ispLEVER are also compatible with many third-party analysis tools. A bit stream generator is then used to generate the configuration data which is loaded into the FPGAs internal configuration RAM, embedded block RAM, and/or FPSC memory.

When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, ispLEVER produces configuration data that implements the various logic and routing options discussed in this data sheet.

FPSC Design Kit

Development is facilitated by an FPSC design kit which, together with ispLEVER software and third-party synthesis and simulation engines, provides all software and documentation required to design and verify an FPSC implementation. Included in the kit are the FPSC configuration manager, *Synopsys Smart Model* ®, and/or compiled *Verilog* ® simulation model, *HSPICE* ® and/or IBIS models for I/O buffers, and complete online documentation. The kit's software couples with ispLEVER software, providing a seamless FPSC design environment. More information can be obtained by visiting the Lattice website at www.latticesemi.com or contacting a local sales office.

FPGA Logic Overview

The *ORCA* Series 4 architecture is a new generation of SRAM-based programmable devices from Lattice. It includes enhancements and innovations geared toward today's high-speed systems on a single chip. Designed with networking applications in mind, the Series 4 family incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 4 devices contain many new patented enhancements and are offered in a variety of packages and speed grades.

The hierarchical architecture of the logic, clocks, routing, RAM, and system-level blocks create a seamless merge of FPGA and ASIC designs. Modular hardware and software technologies enable System-on-a-Chip integration with true plug-and-play design implementation.

The architecture consists of four basic elements: Programmable Logic Cells (PLCs), Programmable I/O cells (PIOs), Embedded Block RAMs (EBRs), and system level features. These elements are interconnected with a rich routing fabric of both global and local wires. An array of PLCs are surrounded by common interface blocks which provide an abundant interface to the adjacent PLCs or system blocks. Routing congestion around these critical blocks is eliminated by the use of the same routing fabric implemented within the programmable logic core. Each PLC contains a PFU, (Supplementary Logic Interconnect) SLIC, local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU, but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC. The PIOs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, uplink and downlink functions, and other functions on two output signals. Large blocks of 512 x 18 quadport RAM complement the existing distributed PFU memory. The RAM blocks can be used to implement RAM, ROM, FIFO, multiplier, and CAM. Some of the other system-level functions include the MPI, PLLs, and the Embedded System Bus (ESB).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) LUTs, eight latches/Flip-Flops, and one additional Flip-Flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion; two sets of four LUTs and Flip-Flops that can be controlled independently. Each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth Flip-Flop for pipelining. Each PFU may also be

configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The Flip-Flops (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The Flip-Flops also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected from PLC routing resources and from the outputs of the PFU. It contains eight 3-state, bidirectional buffers, and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections from the PFU outputs make fast, true, 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

Programmable I/O

The Series 4 PIO addresses the demand for the flexibility to select I/Os that meet system interface requirements. I/Os can be programmed in the same manner as in previous *ORCA* devices, with the additional new features that allow the user the flexibility to select new I/O types that support high-speed interfaces.

Each PIO contains four programmable I/O pads and is interfaced through a common interface block to the FPGA array. The PIO is split into two pairs of I/O pads with each pair having independent clock enables, local set/reset, and global set/reset. On the input side, each PIO contains a programmable latch/Flip-Flop which enables very fast latching of data from any pad. The combination provides very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer with a PFU.

On the output side of each PIO, an output from the PLC array can be routed to each output Flip-Flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows multiplexing of output signals and other functions of two output signals.

The output Flip-Flop, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The output buffer signal can be inverted, and the 3-state control can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered.

The Series 4 I/O logic has been enhanced to include modes for speed uplink and downlink capabilities. These modes are supported through shift register logic, which divides down incoming data rates or multiplies up outgoing data rates. This new logic block also supports high-speed DDR mode requirements where data is clocked into and out of the I/O buffers on both edges of the clock.

The new programmable I/O cell allows designers to select I/Os which meet many new communication standards, permitting the device to hook up directly without any external interface translation. They support traditional FPGA standards as well as high-speed, single-ended, and differential-pair signaling. Based on a programmable, bank-oriented I/O ring architecture, designs can be implemented using 3.3 V, 2.5 V, 1.8 V, and 1.5 V referenced output levels.

Routing

The abundant routing resources of the Series 4 architecture are organized to route signals individually or as buses with related control signals. Both local and global signals utilize high-speed buffered and nonbuffered routes. One PLC segmented (x1), six PLC segmented (x6), and bused half-chip (xHL) routes are patterned together to provide high connectivity with fast software routing times and high-speed system performance.

Eight fully distributed primary clocks are routed on a low-skew, high-speed distribution network and may be sourced from dedicated I/O pads, PLLs, or the PLC logic. Secondary and edge-clock routing are available for fast regional clock or control signal routing for both internal regions and on device edges. Secondary clock routing can be sourced from any I/O pin, PLLs, or the PLC logic.

The improved routing resources offer great flexibility in moving signals to and from the logic core. This flexibility translates into an improved capability to route designs at the required speeds when the I/O signals have been locked to specific pins.

System-Level Features

The Series 4 also provides system-level functionality by means of its microprocessor interface, embedded system bus, quad-port embedded block RAMs, universal programmable phase-locked loops, and the addition of highly tuned networking specific phase-locked loops. These functional blocks support easy glueless system interfacing and the capability to adjust to varying conditions in today's high-speed networking systems.

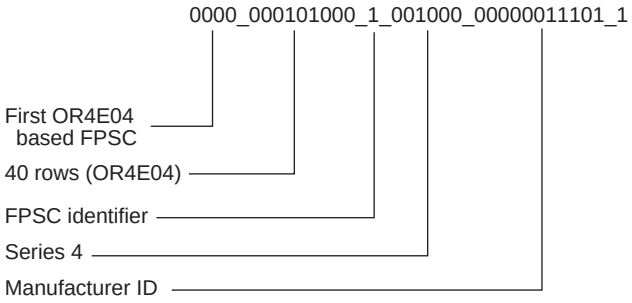
Microprocessor Interface

The MPI provides a glueless interface between the FPGA and *PowerPC* microprocessors. Programmable in 8-bit, 16-bit, and 32-bit interfaces with optional parity to the *Motorola* ® *PowerPC* 860 bus, it can be used for configuration and readback, as well as for FPGA control and monitoring of FPGA status. All MPI transactions utilize the Series 4 embedded system bus at 66 MHz performance.

The MPI provides, following configuration, a system-level microprocessor interface through the system bus to the user-defined logic within the FPGA, and includes access to the embedded block RAM. The MPI supports burst data read and write transfers, allowing short, uneven transmission of data through the interface by including data FIFOs. Transfer accesses can be single beat (1 x 4 bytes or less), 4-beat (4 x 4 bytes), 8-beat (8 x 2 bytes), or 16-beat (16 x 1 bytes).

The 32-bit device identification code (device_id) for the ORLI10G is at system bus register address 0x0-0x3. (see Figure 1.)

Figure 1. ORLI10G 32-bit Device Identification Code



System Bus

An on-chip, multimaster, 8-bit system bus with 1-bit parity facilitates communication among the MPI, configuration logic, FPGA control, and status registers, embedded block RAMs, as well as user logic. Utilizing the *AMBA* specification Rev 2.0 AHB protocol, the embedded system bus offers arbiter, decoder, master, and slave elements.

The system bus control registers can provide control to the FPGA such as signaling for reprogramming, reset functions, and PLL programming. Status registers monitor INIT, DONE, and system bus errors. An interrupt controller is integrated to provide up to eight possible interrupt resources. Bus clock generation can be sourced from the microprocessor interface clock, configuration clock (for slave configuration modes), internal oscillator, user clock from routing, or port clock (for JTAG configuration modes). In the ORLI10G FPSC, the system bus is not connected to the embedded core.

Phase-Locked Loops

Four user PLLs are provided for ORCA Series 4 FPSCs. Programmable PLLs can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Each PPLL is capable of manipulating and conditioning clocks

from 20 MHz to 420 MHz. Frequencies can be adjusted from 1/8x to 8x (the input clock frequency). Each programmable PLL provides two outputs that have different multiplication factors but can have the same phase relationships. Duty cycles and phase delays can be adjusted in 12.5% of the clock period increments. An automatic input buffer delay compensation mode is available for phase delay. Each PPLL provides two outputs that can have programmable (12.5% steps) phase differences.

Additional highly tuned and characterized Dedicated Phase-Locked Loops (DPLLs) are included to ease system designs. These DPLLs meet ITU-T G.811 primary clocking specifications and enable system designers to very tightly target specified clock conditioning not traditionally available in the universal PPLLs. Initial DPLLs are targeted to low-speed networking DS1 and E1, and also high-speed SONET/SDH networking STS-3 and STM-1 systems.

Embedded Block RAM

New 512 x 18 quad-port RAM blocks are embedded in the FPGA core to significantly increase the amount of memory and complement the distributed PFU memories. The EBRs include two write ports, two read ports, and two byte lane enables which provide four-port operation. Optional arbitration between the two write ports is available, as well as direct connection to the high-speed system bus.

Additional logic has been incorporated to allow significant flexibility for FIFO, constant multiply, and two-variable multiply functions. The user can configure FIFO blocks with flexible depths of 512k, 256k, and 1k, including asynchronous and synchronous modes and programmable status and error flags. Multiplier capabilities allow a multiple of an 8-bit number with a 16-bit fixed coefficient or vice versa (24-bit output), or a multiply of two 8-bit numbers (16-bit output). On-the-fly coefficient modifications are available through the second read/write port. Two 16 x 8-bit CAMs per embedded block can be implemented in single match, multiple match, and clear modes. The EBRs can also be preloaded at device configuration time.

Configuration

The FPGAs functionality is determined by internal configuration RAM. The FPGAs internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The configuration data can reside externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low, pin-count method for configuring FPGAs.

The RAM is loaded by using one of several configuration modes. Supporting the traditional master/slave serial, master/slave parallel, and asynchronous peripheral modes, the Series 4 also utilizes its microprocessor interface and embedded system bus to perform both programming and readback. Daisy chaining of multiple devices and partial reconfiguration are also permitted.

Other configuration options include the initialization of the embedded-block RAM memories and FPSC memory as well as system bus options and bit stream error checking. Programming and readback through the JTAG (*IEEE* 1149.2) port is also available meeting in-system programming (ISP) standards (*IEEE* 1532 Draft).

Additional Information

Contact your local Lattice representative for additional information regarding the *ORCA* Series 4 FPGA and FPSC devices, or visit our website at: http://www.latticesemi.com

ORLI10G Overview

Device Layout

The ORLI10G FPSC provides a high-speed transmit and receive line interface combined with FPGA logic. The device is based on the 1.5 V OR4E04 FPGA. The ORLI10G consists of an embedded backplane transceiver core and a full OR4E04 36x36 FPGA array.

The ORLI10G is a line interface device that contains an FPGA base array, a 10 Gbits/s line interface block, and programmable PLLs to do the overhead clock rate conversions on a single monolithic chip. The embedded portion includes:

- Line Interface: This consists of a 16-bit LVDS receive data bus and a 16-bit LVDS transmit bus operating up to 850 Mbits/s per input/output pair. Each 4-bit LVDS I/O has a high-speed LVDS clock (operating up to 850 MHz) associated with it. The bit order (i.e. whether bit 0 is the most significant or least significant bit) of the 16-bit transmitted and received busses can be defined separately in the user's programmable logic netlist that interfaces to the embedded core so that any required interface standard can be met.
- MUX/deMUX: This performs the MUXing and deMUXing between the high-speed line interface data operating at the line rate and system data operating at 1/4 or 1/8 the line rate.
- On-board PLLs: This is used to align system-side data with the line-side data, which is at a slightly higher data bandwidth than the system data because of the addition of overhead due to encoding.

Figure 2 shows the ORLI10G block diagram.

10G Mode

The ORLI10G can operate in one of two data modes: 10G mode or Quad 2.5G mode.

In 10G (or single-channel) mode, all 16 LVDS transmit data outputs are assumed to be one data bus with one LVDS clock provided off chip for the data. Likewise, all 16 LVDS receive data inputs are assumed to be one data bus with one LVDS input clock provided for the data.

Transmit Path

In 10G mode, the transmit data from the FPGA logic is passed to the embedded core as a single 128- or 64-bit bus. An off-chip transmit reference clock is divided down in the core by 8 (for 128-bit to 16-bit MUX) or by 4 (for 64-bit to 16-bit MUX). All four transmit clock outputs are therefore synchronized.

Receive Path

The 16-bit receive data is deMUXed in the embedded core to a single 128-bit or 64-bit data bus and passed to the FPGA logic. The lowest-order LVDS input clock (rx_clk_in[0]) is used as the receive clock for all 16 data bits (the other three LVDS input clock pairs should be left unconnected). This clock is divided down in the core by 8 (for 16-bit to 128-bit deMUX) or by 4 (for 16-bit to 64-bit deMUX) and passed to the FPGA logic with the data.

The ORLI10G supports transmit and receive data rates up to 850 Mbits/s. Therefore, the total data rate for this mode is 850 Mbits/s x 16 or 13.6 Gbits/s.

2.5G Mode

In 2.5G (or quad-channel) mode, the 16 LVDS receive data inputs are assumed to be four independent 4-bit data buses with four LVDS asynchronous input clocks provided for each data bus. There is no 2.5 G mode in the transmit direction for the ORLI10G device.

Receive Path

Each of the four 4-bit receive data buses are deMUXed in the embedded core to one of four independent 32- or 16-bit data buses and passed to the FPGA logic. The four receive clock inputs are divided down in the core by 8 (for each 4- to 32-bit deMUX) or by 4 (for each

4- to 16-bit deMUX), and each divided clock is passed to the FPGA logic with its associated data bus. All four data paths act as separate data interfaces that are asynchronous to each other.

The ORLI10G supports transmit and receive data rates up to 850 Mbits/s. Therefore, the total data rate each of the quad channels is 850 Mbits/s x 4 or 3.4 Gbits/s. Figure 2 shows a representation of the 10G and 2.5G modes in both transmit and receive directions.

Figure 2. ORCA ORLI10G Block Diagram

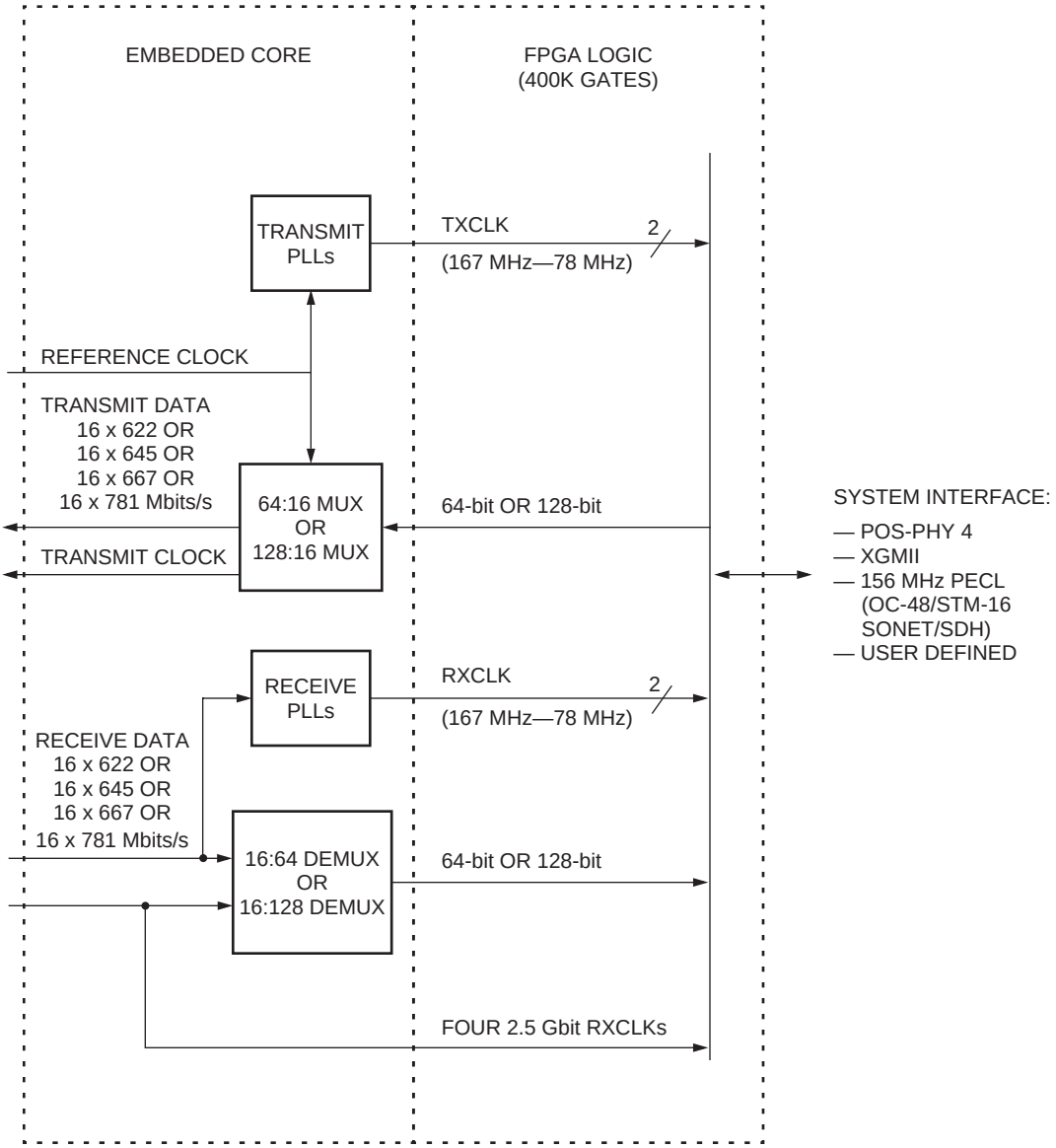
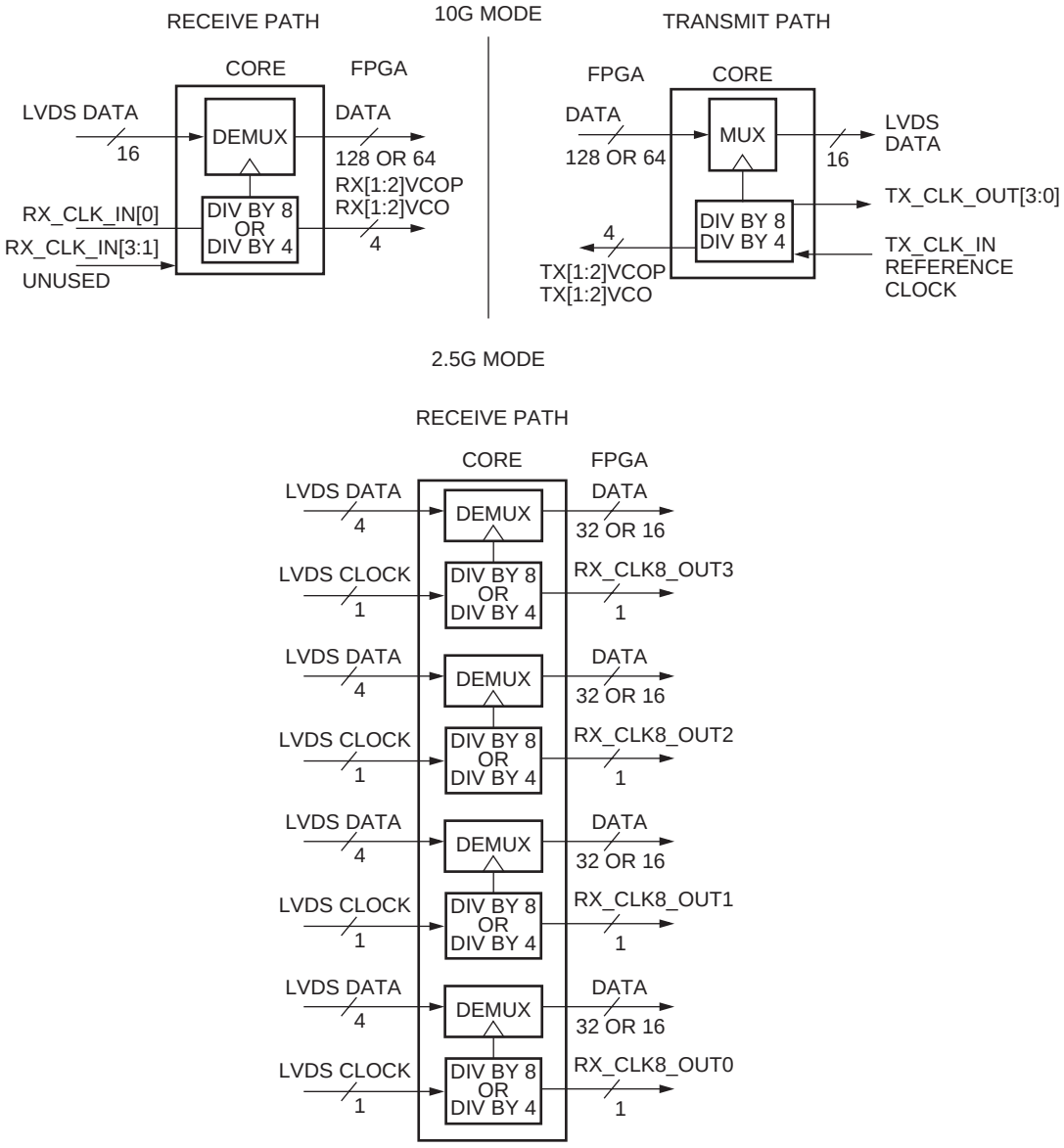


Figure 3. 10G (Single-Channel) and 2.5G (Quad-Channel) Modes



Receive Path Details

In the receive path, the ORLI10G embedded core can be broken down into three sections: the high-speed line interface, the demultiplexer, and the receive-side onboard PLLs. Note that both transmit and receive PLLs are in addition to the four Programmable PLLs (PPLLs) in the FPGA portion of the ORLI10G.

Line Interface

In the receive path, 16-bit data and associated clocks are inputs to the line interface. Typical data rates are expected to range from 622 Mbits/s to 850 Mbits/s for most applications. The 16-bit LVDS input data bus is actually composed of four 4-bit data buses with one clock for each 4-bit data bus. In the 10G mode, all four input clocks are tied together internal to the device and driven by the lowest-order input clock. In 2.5G mode, the four clocks may be asynchronous to each other. The ORLI10G uses LVDS (Low-Voltage Differential Signaling) drivers/receivers, which are intended to provide point-to-point connection between the ORLI10G and optical transceiver (MUX/deMUX) parts. The LVDS inputs are hot-swap compatible and can connect to other vendor's LVDS I/O buffers. The LVDS inputs are terminated with a 100 Ω resistor to improve performance.

The receive line interface on the ORLI10G can connect to devices that are compliant to either the XSBI standard or the SFI-4 standard. The major difference for these standards is that for XSBI (*IEEE* 802.3ae version 2.1), the least significant bit [0] is received first after deserialization by the external deMUX device, whereas SFI-4 receives the most significant bit first. In some cases, bits [15:0] on the ORLI10G should be connected to bits [0:15] on the device to which the ORLI10G device interfaces. An example of this is the PCS IP core in the ORLI10G when the ORLI10G is connected to an XSBI version 2.1 device.

It should be noted that *IEEE* 802.3ae version 3.1 to D3.4 (version D3.4 is the latest draft version of this specification as of the writing of this data sheet) swaps XSBI so that the most significant bit is received first, thus requiring that bits [0:15] on the ORLI10G be connected directly to bits [0:15] on the XSBI device.

DeMUX

The demultiplexer takes the high-speed line data and clocks and converts the data and clock to rates appropriate for transfer to the FPGA logic. The demultiplexer supports two modes of operation:

- Divide-by-8
  - 10G (or single channel): The demultiplexer converts the incoming 16 bits of data at 622 Mbits/s to 850 Mbits/s into 128 bits at 78 Mbits/s to 106 Mbits/s. The incoming clocks are divided by 8.
  - 2.5G (or quad channel): The demultiplexer converts the incoming four bits of data at 622 Mbits/s to 850 Mbits/s into 32 bits at 78 Mbits/s to 106 Mbits/s. The associated clock is also divided by 8. This is repeated four times with each 4-bit data/clock group assumed to be asynchronous to the others.
- Divide-by-4
  - 10G (or single channel): The demultiplexer converts the incoming 16 bits of data at 622 Mbits/s to 850 Mbits/s into 64 bits at 156 Mbits/s to 212 Mbits/s. The incoming clocks are divided by 4.
  - 2.5G (or quad channel): The demultiplexer converts the incoming 4 bits of data at 622 Mbits/s to 850 Mbits/s into 16 bits at 156 Mbits/s to 212 Mbits/s. The associated clock is also divided by 4. This is repeated four times with each 4-bit data/clock group assumed to be asynchronous to the others.

Onboard Receive PLLs

The function of the onboard PLLs is to align the system data with the line data, which will be at a slightly higher rate owing to the addition of the overhead bits. There are two PLLs on the receive path. The input to the first PLL, RX1_PLL (see Figure 3), is the divided down lowest-order clock from the demultiplexer. The RX1_PLL generates a clock with a user-defined frequency ratio of M/N to the divided clock. This clock would generally be used to compensate for different data rates due to overhead bits. M and N can independently be set from 1 to 40.

The RX2_PLL also takes its input from the divided down clock and is used to provide a balanced, divided clock across the FPGA-embedded core interface.

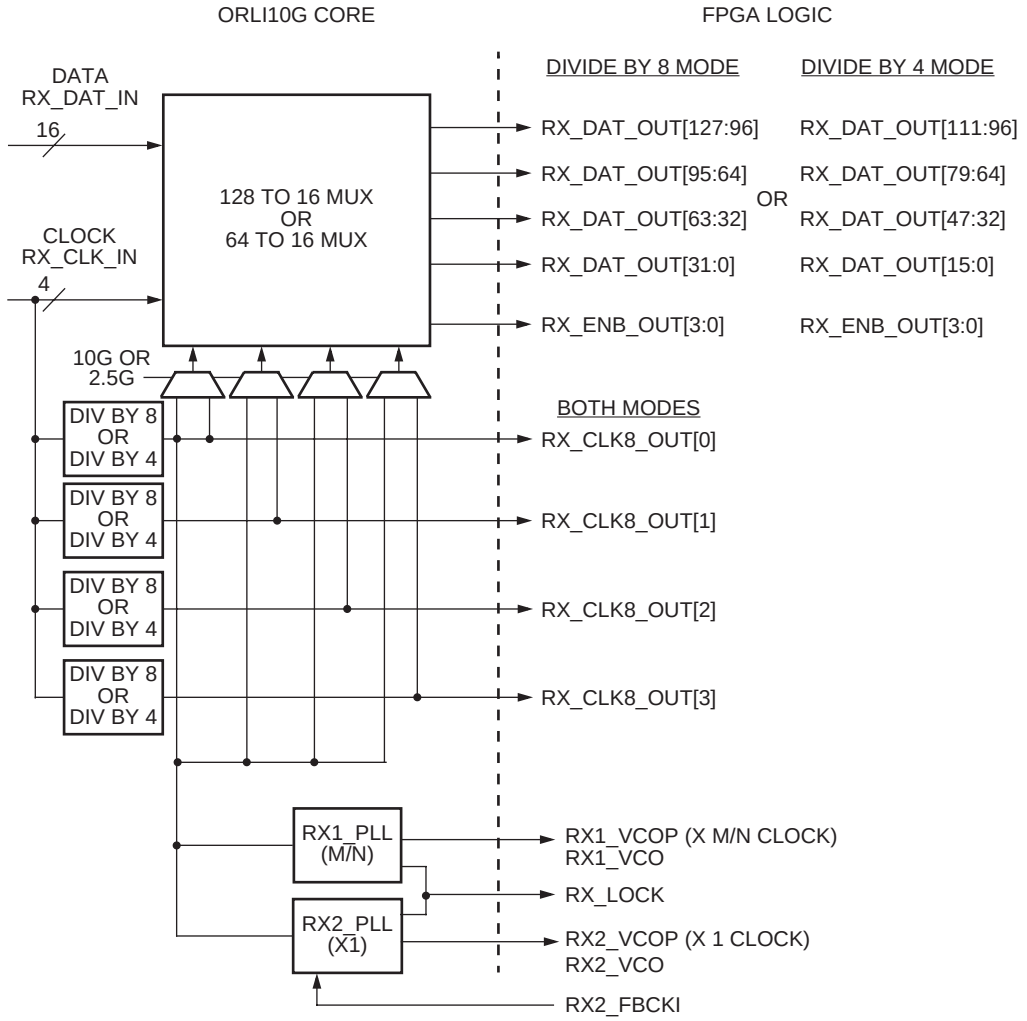
The RX2_PLL has a feedback path that compensates for routing delays to the embedded core/FPGA logic interface for minimum clock skew.

In addition, the user can specify an additional skew on each clock in increments of 1/8 the clock period.

The selection of the deMUX width (and corresponding clock division value), the RX1_PLL M and N values, and the additional skew for RX1_PLL and RX2_PLL are specified by the user in a GUI interface provided in the ORLI10G design kit.

A detailed block diagram of the receive path in shown in Figure 4.

Figure 4. ORLI10G Embedded Core Receive Path Diagram



Transmit Path Details

In the transmit path, the ORLI10G embedded core can be broken down into three sections: the multiplexer, the transmit side onboard PLLs, and the high-speed line interface. Note that both transmit and receive PLLs are in addition to the four Programmable PLLs (PPLLs) in the FPGA portion of the ORLI10G.

MUX

The multiplexer takes data from the FPGA logic and multiplexes the data to rates for transfer by the highspeed line interface. The multiplexer supports two modes of operation:

- Multiplex-by-8
  - The multiplexer converts the incoming 128 bits of data at 78 Mbits/s to 106 Mbits/s into 16 bits at 622 Mbits/s to 850 Mbits/s. The incoming transmit reference clock is divided by 8 for connection to the internal FPGA logic.
- Multiplex-by-4
  - The multiplexer converts the incoming 64 bits of data at 156 Mbits/s to 212 Mbits/s into 16 bits at 622 Mbits to 850 Mbits/s. The transmit reference clock is divided by 4 for connection to the internal FPGA logic.

Onboard Transmit PLLs

The function of the onboard PLLs is to align the system data with the line data, which will be at a slightly higher rate owing to the addition of the overhead bits. There are two PLLs on the transmit path. The input to the first PLL, TX1_PLL (see Figure 4), is the divided down transmit reference clock from the multiplexer. The TX1_PLL generates a clock with a user-defined frequency ratio of M/N to the divided clock. This clock would generally be used to compensate for different data rates due to overhead bits. M and N can be independently set from 1 to 40.

The TX2_PLL also takes its input reference from the divided down reference clock and is used to provide a balanced divided clock across the FPGA-embedded core interface.

The TX2_PLL has a feedback path that compensates for routing delays to the embedded core/FPGA logic interface for minimum clock skew.

In addition, the user can specify an additional skew on each clock in increments of 1/8 the clock period.

The selection of the MUX width (and corresponding clock division value), the TX1_PLL M and N values, and the additional skew for TX1_PLL and TX2_PLL are specified by the user in a GUI interface provided in the ORLI10G design kit.

A detailed block diagram of the transmit path in shown in Figure 4. Either TX1_VCOP, TX1_VCO, TX2_VCOP, or TX2_VCO must be used to clock TX_DAT_IN[127:0] that is transmitted to the embedded block since this interface must be frequency locked to the divided version of the referance clock. These PLLs can also be bypassed, where the divided transmit reference clock is sent directly to the FPGA. TX_CLK8_IN[3:0] can be used to clock data transmitted to the embedded block, but the preferred method is to use the internally generated clocks as described above. If TX_CLK8_IN[3:0] are used, they must also be frequency locked to the reference clock and are thus also required to be driven by TX1_VCOP, TX1_VCO, TX2_VCOP, or TX2_VCO.

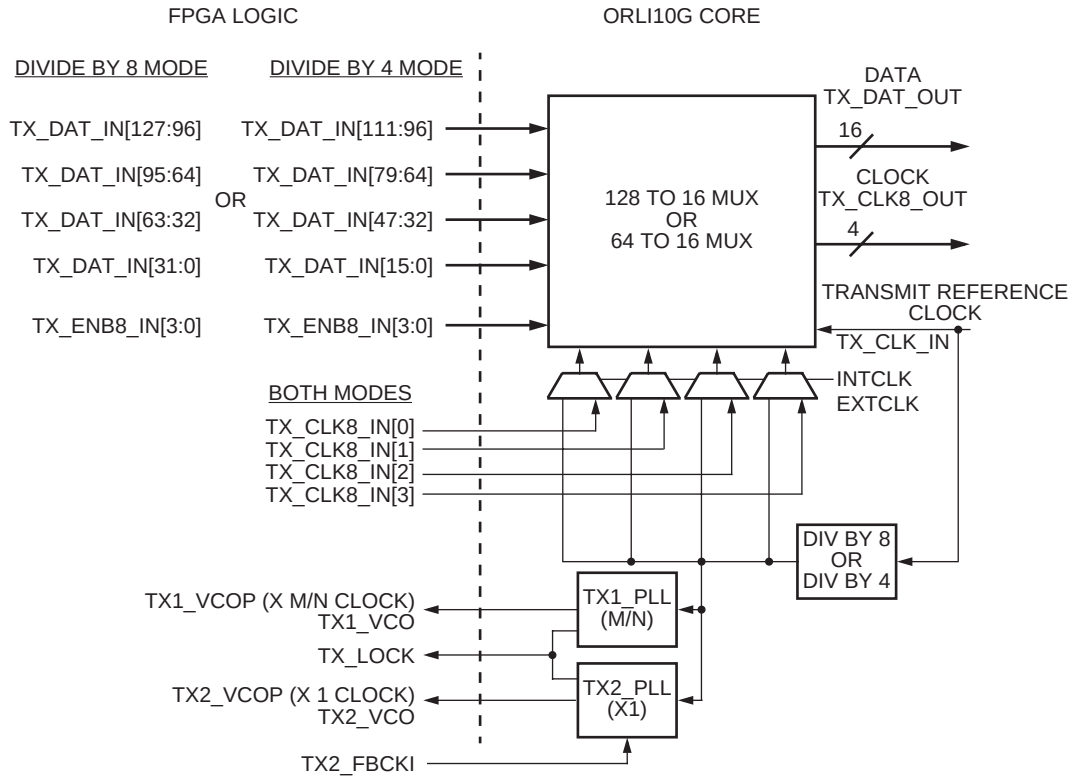
Line Interface

In the transmit path, 16-bit data and associated clocks are outputs from the line interface. Typical data rates are expected to range from 622 Mbits/s to 850 Mbits/s for most applications. The 16-bit LVDS output data bus is actually composed of four 4-bit data buses with one clock for each 4-bit data bus. On the transmit side, these clocks will all be synchronized. The ORLI10G uses LVDS (Low-Voltage Differential Signaling) drivers/receivers, which are intended to provide point-to-point connection between the ORLI10G and optical transceiver (MUX/deMUX) parts. The LVDS drivers are hot-swap compatible and can connect to other vendor's LVDS I/O buffers. The LVDS drivers are terminated with a 100 Ω resistor to improve performance.

The transmit line interface on the ORLI10G can connect to devices that are compliant to either the XSBI standard or the SFI-4 standard. The major difference for these standards is that for XSBI, the least significant bit [0] is transferred first after serialization by the external MUX device, whereas SFI-4 transmits the most significant bit first. In some cases, bits [15:0] on the ORLI10G should connect to bits [0:15] on the device to which the ORLI10G device interfaces. An example of this is the PCS IP core in the ORLI10G when the ORLI10G is connected to an XSBI version 2.1 device.

It should be noted that *IEEE* 802.3ae version 3.1 to D3.4 (version D3.4 is the latest draft version of this specification as of the writing of this data sheet) swaps XSBI so that the most significant bit is transferred first, thus requiring that bits [0:15] on the ORLI10G be connected directly to bits [0:15] on the XSBI device.

Figure 5. ORLI10G Embedded Core Transmit Path Diagram



Note: TX_ENB8_IN[3:0] and TX_CLK8_IN[3:0] are generally not used. See text for explanation.

ORLI10G Demultiplexer (Rx) Detail

The demultiplexer module converts the incoming 16 bits of data at 622 MHz/850 MHz into 128 bits of data at 78 MHz/106 MHz or 64 bits of data at 156 MHz/212 MHz and sends it to the FPGA logic. It has been implemented in two stages; the first stage converts each incoming bit into a byte stream and the second stage bit interleaves these bytes into 128/64 bits, depending upon the mode of operation. The low-speed clocks are generated by this block. These clocks are then driven back to this block from the low-speed clock tree network. Functionally, the demultiplexer architecture consists of three blocks: the serial to parallel conversion, the counters, and the interleaving.

The first stage of the line interface module (demultiplexer) converts each incoming bit of data into a byte stream on a divided-by-8 clock. The data is first registered on the rising edge of the clock input. The clock dividers also runs parallel to data shift (serial to parallel) on the rising edge of the input clock. An enable is created when a complete byte is taken in. This enable signal is used to register the serial-to-parallel converted data at the high-speed input clock. This ensures that the data can be safely transferred to the low-speed clock. This data is then transferred to the divided clock, allowing a timing margin of approximately half the divided clock period.

The high-speed demultiplexer converts the incoming data as blocks of bytes. The byte boundaries of incoming data are unknown and are irrelevant to this module.

This data is then interleaved to the 128/64 bits of output data, depending on the mode of operation (divide-by-4/divide-by-8). In 10G mode, the output data is assigned the retimed 128/64 bits of data from the first stage of line interface registered at the input clock [0]. In 2.5G mode, the output data is assigned four concatenated 32/16 bits of data from the first stage of line interface registered at input clocks [0 to 3]. The interleaving is done at bit level because the serial-to-parallel converter operates on bits of incoming data. In 10G mode, it is assumed that all the incoming 16 bits of data are synchronized to the input clock [0]. This block also generates the clock enables used by the output line interface (multiplexer) module for registering the data on the high-speed clock. These enables along with the enables from other clocks are selected through the high-speed clock MUX for the output line interface block.

Figure 6 shows the valid data output bits from the demultiplexer in each of the four modes (divide-by-8, 10G and 2.5G modes, and divide-by-4, 10G and 2.5G modes). Figure 7—Figure 10 show the demultiplexer input data and clock waveforms and output clock, enable, and data waveforms for all four modes.

Figure 6. Demultiplexer Output Data Structure

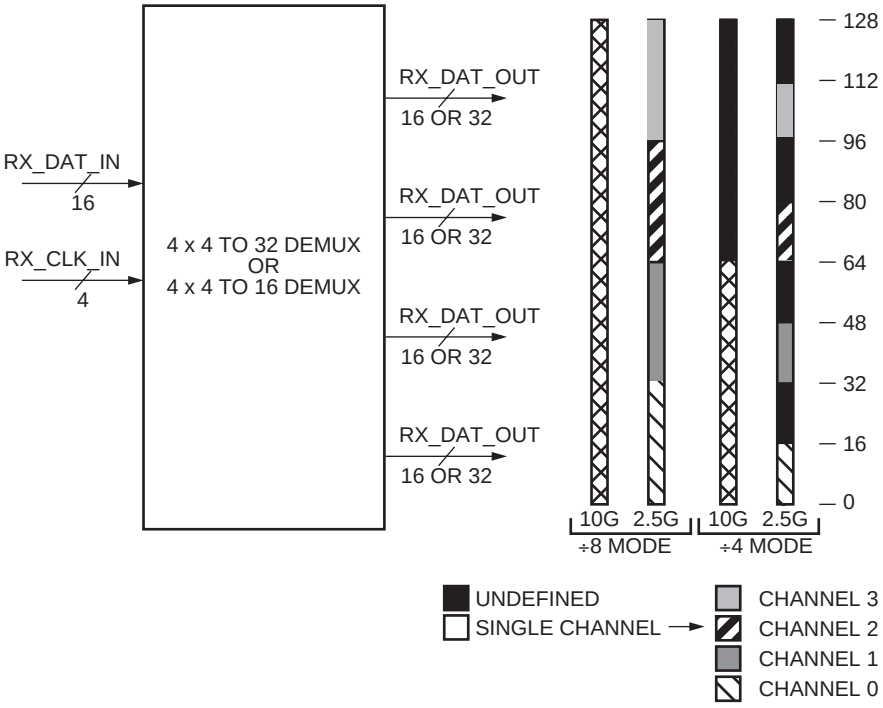


Figure 7. Demultiplexer Serial-to-Parallel Conversion Divide by 8, 10G Mode

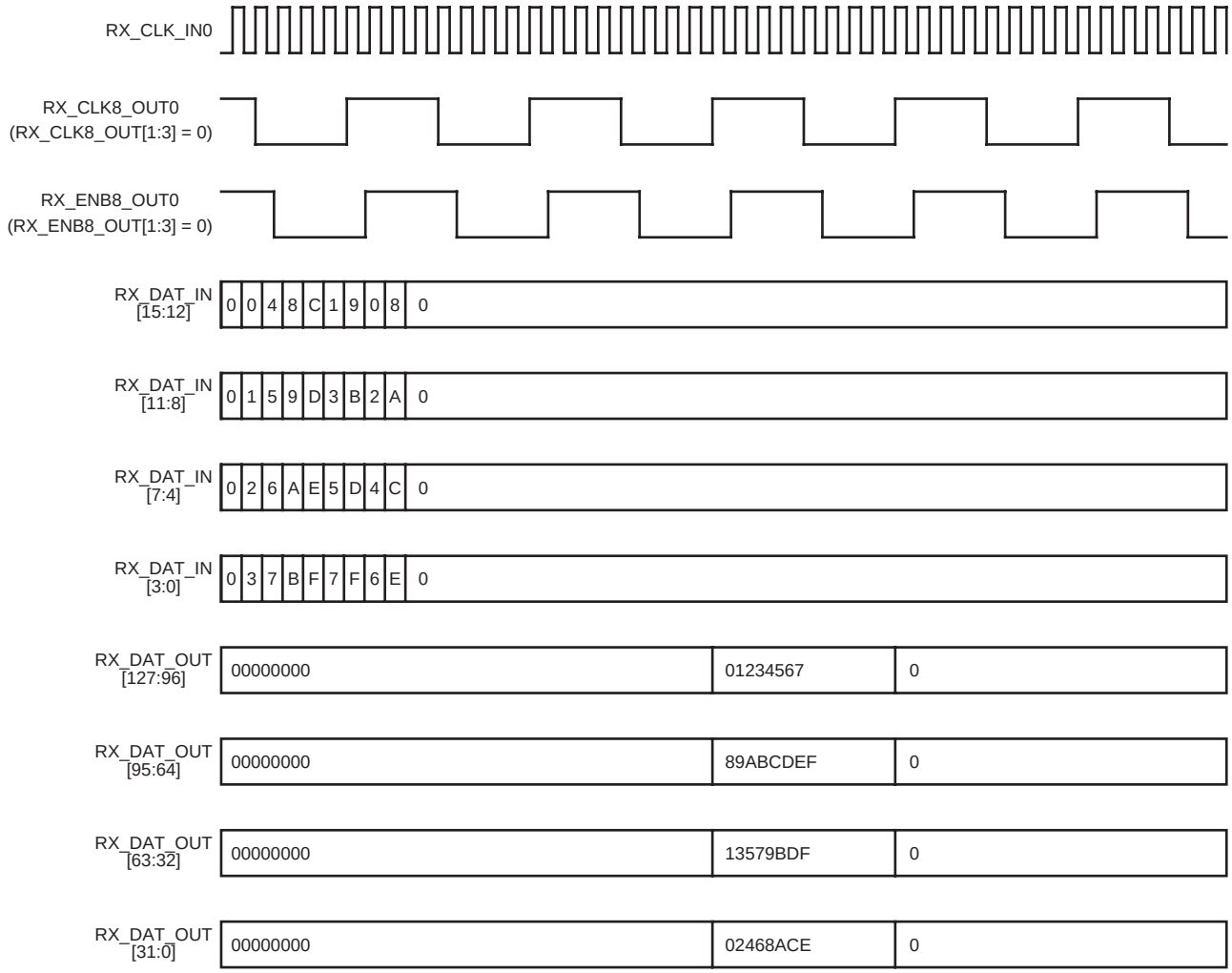


Figure 8. Demultiplexer Serial-to-Parallel Conversion Divide by 4, 10G Mode

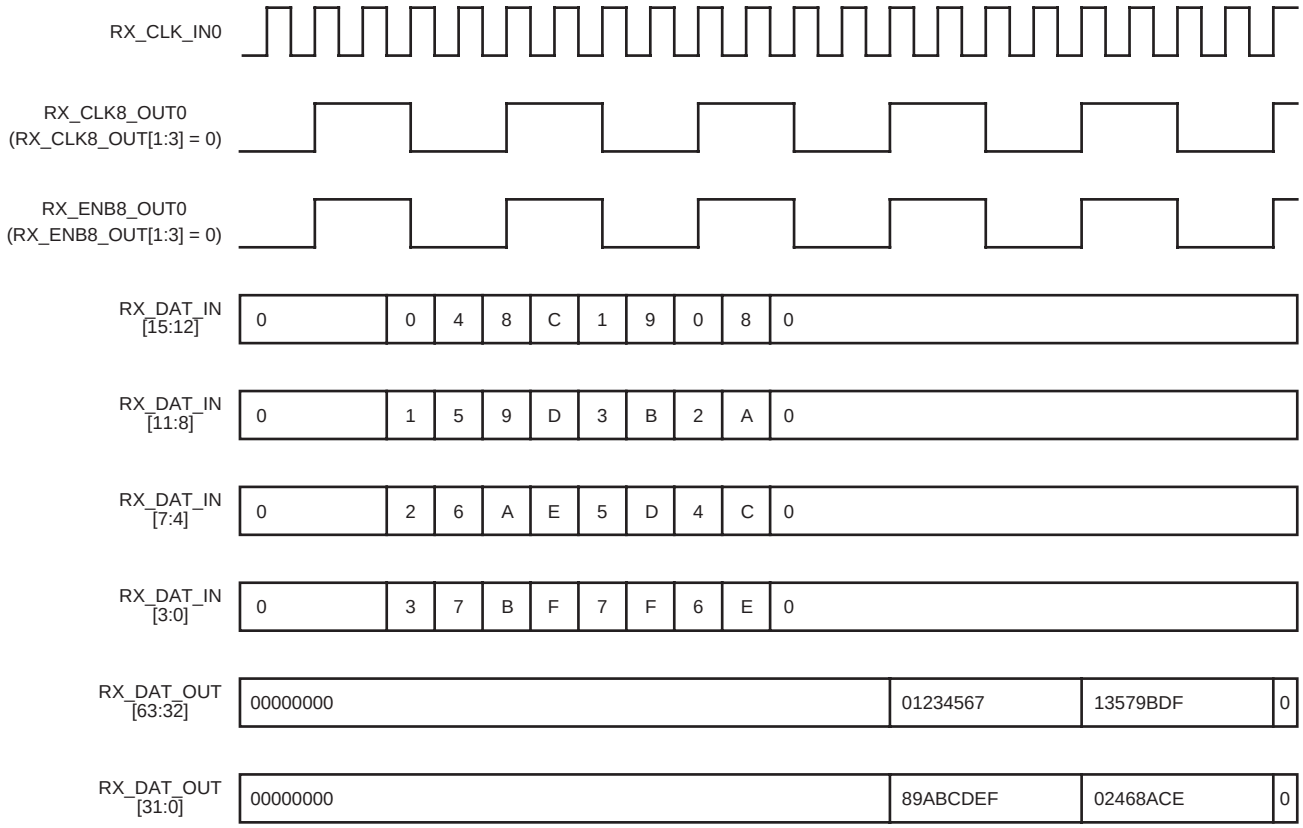


Figure 9. Demultiplexer Serial-to-Parallel Conversion Divide by 8, 2.5G Mode

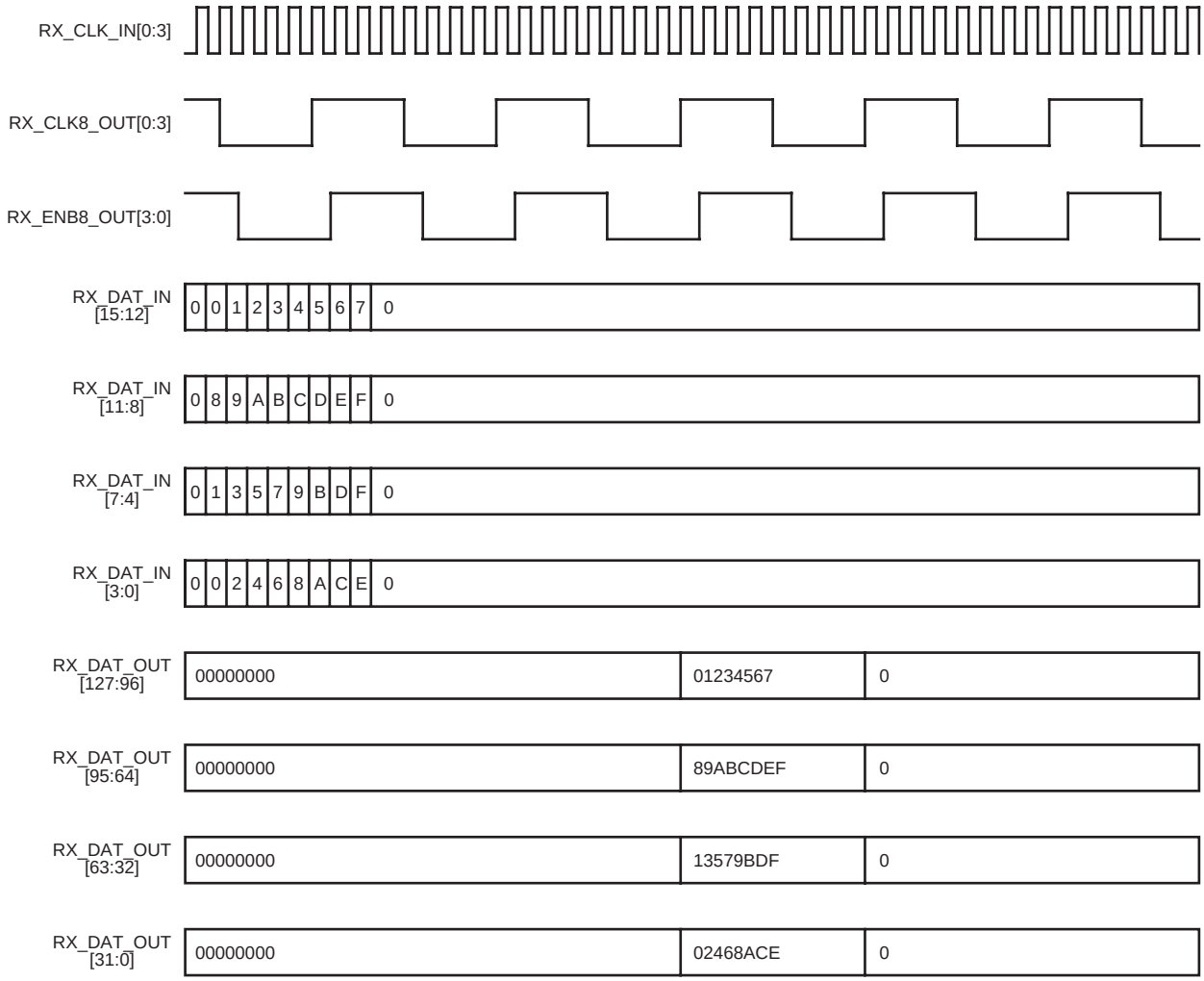
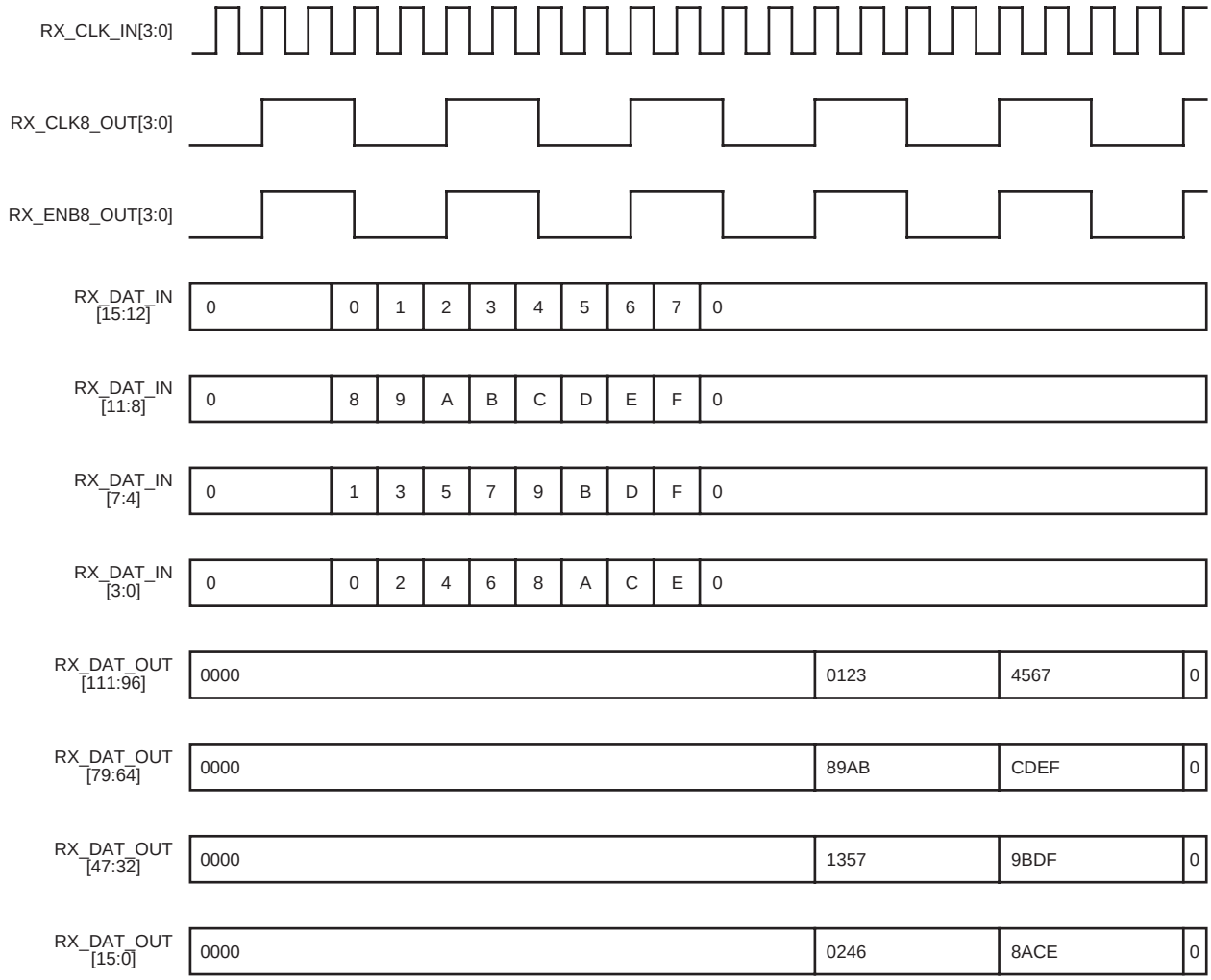


Figure 10. Demultiplexer Serial-to-Parallel Conversion Divide by 4, 2.5G Mode



ORLI10G Multiplexer (Tx) Detail

The multiplexer module converts the incoming 128 bits of data from the FPGA logic at 78 MHz/106 MHz or 64 bits of data from the FPGA logic at 156 MHz/212 MHz into 16 bits of data at 622 MHz/850 MHz. It has been implemented as two stages. The first stage deinterleaves each incoming byte into a different byte stream that can be serially output on the output data pins. The second stage outputs these bytes into 16 bits or four groups of 4 bits, depending upon the mode of operation. Functionally, the multiplexer architecture consists of three blocks: the parallel-to-serial conversion, the counters, and the deinterleaving.

Two options are available for the transmit clocks. The clock signals TX_CLK_IN[3:0] can be used to transfer data to the internal core or an internal clock can be used. The preferred method is to use the internal clock. Two options are also available for the enable signals. The enable signals TX_ENB8_IN[3:0] can be used or they can be generated internally. The preferred method is to use the internal enables.

For divide-by-8 mode, the first stage of the line interface module deinterleaves each incoming byte of data into a different byte stream on the 78 MHz/106 MHz (TX_CLK8_IN[3:0] or internal) clock. This data is then registered on the rising edge of the 622 MHz/850 MHz (TX_CLK_IN) clock at the falling edge of the 78 MHz/106 MHz clock. The enable inputs (TX_ENB8_IN[3:0] or internal) are used to transfer data from the low-speed clock to the high-speed clock, as well as synchronizing the counters of parallel-to-serial conversion which are running at the high-speed clock. Generally, these enables are generated in the embedded core and the TX_ENB8_IN[3:0] signals to the embedded core are not used.

For divide-by-4 mode, the first stage of the line interface module deinterleaves each incoming byte of data into a different byte stream on the 156 MHz/212 MHz (TX_CLK8_IN[3:0] or internal) clock. This data is then registered on the rising edge of the 622 MHz/850 MHz (TX_CLK_IN) clock at the falling edge of the 156 MHz/212 MHz clock. The enable inputs (TX_ENB8_IN[3:0] or internal) are used to transfer data from the low-speed clock to the high-speed clock, as well as synchronizing the counters of parallel-to-serial conversion which are running at the high-speed clock. Again, both TX_CLK8_IN[3:0] and TX_ENB8_IN[3:0] are not generally used.

The enable inputs (TX_ENB8_IN[3:0]) are required to be four (divide by 4) or eight (divide by 8) TX_CLK_IN clock cycles wide. If they are used, they have to be synchronous to their corresponding TX_CLK8_IN[3:0] clock. Each of these four TX_CLK8_IN[3:0] clocks must also be frequency locked to the TX_CLK_IN signal.

The TX_CLK_OUT[3:0] clock outputs from the ORLI10G are provided for transferring each 4 bits of data per clock.

All data to be transmitted to the embedded core must be frequency locked to the TX_CLK_IN signal. Thus, the divided version of this clock found at the embedded core interface should always be used to transfer data from the FPGA logic to the embedded core. These clock signals are available from the TX PLL outputs (TX1_VCO, TX1_VCOP, TX2_VCO, TX2_VCOP). Figure 11 shows the valid data input bits to the multiplexer in each of the four modes (divide-by-8 and divide-by-4 modes). Figure 12— Figure 15 show the multiplexer input transmit reference clock, data, enable, and clock waveforms and output clock and data waveforms for all four modes.

Figure 11. Multiplexer Input Data Structure

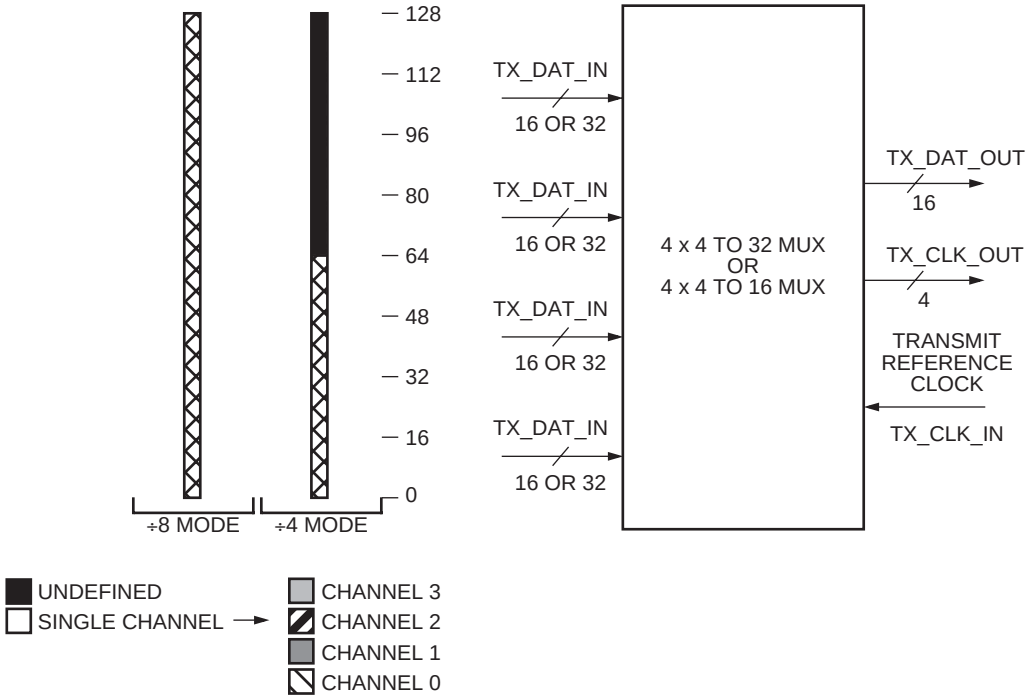
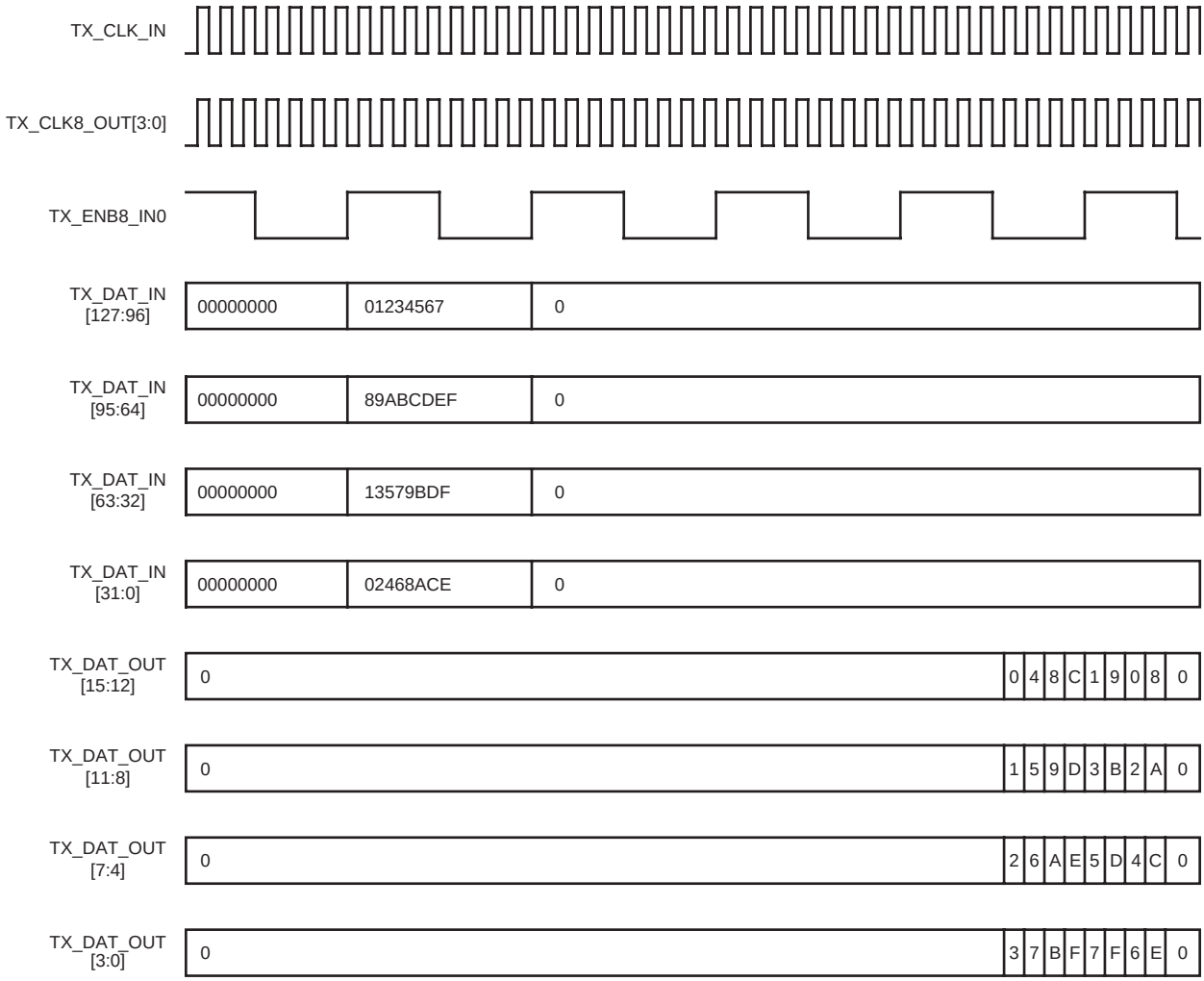
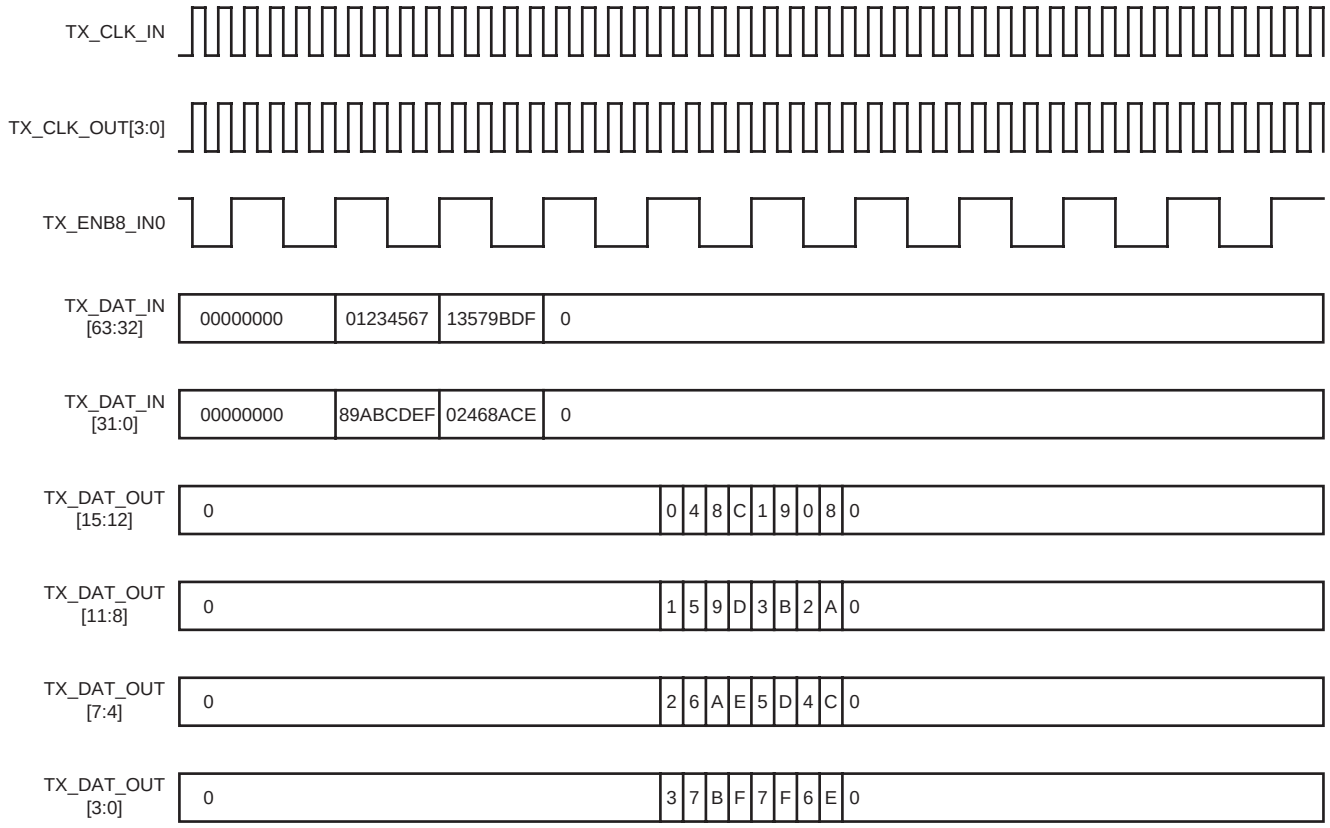


Figure 12. Multiplexer Parallel-to-Serial Conversion Divide by 8, 10G Mode



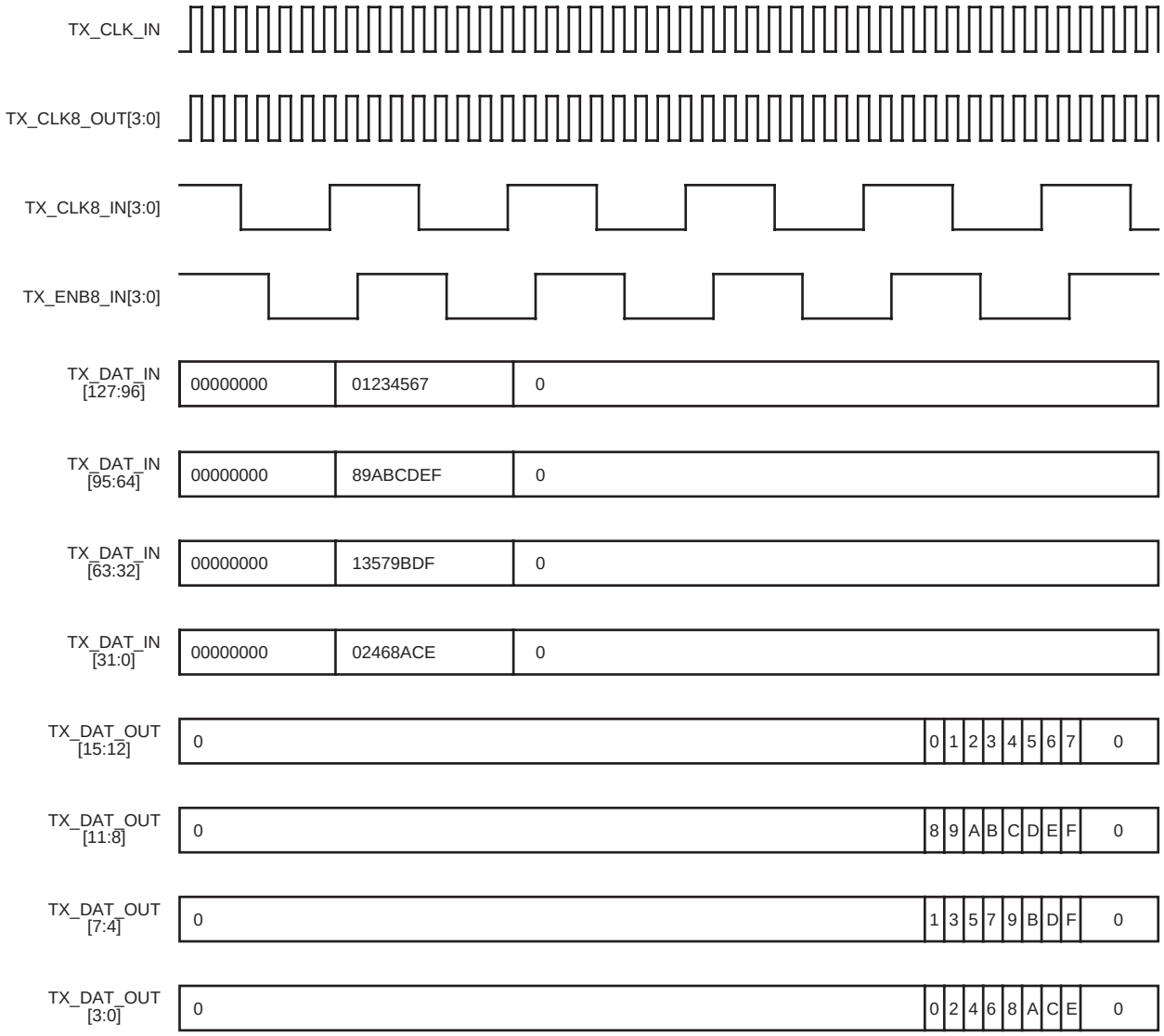
Note: TX_ENB8_IN0 is generally not used because the enable is created internal to the embedded core, but is shown for reference

Figure 13. Multiplexer Parallel-to-Serial Conversion Divide by 4, 10G Mode



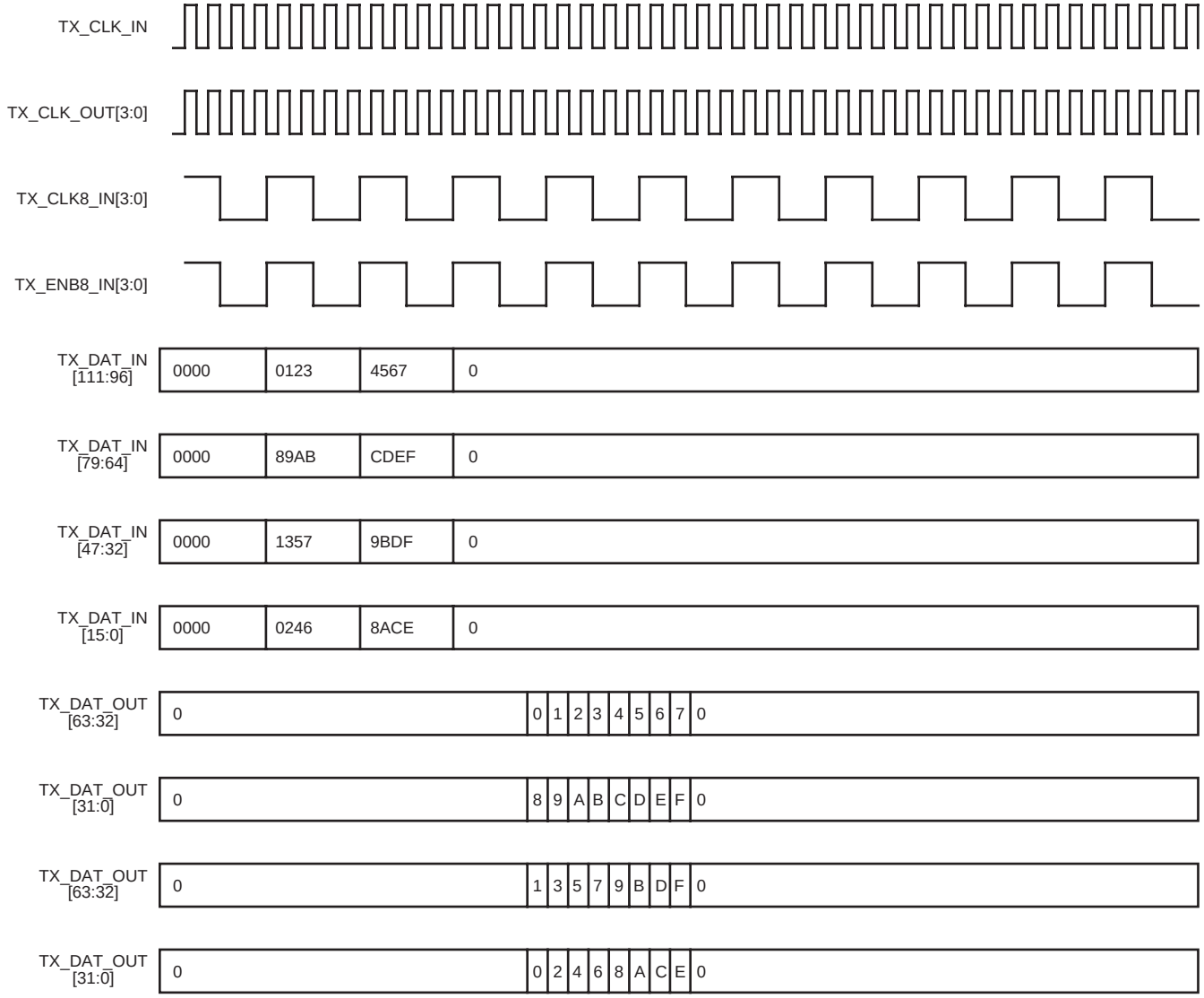
Note: TX_ENB8_IN0 is generally not used because the enable is created internal to the embedded core, but is shown for reference

Figure 14. Multiplexer Parallel-to-Serial Conversion Divide by 8, 2.5G Mode



Note: TX_CLK8_IN[3:0] and TX_ENB8_IN[3:0] are generally not used because the clocks and enables are created internal to the embedded core, but are shown for reference

Figure 15. Multiplexer Parallel-to-Serial Conversion Divide by 4, 2.5G Mode



Note: TX_CLK8_IN[3:0] and TX_ENB8_IN[3:0] are generally not used because the clocks and enables are created internal to the embedded core, but are shown for reference

ORLI10G Embedded PLLs

The ORLI10G embedded (transmit and receive) PLLs are based on the 4E series FPGA High-Speed Programmable PLL (HPPLL). The 4E PLL consists of a Phase/Frequency Detector (PFD), a charge pump/filter, a multitap Voltage Controlled Oscillator (VCO), a duty cycle synthesis circuitry, a power regulator, two programmable dividers, phase shift selector multiplexers, a lock signal generator, and a current DAC. A block diagram of the programmable PLL is shown in Figure 16. The receive path RX1_PLL and transmit path TX1_PLL, which can be programmed to create a N/M frequency clock, are based on this design.

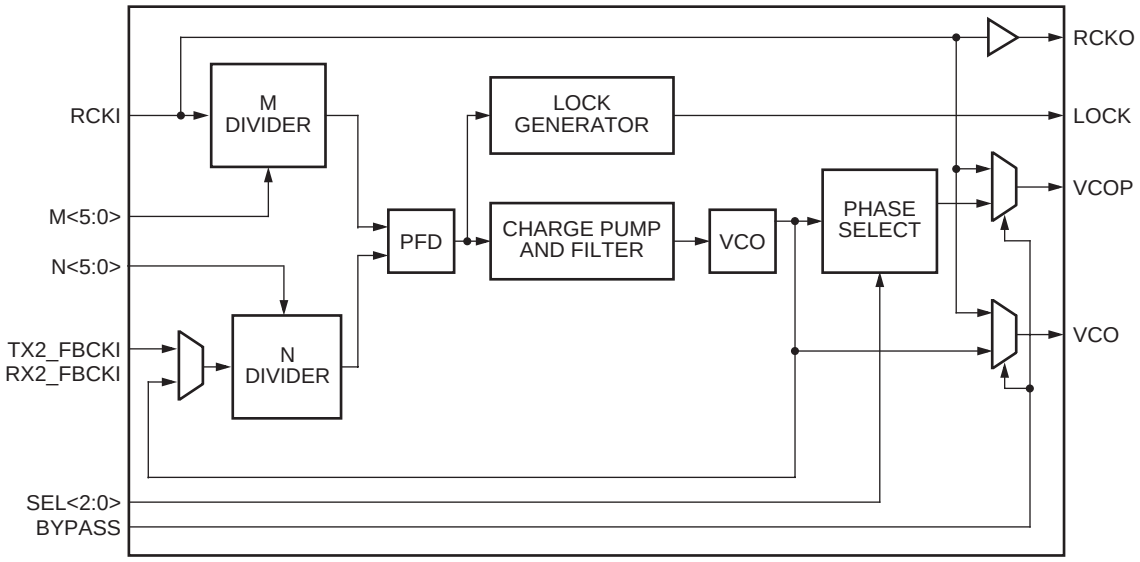
The receive path RX2_PLL and transmit path TX2_PLL create a X1 clock. This is essentially the same PLL without the M and N divider.

The RCKI input to the PLLs comes from an input clock to the ORLI10G that has been divided in frequency by either 4 or 8 (programmable). As shown in Figure 4, RX1_PLL and RX2_PLL are driven by the divided version of RX_CLK_IN0. As shown in Figure 5, TX1_PLL and TX2_PLL are driven by the divided versions of TX_CLK_IN. It should be noted that the speed of the ORLI10G line interface is therefore either 4x or 8x the operating speed of the embedded PLLs.

The clock feedback loops for the RX2_PLL and TX2_PLL should be routed from the clock network in the FPGA core to compensate for the routing delays to the FPGA logic interface. The source to the TX2_FBCKI or RX2_FBCKI inputs must come from an FPGA clock network driven by the VCO output (otherwise, any phase shifting on VCOP is removed by the feedback loops). In this way, the clock skew at the embedded core/FPGA logic boundary is zero for the receive and transmit PLLs.

All PLLs include a phase shift selector which allows phase shift adjustments of each clock in increments of 1/8 the period of the clock. This phase shifted output is available on the VCOP output of the PLL. All functions of the embedded core PLLs are user controlled through a GUI provided with the ORLI10G design kit software.

Figure 16. ORLI10G Programmable PLL Block Diagram



ORLI10G Embedded Programmable PLLs Specifications

Table 2. Programmable PLL Specifications

Parameters	Min	Nom	Max	Unit
$V_{DD}15$	1.425	1.5	1.575	V
$V_{DD}33$	3.0	3.3	3.6	V
Operating Temperature (T_A)	–40	—	125	˚C
Input Clock Frequency	60	—	420	MHz
Input Duty Cycle	30	—	70	%
Output Clock Frequency	7.5	—	420	MHz
Output Duty Cycle	45	50	55	%
Lock Time	—	<50	—	µs
Frequency Multiplication (TX1_PLL and RX1_PLL)	2x, 3x, 4x, 5x, 6x, 7x, 8x			—
Frequency Division (TX1_PLL and RX1_PLL)	1/8x, 1/7x, 1/6x, 1/5x, 1/4x, 1/3x, 1/2x			—
Duty Cycle Adjust of Output Clock(s)	12.5, 25, 37.5, 50, 62.5, 75, 87.5			%
Delay Adjust of Output Clock	0, 45, 90, 135, 180, 225, 270, 315			degrees
Phase Shift Between VCO and VCOP	0, 45, 90, 135, 180, 225, 270, 315			degrees

Notes:
Multiplication and division values can both be used on one PLL output (example 3/4x).
For more information about the HPPLL, see the Series 4 PLL Application Note.

ORLI10G Reset Requirements

Both the embedded core portion and the FPGA portion are reset at powerup. The embedded core is also reset, as shown in Table 3, based on other conditions. All resets to the core can either be asynchronous or asynchronous on with a synchronous release. Asynchronous resets must be held in reset for at least 8 ns. Two signals from the FPGA logic can also reset the embedded core: the global set/reset (GSRN) which can be inhibited, and a signal routed from the FPGA general routing (FPGA_RESET). Both of these affect both the TX and RX reset simultaneously. Table 3 also shows the conditions upon which the I/O are 3-stated.

Reset of PLL blocks directly affects only the digital logic. For the PLL_RX2 and PLL_TX2 (x1) PLLs, the VCO outputs from the PLL should be in the 3-6Mhz range during reset. For PLL_RX1 and PLL_TX1 (xM/N) PLLs using the M and N counters, the VCO will go to the low state. Coming out of reset will require about 25 microseconds for the PLLs to become stable.

Table 3. ORLI10G Reset Requirements

Condition	TX MUX Block	TX PLL	RX DeMUX Block	RX PLL	Embedded I/O
Powerup	Reset	Reset	Reset	Reset	3-state
FPGA Configuration	Reset	Reset	Reset	Reset	Active
FPGA GSRN	Reset	Reset	Reset	Reset	Active
FPGA_RESET Signal	Reset	Reset	Reset	Reset	Active
TS_ALL Pin = 1	—	—	—	—	3-state
RESET_TX Pin = 1	Reset	Reset	—	—	Active
RESET_RX Pin = 1	—	—	Reset	Reset	Active
PWRON Pin = 1	—	Powerdown	—	Powerdown	Active

Typically, the following reset sequence should be followed for the ORLI10G:

- Place the device in reset by driving RESET_TX = 1 and RESET_RX = 1 (or FPGA_RESET signal = 1), and by placing the FPGA portion into reset.
- Release the embedded core from reset by driving RESET_TX = 0 and RESET_RX = 0 and FPGA_RESET signal = 0).
- Release the FPGA portion from reset.

Line Interface Circuit Specifications

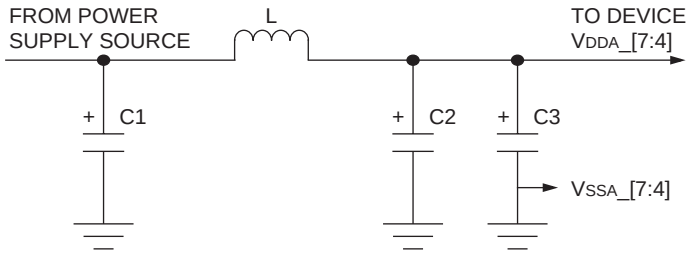
Power Supply Decoupling LC Circuit

The 622 MHz—850 MHz line interface macro contains both analog and digital circuitry. The line interface function, for example, is implemented as primarily a digital function, but it relies on a conventional analog phase-locked loop to provide its divided clocks. The internal analog phase-locked loop contains a voltage-controlled oscillator. This circuit will be sensitive to digital noise generated from the rapid switching transients associated with internal logic gates and parasitic inductive elements. Generated noise that contains frequency components beyond the bandwidth of the internal phase-locked loop (about 3 MHz) will not be attenuated by the phase-locked loop and will impact bit error rate directly. Thus, separate power supply pins are provided for these critical analog circuit elements.

Additional power supply filtering in the form of an LC π filter section will be used between the power supply source and these device pins as shown in Figure 17. The corner frequency of the LC filter is chosen based on the power supply switching frequency, which is between 100 kHz and 300 kHz in most applications.

Capacitor C1 is a large electrolytic capacitor to provide the basic cut-off frequency of the LC filter. For example, the cutoff frequency of the combination of these elements might fall between 5 kHz and 50 kHz. Capacitors C2 and C3 are smaller ceramic capacitors designed to provide a low-impedance path for a wide range of high-frequency signals at the analog power supply pins of the device. The physical location of capacitor C3 must be as close to the device lead as possible. Multiple instances of capacitors C3 can be used if necessary. The recommended filter for the HSI macro is shown below: L= 4.7 µH, RL = 1Ω, C1 = 4.7 µF, C2 = 0.01 µF, C3 = 0.01 µF.

Figure 17. Sample Power Supply Filter Network for Analog LI Power Supply Pins



XGMII *ORCA* 4E Receive Analysis

XGMII Considerations

The stringent 10 Gbit Media Independent Interface (XGMII) specifications from the *IEEE* 802.3ae standards are met in the FPGA side of the ORLI10G device. This interface is implemented in the PCS IP core and targeted to the ORLI10G FPSC. Figure 18 shows a simplified block diagram for the XGMII interface. Other I/O standards are also possible, such as SSTL or HSTL, with a reference voltage of 1.8 V. Further details are available in the Series 4 I/O application note and the *Series 4 Fast Input DDR and Output DDR with Clock Forwarding* Application Note.

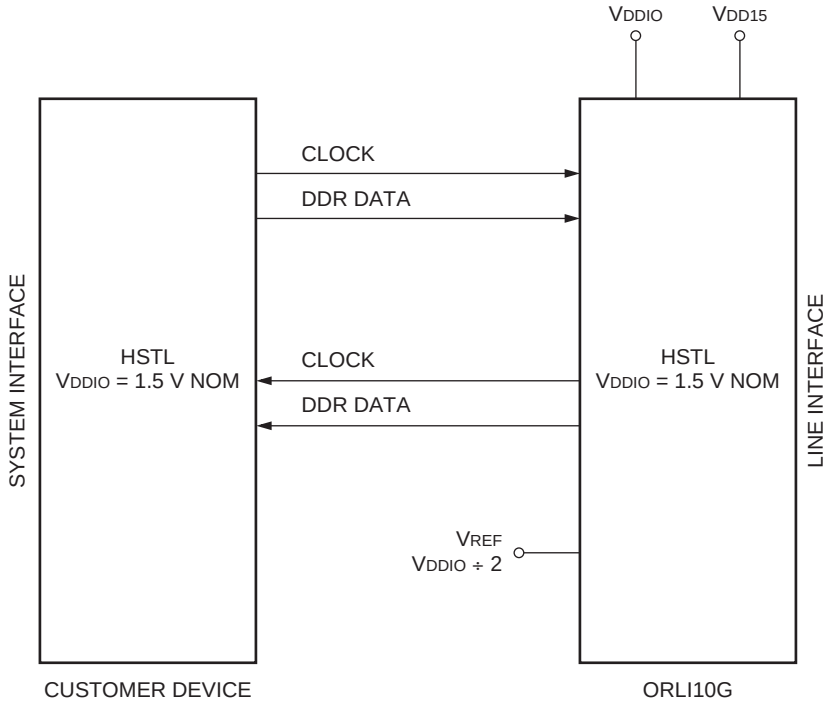
The ORLI10G device meets the 480 ps input setup time and 480 ps input hold time requirements for the XGMII receiver inputs into the FPGA side of the FPSC with the embedded I/O DDR cells on the FPGA side of the FPSC. The PLLs are not used on input because this is a forward clocked interface. The ORLI10G meets the clock-to-out specification on the XGMII DDR outputs by using the output shift register to produce a non-duty-cycle-dependent output. An embedded output DDR capability is also available. The output clock is then centered around this data eye using internal PLLs.

There are two considerations to note about the pinout location of the XGMII input clocks:

1. The XGMII input clocks must be located at the C pad of the programmable I/O cells (PICs). In the pinout tables, the pads are labeled on a pin-by-pin basis. For example, a pin whose pad is referenced as PL1C can be used as an XGMII input clock, but pins referenced as PL1A, PL1B, or PL1D cannot be used as an XGMII input clock.

2. The XGMII input data pins can be no further then six PICs away from the XGMII input clock pin.

Figure 18. Simplified XGMII Block Diagram



Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

The *ORCA* Series 4 FPSCs include circuitry designed to protect the chips from damaging substrate injection currents and to prevent accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use to avoid exposure to excessive electrical stress.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	150	˚C
Power Supply Voltage with Respect to Ground	V_{DD33}	–0.3	4.2	V
	V_{DDIO}	–0.3	4.2	V
	V_{DD33}, V_{DD33_A}	–0.3	4.2	V
	V_{DD15}	–0.3	2.0	V
Input Signal with Respect to Ground	V_{IN}	–0.3	V_{DDIO} + 0.3	V
Signal Applied to High-impedance Output	—	–0.3	V_{DDIO} + 0.3	V
Maximum Package Body (Soldering) Temperature	—	—	220	˚C

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage with Respect to Ground	V_{DD33}	3.0	3.6	V
	V_{DDIO}	1.4	3.6	V
	V_{DD33}, V_{DD33_A}	3.0	3.6	V
	V_{DD15}	1.425	1.575	V
Input Voltages	V_{IN}	–0.3	V_{DDIO} + 0.3	V
Junction Temperature	T_J	–40	125	˚C

For FPGA Recommended Operating Conditions and Electrical Characteristics, see the Recommended Operating Conditions and Electrical Characteristics tables in the ORCA Series 4 FPGA data sheet (OR4E04) and the ORCA Series 4 I/O Buffer Technical Note. FPSC Standby Currents ($I_{DD}SB15$ and $I_{DD}SB33$) are tested with the Embedded Core in the powered down state.

Notes:
The maximum recommended junction temperature (TJ) during operation is 125 ˚C.

Timing parameters in this data sheet are characterized under tighter voltage and temperature conditions than the recommended operating conditions in this table.

The internal PLLs operate from the $V_{DD}33$ and $V_{DD}33\_A$ power supplies. These power supplies should be well isolated from all other power supplies on the board for proper operation.

Embedded Core LVDS I/O

Table 6. Driver dc Data*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage High, VOA or VOB	VOH	RLOAD = 100 Ω	—	—	1.475†	V
Output Voltage Low, VOA or VOB	VOL	RLOAD = 100 Ω	0.925†	—	—	V
Output Differential Voltage	|VOD|	RLOAD = 100 Ω	0.25	—	0.45†	V
Output Offset Voltage	VOS	RLOAD = 100 Ω	1.125*	—	1.275†	V
Output Impedance, Differential	RO	VCM = 1.0 V and 1.4 V	80	100	120	Ω
RO Mismatch Between A and B	Δ RO	VCM = 1.0 V and 1.4 V	—	—	25	mV
Change in Differential Voltage Between Complementary States	|Δ VOD|	RLOAD = 100 Ω	—	—	25	mV
Change in Output Offset Voltage Between Complementary States	Δ VOS	RLOAD = 100 Ω	—	—	25	mV
Output Current	ISA, ISB	Driver shorted to GND	—	—	24	mA
Output Current	ISAB	Drivers shorted together	—	—	12	mA
Power-off Output Leakage	| Ixa, Ixb |	VDD = 0V VPAD, VPADN = 0 V—2.5 V	—	—	10	mA

* Characterized at VDD33 = 3.1 V—3.5 V, VDD15 = 1.425 V—1.575 V, TJ = –40 ˚C - 125 ˚C.
† External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%
.

Table 7. Driver ac Data*

Parameter	Symbol	Test Conditions	Min	Max	Unit
VOD Fall Time, 80% to 20%	tF	ZL = 100 Ω ± 1% CPAD = 3.0 pF, CPAD = 3.0 pF	100	210	ps
VOD Rise Time, 20% to 80%	tR	ZL = 100 Ω ± 1% CPAD = 3.0 pF, CPAD = 3.0 pF	100	210	ps
Differential Skew: |tPHLA –tPLHB| or |tPHLB – tPLHA|	tSKEW1	Any differential pair on package at 50% point of the transition	—	50	ps
Channel-to-channel Skew: |tpDIFFm – tpDIFFn|	tSKEW2	Any two signals on package at 0 V differential	—	—	ps
Propagation Delay Time	tPLH tPHL	ZL = 100 Ω ± 1% CPAD = 3.0 pF, CPAD = 3.0 pF	0.54 0.55	1.10 1.09	ns ns

* Characterized at VDD33 = 3.1 V—3.5 V, VDD15 = 1.425 V—1.575 V, TJ = –40 ˚C - 125 ˚C..

Table 8. Driver Power Consumption*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver dc Power	PDdc	ZL = 100 Ω ± 1%	—	26.0	mW
Driver ac Power	PDac	ZL = 100 Ω ± 1% CPAD = 3.0 pF, CPAD = 3.0 pF	—	64	µW/MHz

* Characterized at VDD33 = 3.1 V—3.5 V, VDD15 = 1.425 V—1.575 V, TJ = –40 ˚C - 125 ˚C.

LVDS Receiver Buffer Requirements

Table 9. Receiver ac Data*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Pulse-width Distortion	t_{PWD}	VIDTH = 100 mV, 311 MHz	—	160	ps
Propagation Delay Time	t_{PLH} t_{PHL}	C_L = 0.5 pF	0.60 0.60	1.42 1.47	ns ns
With Common-mode Variation (0 V to 2.4 V)	t_{PD}	C_L = 0.5 pF	—	50	ps
Output Rise Time, 20% to 80%	t_R	C_L = 0.5 pF	150	350	ps
Output Fall Time, 80% to 20%	t_F	C_L = 0.5 pF	150	350	ps

* Characterized at $V_{DD}33$ = 3.1 V—3.5 V, $V_{DD}15$ = 1.425 V—1.575 V, T_J = –40 ˚C - 125 ˚C.

Table 10. Receiver Power Consumption*

Parameter	Symbol	Test Conditions	Min	Max	Unit
Receiver dc Power	PRdc	dc	—	20.4	mW
Receiver ac Power	PRac	ac C_L = 1.5 pF	—	4.5	µW/MHz

* Characterized at $V_{DD}33$ = 3.1 V—3.5 V, $V_{DD}15$ = 1.425 V—1.575 V, T_J = –40 ˚C - 125 ˚C.

Table 11. Receiver dc Data*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range, V_{IA} or V_{IA}	V_I	$\lvert V_{GPD}\rvert$ < 925 mV dc – 1 MHz	0.0	1.2	2.4	V
Input Differential Threshold	V_{IDTH}	$\lvert V_{GPD}\rvert$ < 925 mV 400 MHz	–100	—	100	mV
Input Differential Hysteresis	V_{HYST}	(+V_{IDTHH}) – (–V_{IDTHL})	25	—	—†	mV
Receiver Differential Input Impedance	R_{IN}	With build-in termination, center-tapped	80	100	120	W

* Characterized at $V_{DD}33$ = 3.1 V—3.5 V, $V_{DD}15$ = 1.425 V—1.575 V, T_J = –40 ˚C - 125 ˚C.
† External reference, REF10 = 1.0 V ± 3%, REF14 = 1.4 V ± 3%.

Table 12. LVDS Operating Parameters

Parameter	Test Conditions	Min	Normal	Max	Unit
Transmit Termination Resistor	—	80	100	120	W
Receiver Termination Resistor	—	80	100	120	W
Temperature Range (T_J)	—	– 40	—	125	°C
Power Supply $V_{DD}33$	—	3.1	—	3.5	V
Power Supply $V_{DD}15$	—	1.4	—	1.6	V
Power Supply V_{SS}	—	—	0	—	V

Note: Under worst-case operating condition, the LVDS driver will withstand a disabled or unpowered receiver for an unlimited period of time without being damaged. Similarly, when outputs are short-circuited to each other or to ground, the LVDS will not suffer permanent damage. The LVDS driver supports hot insertion. Under a well-controlled environment, the LVDS I/O can drive backplane as well as cable.

Timing Characteristics

Receive Input Data Interface

Receive STS-48/STS-192 (2.5G/10G) Data Inputs

Figure 19 illustrates the timing for the receive STS-48/STS-192 data stream. Both the clock and data pins are Low-Voltage Differential Signal (LVDS) input buffers. The expected clock rate is 622 MHz—850 MHz, and the receive data is clocked on the rising edge of the clock. In 2.5G mode, each of the four channels uses one set of one RX_CLK_INn and four RX_DAT_INn data pins. In 10G mode, only RX_CLK_IN0 is used, along with the RX_DAT_IN[15:0] pins. The timing values for the diagram in Figure 19 are given in Table 13.

Figure 19. Receive Input Data Timing

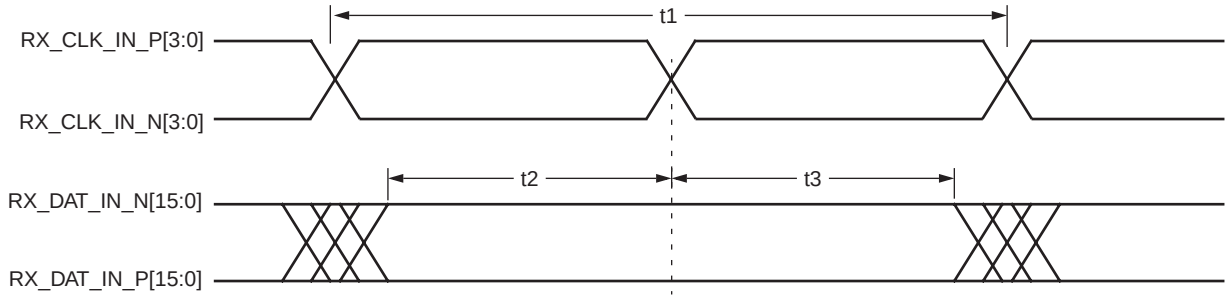


Table 13. Receive Data Input Timing

Parameter	Symbol	–1		–2		–3		Unit
		Min	Max	Min	Max	Min	Max	
Clock Frequency	t1	—	667	—	790	—	850	MHz
Data Setup Time Required	t2	300	—	225	—	210	—	pS
Data Hold Time Required	t3	300	—	225	—	210	—	pS

- It is recommended that the Rx clock be inverted by crossing the LVDS pin pair, that is, connect the RX_CLK_IN_P[3:0] input signal on the ORLI10G to the N (i.e., complement) clock output from the transmitting device and connect the RX_CLK_IN_N[3:0] input on the ORLI10G to the P (i.e., true) clock output from the transmitting device. This is because the embedded line interface on the ORLI10G requires the Rx data to be centered on the Rx clock, and typically the devices that drive the ORLI10G transmit clock and data on the same clock edge.

Transmit STS-48/STS-192 (2.5G/10G) Data Outputs

Figure 20 illustrates the timing for the transmit STS-48/STS-192 data stream. Both the clock and data pins are driven with Low-Voltage Differential Signal (LVDS) output buffers. The expected clock rate is 622 MHz-850 MHz and the transmit data is clocked out on the rising edge of the clock. In 2.5G mode, each of the four channels uses one set of TX_CLK_OUTn with four TX_DAT_OUTn data pins. In 10G mode, only TX_CLK_OUT[0] is used with the 16 TX_DAT_OUT[15:0] pins. The timing values for the diagram in Figure 20 are given in Table 14.

Figure 20. Transmit Output Data Timing

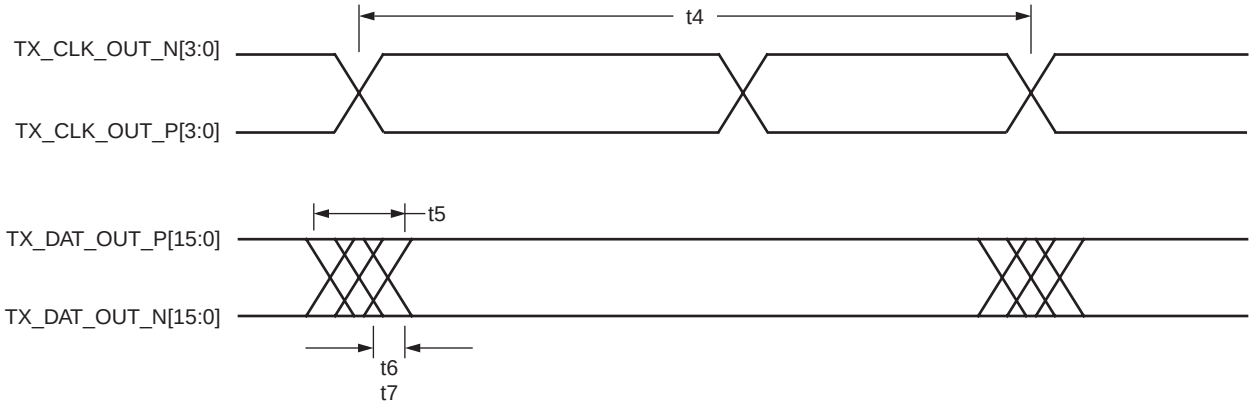


Table 14. Transmit Data Output Timing

Parameter	Symbol	–1		–2		–3		Unit
		Min	Max	Min	Max	Min	Max	
Clock Frequency	t4	—	667	—	790	—	850	MHz
Duty Cycle	—	45	55	45	55	45	55	%
Data Delay from Clock Edge	t5	–300	300	–225	225	–210	210	pS
Data Rise Time: 20%—80%	t6	100	200	100	200	100	200	pS
Data Fall Time: 80%—20%	t7	100	200	100	200	100	200	pS

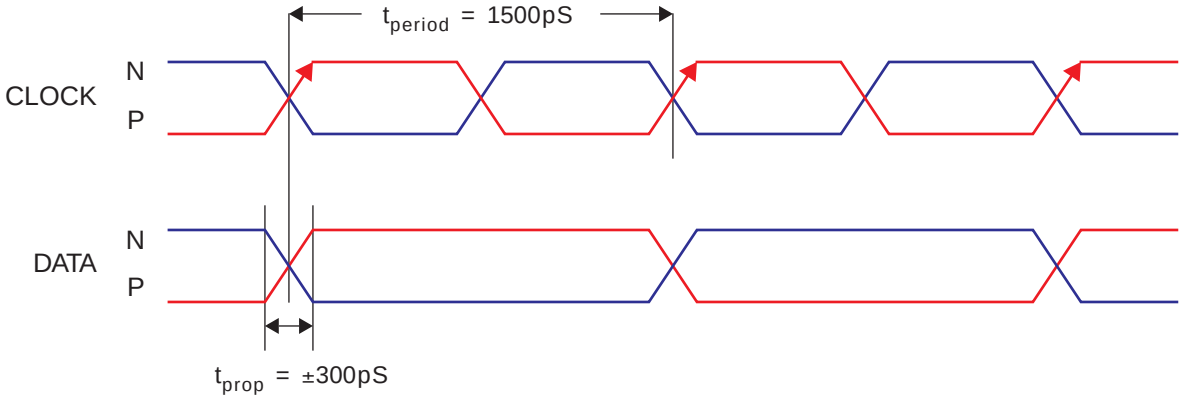
Note: This requirement is for all sources of the output clocks (e.g., RCLKSI, etc.).

It is recommended that the Tx clock be inverted by crossing the LVDS pin pair, that is, connect the TX_CLK_OUT_P[3:0] output on the ORLI10G to the N (i.e., complement) clock input on the receiving device and connect the TX_CLK_OUT_N[3:0] output on the ORLI10G to the P (i.e., true) clock input on the receiving device. This is because the receiving device that will be driven by the ORLI10G typically requires that data be centered around the clock, but the ORLI10G drives both the clock and data from the same clock edge.

Recommended Board Level Routing For ORLI10G XSBI 10G Interface

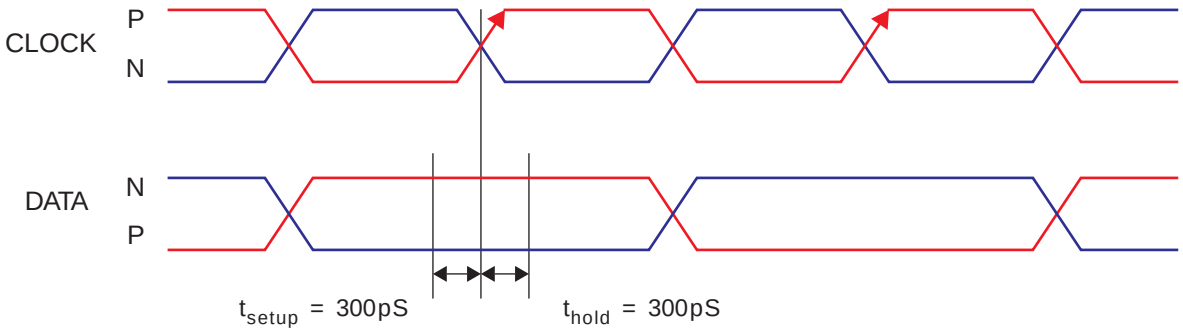
The Transmit XSBI port sends clock and data **simultaneously** as shown in Figure 21.

Figure 21. Clock and Data signals from the TX



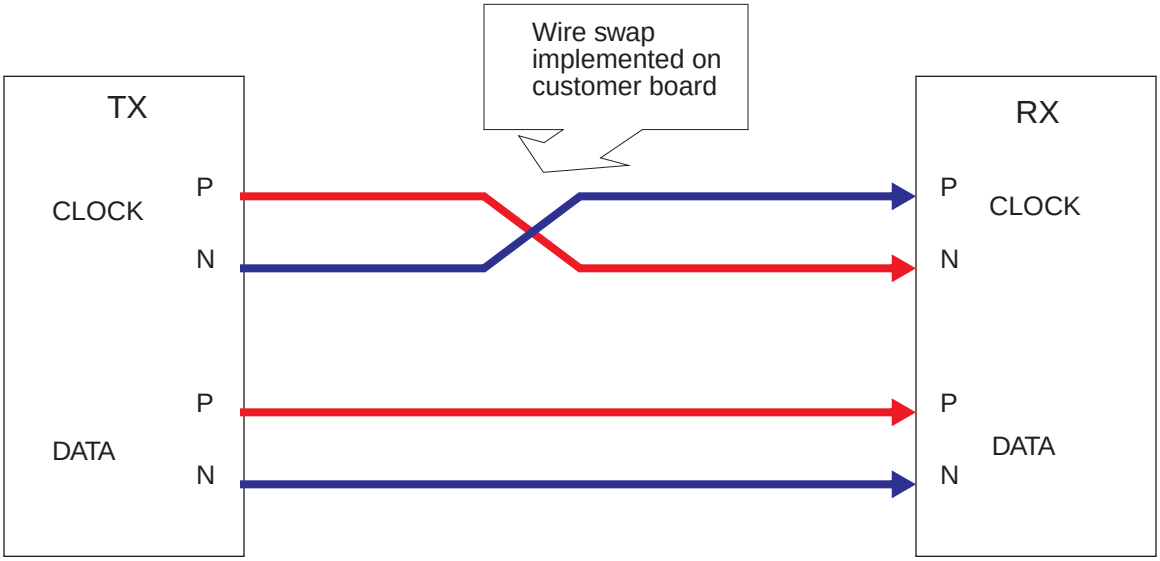
The correct clock and data relation required for the XSBI receiver is to have the clock centered in the data eye (as shown in Figure 22).

Figure 22. Clock and Data Signals at the Receiver



In order to achieve the needed clock and data relationship at the receiver as shown in Figure 21, it is necessary to swap the P and N clock terminals on the board. This is illustrated in Figure 23. The board level signal swap on the receiver clock pins effectively inverts the clock phase at the receiving chip creating the correct clock data relationship shown in Figure 22.

Figure 23. Implementing Clock Wire Swap



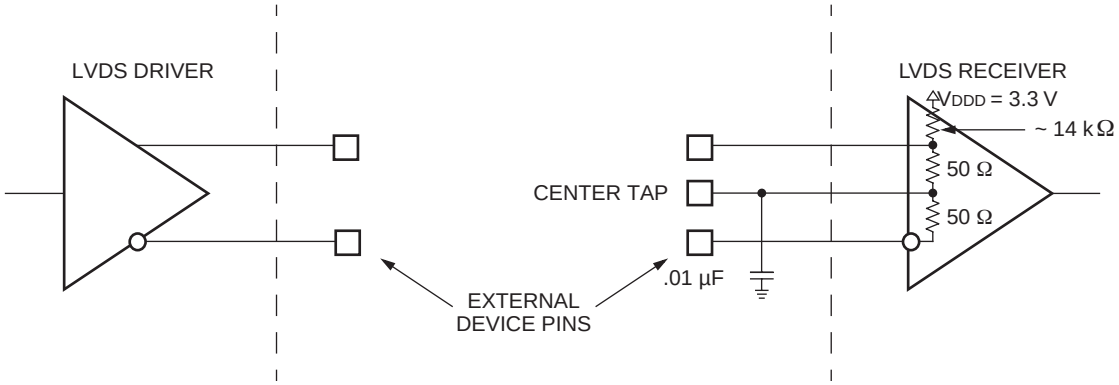
The above describes standard practice for XSBI 10G Interfaces.

LVDS Buffer Characteristics

Termination Resistor

The LVDS drivers and receivers operate on a 100 Ω differential impedance, as shown below. External resistors are not required. The differential receiver buffers include termination resistors inside the device package, as shown in Figure 24.

Figure 24. LVDS Driver and Receiver and Associated Internal Components



LVDS Driver Buffer Capabilities

Under worst-case operating condition, the LVDS driver must withstand a disabled or unpowered receiver for an unlimited period of time without being damaged. Similarly, when its outputs are short-circuited to each other or to ground, the LVDS driver will not suffer permanent damage. Figure 25 illustrates the terms associated with LVDS driver and receiver pairs.

Figure 25. LVDS Driver and Receiver

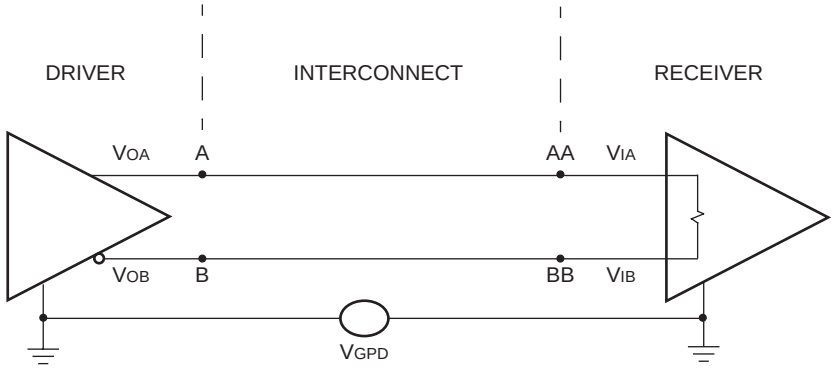
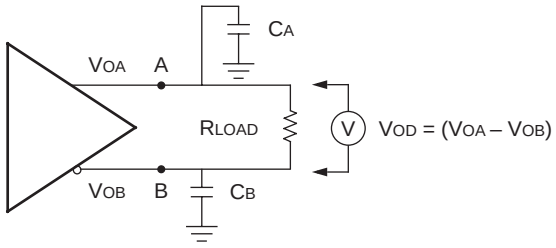


Figure 26. LVDS Driver



ORLI10G Interface Timing Diagrams

This section describes the timing at the FPGA – Core boundary. There are 4 distinct timing modes available for use with the ORLI10G device (note that for TX, 10G mode can be used for either 10G or 2.5G operation):

- 10G RX and TX with PLL used across the interface.
- 10G RX and TX with NO PLL used across the interface.
- Quad 2.5G RX with NO PLL used across the interface plus 10G TX with PLL used across the interface.
- Quad 2.5G RX with NO PLL used across the interface plus 10G TX with NO PLL used across the interface.

Figure 27 shows a simplified, single channel view of the transmit path in divide-by-four mode. The divide-by-8 mode timing is similar, where the slow speed clocks are 1/8th the fast clock speed. PLL_TX2 is used to align clocks across the Embedded Line Interface – FPGA boundary. The PLL_TX1 macro is not used as it is unneeded. The PLLs in the embedded line interface can be bypassed via the PLL_BYPASS external FPSC pin. The feedback loop shown is connected up automatically by the design kit software.

Figure 27. Single Channel Tx Divide-by-4 Diagram (-1 Speed Grade)

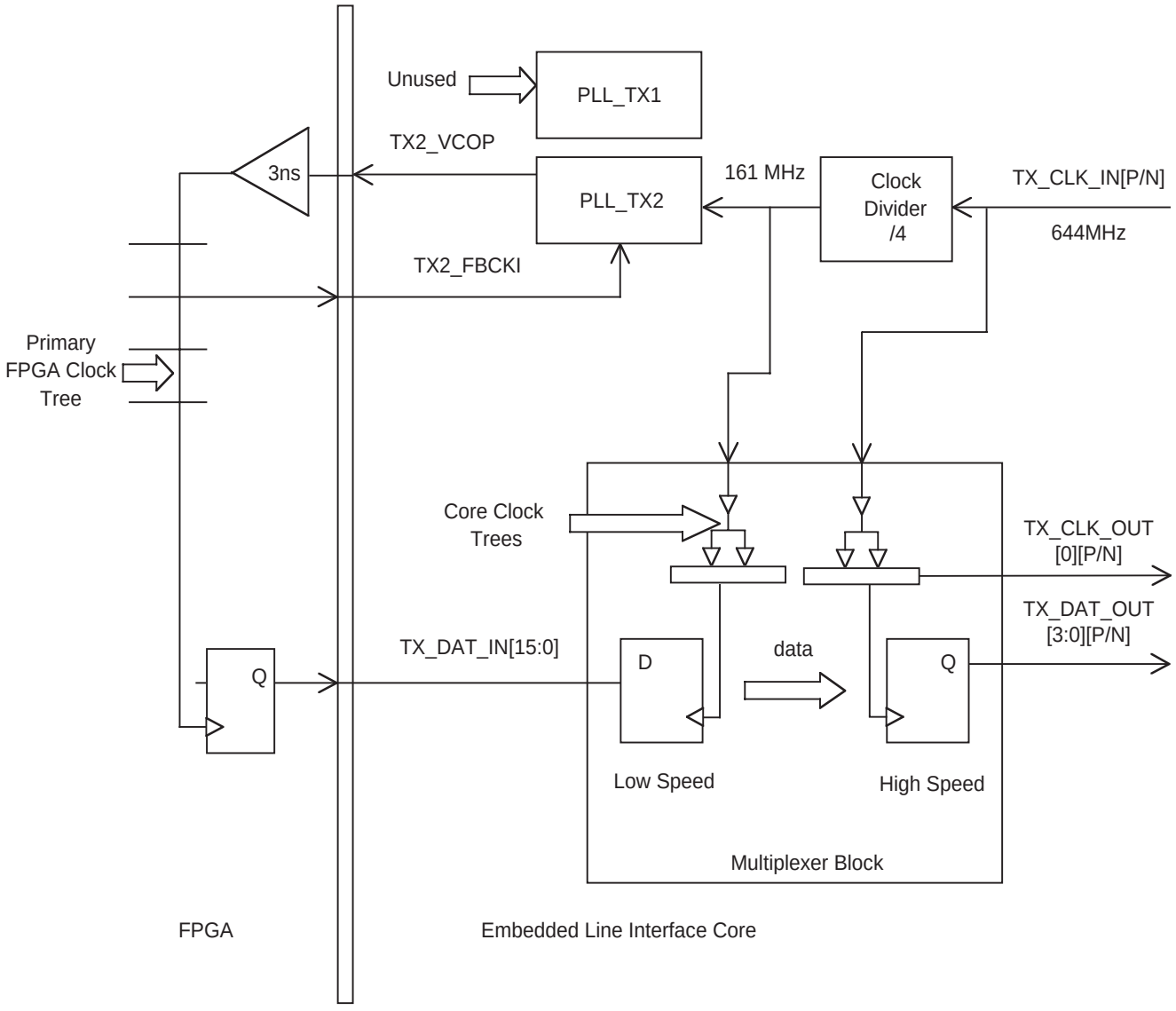


Figure 28 shows the Transmit (FPGA to embedded Line Interface) timing for 10G mode where PLL_TX2 is used to align clocks across the FPGA - Core boundary. The 1.9 ns hold time shown is an approximate hold time value for the embedded line interface. Consult the ispLEVER software, via the static timing analysis tool TRACE, for the exact timing values. Figure 28. shows a full cycle transfer. Designers should make sure to satisfy the hold requirement.

Figure 28. Transmit Timing for 10G Mode with PLL for Clock Alignment (-1 Speed Grade)

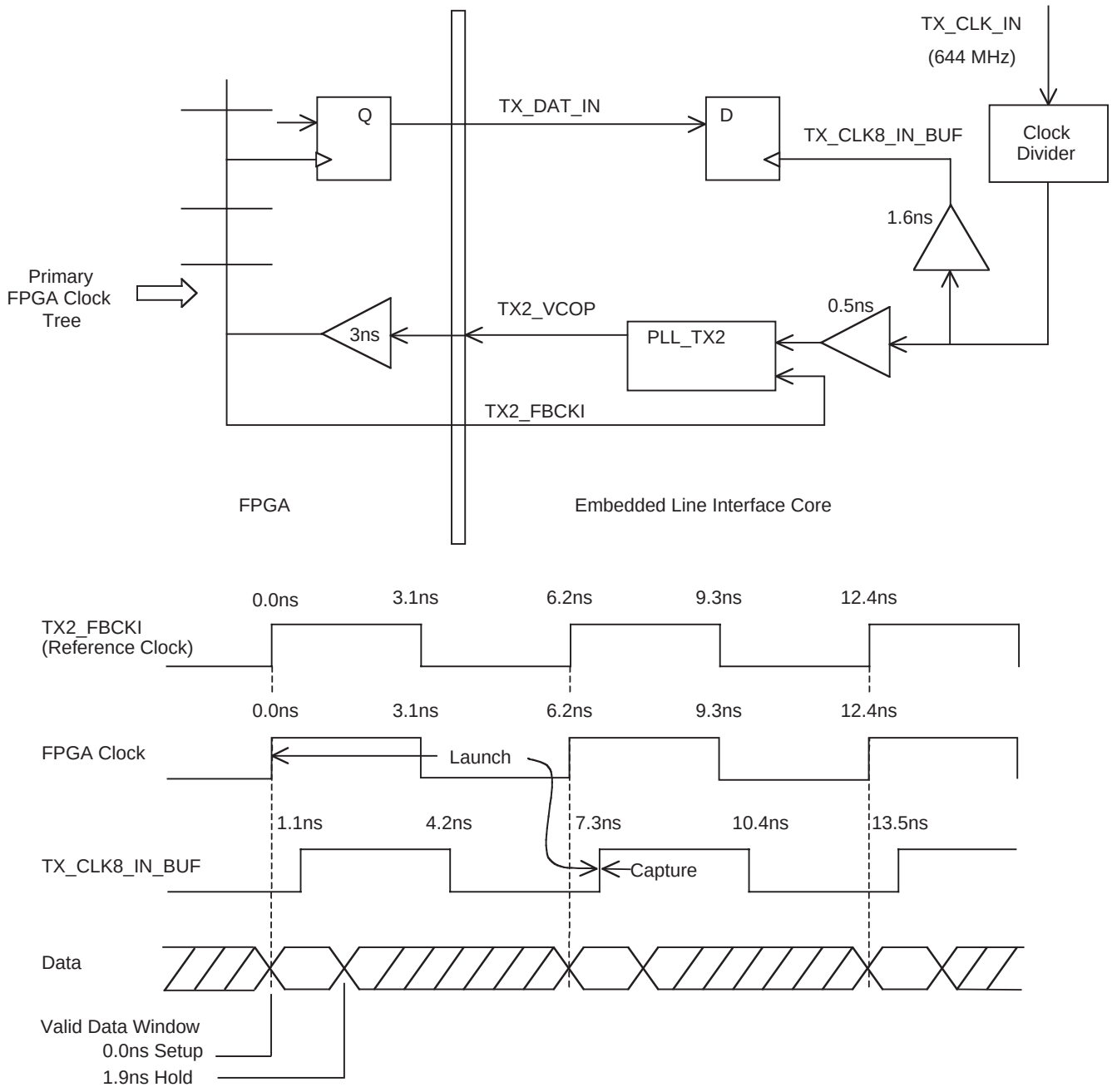


Figure 29 shows the Transmit (FPGA to embedded Line Interface) timing for 10G mode where PLL_TX2 is bypassed via the PLL_BYPASS external FPSC pin. The 0.4 ns setup time and the 1.1 ns hold time shown are approximate values for the embedded line interface. Consult the ispLEVER software, via the static timing analysis tool TRACE, for the exact timing values. Figure 29 shows a half cycle transfer. Designers should make sure to satisfy the hold requirement. A full cycle transfer is also possible for this scenario when the clock period is 10 ns or longer (< 100 MHz).

Figure 29. Transmit Timing for 10G Mode with PLL Bypassed (-1 Speed Grade)

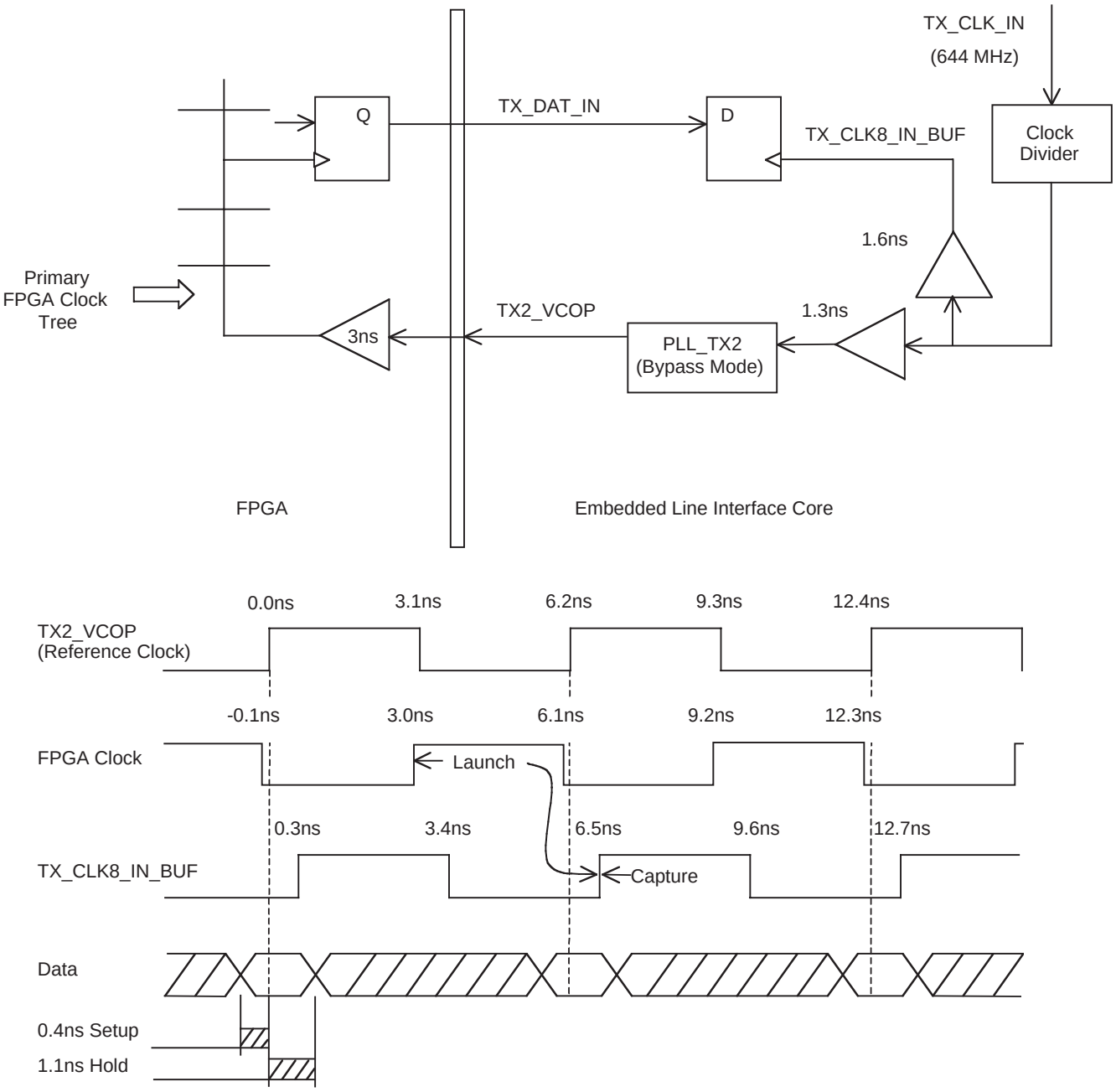


Figure 30 shows a simplified, single channel view of the recieve path in divide-by-four mode. The divide-by-8 mode timing is similar, where the slow speed clocks are 1/8th the fast clock speed. If a primary clock is used in the FPGA, PLL_RX2 is used to align clocks across the embedded ASIC – FPGA boundary. If the secondary clock is used in the FPGA, PLL_RX2 is not and there is a 1.0 ns to 3.5 ns clock insertion delay incurred on the secondary clocks. The quad 2.5 G mode requires four secondary clocks to be used, one for each 2.5 G channel. The PLL_RX1 macro is not used as it is unneeded. The PLLs in the embedded line interface can be bypassed via the PLL_BYPASS external FPSC pin. The feedback loop shown is connected up automatically by the design kit software. The Mode select on the clock multiplexer in the embedded line interface is also connected up automatically by the design kit software. If in 10G mode, one clock is used and corresponds to the RX_CLK_IN[0] external device pin.

Figure 30. Single-Channel Rx Divide-by-4 Diagram (-1 Speed Grade)

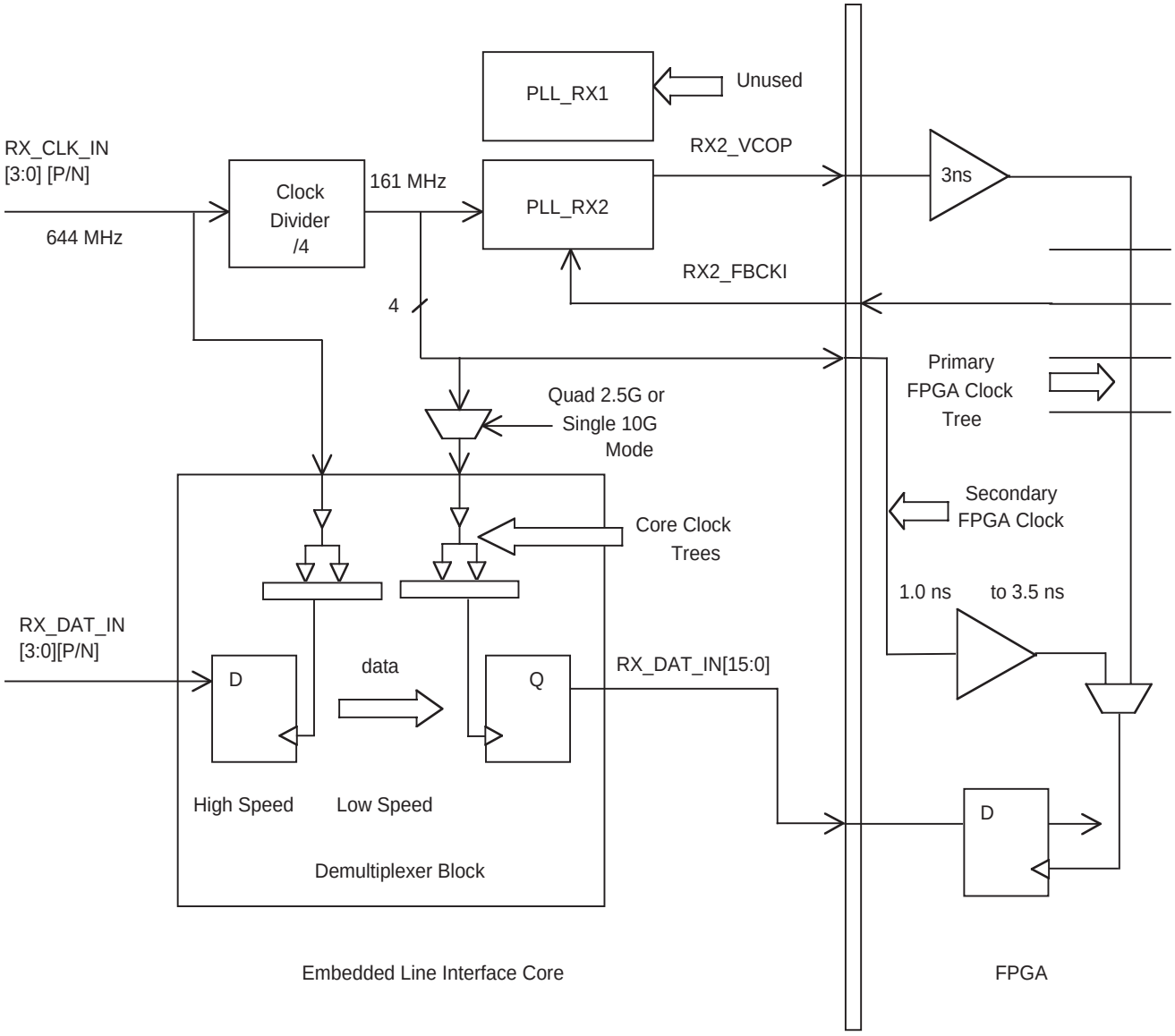
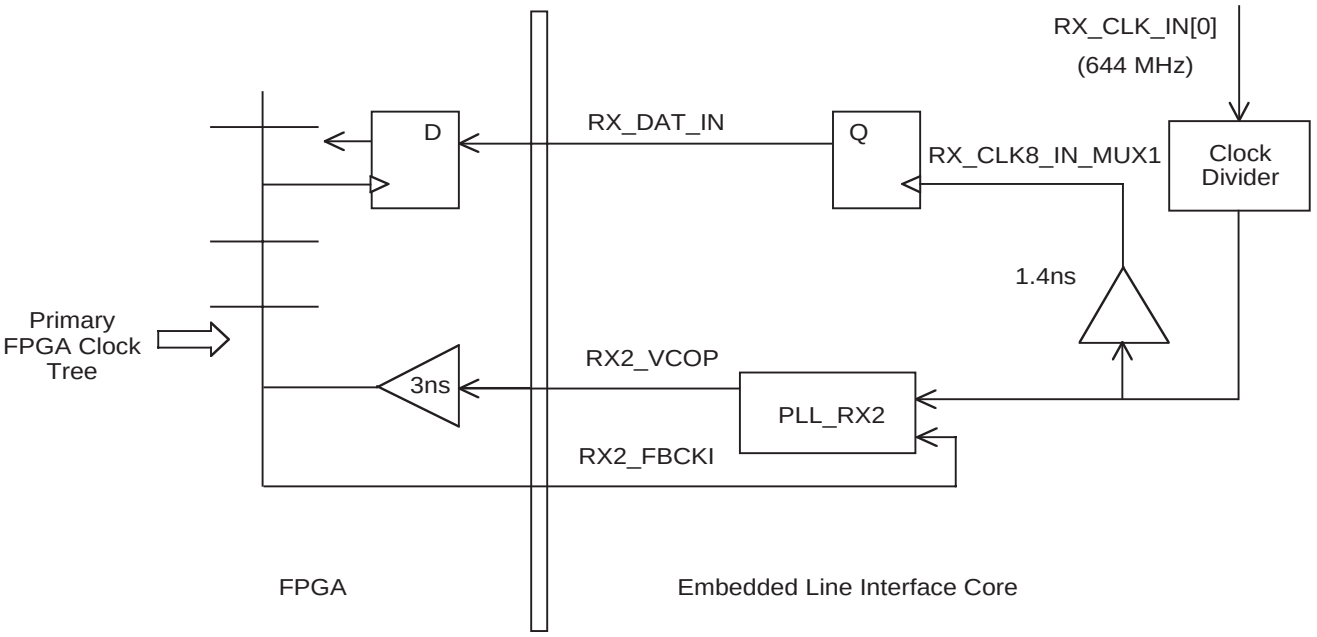


Figure 31 shows the Receive (Embedded Line Interface to FPGA) timing for 10G mode where PLL_RX2 is used to align clocks across the FPGA - Core boundary. The 0.9 ns minimum propagation delay and 2.7 ns maximum propagation delay shown are approximate values for the embedded line interface. In the waveform shown, data will be time shifted at the FPGA capture register due to FPGA data path delay. Consult the ispLEVER software, via the static timing analysis tool TRACE, for the exact timing values. Figure 31 shows a full cycle transfer.

Figure 31. Receive Timing for 10G Mode with PLL for Clock Alignment (-1 Speed Grade)



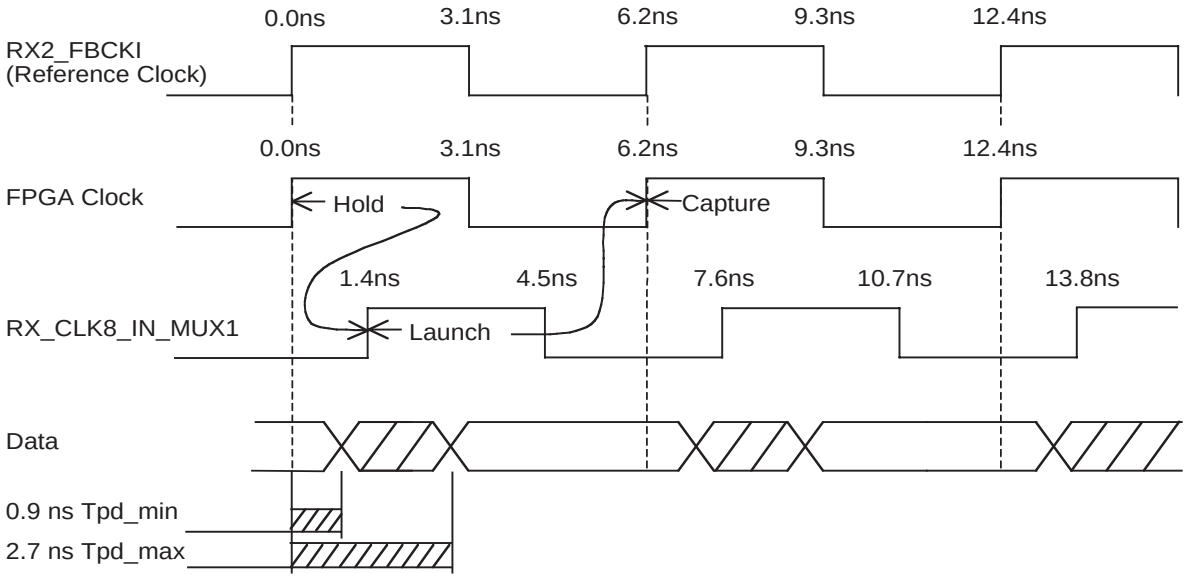


Figure 32 shows the Receive (Embedded Line Interface to FPGA) timing for 10G mode where PLL_RX2 is bypassed via the PLL_BYPASS external FPSC pin. The 0.7 ns minimum propagation delay and 1.9 ns maximum propagation delay shown are approximate values for the embedded line interface in this scenario. In the waveform shown, data will be time shifted at the FPGA capture register due to FPGA data path delay. Consult the ispLEVER software, via the static timing analysis tool TRACE, for the exact timing values. Figure 32 shows a half cycle transfer; note the inversion bubble on the FPGA capture register. This half cycle transfer negates possible hold timing issues. If a full cycle transfer is used with the receive PLL bypassed, check for hold violations with the static timing analysis tool TRACE.

Figure 32. Receive Timing for 10G Mode with PLL Bypassed (-1 Speed Grade)

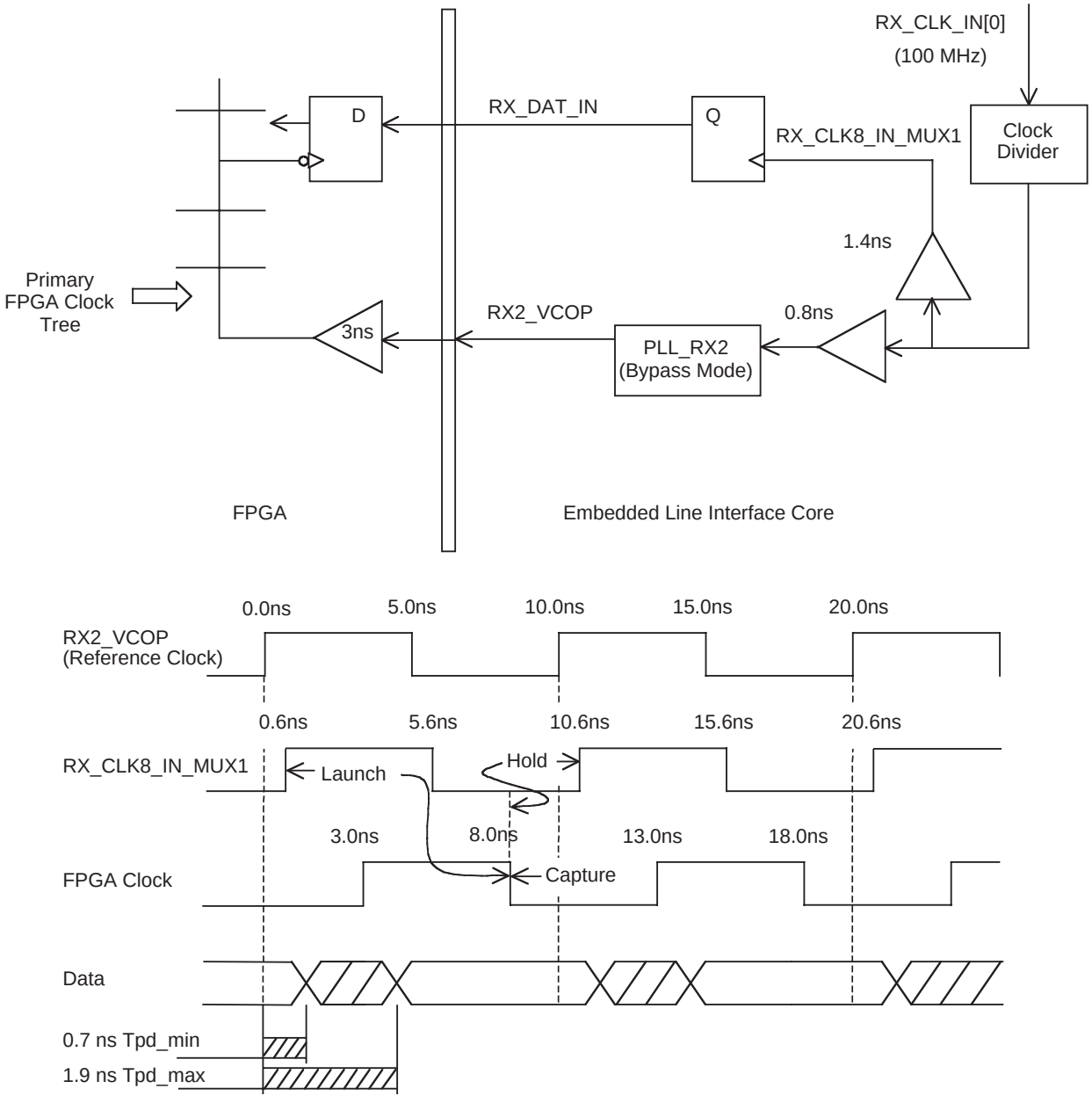
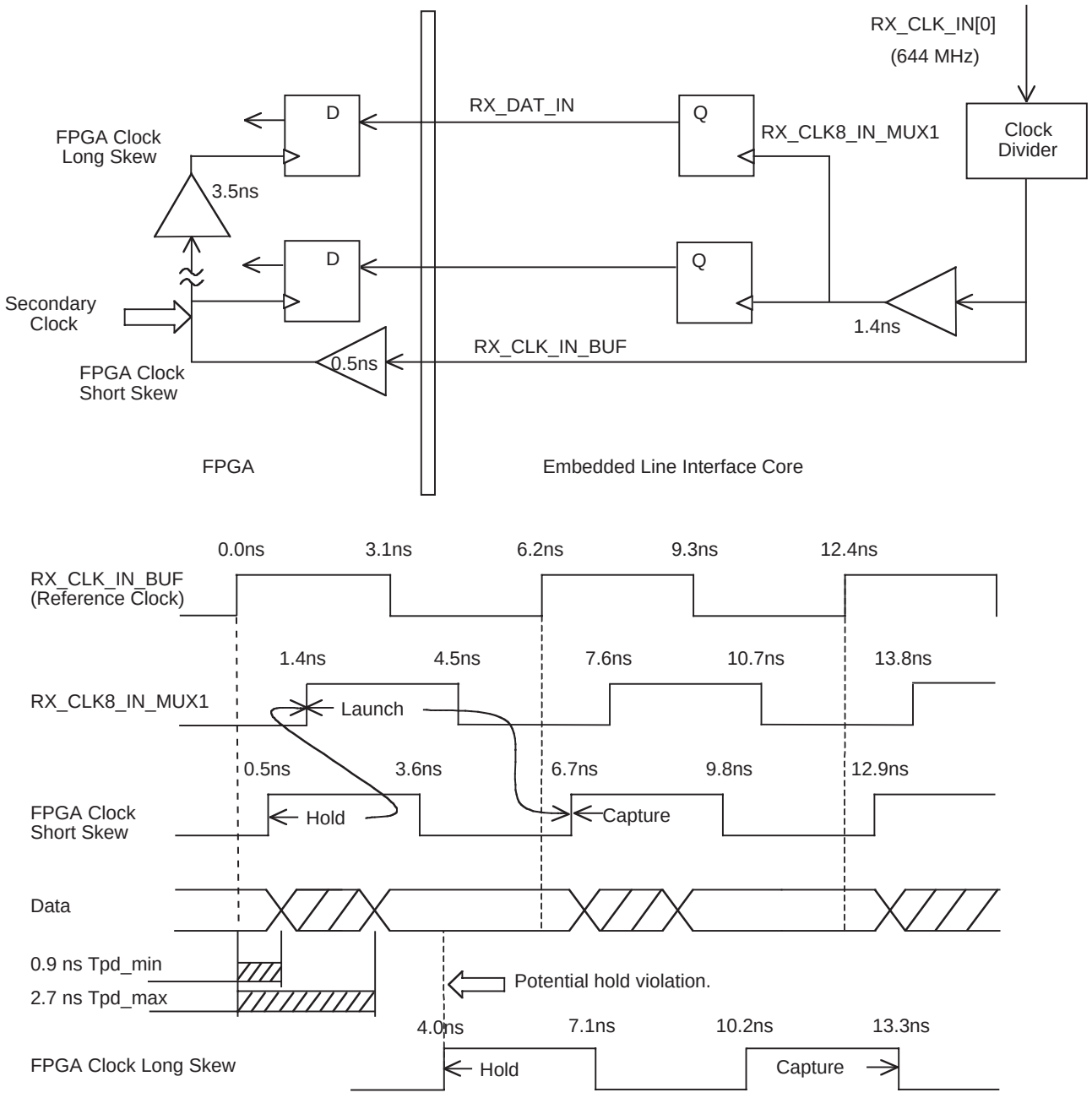


Figure 33 shows the Receive (Embedded Line Interface to FPGA) timing for 2.5G mode where PLL_RX2 is bypassed via the PLL_BYPASS external FPSC pin. The 0.9 ns minimum propagation delay and 2.7 ns maximum propagation delay shown are approximate values for the embedded line interface in this scenario. In the waveform shown, data will be time shifted at the FPGA capture register due to FPGA data path delay. Consult the ispLEVER software, via the static timing analysis tool TRACE, for the exact timing values. The FPGA data path delay needs to increase together with clock skew to avoid hold issues. The FPGA design should be checked for hold violations with TRACE.

Figure 33. Receive Timing for 2.5G Mode with PLL Bypassed (-1 Speed Grade)



Pin Information

Pin Descriptions

This section describes the pins found on the Series 4 FPGAs. Any pin not described in this table is a user-programmable I/O. During configuration, the user-programmable I/Os are 3-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also 3-stated with an internal pull-up resistor enabled after configuration. The pin descriptions in Table 15 and throughout this data sheet show active-low signals with an overscore. The package pinout tables that follow show this as a signal ending with _N. Therefore, $\overline{\text{LDC}}$ and LDC_N are equivalent.

Table 15. Pin Descriptions

Symbol	I/O	Description
Dedicated Pins		
VDD33	—	3.3 V positive power supply. This power supply is used for 3.3 V configuration RAMs and internal PLLs. When using PLLs, this power supply should be well isolated from all other power supplies on the board for proper operation.
VDD15	—	1.5 V positive power supply for internal logic.
VDDIO	—	Positive power supply used by I/O banks.
VSS	—	Ground.
PTEMP	I	Temperature sensing diode pin. Dedicated input.
$\overline{\text{RESET}}$	I	During configuration, $\overline{\text{RESET}}$ forces the restart of configuration and a pull-up is enabled. After configuration, $\overline{\text{RESET}}$ can be used as a general FPGA input or as a direct input, which causes all PLC latches/Flip-Flops to be asynchronously set/reset.
CCLK	O	In the master and asynchronous peripheral modes, CCLK is an output which strobes configuration data in.
	I	In the slave or readback after configuration, CCLK is input synchronous with the data on DIN or D[7:0]. CCLK is an output for daisy-chain operation when the lead device is in master, peripheral, or system bus modes.
DONE	I	As an input, a low level on DONE delays FPGA start-up after configuration.*
	O	As an active-high, open-drain output, a high level on this signal indicates that configuration is complete. DONE has an optional pull-up resistor.
$\overline{\text{PRGM}}$	I	$\overline{\text{PRGM}}$ is an active-low input that forces the restart of configuration and resets the boundary-scan circuitry. This pin always has an active pull-up.
$\overline{\text{RD\_CFG}}$	I	This pin must be held high during device initialization until the $\overline{\text{INIT}}$ pin goes high. This pin always has an active pull-up. During configuration, $\overline{\text{RD\_CFG}}$ is an active-low input that activates the TS_ALL function and 3-states all of the I/O. After configuration, $\overline{\text{RD\_CFG}}$ can be selected (via a bit stream option) to activate the TS_ALL function as described above, or, if readback is enabled via a bit stream option, a high-to-low transition on $\overline{\text{RD\_CFG}}$ will initiate readback of the configuration data, including PFU output states, starting with frame address 0.
RD_DATA/TDO	O	RD_DATA/TDO is a dual-function pin. If used for readback, RD_DATA provides configuration data out. If used in boundary-scan, TDO is test data out.
$\overline{\text{CFG\_IRQ}}$/MPI_IRQ	O	During JTAG, slave, master, and asynchronous peripheral configuration, assertion on this $\overline{\text{CFG\_IRQ}}$ (active-low) indicates an error or errors for block RAM or FPSC initialization. MPI active-low interrupt request output, when the MPI is used.

*The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

***Table 15. Pin Descriptions** (continued)*

Symbol	I/O	Description
Special-Purpose Pins		
M[3:0]	I	During powerup and initialization, M0—M3 are used to select the configuration mode with their values latched on the rising edge of $\overline{\text{INIT}}$. During configuration, a pull-up is enabled.
	I/O	After configuration, these pins are user-programmable I/O.*
PLL_CK[0:7][TC]	I	Semidedicated PLL clock pins. During configuration they are 3-stated with a pull-up.
	I/O	These pins are user-programmable I/O pins if not used by PLLs after configuration.
P[TBLR]CLK[1:0][TC]	I	Pins dedicated for the primary clock. Input pins on the middle of each side with differential pairing.
	I/O	After configuration, these pins are user-programmable I/O, if not used for clock inputs.
TDI, TCK, TMS	I	If boundary-scan is used, these pins are test data in, test clock, and test mode select inputs. If boundary-scan is not selected, all boundary-scan functions are inhibited once configuration is complete. Even if boundary-scan is not used, either TCK or TMS must be held at logic 1 during configuration. Each pin has a pull-up enabled during configuration.
	I/O	After configuration, these pins are user-programmable I/O if boundary scan is not used.*
RDY/$\overline{\text{BUSY}}$/RCLK	O	During configuration in asynchronous peripheral mode, RDY/RCLK indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D7 in asynchronous peripheral mode. During the master parallel configuration mode, RCLK is a read output signal to an external memory. This output is not normally used.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
HDC	O	High during configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
LDC	O	$\overline{\text{Low during configuration}}$ is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{INIT}}$	I/O	$\overline{\text{INIT}}$ is a bidirectional signal before and during configuration. During configuration, a pull-up is enabled, but an external pull-up resistor is recommended. As an active-low open-drain output, $\overline{\text{INIT}}$ is held low during power stabilization and internal clearing of memory. As an active-low input, $\overline{\text{INIT}}$ holds the FPGA in the wait-state before the start of configuration. After configuration, this pin is a user-programmable I/O pin.*
$\overline{\text{CS0}}$, CS1	I	$\overline{\text{CS0}}$ and CS1 are used in the asynchronous peripheral, slave parallel, and microprocessor configuration modes. The FPGA is selected when $\overline{\text{CS0}}$ is low and CS1 is high. During configuration, a pull-up is enabled.
	I/O	After configuration, if MPI is not used, these pins are user-programmable I/O pins.*
$\overline{\text{RD}}$/$\overline{\text{MPI\_STRB}}$	I	$\overline{\text{RD}}$ is used in the asynchronous peripheral configuration mode. A low on $\overline{\text{RD}}$ changes D[7:3] into a status output. $\overline{\text{WR}}$ and $\overline{\text{RD}}$ should not be used simultaneously. If they are, the write strobe overrides. This pin is also used as the MPI data transfer strobe. As a status indication, a high indicates ready, and a low indicates busy.
	I/O	After configuration, if the MPI is not used, this pin is a user-programmable I/O pin.*

* The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

***Table 15. Pin Descriptions** (continued)*

Symbol	I/O	Description
Special-Purpose Pins (continued)		
$\overline{WR}$/MPI_RW	I	$\overline{WR}$ is used in asynchronous peripheral mode. A low on $\overline{WR}$ transfers data on D[7:0] to the FPGA. In MPI mode, a high on MPI_RW allows a read from the data bus, while a low causes a write transfer to the FPGA.
	I/O	After configuration, if the MPI is not used, $\overline{WR}$/MPI_RW is a user-programmable I/O pin.*
PPC_A[14:31]	I	During MPI mode, the PPC_A[14:31] are used as the address bus driven by the *PowerPC* bus master utilizing the least-significant bits of the *PowerPC* 32-bit address.
$\overline{MPI\_BURST}$	I	$\overline{MPI\_BURST}$ is driven low to indicate a burst transfer is in progress in MPI mode. Driven high indicates that the current transfer is not a burst.
$\overline{MPI\_BDIP}$	I	$\overline{MPI\_BDIP}$ is driven by the *PowerPC* processor in MPI mode. Assertion of this pin indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.
MPI_TSZ[0:1]	I	MPI_TSZ[0:1] signals are driven by the bus master in MPI mode to indicate the data transfer size for the transaction. Set 01 for byte, 10 for half-word, and 00 for word.
A[21:0]	O	During master parallel mode, A[21:0] address the configuration EPROMs up to 4 Mbytes.
	I/O	If not used for MPI, these pins are user-programmable I/O pins after configuration.*
MPI_ACK	O	In MPI mode, this is driven low indicating the MPI received the data on the write cycle or returned data on a read cycle.
	I/O	If not used for MPI, these pins are user-programmable I/O pins after configuration.*
MPI_CLK	I	This is the *PowerPC* synchronous, positive-edge bus clock used for the MPI interface. It can be a source of the clock for the embedded system bus. If MPI is used, this will be the *AMBA* bus clock.
	I/O	If not used for MPI, these pins are user-programmable I/O pins after configuration.*
MPI_TEA	O	A low on the MPI transfer error acknowledge indicates that the MPI detects a bus error on the internal system bus for the current transaction.
	I/O	If not used for MPI, these pins are user-programmable I/O pins after configuration.*
MPI_RTRY	O	This pin requests the MPC860 relinquish the bus and retry the cycle.
	I/O	If not used for MPI, these pins are user-programmable I/O pins after configuration.*
D[0:31]	I/O	Selectable data bus width from 8-, 16-, 32-bit in MPI mode. Driven by the bus master in a write transaction and driven by MPI in a read transaction.
	I	D[7:0] receive configuration data during master parallel, peripheral, and slave parallel configuration modes when $\overline{WR}$ is low and each pin has a pull-up enabled. During serial configuration modes, D0 is the DIN input.
	O	D[7:3] output internal status for asynchronous peripheral mode when $\overline{RD}$ is low.
	I/O	After configuration, if MPI is not used, the pins are user-programmable I/O pins.*
DP[0:3]	I/O	Selectable parity bus width in MPI mode from 1-, 2-, 4-bit, DP[0] for D[0:7], DP[1] for D[8:15], DP[2] for D[16:23], and DP[3] for D[24:31]. After configuration, if MPI is not used, the pins are user-programmable I/O pin.*

* The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

***Table 15. Pin Descriptions** (continued)*

Symbol	I/O	Description
Special-Purpose Pins (continued)		
DIN	I	During slave serial or master serial configuration modes, DIN accepts serial configuration data synchronous with CCLK. During parallel configuration modes, DIN is the D0 input. During configuration, a pull-up is enabled.
	I/O	After configuration, this pin is a user-programmable I/O pin.*
DOUT	O	During configuration, DOUT is the serial data output that can drive the DIN of daisy-chained slave devices. Data out on DOUT changes on the rising edge of CCLK.
	I/O	After configuration, DOUT is a user-programmable I/O pin.*
TESTCFG	I	During configuration this pin should be held high, to allow configuration to occur. A pull-up is enabled during configuration.
	I/O	After configuration, TESTCFG is a user-programmable I/O pin.*

* The timing of DONE release is controlled by one set of bit stream options, and the timing of the simultaneous release of all other configuration pins (and the activation of all user I/Os) is controlled by a second set of options.

Pin Information (continued)

This table describes the I/O signal ports on the embedded core portion of the device.

Table 16. FPSC Function Pin Description

Symbol	I/O	Description
Control and Global Pins		
PLL_BYPASS	I	3.3 V active-high. Enables the bypass mode for both receive and both transmit PLLs.
PWRDN	I	3.3 V active-high. Power down all LVDS links and both receive and both transmit PLLs.
RESET_RX	I	3.3 V active-high. Resets the receive PLLs and the demultiplexer block.
RESET_TX	I	3.3 V active-high. Resets the transmit PLLs and the multiplexer block.
Receive I/O Pins		
RX_DAT_IN_N<15:0>	I	LVDS data input for receive side.
RX_DAT_IN_P<15:0>	I	LVDS data input for receive side.
RX_CLK_IN_N<3:0>	I	LVDS clock inputs for receive side.
RX_CLK_IN_P<3:0>	I	LVDS clock inputs for receive side.
Transmit I/O Pins		
TX_DAT_OUT_N<15:0>	O	LVDS data outputs on transmit side.
TX_DAT_OUT_P<15:0>	O	LVDS data outputs on transmit side.
TX_CLK_OUT_N<3:0>	O	LVDS clock outputs on transmit side.
TX_CLK_OUT_P<3:0>	O	LVDS clock outputs on transmit side.
TX_CLK_IN_N	I	LVDS transmit reference clock input.
TX_CLK_IN_P	I	LVDS transmit reference clock input.
LVDS Input Reference Pins		
LV_REF10	—	LVDS reference voltage: 1.0 V ± 3%.
LV_REF14	—	LVDS reference voltage: 1.4 V ± 3%.
LV_RESHI	—	LVDS resistor high pin (use 100 Ω to LV_RESLO pin).
LV_RESLO	—	LVDS resistor low pin (use 100 Ω to LV_RESHI pin).
LVCTAP_[6:1]	—	LVDS input centertap (use 0.01 µF to GRD).

Pin Information (continued)

In Table 17, an output refers to a signal flowing into the FGPA logic (out of the embedded core) and an input refers to a signal flowing out of the FPGA logic (into the embedded core).

Table 17. Embedded Core/FPGA Interface Signal Description

Symbol	I/O	Description
Receive Signals		
RX_DAT_OUT<127:0>	O	Data from demultiplexer on receive side.
RX_CLK8_OUT<3:0>	O	Divided down clocks on receive side.
RX_ENB8_OUT<3:0>	O	Data enables on receive side.
RX1_VCOP	O	RX1_PLL output clock on receive side (M/N clock) after phase select.
RX1_VCO	O	RX1_PLL output clock on receive side (M/N clock) before phase select.
RX2_VCOP	O	RX2_PLL output clock on receive side (x1 clock) before phase select.
RX2_VCO	O	RX2_PLL output clock on receive side (x1 clock) before phase select.
RX2_FBCKI	I	PLL feedback input to RX2_PLL. This allows for the removal of the FPGA clock routing delay.
RX1_BYPASS	I	Set to 1 to bypass the RX1 PLL.
RX2_BYPASS	I	Set to 1 to bypass the RX2 PLL
RX_LOCK	O	Lock the signal for RX1_PLL and RX2_PLL. This signal is a logical OR of the lock signal from both PLLs. It is not integrated; thus, small glitches can occur on this signal during normal PLL operation.
Transmit Signals		
TX_DAT_IN<127:0>	I	Data to multiplexer on transmit side.
TX_CLK8_IN<3:0>	I	Clocks to multiplexer on transmit side.
TX_ENB8_IN<3:0>	I	Data enables on transmit side.
TX1_VCOP	O	TX1_PLL output clock on transmit side (M/N clock) after phase select.
TX1_VCO	O	TX1_PLL output clock on transmit side (M/N clock) before phase select.
TX2_VCOP	O	TX2_PLL output clock on transmit side (x1 clock) after phase select.
TX2_VCO	O	TX2_PLL output clock on transmit side (x1 clock) before phase select.
TX2_FBCKI	I	PLL feedback input to TX2 PLL. This allows for the removal of the FPGA clock routing delay.
TX1_BYPASS	I	Set to 1 to bypass the TX1 PLL.
TX2_BYPASS	I	Set to 1 to bypass the TX2 PLL.
TX_LOCK	O	Lock signal for TX1_PLL and TX2_PLL. This signal is a logical OR of the lock signal from both PLLs. It is not integrated; thus, small glitches can occur on this signal during normal operation.
VSS_A<7:4>	—	Analog ground for the embedded line interface PLLs.
VDD33_A<7:4>	—	Analog power supply for the embedded line interface PLLs.
Miscellaneous Signals		
FPGA_RESET	I	A logic 1 resets all receive and transmit logic, including PLLs.

Package Pinouts

Table 18 provides the number of user-programmable I/Os available for each available package. Table 19 provides the package pin and pin function for the ORLI10G FPSC and packages. The bond pad name is identified in the PIO nomenclature used in the ispLEVER design editor. The bank column provides information as to which output voltage level bank the given pin is in. The group column provides information as to the group of pins the given pin is in. This is used to show which VREF pin is used to provide the reference voltage for single-ended limited-swing I/Os. If none of these buffer types (such as SSTL, GTL, HSTL) are used in a given group, then the VREF pin is available as an I/O pin.

When the number of FPGA bond pads exceeds the number of package pins, bond pads are unused. When the number of package pins exceeds the number of bond pads, package pins are left unconnected (no connects). When a package pin is to be left as a no connect for a specific die, it is indicated as a note in the device column for the FPGA. The tables provide no information on unused pads.

Table 18. ORCA Programmable I/Os Summary

Device	680 PBGAM
User programmable I/O	316
Available programmable differential pair pins	272
FPGA configuration pins	7
FPGA dedicated function pins	2
Core function pins	86
$V_{DD}15$	86
$V_{DD}33\_A$	4
$V_{DD}33$	28
$V_{DD}IO$	44
V_{SS}	95
V_{SS}_A	4
LVCTAP for dedicated differential channels	6
Core LV_REF pins	4
Total package pins	680

The built-in MicroProcessor Interface (MPI) cannot be fully utilized in the 680-pin PBGA package because the implementation of the XGMII interface limits the number of available address and data pins.

As shown in the Pair columns in Table 19, differential pairs and physical locations are numbered within each bank (e.g., L19C_A0 is the nineteenth pair in an associated bank). A C indicates complementary differential, whereas a T indicates true differential. An _A0 indicates the physical location of adjacent balls in either the horizontal or vertical direction. Other physical indicators are as follows:

- _A1 indicates one ball between pairs.
- _A2 indicates two balls between pairs.
- _D0 indicates balls are diagonally adjacent.
- _D1 indicates balls are diagonally adjacent separated by one physical ball.

VREF pins, shown in the Pin Description column in Table 19, are associated to the bank and group (e.g., VREF_TL_01 is the VREF for group one of the Top Left (TL) bank).

Pin Configuration

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
A1	—	—	VSS	VSS	—	—
E5	—	—	VDD33	VDD33	—	—
E4	—	—	O	PRD_DATA	RD_DATA/TDO	—
—	—	—	VDD15	VDD15	—	—
C1	—	—	I	PRESET_N	RESET_N	—
D1	—	—	I	PRD_CFG_N	RD_CFG_N	—
E2	—	—	I	PPRGRM_N	PRGRM_N	—
A2	0 (TL)	—	VDDIO0	VDDIO0	—	—
F4	0 (TL)	7	IO	PL2D	PLL_CK0C/HPPLL	L21C_A0
F3	0 (TL)	7	IO	PL2C	PLL_CK0T/HPPLL	L21T_A0
A3	0 (TL)	—	VDDIO0	VDDIO0	—	—
G5	0 (TL)	7	IO	PL3D	—	L22C_A0
F5	0 (TL)	7	IO	PL3C	VREF_0_07	L22T_A0
A18	—	—	VSS	VSS	—	—
G4	0 (TL)	7	IO	PL4D	D5	L23C_D1
F2	0 (TL)	7	IO	PL4C	D6	L23T_D1
B1	0 (TL)	—	VDDIO0	VDDIO0	—	—
H5	0 (TL)	8	IO	PL4B	—	L24C_D1
G3	0 (TL)	8	IO	PL4A	VREF_0_08	L24T_D1
F1	0 (TL)	8	IO	PL5D	HDC	L25C_A0
G2	0 (TL)	8	IO	PL5C	LDC_N	L25T_A0
A33	—	—	VSS	VSS	—	—
H4	0 (TL)	8	IO	PL5B	—	L26C_A0
J5	0 (TL)	8	IO	PL5A	—	L26T_A0
H3	0 (TL)	9	IO	PL6D	TESTCFG	L27C_D1
G1	0 (TL)	9	IO	PL6C	D7	L27T_D1
B3	0 (TL)	—	VDDIO0	VDDIO0	—	—
J4	0 (TL)	9	IO	PL7D	VREF_0_09	L28C_D1
H2	0 (TL)	9	IO	PL7C	A17/PPC_A31	L28T_D1
A34	—	—	VSS	VSS	—	—
K5	0 (TL)	9	IO	PL8D	CS0_N	L29C_D1
J3	0 (TL)	9	IO	PL8C	CS1	L29T_D1
C2	0 (TL)	—	VDDIO0	VDDIO0	—	—
H1	0 (TL)	10	IO	PL9D	—	L30C_A0
J2	0 (TL)	10	IO	PL9C	—	L30T_A0
B2	—	—	VSS	VSS	—	—
K4	0 (TL)	10	IO	PL9A	—	—
L5	0 (TL)	10	IO	PL10D	INIT_N	L31C_D1
K3	0 (TL)	10	IO	PL10C	DOUT	L31T_D1
—	—	—	VDD15	VDD15	—	—
J1	0 (TL)	10	IO	PL11D	VREF_0_10	L32C_A0
K2	0 (TL)	10	IO	PL11C	A16/PPC_A30	L32T_A0

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
B33	—	—	VSS	VSS	—	—
K1	0 (TL)	10	IO	PL11A	—	—
M5	7 (CL)	1	IO	PL12D	A15/PPC_A29	L1C_A0
L4	7 (CL)	1	IO	PL12C	A14/PPC_A28	L1T_A0
L1	7 (CL)	—	VDDIO7	VDDIO7	—	—
M4	7 (CL)	1	IO	PL12B	—	L2C_A0
N5	7 (CL)	1	IO	PL12A	—	L2T_A0
L3	7 (CL)	1	IO	PL13D	VREF_7_01	L3C_A0
L2	7 (CL)	1	IO	PL13C	D4	L3T_A0
B34	—	—	VSS	VSS	—	—
N4	7 (CL)	2	IO	PL13B	—	L4C_A0
P5	7 (CL)	2	IO	PL13A	—	L4T_A0
M2	7 (CL)	2	IO	PL14D	RDY/BUSY_N/RCLK	L5C_A0
M1	7 (CL)	2	IO	PL14C	VREF_7_02	L5T_A0
M3	7 (CL)	—	VDDIO7	VDDIO7	—	—
N3	7 (CL)	2	IO	PL15D	A13/PPC_A27	L6C_A0
N2	7 (CL)	2	IO	PL15C	A12/PPC_A26	L6T_A0
C3	—	—	VSS	VSS	—	—
P4	7 (CL)	3	IO	PL16D	—	L7C_A0
P3	7 (CL)	3	IO	PL16C	—	L7T_A0
R3	7 (CL)	—	VDDIO7	VDDIO7	—	—
R5	7 (CL)	3	IO	PL16A	—	—
N1	7 (CL)	3	IO	PL17D	A11/PPC_A25	L8C_A0
P2	7 (CL)	3	IO	PL17C	VREF_7_03	L8T_A0
C13	—	—	VSS	VSS	—	—
R4	7 (CL)	3	IO	PL17A	—	—
P1	7 (CL)	3	IO	PL18D	—	L9C_A0
R2	7 (CL)	3	IO	PL18C	—	L9T_A0
—	—	—	VDD15	VDD15	—	—
T2	7 (CL)	3	IO	PL18B	—	L10C_A0
R1	7 (CL)	3	IO	PL18A	—	L10T_A0
T5	7 (CL)	4	IO	PL19D	RD_N/MPI_STRB_N	L11C_A0
T4	7 (CL)	4	IO	PL19C	VREF_7_04	L11T_A0
C22	—	—	VSS	VSS	—	—
U5	7 (CL)	4	IO	PL19B	—	L12C_D1
T3	7 (CL)	4	IO	PL19A	—	L12T_D1
T1	7 (CL)	4	IO	PL20D	PLCK0C	L13C_D1
U3	7 (CL)	4	IO	PL20C	PLCK0T	L13T_D1
U1	7 (CL)	—	VDDIO7	VDDIO7	—	—
U4	7 (CL)	4	IO	PL20B	—	L14C_A1

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
U2	7 (CL)	4	IO	PL20A	—	L14T_A1
—	—	—	VDD15	VDD15	—	—
C32	—	—	VSS	VSS	—	—
V1	7 (CL)	5	IO	PL21D	A10/PPC_A24	L15C_A0
V2	7 (CL)	5	IO	PL21C	A9/PPC_A23	L15T_A0
D4	—	—	VSS	VSS	—	—
V3	7 (CL)	5	IO	PL21B	—	L16C_A0
V4	7 (CL)	5	IO	PL21A	—	L16T_A0
V5	7 (CL)	5	IO	PL22D	A8/PPC_A22	L17C_A0
W4	7 (CL)	5	IO	PL22C	VREF_7_05	L17T_A0
—	—	—	VDD15	VDD15	—	—
W3	7 (CL)	5	IO	PL23D	—	L18C_A0
W2	7 (CL)	5	IO	PL23C	—	L18T_A0
D30	—	—	VSS	VSS	—	—
Y1	7 (CL)	5	IO	PL23A	—	—
W5	7 (CL)	6	IO	PL24D	PLCK1C	L19C_A0
Y4	7 (CL)	6	IO	PL24C	PLCK1T	L19T_A0
W1	7 (CL)	—	VDDIO7	VDDIO7	—	—
Y2	7 (CL)	6	IO	PL24A	—	—
Y5	7 (CL)	6	IO	PL25D	VREF_7_06	L20C_D1
AA3	7 (CL)	6	IO	PL25C	A7/PPC_A21	L20T_D1
D31	—	—	VSS	VSS	—	—
AA2	7 (CL)	6	IO	PL25A	—	—
AA1	7 (CL)	6	IO	PL26D	A6/PPC_A20	L21C_A0
AB1	7 (CL)	6	IO	PL26C	A5/PPC_A19	L21T_A0
Y3	7 (CL)	—	VDDIO7	VDDIO7	—	—
AA4	7 (CL)	7	IO	PL26B	—	—
AB2	7 (CL)	7	IO	PL27D	WR_N/MPI_RW	L22C_A0
AB3	7 (CL)	7	IO	PL27C	VREF_7_07	L22T_A0
AA5	7 (CL)	7	IO	PL27B	—	L23C_A0
AB4	7 (CL)	7	IO	PL27A	—	L23T_A0
AC2	7 (CL)	8	IO	PL28D	A4/PPC_A18	L23C_A0
AC1	7 (CL)	8	IO	PL28C	VREF_7_08	L23T_A0
AC3	7 (CL)	—	VDDIO7	VDDIO7	—	—
AB5	7 (CL)	8	IO	PL29D	A3/PPC_A17	L23C_A0
AC4	7 (CL)	8	IO	PL29C	A2/PPC_A16	L23T_A0
D33	—	—	VSS	VSS	—	—
AD2	7 (CL)	8	IO	PL29A	—	—
AC5	7 (CL)	8	IO	PL30D	A1/PPC_A15	L24C_D1
AD3	7 (CL)	8	IO	PL30C	A0/PPC_A14	L24T_D1

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AE1	7 (CL)	8	IO	PL31D	DP0	L25C_A0
AE2	7 (CL)	8	IO	PL31C	DP1	L25T_A0
E34	—	—	VSS	VSS	—	—
AF1	7 (CL)	8	IO	PL31A	—	—
AD5	6 (BL)	1	IO	PL32D	D8	L1C_A0
AD4	6 (BL)	1	IO	PL32C	VREF_6_01	L1T_A0
AK4	6 (BL)	—	VDDIO6	VDDIO6	—	—
AE3	6 (BL)	1	IO	PL32A	—	—
AE5	6 (BL)	1	IO	PL33D	D9	L2C_A0
AE4	6 (BL)	1	IO	PL33C	D10	L2T_A0
F33	—	—	VSS	VSS	—	—
AF2	6 (BL)	2	IO	PL34D	—	L3C_A0
AG1	6 (BL)	2	IO	PL34C	VREF_6_02	L3T_A0
AK5	6 (BL)	—	VDDIO6	VDDIO6	—	—
AF3	6 (BL)	2	IO	PL34B	—	L4C_A1
AF5	6 (BL)	2	IO	PL34A	—	L4T_A1
H34	—	—	VSS	VSS	—	—
AG2	6 (BL)	3	IO	PL35B	D11	L5C_D1
AF4	6 (BL)	3	IO	PL35A	D12	L5T_D1
AH1	6 (BL)	3	IO	PL36D	—	L6C_D1
AG3	6 (BL)	3	IO	PL36C	—	L6T_D1
AL1	6 (BL)	—	VDDIO6	VDDIO6	—	—
AH2	6 (BL)	3	IO	PL36B	VREF_6_03	L7C_A0
AJ1	6 (BL)	3	IO	PL36A	D13	L7T_A0
AG4	6 (BL)	4	IO	PL37D	—	—
J33	—	—	VSS	VSS	—	—
AH3	6 (BL)	4	IO	PL37B	—	L8C_D1
AG5	6 (BL)	4	IO	PL37A	VREF_6_04	L8T_D1
AJ2	6 (BL)	4	IO	PL38C	—	—
AL3	6 (BL)	—	VDDIO6	VDDIO6	—	—
AK1	6 (BL)	4	IO	PL38B	—	—
AH4	6 (BL)	4	IO	PL38A	—	—
AJ3	6 (BL)	4	IO	PL39D	PLL_CK7C/HPPLL	L9C_A0
AK2	6 (BL)	4	IO	PL39C	PLL_CK7T/HPPLL	L9T_A0
L34	—	—	VSS	VSS	—	—
AH5	6 (BL)	4	IO	PL39B	—	L10C_A0
AJ4	6 (BL)	4	IO	PL39A	—	L10T_A0
N13	—	—	VSS	VSS	—	—
AK3	—	—	I	PTEMP	PTEMP	—
AM1	6 (BL)	—	VDDIO6	VDDIO6	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
—	—	—	VDD15	VDD15	—	—
AN1	—	—	IO	LVDS_R	LVDS_R	—
AJ5	—	—	VDD33	VDD33	—	—
N14	—	—	VSS	VSS	—	—
AL5	—	—	VDD33	VDD33	—	—
—	—	—	VDD15	VDD15	—	—
AM5	6 (BL)	5	IO	PB2A	DP2	L11T_A0
AN4	6 (BL)	5	IO	PB2B	—	L11C_A0
AM2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AK6	6 (BL)	5	IO	PB2C	PLL_CK6T/PPLL	L12T_A0
AL6	6 (BL)	5	IO	PB2D	PLL_CK6C/PPLL	L12C_A0
AK7	6 (BL)	5	IO	PB3A	—	—
N15	—	—	VSS	VSS	—	—
AN5	6 (BL)	5	IO	PB3C	—	L13T_A0
AM6	6 (BL)	5	IO	PB3D	—	L13C_A0
AN6	6 (BL)	5	IO	PB4A	VREF_6_05	L14T_A0
AP5	6 (BL)	5	IO	PB4B	DP3	L14C_A0
AM4	6 (BL)	—	VDDIO6	VDDIO6	—	—
AL7	6 (BL)	6	IO	PB4C	—	L15T_A0
AM7	6 (BL)	6	IO	PB4D	—	L15C_A0
N20	—	—	VSS	VSS	—	—
AN7	6 (BL)	6	IO	PB5C	VREF_6_06	L16T_A0
AP6	6 (BL)	6	IO	PB5D	D14	L16C_A0
AK8	6 (BL)	6	IO	PB6A	—	L17T_A0
AL8	6 (BL)	6	IO	PB6B	—	L17C_A0
AN3	6 (BL)	—	VDDIO6	VDDIO6	—	—
AM8	6 (BL)	7	IO	PB6C	D15	L18T_D1
AK9	6 (BL)	7	IO	PB6D	D16	L18C_D1
AP7	6 (BL)	7	IO	PB7A	—	—
N21	—	—	VSS	VSS	—	—
AL9	6 (BL)	7	IO	PB7C	D17	L19T_A0
AK10	6 (BL)	7	IO	PB7D	D18	L19C_A0
AN8	6 (BL)	7	IO	PB8A	—	—
AP2	6 (BL)	—	VDDIO6	VDDIO6	—	—
AM9	6 (BL)	7	IO	PB8C	VREF_6_07	L20T_A0
AL10	6 (BL)	7	IO	PB8D	D19	L20C_A0
AP8	6 (BL)	8	IO	PB9A	—	—
N22	—	—	VSS	VSS	—	—
AL11	6 (BL)	8	IO	PB9C	D20	L21T_A0
AK11	6 (BL)	8	IO	PB9D	D21	L21C_A0

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AM10	6 (BL)	8	IO	PB10A	—	—
—	—	—	VDD15	VDD15	—	—
AN9	6 (BL)	8	IO	PB10C	VREF_6_08	L22T_A0
AP9	6 (BL)	8	IO	PB10D	D22	L22C_A0
AM11	6 (BL)	9	IO	PB11A	—	L23T_D1
AK12	6 (BL)	9	IO	PB11B	—	L23C_D1
P13	—	—	VSS	VSS	—	—
AN10	6 (BL)	9	IO	PB11C	D23	L24T_A0
AP10	6 (BL)	9	IO	PB11D	D24	L24C_A0
AL12	6 (BL)	9	IO	PB12A	—	L25T_A0
AK13	6 (BL)	9	IO	PB12B	—	L25C_A0
AP3	6 (BL)	—	VDDIO6	VDDIO6	—	—
AN11	6 (BL)	9	IO	PB12C	VREF_6_09	L26T_A0
AN12	6 (BL)	9	IO	PB12D	D25	L26C_A0
AK14	6 (BL)	9	IO	PB13A	—	L27T_A0
AL13	6 (BL)	9	IO	PB13B	—	L27C_A0
P14	—	—	VSS	VSS	—	—
AP12	6 (BL)	10	IO	PB13C	D26	L28T_A0
AN13	6 (BL)	10	IO	PB13D	D27	L28C_A0
AL14	6 (BL)	10	IO	PB14A	—	L29T_A0
AK15	6 (BL)	10	IO	PB14B	—	L29C_A0
—	6 (BL)	—	VDDIO6	VDDIO6	—	—
AP13	6 (BL)	10	IO	PB14C	VREF_6_10	L30T_A0
AP14	6 (BL)	10	IO	PB14D	D28	L30C_A0
AN14	6 (BL)	11	IO	PB15A	—	—
P15	—	—	VSS	VSS	—	—
AM14	6 (BL)	11	IO	PB15C	D29	L31T_A0
AL15	6 (BL)	11	IO	PB15D	D30	L31C_A0
AN15	6 (BL)	11	IO	PB16A	—	—
AM16	6 (BL)	11	IO	PB16C	VREF_6_11	L32T_A0
AL16	6 (BL)	11	IO	PB16D	D31	L32C_A0
AP15	5 (BC)	1	IO	PB17A	—	—
P20	—	—	VSS	VSS	—	—
AN16	5 (BC)	1	IO	PB17C	—	L1T_A0
AP16	5 (BC)	1	IO	PB17D	—	L1C_A0
AK16	5 (BC)	1	IO	PB18A	—	—
—	—	—	VDD15	VDD15	—	—
AL17	5 (BC)	1	IO	PB18C	VREF_5_01	L2T_A0
AK17	5 (BC)	1	IO	PB18D	—	L2C_A0
—	—	—	VDD15	VDD15	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
P21	—	—	VSS	VSS	—	—
AM17	5 (BC)	2	IO	PB19A	—	L3T_A0
AN17	5 (BC)	2	IO	PB19B	—	L3C_A0
P22	—	—	VSS	VSS	—	—
AP18	5 (BC)	2	IO	PB19C	PBCK0T	L4T_A1
AM18	5 (BC)	2	IO	PB19D	PBCK0C	L4C_A1
AN18	5 (BC)	2	IO	PB20A	—	L5T_A1
AL18	5 (BC)	2	IO	PB20B	—	L5C_A1
AM12	5 (BC)	—	VDDIO5	VDDIO5	—	—
AN19	5 (BC)	2	IO	PB20C	VREF_5_02	L6T_D2
AK18	5 (BC)	2	IO	PB20D	—	L6C_2
AM19	5 (BC)	2	IO	PB21A	—	L7T_D1
AP20	5 (BC)	2	IO	PB21B	—	L7C_D1
—	—	—	VDD15	VDD15	—	—
AL19	5 (BC)	3	IO	PB21C	—	L8T_D1
AN20	5 (BC)	3	IO	PB21D	VREF_5_03	L8C_D1
AP21	5 (BC)	3	IO	PB22A	—	—
P34	—	—	VSS	VSS	—	—
AL20	5 (BC)	3	IO	PB22C	—	L9T_A0
AK19	5 (BC)	3	IO	PB22D	—	L9C_A0
AN21	5 (BC)	3	IO	PB23A	—	—
AM15	5 (BC)	—	VDDIO5	VDDIO5	—	—
AK20	5 (BC)	3	IO	PB23C	PBCK1T	L10T_D1
AM21	5 (BC)	3	IO	PB23D	PBCK1C	L10C_D1
AP22	5 (BC)	3	IO	PB24A	—	—
R13	—	—	VSS	VSS	—	—
AL21	5 (BC)	4	IO	PB24C	—	L11T_D1
AN22	5 (BC)	4	IO	PB24D	—	L11C_D1
AP23	5 (BC)	4	IO	PB25A	—	—
AM20	5 (BC)	—	VDDIO5	VDDIO5	—	—
AN23	5 (BC)	4	IO	PB25C	—	L12T_A0
AN24	5 (BC)	4	IO	PB25D	VREF_5_04	L12C_A0
AK21	5 (BC)	4	IO	PB26A	—	L13T_A0
AL22	5 (BC)	4	IO	PB26B	—	L13C_A0
R14	—	—	VSS	VSS	—	—
AP25	5 (BC)	5	IO	PB26C	—	L14T_D1
AM24	5 (BC)	5	IO	PB26D	VREF_5_05	L14C_D1
AK22	5 (BC)	5	IO	PB27A	—	L15T_A0
AL23	5 (BC)	5	IO	PB27B	—	L15C_A0
AM23	5 (BC)	—	VDDIO5	VDDIO5	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AN25	5 (BC)	5	IO	PB27C	—	L16T_D1
AL24	5 (BC)	5	IO	PB27D	—	L16T_D1
AP26	5 (BC)	6	IO	PB28A	—	—
R15	—	—	VSS	VSS	—	—
AM25	5 (BC)	6	IO	PB28C	—	L17T_D1
AK23	5 (BC)	6	IO	PB28D	VREF_5_06	L17C_D1
AN26	5 (BC)	6	IO	PB29A	—	—
AL25	5 (BC)	6	IO	PB29C	—	L18T_A0
AK24	5 (BC)	6	IO	PB29D	—	L18C_A0
AP27	5 (BC)	7	IO	PB30A	—	—
R20	—	—	VSS	VSS	—	—
AM26	5 (BC)	7	IO	PB30C	—	L19T_A0
AN27	5 (BC)	7	IO	PB30D	—	L19C_A0
AP11	5 (BC)	—	VDDIO5	VDDIO5	—	—
AP28	5 (BC)	7	IO	PB31C	VREF_5_07	L20T_D1
AM27	5 (BC)	7	IO	PB31D	—	L20C_D1
R21	—	—	VSS	VSS	—	—
AL26	5 (BC)	7	IO	PB32C	—	L21T_A0
AK25	5 (BC)	7	IO	PB32D	—	L21C_A0
AP17	5 (BC)	—	VDDIO5	VDDIO5	—	—
AN28	5 (BC)	8	IO	PB33C	—	L22T_A0
AP29	5 (BC)	8	IO	PB33D	VREF_5_08	L22C_A0
R22	—	—	VSS	VSS	—	—
AP19	5 (BC)	—	VDDIO5	VDDIO5	—	—
T16	—	—	VSS	VSS	—	—
T17	—	—	VSS	VSS	—	—
A31	—	—	VDD15	VDD15	—	—
AL27	—	—	I	RX_DAT_IN_10_P/RX_DAT_IN_0_P	—	L1_A0
AM28	—	—	I	RX_DAT_IN_10_N/RX_DAT_IN_0_N	—	L1_A0
C30	—	—	VDD15	VDD15	—	—
AN29	—	—	I	RX_DAT_IN_11_P/RX_DAT_IN_1_P	—	L2_A0
AP30	—	—	I	RX_DAT_IN_11_N/RX_DAT_IN_1_N	—	L2_A0
—	—	—	VDD33	VDD33	—	—
AL28	—	—	I	RX_DAT_IN_12_P/RX_DAT_IN_2_P	—	L3_A0
AM29	—	—	I	RX_DAT_IN_12_N/RX_DAT_IN_2_N	—	L3_A0
Y34	—	—	VSS	VSS	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AN30	—	—	VDD33	VDD33	—	—
AK27	—	—	I	RX_DAT_IN_13_P/RX_DAT_IN_3_P	—	L4_A0
AK28	—	—	I	RX_DAT_IN_13_N/RX_DAT_IN_3_N	—	L4_A0
AL29	—	—	I	RX_CLK_IN_0_P	—	L5_A0
AM30	—	—	I	RX_CLK_IN_0_N	—	L5_A0
AN31	—	—	I	LVCTAP_1	—	—
AP32	—	—	VSSA_4	VSSA_4	—	—
AK30	—	—	VDD33A_4	VDD33A_4	—	—
AA13	—	—	VSS	VSS	—	—
AA14	—	—	VSS	VSS	—	—
C33	—	—	VDD15	VDD15	—	—
AK31	—	—	VDD33A_5	VDD33A_5	—	—
AJ30	—	—	VDD33	VDD33	—	—
AK32	—	—	VSSA_5	VSSA_5	—	—
AJ31	—	—	I	LVCTAP_2	—	—
AA15	—	—	VSS	VSS	—	—
AH30	—	—	VDD33	VDD33	—	—
C34	—	—	VDD15	VDD15	—	—
AK33	—	—	I	RX_DAT_IN_20_P/RX_DAT_IN_4_P	—	L6_A0
AJ32	—	—	I	RX_DAT_IN_20_N/RX_DAT_IN_4_N	—	L6_A0
AH31	—	—	I	RX_DAT_IN_21_P/RX_DAT_IN_5_P	—	L7_A0
AG30	—	—	I	RX_DAT_IN_21_N/RX_DAT_IN_5_N	—	L7_A0
AA20	—	—	VSS	VSS	—	—
AF30	—	—	I	RX_DAT_IN_22_P/RX_DAT_IN_6_P	—	L8_A0
AG31	—	—	I	RX_DAT_IN_22_N/RX_DAT_IN_6_N	—	L8_A0
AK34	—	—	I	RX_DAT_IN_23_P/RX_DAT_IN_7_P	—	L9_A0
AJ33	—	—	I	RX_DAT_IN_23_N/RX_DAT_IN_7_N	—	L9_A0
D28	—	—	VDD15	VDD15	—	—
AA21	—	—	VSS	VSS	—	—
AH32	—	—	VDD33	VDD33	—	—
AE30	—	—	I	LVCTAP_3	—	—
AA22	—	—	VSS	VSS	—	—
D32	—	—	VDD15	VDD15	—	—
AG32	—	—	I	RX_CLK_IN_1_P	—	L10_A0

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AF31	—	—	I	RX_CLK_IN_1_N	—	L10_A0
AF32	—	—	VDD33	VDD33	—	—
AB13	—	—	VSS	VSS	—	—
AC30	—	—	I	RX_DAT_IN_30_P/RX_DAT_IN_8_P	—	L11_A0
AD30	—	—	I	RX_DAT_IN_30_N/RX_DAT_IN_8_N	—	L11_A0
D34	—	—	VDD15	VDD15	—	—
AE31	—	—	I	RX_DAT_IN_31_P/RX_DAT_IN_9_P	—	L12_A0
AE32	—	—	I	RX_DAT_IN_31_N/RX_DAT_IN_9_N	—	L12_A0
AB14	—	—	VSS	VSS	—	—
AF33	—	—	VDD33	VDD33	—	—
AD31	—	—	I	RX_DAT_IN_32_P/RX_DAT_IN_10_P	—	L13_A0
AD32	—	—	I	RX_DAT_IN_32_N/RX_DAT_IN_10_N	—	L13_A0
F34	—	—	VDD15	VDD15	—	—
AB30	—	—	I	LVCTAP_4	—	—
AC31	—	—	I	RX_DAT_IN_33_P/RX_DAT_IN_11_P	—	L14_A0
AC32	—	—	I	RX_DAT_IN_33_N/RX_DAT_IN_11_N	—	L14_A0
AC33	—	—	VDD33	VDD33	—	—
AB15	—	—	VSS	VSS	—	—
AB31	—	—	I	RX_CLK_IN_2_P	—	L15_A0
AB32	—	—	I	RX_CLK_IN_2_N	—	L15_A0
AA30	—	—	I	LVCTAP_5	—	—
G33	—	—	VDD15	VDD15	—	—
AB33	—	—	VDD33	VDD33	—	—
AB20	—	—	VSS	VSS	—	—
AA31	—	—	I	RX_CLK_IN_3_P	—	L16_A0
Y30	—	—	I	RX_CLK_IN_3_N	—	L16_A0
AA32	—	—	I	RX_DAT_IN_40_P/RX_DAT_IN_12_P	—	L17_A0
AA33	—	—	I	RX_DAT_IN_40_N/RX_DAT_IN_12_N	—	L17_A0
AB21	—	—	VSS	VSS	—	—
G34	—	—	VDD15	VDD15	—	—
Y31	—	—	I	RX_DAT_IN_41_P/RX_DAT_IN_13_P	—	L18_A0
Y32	—	—	I	RX_DAT_IN_41_N/RX_DAT_IN_13_N	—	L18_A0

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
W30	—	—	VDD33	VDD33	—	—
AB22	—	—	VSS	VSS	—	—
Y33	—	—	VDD33	VDD33	—	—
J34	—	—	VDD15	VDD15	—	—
W31	—	—	I	RX_DAT_IN_42_P/RX_DAT_IN_14_P	—	L19_A0
W32	—	—	I	RX_DAT_IN_42_N/RX_DAT_IN_14_N	—	L19_A0
AC34	—	—	VSS	VSS	—	—
K33	—	—	VDD15	VDD15	—	—
V30	—	—	I	RX_DAT_IN_43_P/RX_DAT_IN_15_P	—	L20_A0
V31	—	—	I	RX_DAT_IN_43_N/RX_DAT_IN_15_N	—	L20_A0
W33	—	—	VDD33	VDD33	—	—
AE33	—	—	VSS	VSS	—	—
V32	—	—	I	LV_REF10	—	—
V33	—	—	I	LV_REF14	—	—
U33	—	—	I	LV_RESHI	—	—
U31	—	—	I	LV_RESLO	—	—
AF34	—	—	VSS	VSS	—	—
U30	—	—	VDD33	VDD33	—	—
K34	—	—	VDD15	VDD15	—	—
U32	—	—	O	TX_CLK_OUT_0_P	—	L21_A0
T33	—	—	O	TX_CLK_OUT_0_N	—	L21_A0
AH33	—	—	VSS	VSS	—	—
T32	—	—	VDD33	VDD33	—	—
T31	—	—	O	TX_DAT_OUT_10_P/TX_DAT_OUT_0_P	—	L22_A0
T30	—	—	O	TX_DAT_OUT_10_N/TX_DAT_OUT_0_N	—	L22_A0
AJ34	—	—	VSS	VSS	—	—
R33	—	—	O	TX_DAT_OUT_11_P/TX_DAT_OUT_1_P	—	L23_A0
R32	—	—	O	TX_DAT_OUT_11_N/TX_DAT_OUT_1_N	—	L23_A0
M34	—	—	VDD15	VDD15	—	—
R31	—	—	O	TX_DAT_OUT_12_P/TX_DAT_OUT_2_P	—	L24_A0
R30	—	—	O	TX_DAT_OUT_12_N/TX_DAT_OUT_2_N	—	L24_A0
AL2	—	—	VSS	VSS	—	—
—	—	—	VDD33	VDD33	—	—
P33	—	—	VDD33	VDD33	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
N33	—	—	O	TX_DAT_OUT_13_P/TX_DAT_OUT_3_P	—	L25_A0
P32	—	—	O	TX_DAT_OUT_13_N/TX_DAT_OUT_3_N	—	L25_A0
P30	—	—	O	TX_CLK_OUT_1_P	—	L26_A0
P31	—	—	O	TX_CLK_OUT_1_N	—	L26_A0
AL4	—	—	VSS	VSS	—	—
N32	—	—	O	TX_DAT_OUT_20_P/TX_DAT_OUT_4_P	—	L27_A0
N31	—	—	O	TX_DAT_OUT_20_N/TX_DAT_OUT_4_N	—	L27_A0
N16	—	—	VDD15	VDD15	—	—
N30	—	—	VDD33	VDD33	—	—
M33	—	—	O	TX_DAT_OUT_21_P/TX_DAT_OUT_5_P	—	L28_A0
M32	—	—	O	TX_DAT_OUT_21_N/TX_DAT_OUT_5_N	—	L28_A0
AL30	—	—	VSS	VSS	—	—
M31	—	—	O	TX_DAT_OUT_22_P/TX_DAT_OUT_6_P	—	L29_A0
M30	—	—	O	TX_DAT_OUT_22_N/TX_DAT_OUT_6_N	—	L29_A0
L33	—	—	VDD33	VDD33	—	—
N17	—	—	VDD15	VDD15	—	—
L32	—	—	O	TX_DAT_OUT_23_P/TX_DAT_OUT_7_P	—	L30_A0
K32	—	—	O	TX_DAT_OUT_23_N/TX_DAT_OUT_7_N	—	L30_A0
AL31	—	—	VSS	VSS	—	—
L30	—	—	O	TX_CLK_OUT_2_P	—	L31_A0
L31	—	—	O	TX_CLK_OUT_2_N	—	L31_A0
N18	—	—	VDD15	VDD15	—	—
J31	—	—	O	TX_DAT_OUT_30_P/TX_DAT_OUT_8_P	—	L32_A0
K31	—	—	O	TX_DAT_OUT_30_N/TX_DAT_OUT_8_N	—	L32_A0
K30	—	—	VDD33	VDD33	—	—
AM3	—	—	VSS	VSS	—	—
H33	—	—	O	TX_DAT_OUT_31_P/TX_DAT_OUT_9_P	—	L33_A0
J32	—	—	O	TX_DAT_OUT_31_N/TX_DAT_OUT_9_N	—	L33_A0
H32	—	—	VDD33	VDD33	—	—
H31	—	—	I	TX_CLK_IN_P	—	L34_A0
J30	—	—	I	TX_CLK_IN_N	—	L34_A0
N19	—	—	VDD15	VDD15	—	—
G32	—	—	I	LVCTAP_6	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AM13	—	—	VSS	VSS	—	—
G31	—	—	O	TX_DAT_OUT_32_P/TX_DAT_OUT_10_P	—	L35_A0
F32	—	—	O	TX_DAT_OUT_32_N/TX_DAT_OUT_10_N	—	L35_A0
N34	—	—	VDD15	VDD15	—	—
H30	—	—	VDD33	VDD33	—	—
E33	—	—	O	TX_DAT_OUT_33_P/TX_DAT_OUT_11_P	—	L36_A0
E32	—	—	O	TX_DAT_OUT_33_N/TX_DAT_OUT_11_N	—	L36_A0
AM22	—	—	VSS	VSS	—	—
F31	—	—	O	TX_CLK_OUT_3_P	—	L37_A0
E31	—	—	O	TX_CLK_OUT_3_N	—	L37_A0
G30	—	—	VDD33	VDD33	—	—
P16	—	—	VDD15	VDD15	—	—
F30	—	—	VDD33	VDD33	—	—
E30	—	—	VSSA_6	VSSA_6	—	—
B32	—	—	VDD33	VDD33	—	—
C31	—	—	VDD33A_6	VDD33A_6	—	—
AM32	—	—	VSS	VSS	—	—
AN2	—	—	VSS	VSS	—	—
E29	—	—	VDD33A_7	VDD33A_7	—	—
E28	—	—	VSSA_7	VSSA_7	—	—
A32	—	—	O	TX_DAT_OUT_40_N/TX_DAT_OUT_12_N	—	L38_A0
B31	—	—	O	TX_DAT_OUT_40_P/TX_DAT_OUT_12_P	—	L38_A0
E27	—	—	O	TX_DAT_OUT_41_N/TX_DAT_OUT_13_N	—	L39_A0
E26	—	—	O	TX_DAT_OUT_41_P/TX_DAT_OUT_13_P	—	L39_A0
B30	—	—	VDD33	VDD33	—	—
P17	—	—	VDD15	VDD15	—	—
D29	—	—	O	TX_DAT_OUT_42_N/TX_DAT_OUT_14_N	—	L40_A0
C29	—	—	O	TX_DAT_OUT_42_P/TX_DAT_OUT_14_P	—	L40_A0
AN33	—	—	VSS	VSS	—	—
C28	—	—	O	TX_DAT_OUT_43_N/TX_DAT_OUT_15_N	—	L41_A0
D27	—	—	O	TX_DAT_OUT_43_P/TX_DAT_OUT_15_P	—	L41_A0
A30	—	—	I	PWRDN	—	—
E25	—	—	I	RESET_RX	—	—
B29	—	—	I	RESET_TX	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
A29	—	—	I	PLL_BYPASS	—	—
T18	—	—	VSS	VSS	—	—
T19	—	—	VSS	VSS	—	—
A11	1 (TC)	—	VDDIO1	VDDIO1	—	—
U16	—	—	VSS	VSS	—	—
A17	1 (TC)	—	VDDIO1	VDDIO1	—	—
C27	1 (TC)	9	IO	PT32D	—	—
D26	1 (TC)	9	IO	PT32C	—	—
U17	—	—	VSS	VSS	—	—
B28	1 (TC)	10	IO	PT31D	—	L1C_A0
A28	1 (TC)	10	IO	PT31C	VREF_1_10	L1T_A0
A19	1 (TC)	—	VDDIO1	VDDIO1	—	—
B27	1 (TC)	10	IO	PT30D	—	—
U18	—	—	VSS	VSS	—	—
C26	1 (TC)	10	IO	PT30A	—	—
B26	1 (TC)	10	IO	PT29D	—	L2C_A0
A27	1 (TC)	10	IO	PT29C	—	L2T_A0
—	—	—	VDD15	VDD15	—	—
E24	1 (TC)	10	IO	PT29B	—	L3C_A0
D25	1 (TC)	10	IO	PT29A	—	L3T_A0
D24	1 (TC)	1	IO	PT28D	—	L4C_A0
C25	1 (TC)	1	IO	PT28C	—	L4T_A0
U19	—	—	VSS	VSS	—	—
B25	1 (TC)	1	IO	PT28B	—	L5C_A0
A26	1 (TC)	1	IO	PT28A	—	L5T_A0
E23	1 (TC)	1	IO	PT27D	VREF_1_01	L6C_A0
D23	1 (TC)	1	IO	PT27C	—	L6T_A0
A24	1 (TC)	—	VDDIO1	VDDIO1	—	—
C24	1 (TC)	1	IO	PT27B	—	L7C_D1
A25	1 (TC)	1	IO	PT27A	—	L7T_D1
E22	1 (TC)	2	IO	PT26D	—	L8C_A0
E21	1 (TC)	2	IO	PT26C	VREF_1_02	L8T_A0
U34	—	—	VSS	VSS	—	—
B24	1 (TC)	2	IO	PT26B	—	L9C_D1
D22	1 (TC)	2	IO	PT26A	—	L9T_D1
B23	1 (TC)	2	IO	PT25D	—	L10C_A0
A23	1 (TC)	2	IO	PT25C	—	L10T_A0
C12	1 (TC)	—	VDDIO1	VDDIO1	—	—
D21	1 (TC)	3	IO	PT24D	—	L11C_D1
B22	1 (TC)	3	IO	PT24C	VREF_1_03	L11T_D1

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
V16	—	—	VSS	VSS	—	—
A22	1 (TC)	3	IO	PT24A	—	—
D20	1 (TC)	3	IO	PT23D	—	L12C_A0
E20	1 (TC)	3	IO	PT23C	—	L12T_A0
C15	1 (TC)	—	VDDIO1	VDDIO1	—	—
C21	1 (TC)	3	IO	PT23A	—	—
B21	1 (TC)	3	IO	PT22D	—	L13C_A0
A21	1 (TC)	3	IO	PT22C	—	L13T_A0
V17	—	—	VSS	VSS	—	—
B20	1 (TC)	3	IO	PT22A	—	—
C19	1 (TC)	4	IO	PT21D	—	L14C_D1
A20	1 (TC)	4	IO	PT21C	—	L14T_D1
—	—	—	VDD15	VDD15	—	—
D19	1 (TC)	4	IO	PT20D	—	L15C_A0
E19	1 (TC)	4	IO	PT20C	—	L15T_A0
V18	—	—	VSS	VSS	—	—
B19	1 (TC)	4	IO	PT19D	—	L16C_A0
B18	1 (TC)	4	IO	PT19C	VREF_1_04	L16T_A0
C20	1 (TC)	—	VDDIO1	VDDIO1	—	—
D18	1 (TC)	4	IO	PT19B	—	L17C_A0
E18	1 (TC)	4	IO	PT19A	—	L17T_A0
V19	—	—	VSS	VSS	—	—
—	—	—	VDD15	VDD15	—	—
B17	1 (TC)	5	IO	PT18D	PTCK1C	L18C_A0
C17	1 (TC)	5	IO	PT18C	PTCK1T	L18T_A0
W16	—	—	VSS	VSS	—	—
D17	1 (TC)	5	IO	PT18B	—	L19C_A0
C18	1 (TC)	5	IO	PT18A	—	L19T_A0
A16	1 (TC)	5	IO	PT17D	PTCK0C	L20C_A0
B16	1 (TC)	5	IO	PT17C	PTCK0T	L20T_A0
E17	1 (TC)	5	IO	PT17A	—	—
C16	1 (TC)	5	IO	PT16D	VREF_1_05	L21C_A0
D16	1 (TC)	5	IO	PT16C	—	L21T_A0
W17	—	—	VSS	VSS	—	—
A15	1 (TC)	5	IO	PT16A	—	—
B15	1 (TC)	6	IO	PT15D	—	L22C_A1
D15	1 (TC)	6	IO	PT15C	—	L22T_A1
C23	1 (TC)	—	VDDIO1	VDDIO1	—	—
A14	1 (TC)	6	IO	PT15A	—	—
E16	1 (TC)	6	IO	PT14D	—	L23C_D1

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
C14	1 (TC)	6	IO	PT14C	VREF_1_06	L23T_D1
W18	—	—	VSS	VSS	—	—
B14	1 (TC)	6	IO	PT14A	—	—
E15	0 (TL)	1	IO	PT13D	MPI_RTRY_N	L1C_A0
D14	0 (TL)	1	IO	PT13C	MPI_ACK_N	L1T_A0
C4	0 (TL)	—	VDDIO0	VDDIO0	—	—
A13	0 (TL)	1	IO	PT13B	—	L2C_A0
B13	0 (TL)	1	IO	PT13A	VREF_0_01	L2T_A0
A12	0 (TL)	1	IO	PT12D	M0	L3C_A0
B12	0 (TL)	1	IO	PT12C	M1	L3T_A0
W19	—	—	VSS	VSS	—	—
D13	0 (TL)	2	IO	PT12B	MPI_CLK	L4C_A0
E14	0 (TL)	2	IO	PT12A	A21/MPI_BURST_N	L4T_A0
B11	0 (TL)	2	IO	PT11D	M2	L5C_A0
A10	0 (TL)	2	IO	PT11C	M3	L5T_A0
D2	0 (TL)	—	VDDIO0	VDDIO0	—	—
E13	0 (TL)	2	IO	PT11B	VREF_0_02	L6C_A0
D12	0 (TL)	2	IO	PT11A	MPI_TEA_N	L6T_A0
C11	0 (TL)	3	IO	PT10D	—	L7C_A0
B10	0 (TL)	3	IO	PT10C	—	L7T_A0
—	—	—	VDD15	VDD15	—	—
A9	0 (TL)	3	IO	PT10A	—	—
D11	0 (TL)	3	IO	PT9D	VREF_0_03	L8C_D1
B9	0 (TL)	3	IO	PT9C	—	L8T_D1
Y13	—	—	VSS	VSS	—	—
A8	0 (TL)	3	IO	PT9A	—	—
E12	0 (TL)	3	IO	PT8D	D0	L9C_D1
C10	0 (TL)	3	IO	PT8C	TMS	L9T_D1
D3	0 (TL)	—	VDDIO0	VDDIO0	—	—
D10	0 (TL)	4	IO	PT7D	A20/MPI_BDIP_N	L10C_A0
C9	0 (TL)	4	IO	PT7C	A19/MPI_TSZ1	L10T_A0
Y14	—	—	VSS	VSS	—	—
E11	0 (TL)	4	IO	PT6D	A18/MPI_TSZ0	L11C_D1
D9	0 (TL)	4	IO	PT6C	D3	L11T_D1
E1	0 (TL)	—	VDDIO0	VDDIO0	—	—
A7	0 (TL)	4	IO	PT6B	VREF_0_04	L12C_A0
B8	0 (TL)	4	IO	PT6A	—	L12T_A0
E10	0 (TL)	5	IO	PT5D	D1	L13C_D1
C8	0 (TL)	5	IO	PT5C	D2	L13T_D1
Y15	—	—	VSS	VSS	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
B7	0 (TL)	5	IO	PT5B	—	L14C_A0
A6	0 (TL)	5	IO	PT5A	VREF_0_05	L14T_A0
D8	0 (TL)	5	IO	PT4D	TDI	L15C_D1
B6	0 (TL)	5	IO	PT4C	TCK	L15T_D1
E3	0 (TL)	—	VDDIO0	VDDIO0	—	—
C7	0 (TL)	5	IO	PT4B	—	L16C_D1
A5	0 (TL)	5	IO	PT4A	—	L16T_D1
C6	0 (TL)	6	IO	PT3D	—	L17C_A0
B5	0 (TL)	6	IO	PT3C	VREF_0_06	L17T_A0
Y20	—	—	VSS	VSS	—	—
E9	0 (TL)	6	IO	PT3B	—	L18C_D1
D7	0 (TL)	6	IO	PT3A	—	L18T_D1
C5	0 (TL)	6	IO	PT2D	PLL_CK1C/PPLL	L19C_A0
D6	0 (TL)	6	IO	PT2C	PLL_CK1T/PPLL	L19T_A0
E8	0 (TL)	6	IO	PT2B	—	L20C_A0
E7	0 (TL)	6	IO	PT2A	—	L20T_A0
A4	—	—	O	PCFG_MPI_IRQ	CFG_IRQ_N/MPI_IRQ_N	—
B4	—	—	IO	PCCLK	CCLK	—
—	—	—	VDD15	VDD15	—	—
E6	—	—	IO	PDONE	DONE	—
D5	—	—	VDD33	VDD33	—	—
Y21	—	—	VSS	VSS	—	—
AK26	—	—	VDD33	VDD33	—	—
P18	—	—	VDD15	VDD15	—	—
—	—	—	VDD15	VDD15	—	—
P19	—	—	VDD15	VDD15	—	—
R16	—	—	VDD15	VDD15	—	—
R17	—	—	VDD15	VDD15	—	—
R18	—	—	VDD15	VDD15	—	—
R19	—	—	VDD15	VDD15	—	—
R34	—	—	VDD15	VDD15	—	—
T13	—	—	VDD15	VDD15	—	—
T14	—	—	VDD15	VDD15	—	—
T15	—	—	VDD15	VDD15	—	—
T20	—	—	VDD15	VDD15	—	—
T21	—	—	VDD15	VDD15	—	—
T22	—	—	VDD15	VDD15	—	—
T34	—	—	VDD15	VDD15	—	—
U13	—	—	VDD15	VDD15	—	—
U14	—	—	VDD15	VDD15	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
U15	—	—	VDD15	VDD15	—	—
U20	—	—	VDD15	VDD15	—	—
U21	—	—	VDD15	VDD15	—	—
U22	—	—	VDD15	VDD15	—	—
V13	—	—	VDD15	VDD15	—	—
V14	—	—	VDD15	VDD15	—	—
V15	—	—	VDD15	VDD15	—	—
V20	—	—	VDD15	VDD15	—	—
V21	—	—	VDD15	VDD15	—	—
V22	—	—	VDD15	VDD15	—	—
V34	—	—	VDD15	VDD15	—	—
W13	—	—	VDD15	VDD15	—	—
W14	—	—	VDD15	VDD15	—	—
W15	—	—	VDD15	VDD15	—	—
W20	—	—	VDD15	VDD15	—	—
W21	—	—	VDD15	VDD15	—	—
W22	—	—	VDD15	VDD15	—	—
W34	—	—	VDD15	VDD15	—	—
Y16	—	—	VDD15	VDD15	—	—
Y17	—	—	VDD15	VDD15	—	—
Y18	—	—	VDD15	VDD15	—	—
Y19	—	—	VDD15	VDD15	—	—
AA16	—	—	VDD15	VDD15	—	—
AA17	—	—	VDD15	VDD15	—	—
AA18	—	—	VDD15	VDD15	—	—
AA19	—	—	VDD15	VDD15	—	—
AA34	—	—	VDD15	VDD15	—	—
AB16	—	—	VDD15	VDD15	—	—
AB17	—	—	VDD15	VDD15	—	—
AB18	—	—	VDD15	VDD15	—	—
AB19	—	—	VDD15	VDD15	—	—
AB34	—	—	VDD15	VDD15	—	—
AD33	—	—	VDD15	VDD15	—	—
AD34	—	—	VDD15	VDD15	—	—
AE34	—	—	VDD15	VDD15	—	—
AG33	—	—	VDD15	VDD15	—	—
AG34	—	—	VDD15	VDD15	—	—
AH34	—	—	VDD15	VDD15	—	—
AK29	—	—	VDD15	VDD15	—	—
AL32	—	—	VDD15	VDD15	—	—

Table 19. PBGA Pinout Table

BM680	VDDIO Bank	VREF Group	I/O	Pin Description	Additional Function	BM680 Pair
AL33	—	—	VDD15	VDD15	—	—
AL34	—	—	VDD15	VDD15	—	—
AM31	—	—	VDD15	VDD15	—	—
AM33	—	—	VDD15	VDD15	—	—
AM34	—	—	VDD15	VDD15	—	—
AN32	—	—	VDD15	VDD15	—	—
AP31	—	—	VDD15	VDD15	—	—
AN34	—	—	VSS	VSS	—	—
AP1	—	—	VSS	VSS	—	—
AP4	—	—	VSS	VSS	—	—
AP33	—	—	VSS	VSS	—	—
AP34	—	—	VSS	VSS	—	—
Y22	—	—	VSS	VSS	—	—
AP24	5 (BC)	—	VDDIO5	VDDIO5	—	—
AD1	7 (CL)	—	VDDIO7	VDDIO7	—	—

Note: The pin descriptions for RX_DAT_IN* and TX_DAT_OUT show both the naming conventions, 2.5 Gbit/10 Gbit, where only one is valid depending on the mode of operation.

Package Thermal Characteristics Summary

There are three thermal parameters that are in common use: ΘJA, ψJC, and ΘJC. It should be noted that all the parameters are affected, to varying degrees, by package design (including paddle size) and choice of materials, the amount of copper in the test board or system board, and system airflow.

ΘJA

This is the thermal resistance from junction to ambient (theta-JA, R-theta, etc.):

$$\Theta JA = \frac{TJ - TA}{Q}$$

Where T_J is the junction temperature, T_A, is the ambient air temperature, and Q is the chip power.

Experimentally, ΘJA is determined when a special thermal test die is assembled into the package of interest, and the part is mounted on the thermal test board. The diodes on the test chip are separately calibrated in an oven. The package/board is placed either in a JEDEC natural convection box or in the wind tunnel, the latter for forced convection measurements. A controlled amount of power (Q) is dissipated in the test chip's heater resistor, the chip's temperature (T_J) is determined by the forward drop on the diodes, and the ambient temperature (T_A) is noted. Note that ΘJA is expressed in units of °C/W.

ψJC

This JEDEC designated parameter correlates the junction temperature to the case temperature. It is generally used to infer the junction temperature while the device is operating in the system. It is not considered a true thermal resistance, and it is defined by:

$$\psi JC = \frac{TJ - TC}{Q}$$

Where T_C is the case temperature at top dead center, T_J is the junction temperature, and Q is the chip power. During the ΘJA measurements described above, besides the other parameters measured, an additional temperature reading, T_C, is made with a thermocouple attached at top-dead-center of the case. ψJC is also expressed in units of °C/W.

ΘJC

This is the thermal resistance from junction to case. It is most often used when attaching a heat sink to the top of the package. It is defined by:

$$\Theta JC = \frac{TJ - TC}{Q}$$

The parameters in this equation have been defined above. However, the measurements are performed with the case of the part pressed against a water-cooled heat sink to draw most of the heat generated by the chip out the top of the package. It is this difference in the measurement process that differentiates ΘJC from ψJC. ΘJC is a true thermal resistance and is expressed in units of °C/W.

ΘJB

This is the thermal resistance from junction to board (ΘJL). It is defined by:

$$\Theta JB = \frac{TJ - TB}{Q}$$

Where T_B is the temperature of the board adjacent to a lead measured with a thermocouple. The other parameters on the right-hand side have been defined above. This is considered a true thermal resistance, and the measurement is made with a water-cooled heat sink pressed against the board to draw most of the heat out of the leads. Note that ΘJB is expressed in units of °C/W, and that this parameter and the way it is measured are still in JEDEC committee.

FPSC Maximum Junction Temperature

Once the power dissipated by the FPSC has been determined (see the Estimating Power Dissipation section), the maximum junction temperature of the FPSC can be found. This is needed to determine if speed derating of the device from the 85 ˚C junction temperature used in all of the delay tables is needed. Using the maximum ambient temperature, TAmax, and the power dissipated by the device, Q (expressed in ˚C), the maximum junction temperature is approximated by:

$TJmax = TAmax + (Q * \Theta_{JA})$

Table 20 lists the thermal characteristics for all packages used with the *ORCA* ORLI10G FPSC.

Package Thermal Characteristics

Table 20. ORCA ORLI10G Plastic Package Thermal Guidelines

Package	ΘJA (˚C/W)			Max Power
	0 fpm	200 fpm	500 fpm	T = 70 ˚C Max TJ = 125 ˚C Max 0 fpm (W)
680-Pin PBGAM	13.4	11.5	10.5	4.10

Note: The 680-Pin PBGAM package includes a 2 oz. copper plate.

The ORLI10G in a 680 PBGAM1T package has Θ_{JC} of 3.5 deg C/W.

Heat Sink Vendors for BGA Packages

The estimated worst-case power requirements for the ORLI10G with a programmable XGMII to XSBI interface for 10 Gbits/s Ethernet applications is 4 W to 5 W. Consequently, for most applications an external heat sink will be required. Below, in alphabetical order, is a list of heat sink vendors who advertise heat sinks aimed at the BGA market.

Table 21. Heat Sink Vendors

Vendor	Location	Phone
Aavid Thermalloy	Concord, NH	(603) 224-9988
Chip Coolers (Tyco Electronics)	Harrisburg, PA	(800) 468-2023
IERC (CTS Corp.)	Burbank, CA	(818) 842-7277
R-Theta	Buffalo, NY	(800) 388-5428
Sanyo Denki	Torrance, CA	(310) 783-5400
Wakefield Thermal Solutions	Pelham, NH	(603) 635-2800

Package Coplanarity

The coplanarity limits of the packages are as follows:

- PBGAM: 8.0 mils

Package Parasitics

The electrical performance of an IC package, such as signal quality and noise sensitivity, is directly affected by the package parasitics. Table 22 lists eight parasitics associated with the *ORCA* packages. These parasitics represent the contributions of all components of a package, which include the bond wires, all internal package routing, and the external leads.

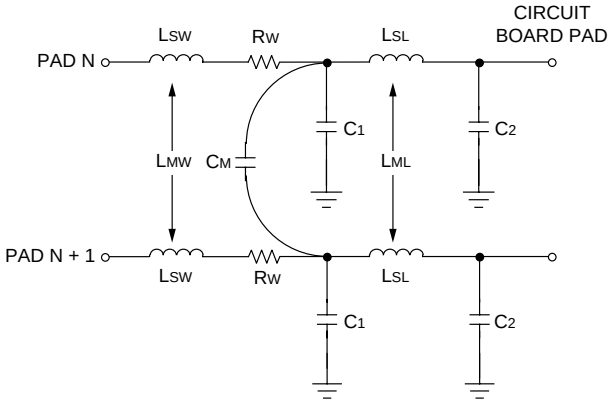
Four inductances in nH are listed: LSW and LSL, the self-inductance of the lead; and LMW and LML, the mutual inductance to the nearest neighbor lead. These parameters are important in determining ground bounce noise and inductive crosstalk noise. Three capacitances in pF are listed: CM, the mutual capacitance of the lead to the nearest neighbor lead; and C1 and C2, the total capacitance of the lead to all other leads (all other leads are assumed to be grounded). These parameters are important in determining capacitive crosstalk and the capacitive loading effect of the lead. Resistance values are in mΩ.

The parasitic values in Table 22 are for the circuit model of bond wire and package lead parasitics. If the mutual capacitance value is not used in the designer's model, then the value listed as mutual capacitance should be added to each of the C1 and C2 capacitors.

Table 22. ORCA ORLI10G Package Parasitics

Package Type	L_{SW}	L_{MW}	R_W	C_1	C_2	C_M	L_{SL}	L_{ML}
680-Pin PBGAM	3.80	1.30	250	0.50	1.0	0.30	2.8—5.0	0.5—1.50

Figure 34. Package Parasitics



Package Outline Diagrams

Terms and Definitions

Basic Size (BSC): The basic size of a dimension is the size from which the limits for that dimension are derived by the application of the allowance and the tolerance.

Design Size: The design size of a dimension is the actual size of the design, including an allowance for fit and tolerance.

Typical (TYP): When specified after a dimension, this indicates the repeated design size if a tolerance is specified or repeated basic size if a tolerance is not specified.

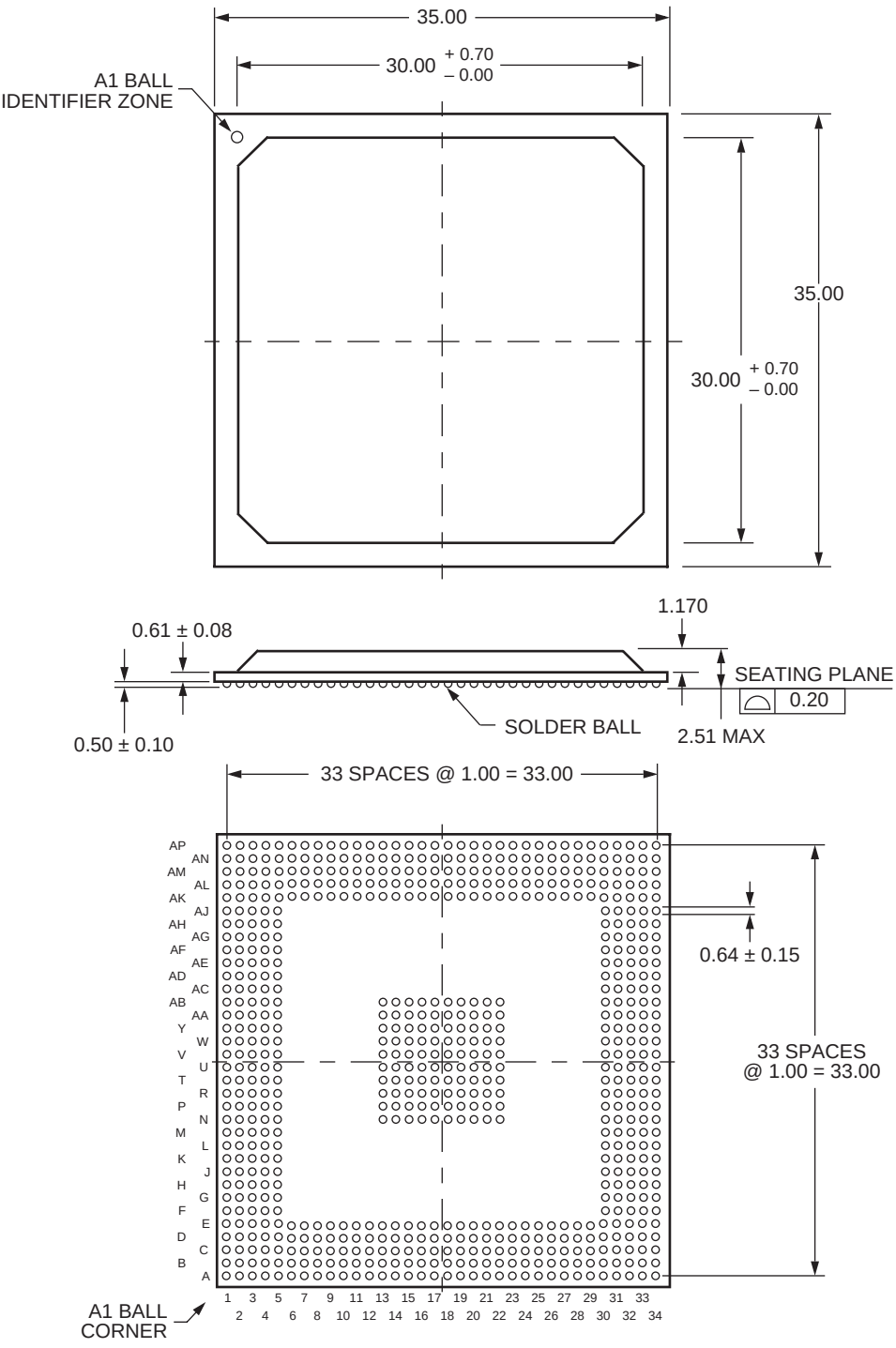
Reference (REF): The reference dimension is an untoleranced dimension used for informational purposes only. It is a repeated dimension or one that can be derived from other values in the drawing.

Minimum (MIN) or Maximum (MAX): Indicates the minimum or maximum allowable size of a dimension.

Package Outline Diagrams (continued)

680-Pin PBGAM

Dimensions are in millimeters.



5-4406(F)

Ordering Information

Figure 35. Part Number Description

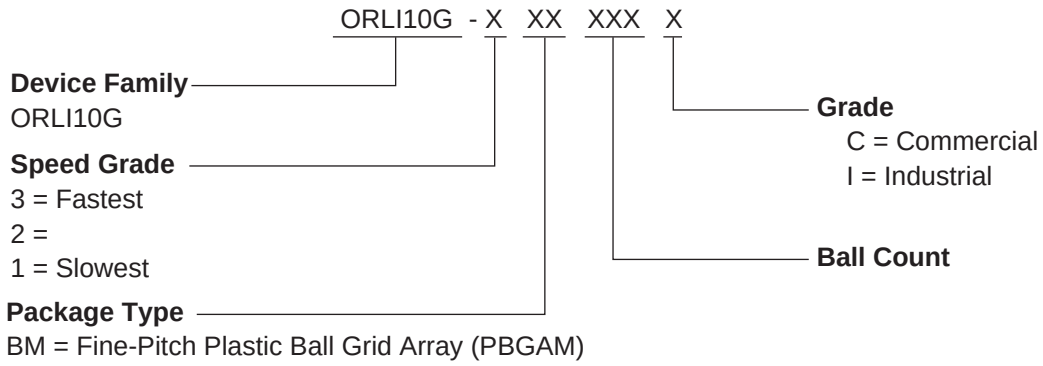


Table 23. Device Type Options

Device	Voltage
ORLI10G	1.5 V internal 3.3 V/2.5 V/1.8 V/1.5 V I/O

Table 24. Temperature Range

Symbol	Description	Ambient Temperature	Junction Temperature
C	Commercial	0 ˚C to +70 ˚C	0 ˚C to +85 ˚C
I	Industrial	–40 ˚C to +85 ˚C	–40 ˚C to +100 ˚C

Table 25. Commercial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORLI10G	ORLI10G-3BM680C	3	PBGAM	680	C
	ORLI10G-2BM680C	2	PBGAM	680	C
	ORLI10G-1BM680C	1	PBGAM	680	C

Table 26. Industrial Ordering Information[1]

Device Family	Part Number	Speed Grade	Package Type	Ball Count	Grade
ORLI10G	ORLI10G-2BM680I	2	PBGAM	680	I
	ORLI10G-1BM680I	1	PBGAM	680	I

1. For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -2XXXXXC is also marked with the industrial grade -1XXXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.