LatticeXP Family Data Sheet

Version 01.0, February 2005

LatticeXP Family Data Sheet Introduction

February 2005 **Advance Data Sheet**

Features

- **Non-volatile, Infinitely Reconfigurable**
  - Instant-on – powers up in microseconds
  - No external configuration memory
  - Excellent design security, no bit stream to intercept
  - Reconfigure SRAM based logic in milliseconds
  - SRAM and non-volatile memory programmable through system configuration and JTAG ports
  - Supports background programming of non-volatile memory
- **Extensive Density and Package Options**
  - 3.1K to 19.7K LUT4s
  - 62 to 340 I/Os
  - Density migration supported
- **Embedded and Distributed Memory**
  - 54 Kbits to 414 Kbits sysMEM™ Embedded Block RAM
  - Up to 79 Kbits distributed RAM
  - Flexible memory resources:
    - Distributed and block memory
- **Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTL
    - SSTL 18 Class I
    - SSTL 3/2 Class I, II
    - HSTL15 Class I, III
    - HSTL 18 Class I, II, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for configuration
  - Devices operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

Table 1-1. LatticeXP Family Selection Guide

Device	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	48	56
PFU/PFF (Total)	384	720	1216	1932	2464
LUTs (K)	3.1	5.8	9.7	15.4	19.7
Distributed RAM (KBits)	12	23	39	61	79
EBR SRAM (KBits)	54	90	216	288	414
EBR SRAM Blocks	6	10	24	32	46
V_{CC} Voltage	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
PLLs	2	2	4	4	4
Max. I/O	136	188	244	300	340
Packages and I/O Combinations:					
100-pin TQFP (14 x 14 mm)	62				
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	136	142			
256-ball fpBGA (17 x 17 mm)		188	188	188	188
388-ball fpBGA (23 x 23 mm)			244	268	268
484-ball fpBGA (23 x 23 mm)				300	340

Introduction

The LatticeXP family of FPGA devices combine logic gates, embedded memory and high performance I/Os in a single architecture that is both non-volatile and infinitely re-programmable to support cost-effective system designs.

The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeXP family of FPGA devices. Synthesis library support for LatticeXP is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeXP Family Data Sheet Architecture

February 2005 Advance Data Sheet

Architecture Overview

The LatticeXP architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR) as shown in Figure 2-1.

On the left and right sides of the PFU array, there are Non-volatile Memory Blocks. In configuration mode this non-volatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an "instant-on" capability that allows easy interfacing in many applications.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional unit without RAM/ROM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM, ROM and register functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row. The PFU blocks are used on the outside rows. The rest of the core consists of rows of PFF blocks interspersed with rows of PFU blocks. For every three rows of PFF blocks there is a row of PFU blocks.

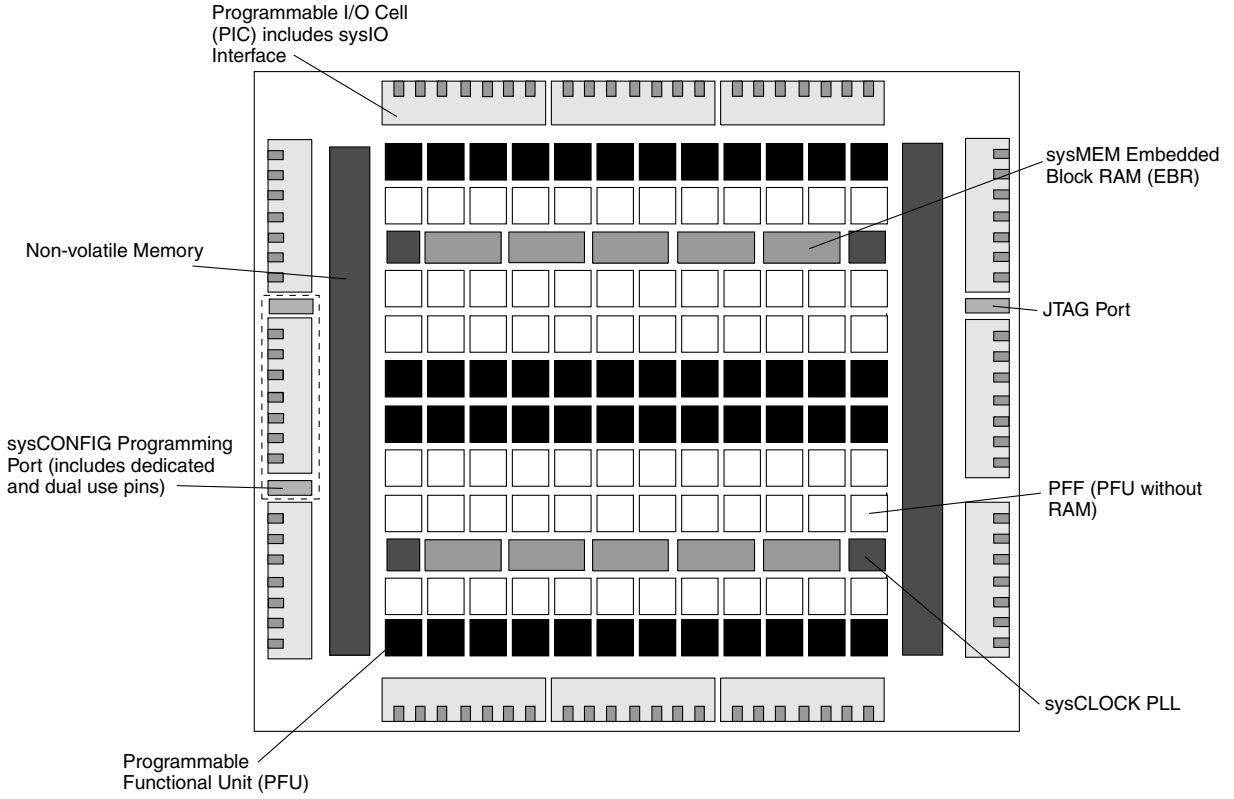
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM or ROM.

The PFU, PFF, PIC and EBR Blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

At the end of the rows containing the sysMEM Blocks are the sysCLOCK Phase Locked Loop (PLL) Blocks. These PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeXP architecture provides up to four PLLs per device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG port which allows for serial or parallel device configuration. The LatticeXP devices are available for operation from 3.3V, 2.5V, 1.8V and 1.2V power supplies, providing easy integration into the overall system.

Figure 2-1. LatticeXP Top Level Block Diagram

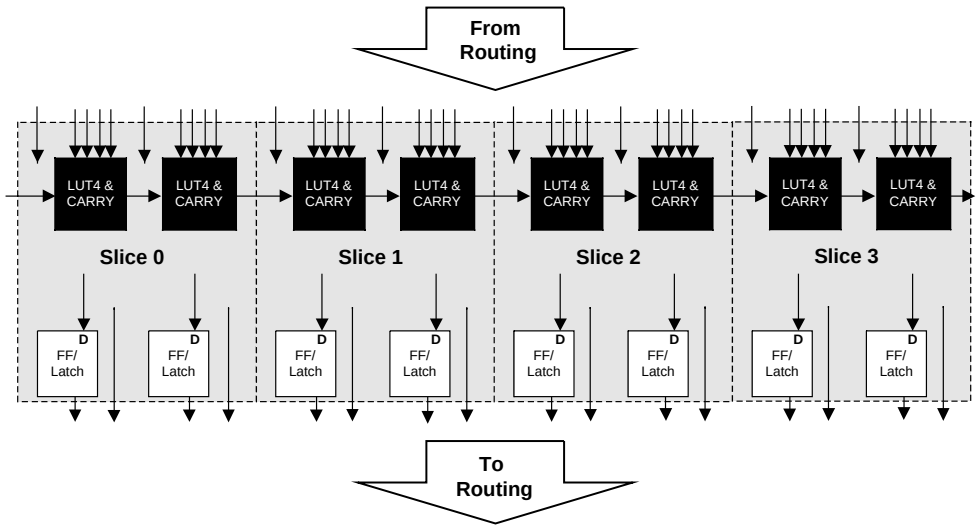


PFU and PFF Blocks

The core of the LatticeXP devices consists of PFU and PFF blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of the data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are 7 outputs: 6 to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-3. Slice Diagram

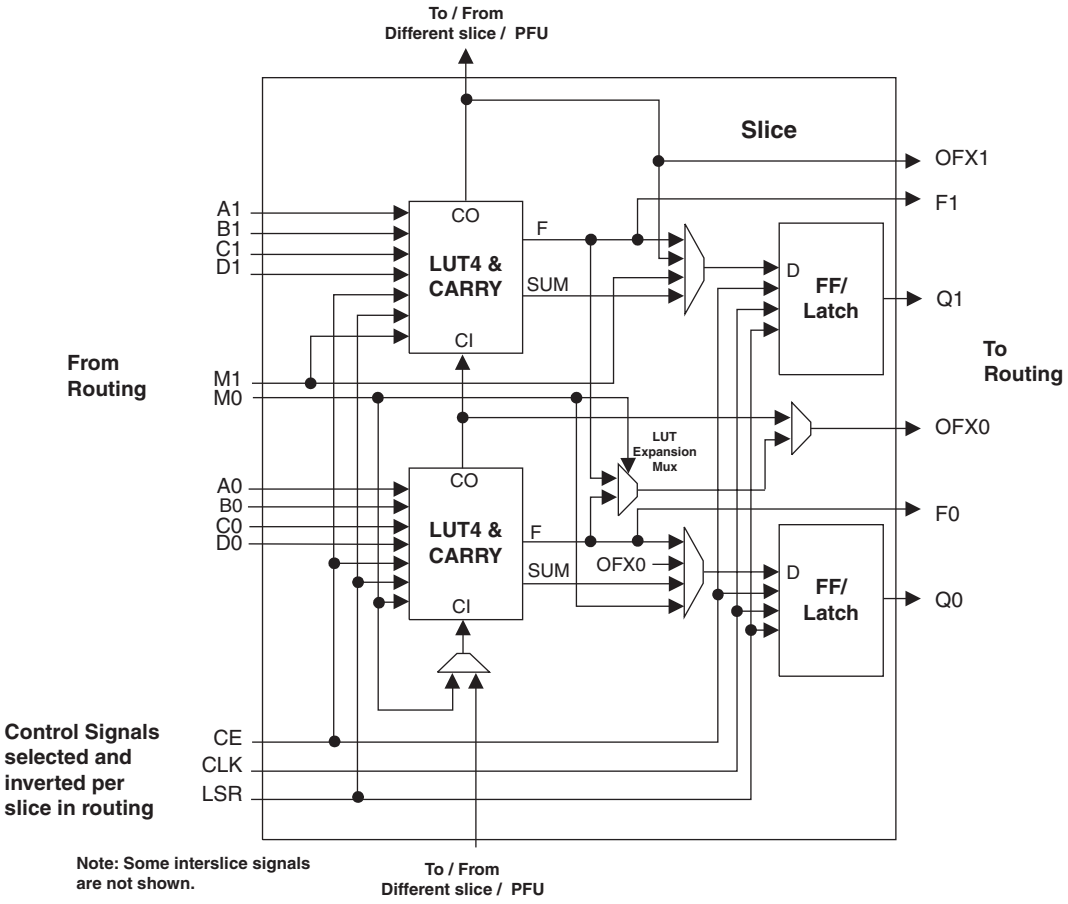


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[1]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. The Slice in the PFF is capable of all modes except RAM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SP 16x2	ROM 16x1 x 2
PFF Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	N/A	ROM 16x1 x 2

Logic Mode: In this mode, the LUTs in each Slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices.

Ripple Mode: Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Ripple mode multiplier building block
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per Slice in this mode, allowing fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode: In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

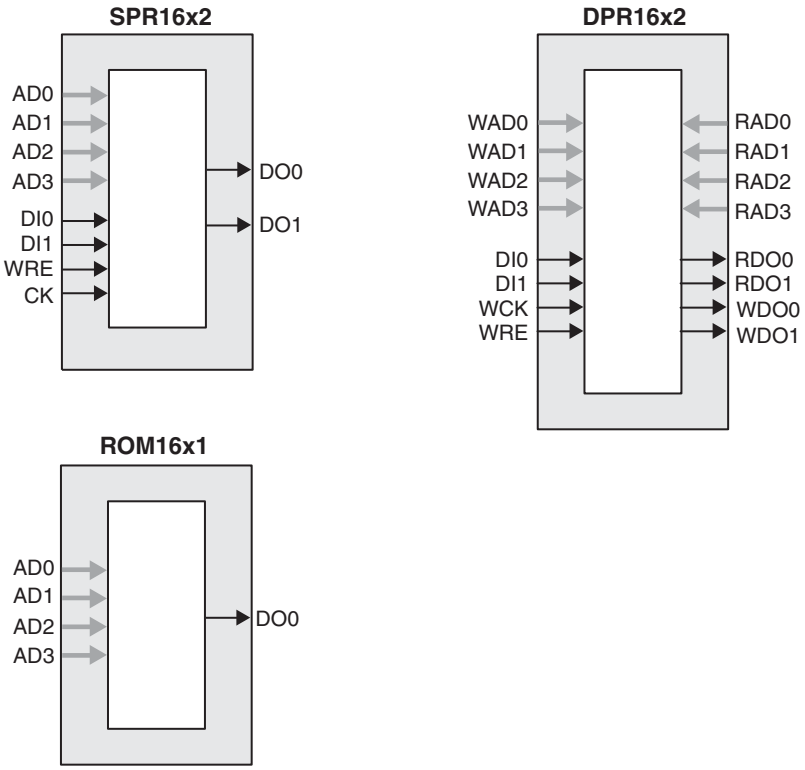
The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Figure 2-4 shows the distributed memory primitive block diagrams. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode in LatticeXP devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required for Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

Figure 2-4. Distributed Memory Primitives



ROM Mode: The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM[1]	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR16x2 x 4 DPR16x2 x 2	ROM16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR16x4 x 2 DPR16x4 x 1	ROM16x2 x 4
LUT 6x 2 or MUX 8x1 x 2	2-bit Counter x 4	SPR16x8 x 1	ROM16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM16x8 x 1

1. These modes are not available in PFF blocks

Routing

There are many resources provided in the LatticeXP devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

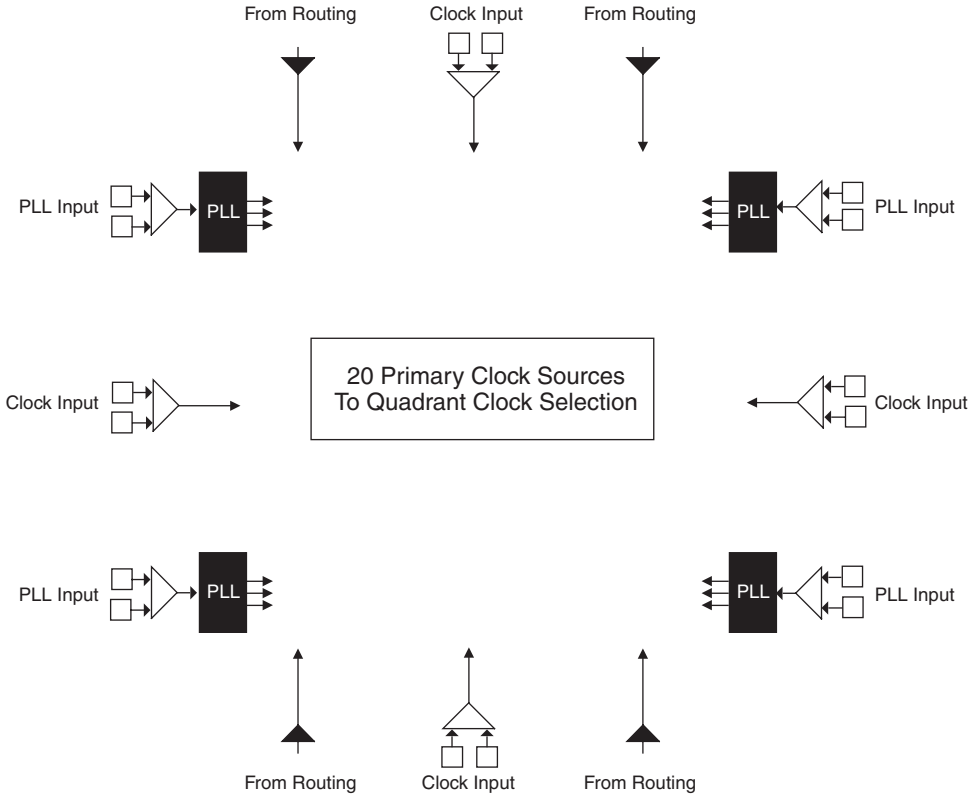
Clock Distribution Network

The clock inputs are selected from external I/O, the sysCLOCK™ PLLs or routing. These clock inputs are fed through the chip via a clock distribution system.

Primary Clock Sources

LatticeXP devices derive clocks from three primary sources: PLL outputs, dedicated clock inputs and routing. LatticeXP devices have two to four sysCLOCK PLLs, located on the left and right sides of the device. There are four dedicated clock inputs, one on each side of the device. Figure 2-5 shows the 20 primary clock sources.

Figure 2-5. Primary Clock Sources

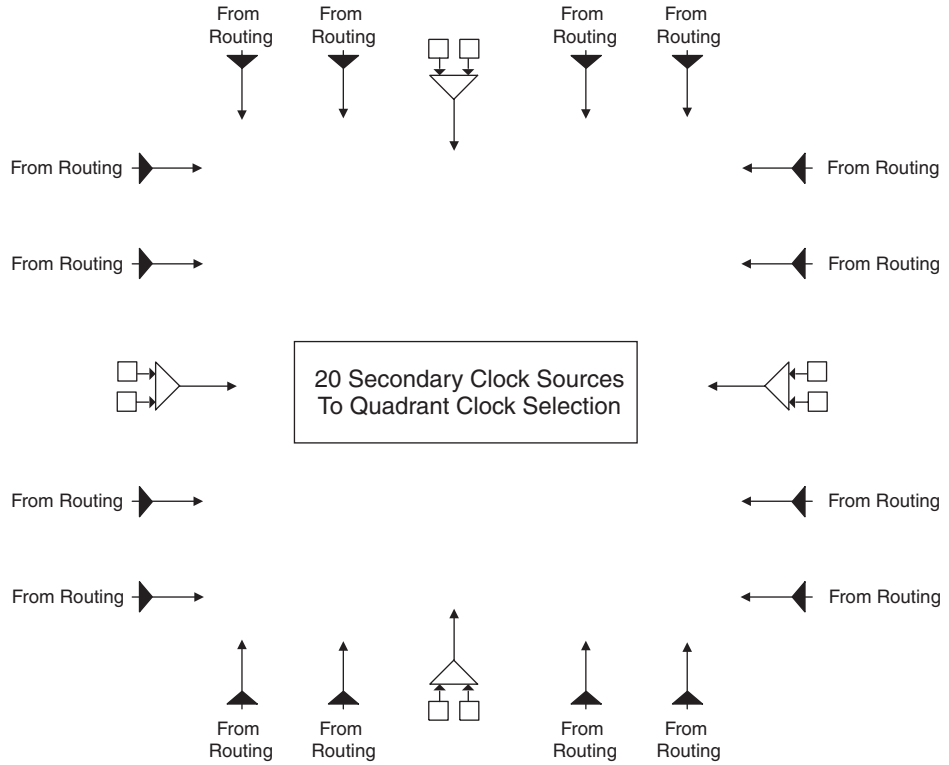


Note: Smaller devices have two PLLs.

Secondary Clock Sources

LatticeXP devices have four secondary clock resources per quadrant. The secondary clock branches are tapped at every PFU. These secondary clock networks can also be used for controls and high fanout data. These secondary clocks are derived from four clock input pads and 16 routing signals as shown in Figure 2-6.

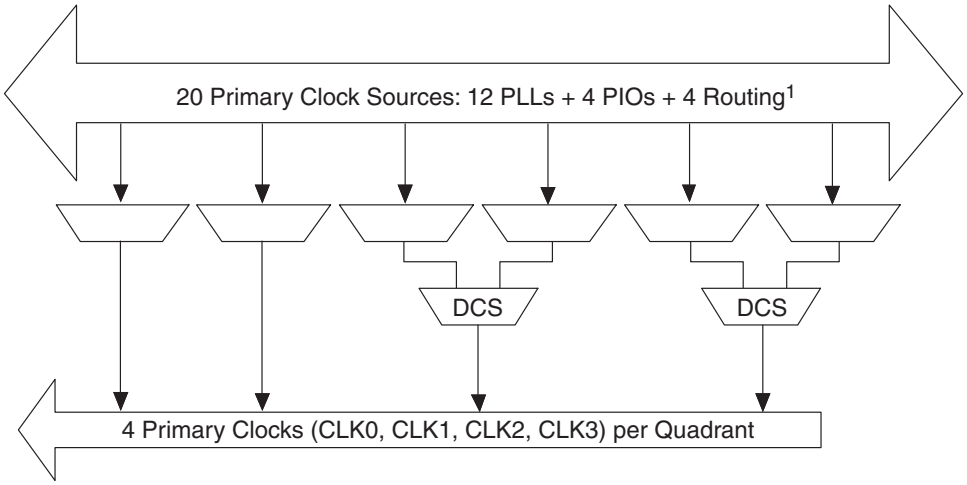
Figure 2-6. Secondary Clock Sources



Clock Routing

The clock routing structure in LatticeXP devices consists of four Primary Clock lines and a Secondary Clock network per quadrant. The primary clocks are generated from MUXs located in each quadrant. Figure 2-7 shows this clock routing. The four secondary clocks are generated from MUXs located in each quadrant as shown in Figure 2-8. Each slice derives its clock from the primary clock lines, secondary clock lines and routing as shown in Figure 2-9.

Figure 2-7. Per Quadrant Primary Clock Selection



1. Smaller devices have fewer PLL related lines.

Figure 2-8. Per Quadrant Secondary Clock Selection

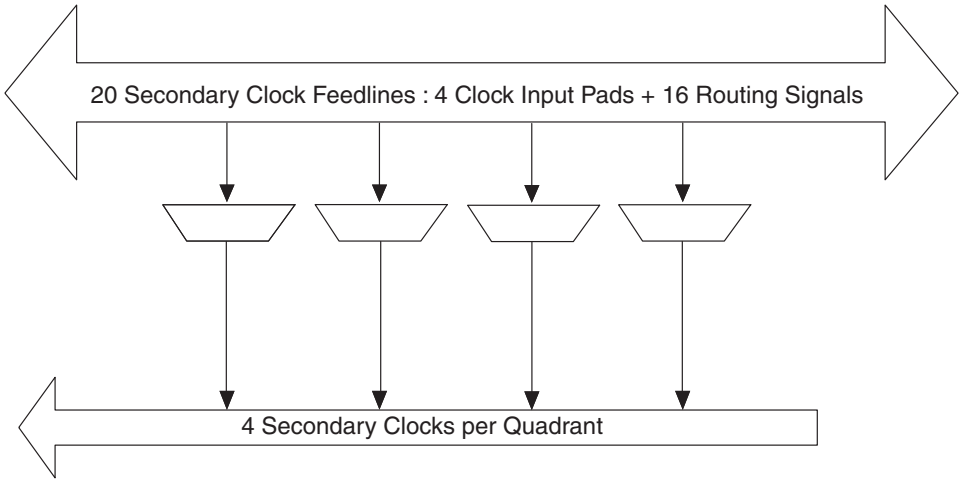
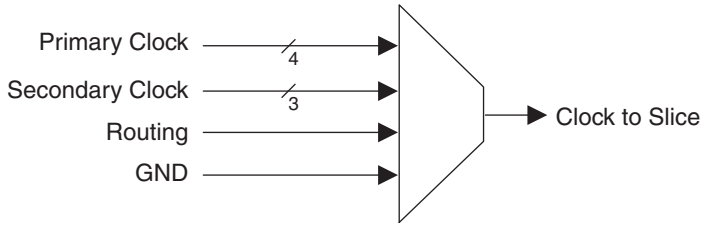


Figure 2-9. Slice Clock Selection



sysCLOCK Phase Locked Loops (PLLs)

The PLL clock input, from pin or routing, feeds into an input clock divider. There are four sources of feedback signal to the feedback divider: from the clock net, from output of the post scalar divider, from the routing or from an external pin. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-10 shows the sysCLOCK PLL diagram.

The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after adjustment and not relock until the t_{LOCK} parameter has been satisfied. Additionally, the phase and duty cycle block allows the user to adjust the phase and duty cycle of the CLKOS output.

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider, port scalar divider and secondary clock divider. The input clock divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal. The post scalar divider allows the VCO to operate at higher frequencies than the clock output, thereby increasing the frequency range. The secondary divider is used to derive lower frequency outputs.

Figure 2-10. PLL Diagram

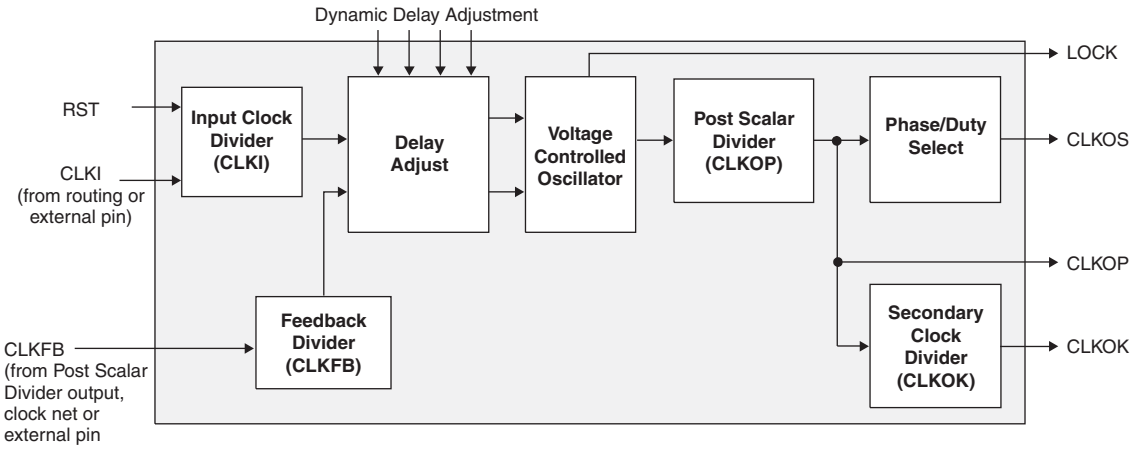


Figure 2-11 shows the available macros for the PLL. Table 2-5 provides signal description of the PLL Block.

Figure 2-11. PLL Primitive

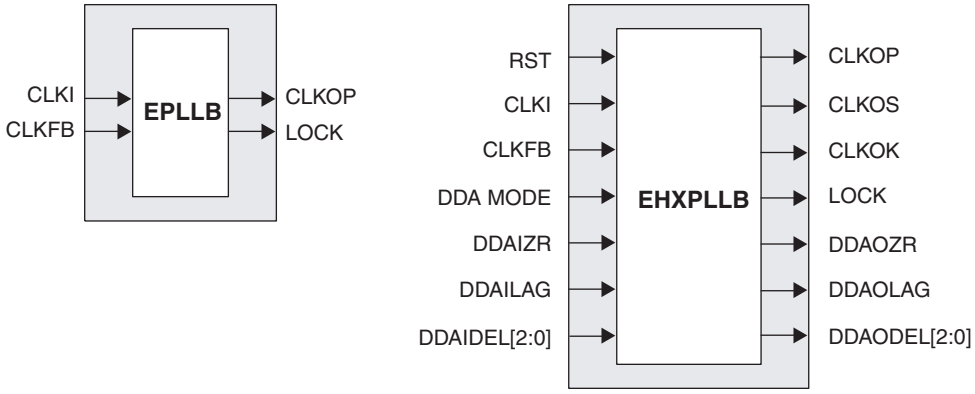


Table 2-5. PLL Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from PLL output, clocknet, routing or external pin
RST	I	“1” to reset input clock divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (No phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	“1” indicates PLL LOCK to CLKI
DDAMODE	I	Dynamic Delay Enable. “1” Pin control (dynamic), “0”: Fuse Control (static)
DDAIZR	I	Dynamic Delay Zero. “1”: delay = 0, “0”: delay = on
DDAILAG	I	Dynamic Delay Lag/Lead. “1”: Lag, “0”: Lead
DDAIDEL[2:0]	I	Dynamic Delay Input
DDAOZR	O	Dynamic Delay Zero Output
DDAOLAG	O	Dynamic Delay Lag/Lead Output
DDAODEL[2:0]	O	Dynamic Delay Output

For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-12 illustrates the DCS Block Macro.

Figure 2-12. DCS Block Primitive

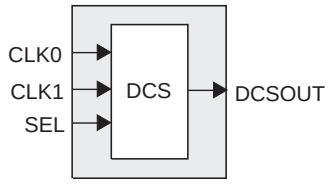
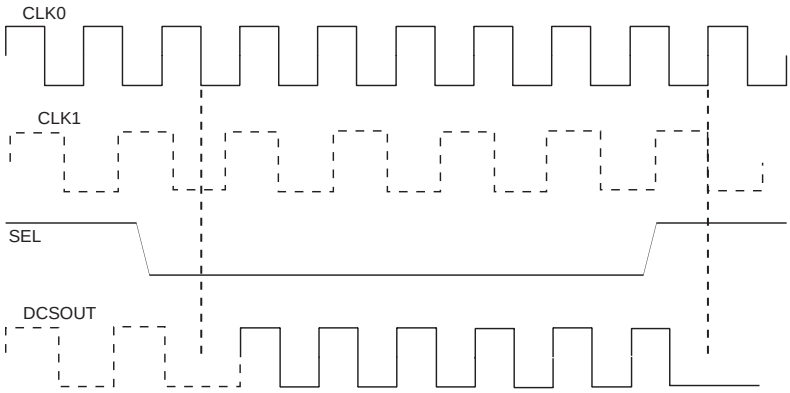


Figure 2-13 shows timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-13. DCS Waveforms



sysMEM Memory

The LatticeXP family of devices contain a number of sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18 256 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

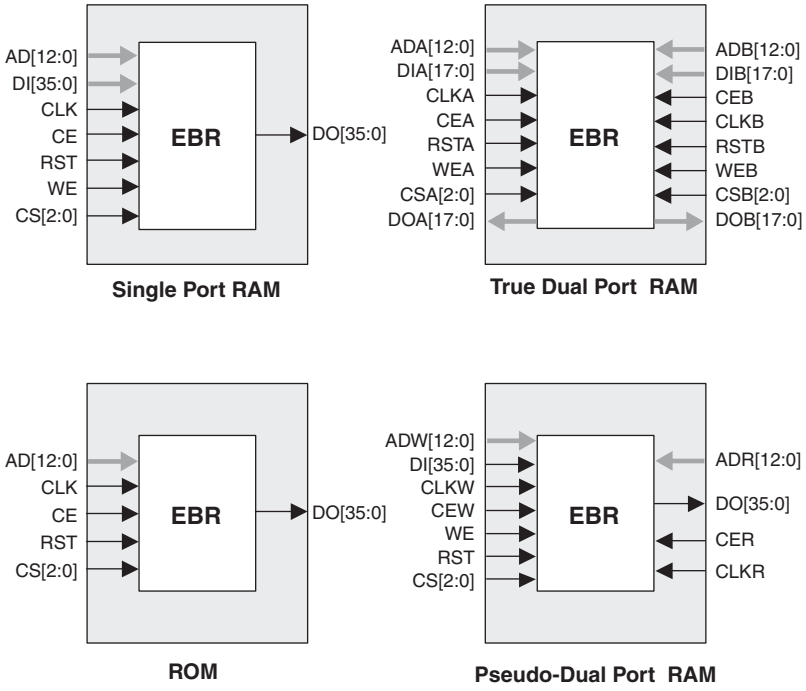
Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

Figure 2-14 shows the four basic memory configurations and their input/output names. In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

Figure 2-14. sysMEM Memory Primitives



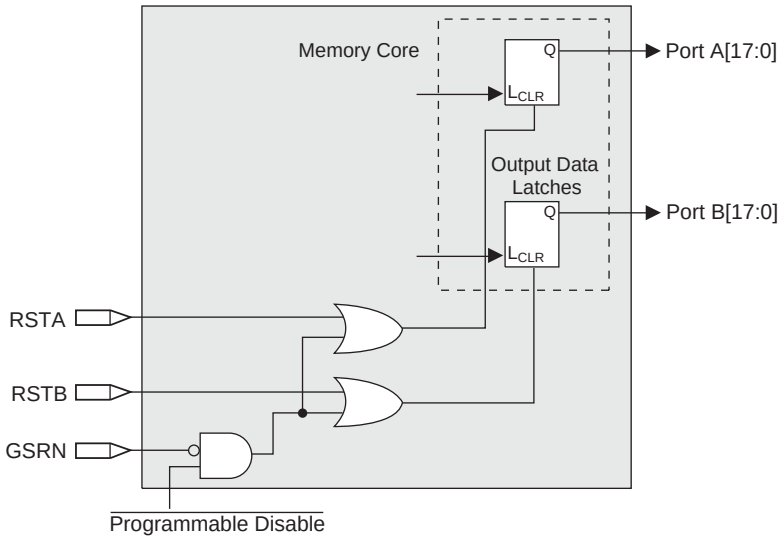
The EBR memory supports three forms of write behavior for dual port operation:

1. **Normal** – data on the output appears only during read cycle. During a write cycle, the data (at the current address) does not appear on the output.
2. **Write Through** – a copy of the input data appears at the output of the same port.
3. **Read-Before-Write** – when new data is being written, the old content of the address appears at the output.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-15.

Figure 2-15. Memory Core Reset

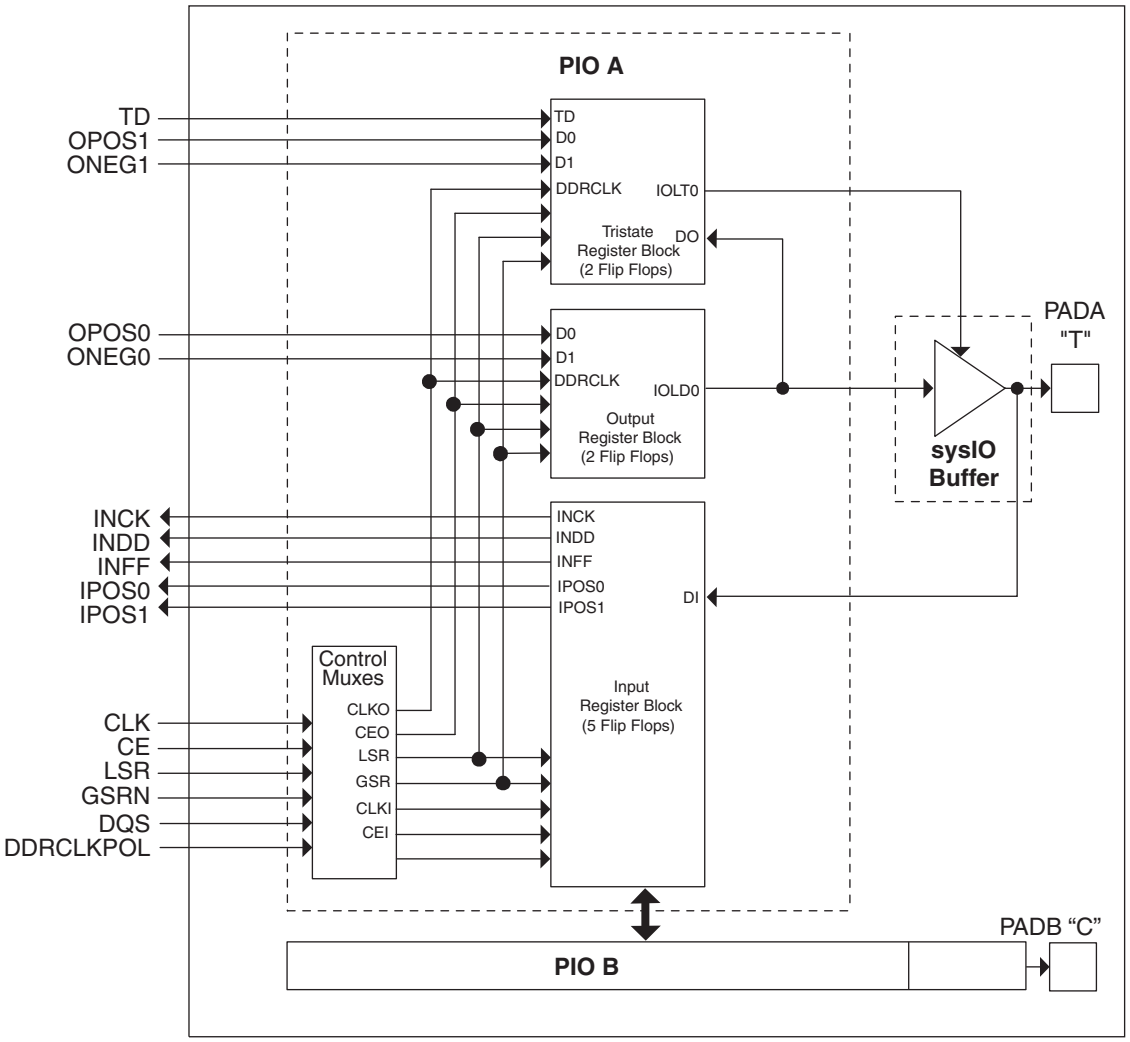


For further information on sysMEM EBR block, see the details of additional technical documentation at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO Buffers which are then connected to the PADs as shown in Figure 2-16. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to sysIO buffer, and receives input from the buffer.

Figure 2-16. PIC Diagram



In the LatticeXP family, seven PIOs or four (3.5) PICs are grouped together to provide two LVDS differential pairs, one PIC pair and one single I/O, as shown in Figure 2-17.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”). The PAD Labels “T” and “C” distinguish the two PIOs. Only the PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs.

One of every 14 PIOs (a group of 8 PICs) contains a delay element to facilitate the generation of DQS signals as shown in Figure 2-18. The DQS signal feeds the DQS bus which spans the set of 13 PIOs (8 PICs). The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. This interface is designed for memories that support one DQS strobe per eight bits of data.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table in this data sheet.

Figure 2-17. Group of Seven PIOs

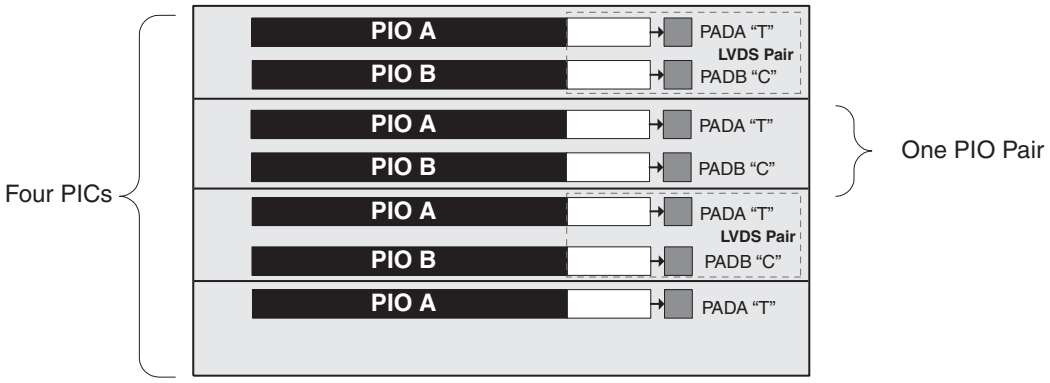
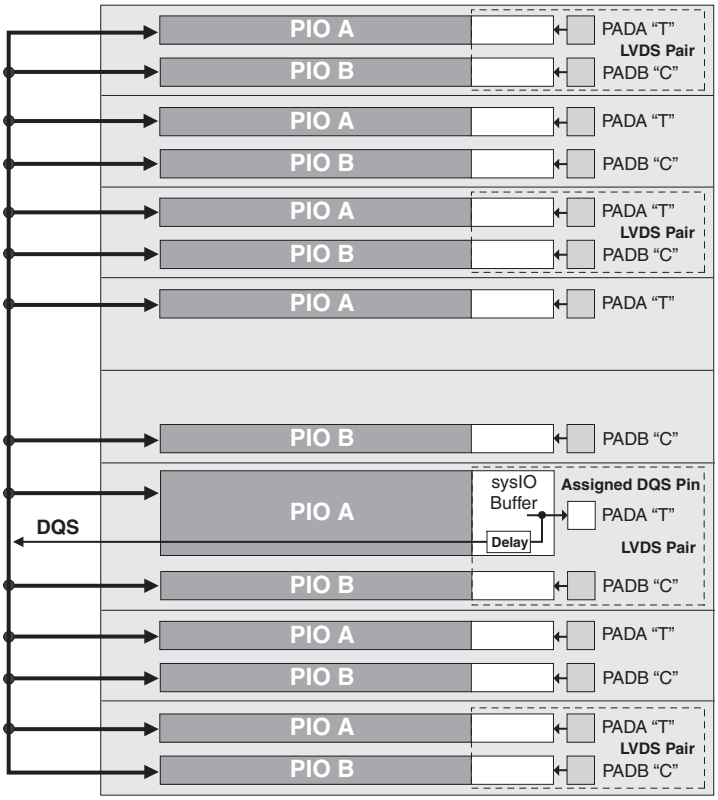


Figure 2-18. DQS Routing



PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for both single data rate (SDR) and double data rate (DDR) operation along with the necessary clock and selection logic. Programmable delay lines used to shift incoming clock and data signals are also included in these blocks.

Input Register Block: The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-19 shows the diagram of the input register block.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and in selected blocks the input to the DQS delay block. If one of the bypass options is not chosen, the signal first

passes through an optional delay block. This delay, if selected, ensures no positive input-register hold-time requirement when using a global clock.

The input block allows two modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In the DDR Mode two registers are used to sample the data on the positive and negative edges of the DQS signal creating two data streams, D0 and D2. These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

Figure 2-20 shows the input register waveforms for DDR operation and Figure 2-21 shows the design tool primitives. The SDR/SYNC registers have reset and clock enable available.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to the system clock domain. For further discussion of this topic, see the DDR memory section of this data sheet.

Figure 2-19. Input Register Diagram

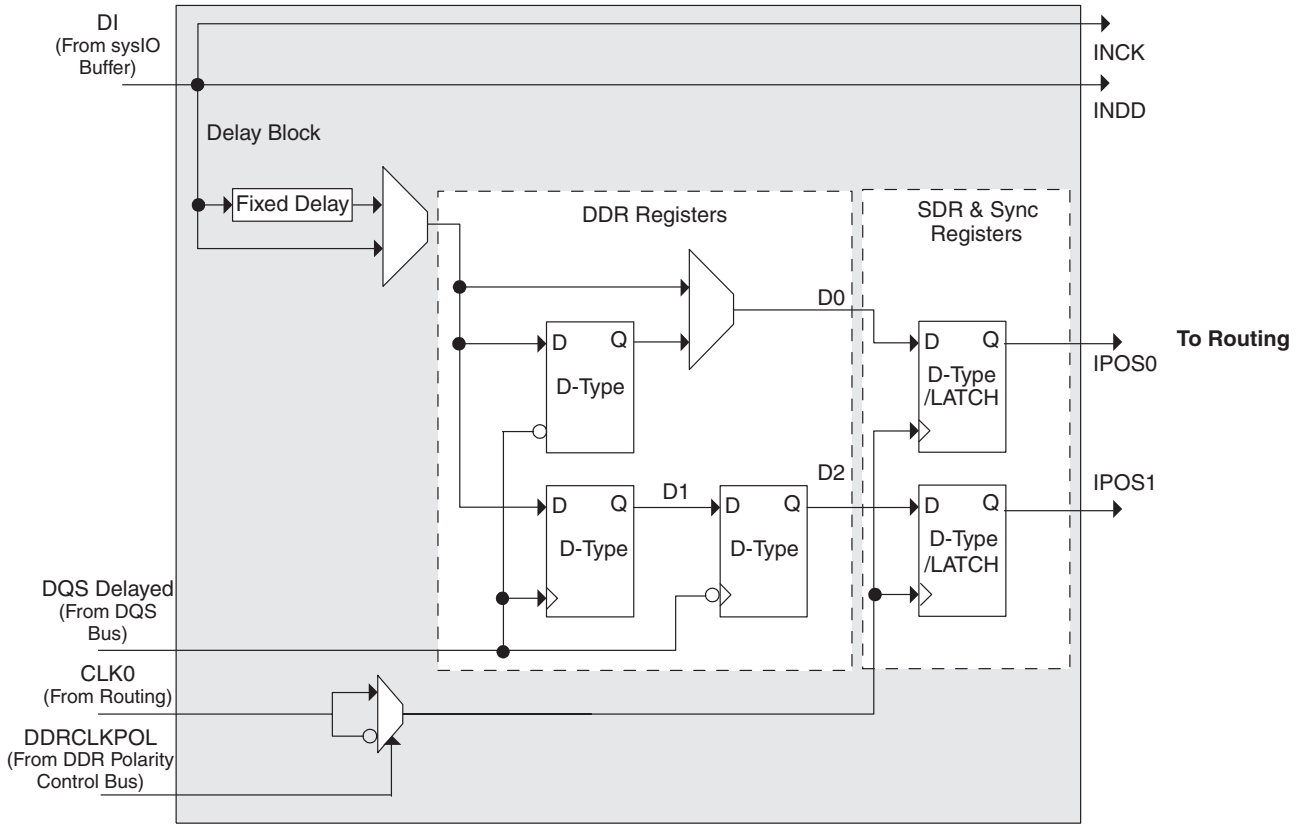


Figure 2-20. Input Register DDR Waveforms

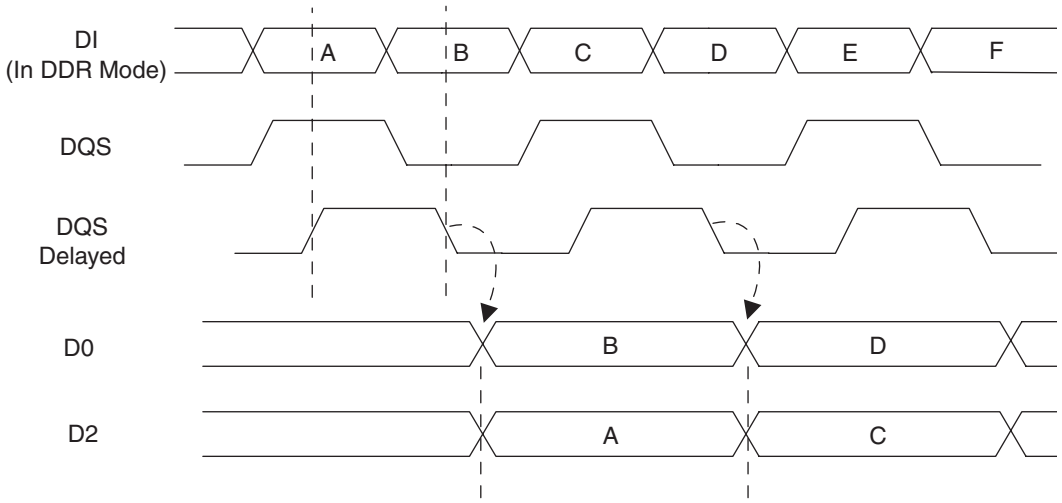
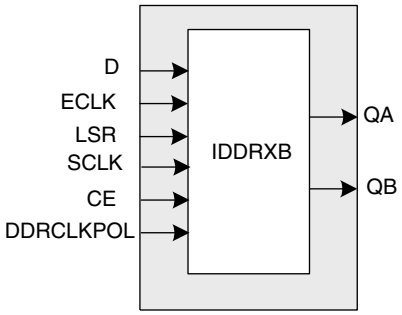


Figure 2-21. INDDRXB Primitive

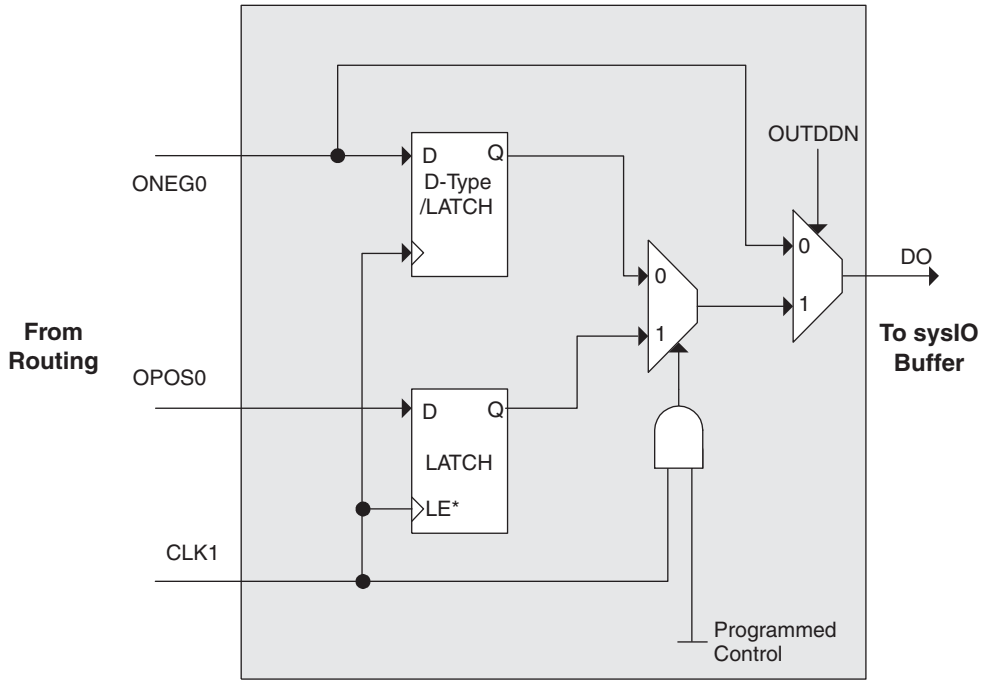


Output Register Block: The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-22 shows the diagram of the Output Register Block.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or as a latch. In DDR mode, ONEG0 is fed into one register on the positive edge of the clock and OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

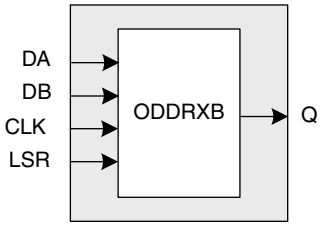
Figure 2-23 shows the design tool DDR primitives. The SDR output register has reset and clock enable available. The additional register for DDR operation does not have reset or clock enable available.

Figure 2-22. Output Register Block



*Latch is transparent when input is low.

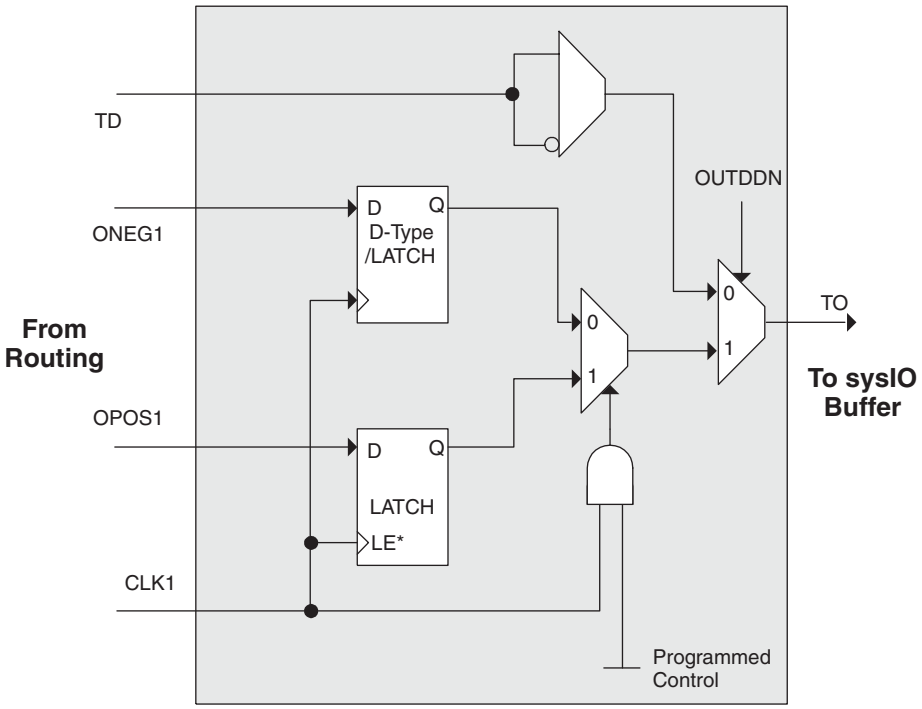
Figure 2-23. ODDRXB Primitive



Tristate Register Block: The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-24 shows the diagram of the Tristate Register Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 is fed into one register on the positive edge of the clock and OPOS1 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

Figure 2-24. Tristate Register Block



*Latch is transparent when input is low.

Control Logic Block: The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing and a DQS signal provided from the programmable DQS pin. The clock can optionally be inverted.

The clock enable and local reset signals are selected from the routing and optionally inverted. The global tristate signal is passed through this block.

DDR Memory Support

Implementing high performance DDR memory interfaces requires dedicated DDR register structures in the input (for read operations) and in the output (for write operations). As indicated in the PIO Logic section, the LatticeXP devices provide this capability. In addition to these registers, the LatticeXP devices contain two elements to simplify the design of input structures for read operations: the DQS delay block and polarity control logic.

DLL Calibrated DQS Delay Block

Source Synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment, however in DDR memories the clock (referred to as DQS) is not free running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds the polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figures 2-25 and 2-26 show how the polarity control logic are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two DLLs on opposite sides of the device. Each DLL compensates DQS Delays in its half of the device as shown in Figure 2-26. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-25. DQS Local Bus

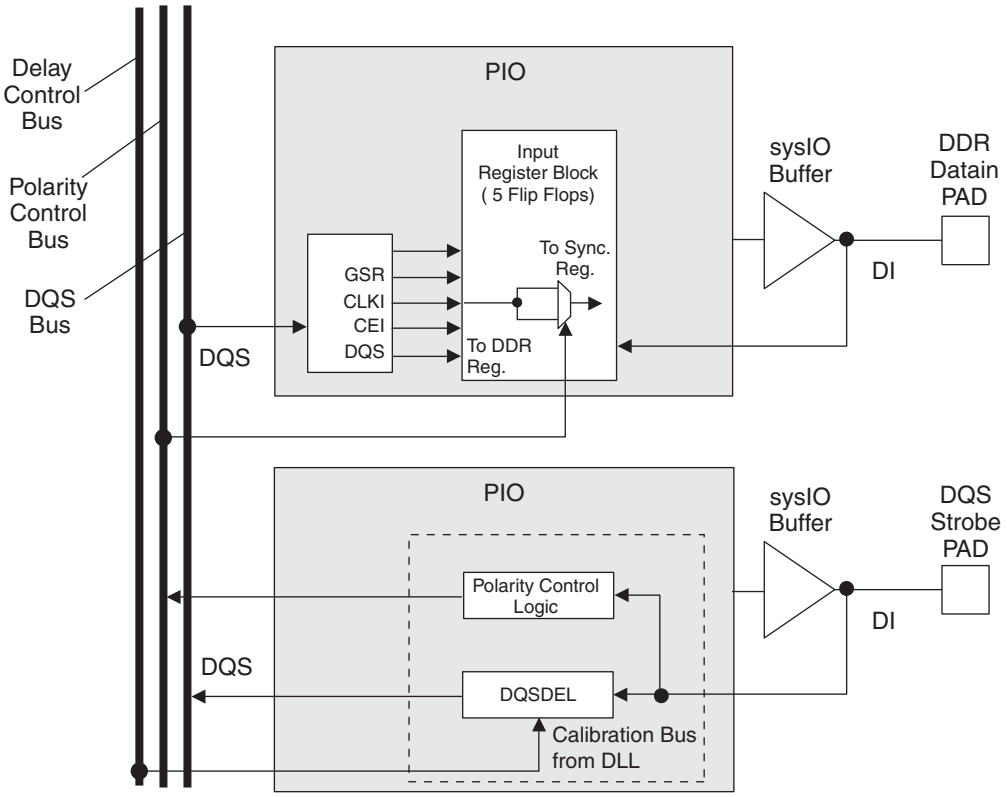
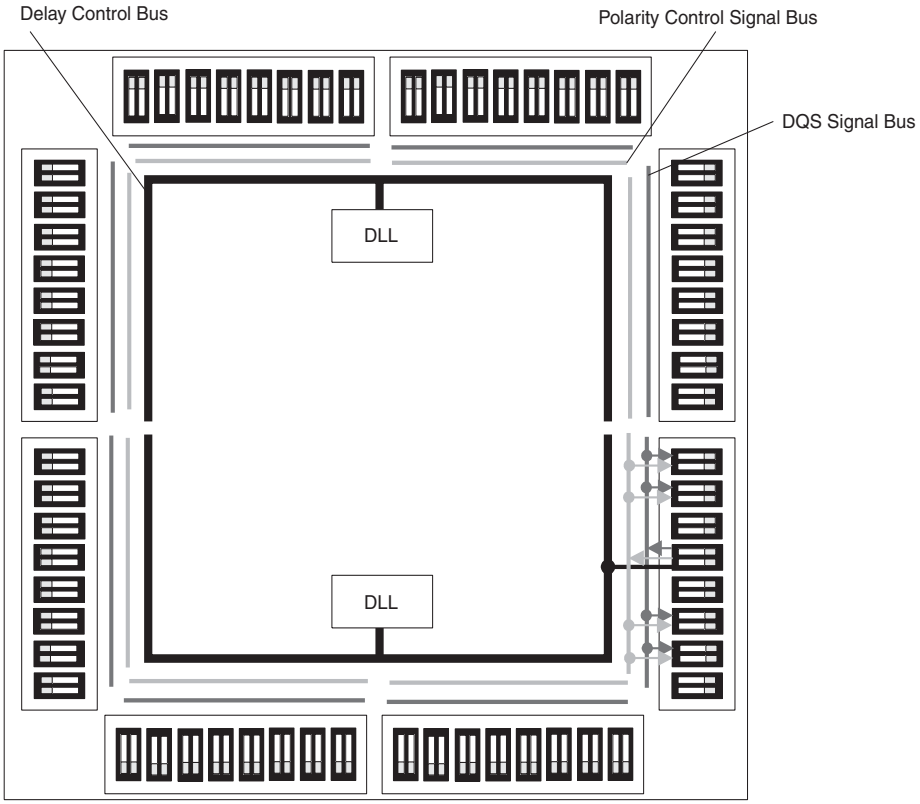


Figure 2-26. DLL Calibration Bus and DQS/DQS Transition Distribution



Polarity Control Logic

In a typical DDR Memory interface design, the phase relation between the incoming delayed DQS strobe and the internal system Clock (during the READ cycle) is unknown.

The LatticeXP family contains dedicated circuits to transfer data between these domains. To prevent setup and hold violations at the domain transfer between DQS (delayed) and the system Clock a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of the each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in eight groups referred to as Banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

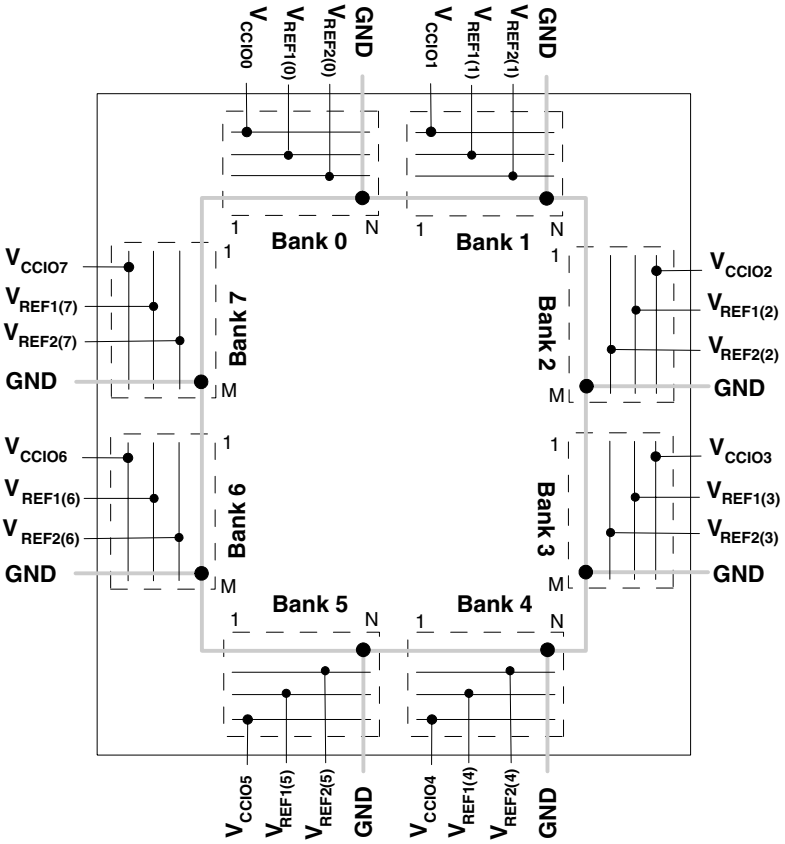
sysIO Buffer Banks

LatticeXP devices have eight sysIO buffer banks; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-27 shows the eight banks and their associated supplies.

In the LatticeXP devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS, PCI and PCI-X) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as a fixed threshold input independent of $V_{CCIO.}$ In addition to the bank V_{CCIO} supplies, the LatticeXP devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeXP devices, a dedicated pin in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-27. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

LatticeXP devices contain two types of sysIO buffer pairs.

1. **Top and Bottom sysIO Buffer Pair (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top and bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on the top and bottom banks have PCI clamp.

2. **Left and Right sysIO Buffer Pair (Differential and Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. The referenced input buffer can also be configured as a differential input. In these banks the two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   Only the left and right banks have LVDS differential output drivers.

Supported Standards

The LatticeXP sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, BLVDS, LVPECL, differential SSTL and differential HSTL. Tables 2-7 and 2-8 show the I/O standards (together with their supply and reference voltages) supported by the LatticeXP devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical documentation at the end of this data sheet.

Table 2-7. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33[2]	—	—
LVCMOS25[2]	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12[2]	—	—
PCI	—	3.3
HSTL18 Class I, II	0.9	—
HSTL18 Class III	1.08	—
HSTL15 Class I	0.75	—
HSTL15 Class III	0.9	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I	0.9	—
Differential Interfaces		
Differential SSTL18 Class I	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I, III	—	—
Differential HSTL18 Class I, II, III	—	—
LVDS, LVPECL	—	—
BLVDS	—	—

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. JTAG inputs do not have a fixed threshold option and always follow V_{CCJ}.

Table 2-8. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA. 6mA	—
PCI33	N/A	3.3
HSTL18 Class I, II, III	N/A	1.8
HSTL15 Class I, III	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I	N/A	1.8
Differential HSTL18, Class I, II, III	N/A	1.8
Differential HSTL15, Class I, III	N/A	1.5
LVDS	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3

1. Emulated with external resistors.

Hot Socketing

The LatticeXP devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, this allows for easy integration with the rest of the system. These capabilities make the LatticeXP ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

The following section describes the configuration and testing features of the LatticeXP family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port

consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeXP devices contain two possible ports that can be used for device configuration and programming. The test access port (TAP), which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration.

The non-volatile memory in the ispXP can be configured in three different modes:

- In sysCONFIG mode via the sysCONFIG port. Note this can be done with the device operating.
- In 1532 mode via the 1149.1 port.
- In background mode via the 1149.1 port. This allows the device to be operated while reprogramming takes place.

The SRAM configuration memory can be configured in four different ways:

- At power-up via the on-chip non-volatile memory.
- On a user-issued refresh command. Note this can be done by toggling the PROGRAMN pin or by issuing a command via the JTAG port in 1532 mode.
- In 1532 mode via the 1149.1 port.
- In sysCONFIG mode via the sysCONFIG port.

Figure 2-28 provides a pictorial representation of the different programming ports and modes available in the LatticeXP devices.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next power-up sequence.

Leave Alone I/O

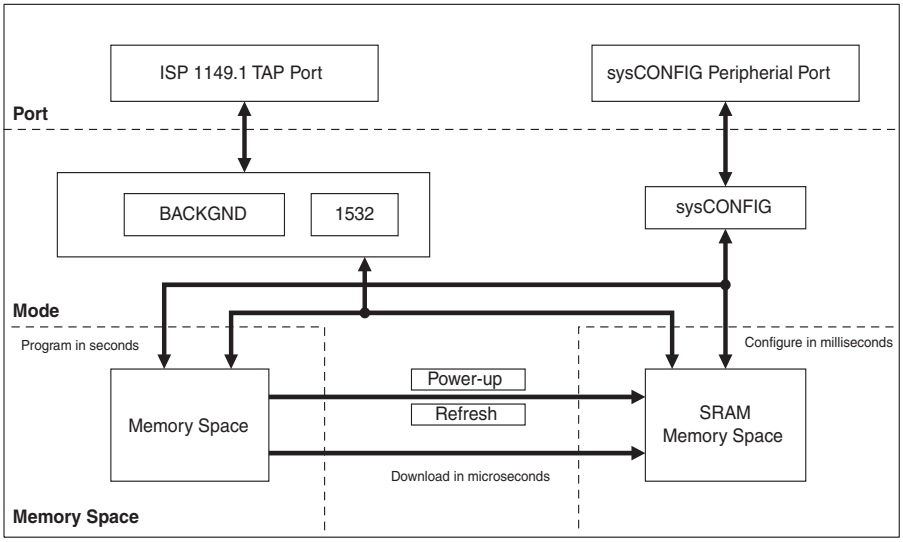
When using 1532 mode for non-volatile memory programming, users may specify I/Os as high, low, tristated or held at current value. This provides excellent flexibility for implementing systems where reprogramming occurs on-the-fly.

Security

The LatticeXP devices contain security bits that, when set, prevent the readback of the SRAM configuration and non-volatile memory spaces. Once set, the only way to clear security bits is to erase the memory space.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Figure 2-28. ispXP Block Diagram



Internal Logic Analyzer Capability (ispTRACY)

All LatticeXP devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time.

For more information on ispTRACY, please see information regarding additional technical documentation at the end of this data sheet.

Oscillator

Every LatticeXP device has an internal CMOS oscillator which is used to derive a master serial clock for configuration. The oscillator and the master serial clock run continuously. The default value of the master serial clock is 2.5MHz. Table 2-9 lists all the available Master Serial Clock frequencies. When a different Master Serial Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Serial Clock frequency for configuration.
2. During configuration the device starts with the default (2.5MHz) Master Serial Clock frequency.
3. The clock configuration settings are contained in the early configuration bit stream.
4. The Master Serial Clock frequency changes to the selected frequency once the clock configuration bits are received.

For further information on the use of this oscillator for configuration, please see details of additional technical documentation at the end of this data sheet.

Table 2-9. Selectable Master Serial Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5[1]	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

1. Default

Density Shifting

The LatticeXP family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeXP Family Data Sheet
DC and Switching Characteristics

February 2005 **Advance Data Sheet**

Absolute Maximum Ratings[1, 2, 3, 4]

	XPE (1.2V)	XPC (1.8V/2.5V/3.3V)
Supply Voltage V_{CC}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCP}	-0.5 to 1.32V	-0.5 to 3.75V
Supply Voltage V_{CCAUX}	-0.5 to 3.75V	-0.5 to 3.75V
Supply Voltage V_{CCJ}	-0.5 to 3.75V	-0.5 to 3.75V
Output Supply Voltage V_{CCIO}	-0.5 to 3.75V	-0.5 to 3.75V
I/O Tristate Voltage Applied [5]	-0.5 to 3.75V	-0.5 to 3.75V
Input Voltage Applied [5]	-0.5 to 3.75V	-0.5 to 4.25V
Storage Temperature (ambient)	-65 to 150°C	-65 to 150°C
Junction Temp. (Tj)	+125°C	+125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. All chip grounds are connected together to a common package GND plane.
5. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage for 1.2V Devices	1.14	1.26	V
	Core Supply Voltage for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCP}	Supply Voltage for PLL for 1.2V Devices	1.14	1.26	V
	Supply Voltage for PLL for 1.8V/2.5V/3.3V Devices	1.71	3.465	V
V_{CCAUX}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Commercial Operation	0	+85	C
t_{JIND}	Junction Industrial Operation	-40	100	C

1. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}. For the XPE devices (1.2V V_{CC}), if V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}.
2. See recommended voltages by I/O standard in subsequent table.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Input or I/O leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.
4. LVCMOS and LVTTL only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	$0 \le V_{IN} \le (V_{CCIO} - 0.2V)$	—	—	10	µA
		$(V_{CCIO} - 0.2V) \le V_{IN} \le 3.6V$	—	—	40	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHLH}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz

Supply Current (Standby)[1, 2, 3]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Device	Typ.[4]	Max.	Units
I_{CC}	Core Power Supply		LFXP3E			mA
			LFXP6E			mA
			LFXP10E	30		mA
			LFXP15E			mA
			LFXP20E			mA
			LFXP3C			mA
			LFXP6C			mA
			LFXP10C	60		mA
			LFXP15C			mA
			LFXP20C			mA
I_{CCP}	PLL Power Supply (per PLL)		LFXP3E,6E			mA
			LFXP10E,15E,20E	40		mA
			LFXP3C,6C			mA
			LFXP10C,15C,20C	40		mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V		LFXP3E			mA
			LFXP6E			mA
			LFXP10E	30		mA
			LFXP15E			mA
			LFXP20E			mA
			LFXP3C			mA
			LFXP6C			mA
			LFXP10C	30		mA
			LFXP15C			mA
			LFXP20C			mA
I_{CCIO}	Bank Power Supply[5]			15		mA
I_{CCJ}	V_{CCJ} Power Supply			2		mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. T_J=25°C, power supplies at normal voltage.
5. Per bank.

Initialization Supply Current[1, 2, 3, 4, 5]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Device	Typ.	Max.	Units
I_{CC}	Core Power Supply		LFXP3E			mA
			LFXP6E			mA
			LFXP10E			mA
			LFXP15E			mA
			LFXP20E			mA
			LFXP3C			mA
			LFXP6C			mA
			LFXP10C			mA
			LFXP15C			mA
			LFXP20C			mA
I_{CCP}	PLL Power Supply (per PLL)		LFXP3E,6E			mA
			LFXP10E,15E,20E			mA
			LFXP3C,6C			mA
			LFXP10C,15C,20C			mA
I_{CCAUX}	Auxiliary Power Supply V_{CCAUX} = 3.3V		LFXP3E			mA
			LFXP6E			mA
			LFXP10E			mA
			LFXP15E			mA
			LFXP20E			mA
			LFXP3C			mA
			LFXP6C			mA
			LFXP10C			mA
			LFXP15C			mA
			LFXP20C			mA
I_{CCIO}	Bank Power Supply[6]					mA
I_{CCJ}	V_{CCJ} Power Supply					mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. T_J=25°C power supplies at nominal voltage.
6. Per bank.

sysIO Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
SSTL18 Class I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2 Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3 Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15 Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15 Class III	1.425	1.5	1.575	—	0.9	—
HSTL 18 Class I, II	1.71	1.8	1.89	—	0.9	—
HSTL 18 Class III	1.71	1.8	1.89	—	1.08	—
LVDS	2.375	2.5	2.625	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	$0.3V_{CCIO}$	$0.5V_{CCIO}$	3.6	$0.1V_{CCIO}$	$0.9V_{CCIO}$	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
SSTL18 class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
HSTL15 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
HSTL15 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8
HSTL18 class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	9.6	-9.6
HSTL18 class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16
HSTL18 class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	24	-8

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{THD}	Differential Input Threshold		+/-100	—	—	mV
V_{CM}	Input Common Mode Voltage	100mV ≤ V_{THD}	V_{THD}/2	1.2	1.8	V
		200mV ≤ V_{THD}	V_{THD}/2	1.2	1.9	V
		350mV ≤ V_{THD}	V_{THD}/2	1.2	2.0	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	6	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

BLVDS

The LatticeXP devices support BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. BLVDS Multi-point Output Example

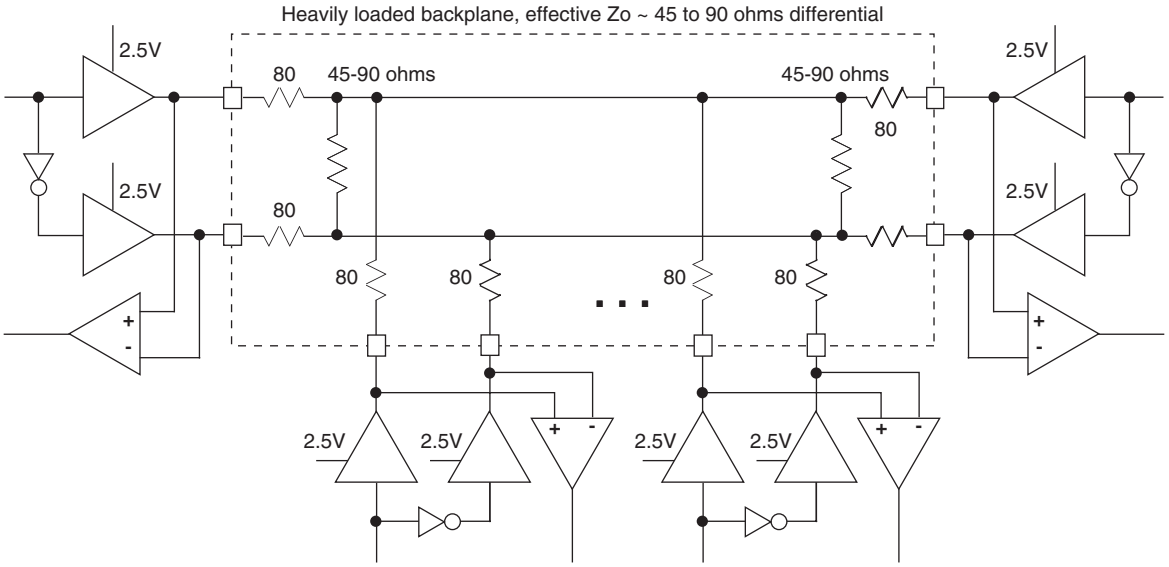


Table 3-1. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Typical		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LVPECL

The LatticeXP devices support differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-2 is one possible solution for point-to-point signals.

Figure 3-2. Differential LVPECL

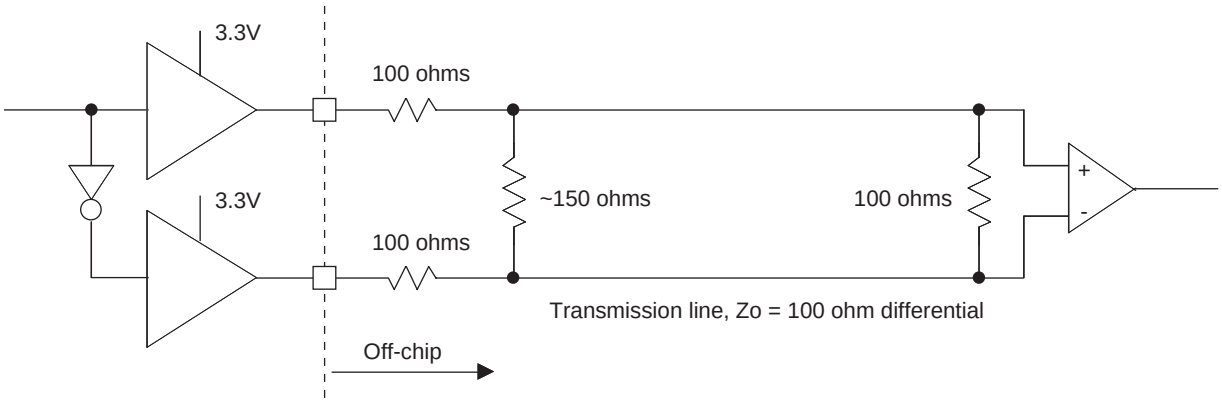


Table 3-2. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Typical	Units
Z_{OUT}	Output impedance	100	ohm
R_P	Driver parallel resistor	150	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	85.7	ohm
I_{DC}	DC output current	12.7	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces please see details of additional technical documentation at the end of the data sheet.

RSDS

The LatticeXP devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for RSDS standard implementation. Use LVDS25E mode with suggested resistors for RSDS operation. Resistor values in Figure 3-3 are industry standard values for 1% resistors.

Figure 3-3. RSDS (Reduced Swing Differential Standard)

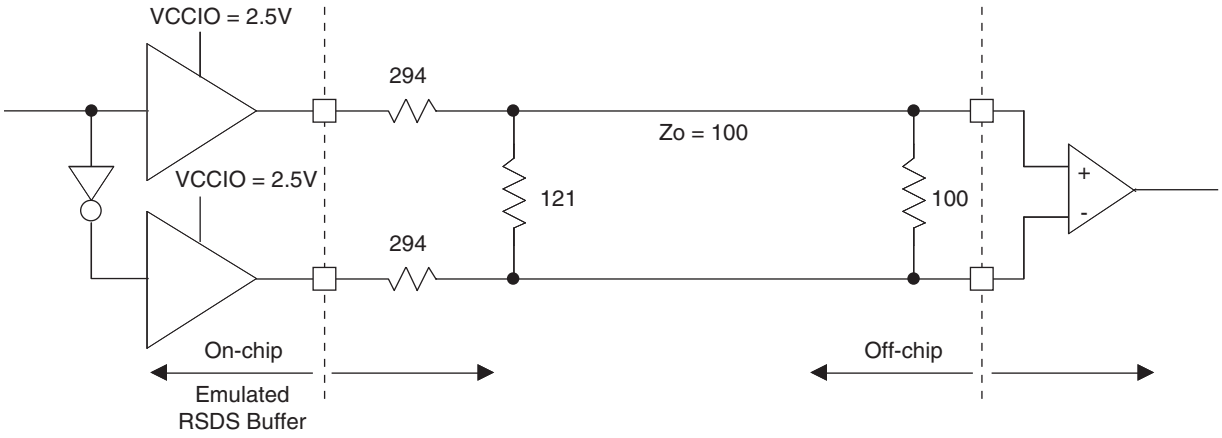


Table 3-3. RSDS DC Conditions

Parameter	Description	Typical	Units
Z_{OUT}	Output impedance	20	ohm
R_S	Driver series resistor	294	ohm
R_P	Driver parallel resistor	121	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	1.35	V
V_{OL}	Output low voltage	1.15	V
V_{OD}	Output differential voltage	0.20	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	101.5	ohm
I_{DC}	DC output current	3.66	mA

5V Tolerant Input Buffer

The input buffers of the LatticeXP family of devices can support 5V signals by using a PCI Clamp and an external series resistor as shown in Figure 3-4. A suitable resistor can be selected by using the PCI Clamp Characteristic as shown in Figure 3-5.

Figure 3-4. 5V Tolerant Input Buffer

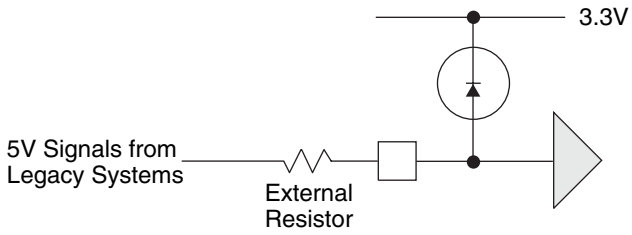
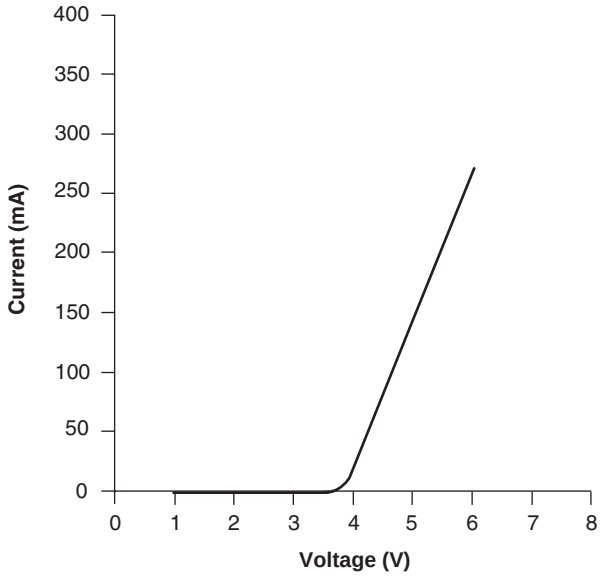


Figure 3-5. Typical PCI Clamp Current



Typical Building Block Function Performance

Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	6.2	ns
32-bit decoder	7.3	ns
64-bit decoder	8.1	ns
4:1 MUX	4.5	ns
8:1 MUX	4.8	ns
16:1 MUX	5.5	ns
32:1 MUX	5.8	ns

Register to Register Performance

Function	-5 Timing	Units
Basic Functions		
16-bit decoder	353	MHz
32-bit decoder	253	MHz
64-bit decoder	224	MHz
4:1 MUX	627	MHz
8:1 MUX	532	MHz
16:1 MUX	441	MHz
32:1 MUX	391	MHz
8-bit adder	357	MHz
16-bit adder	279	MHz
64-bit adder	158	MHz
16-bit counter	366	MHz
32-bit counter	282	MHz
64-bit counter	192	MHz
64-bit accumulator	158	MHz
Embedded Memory Functions		
Single port RAM 256x36 bits	280	MHz
True dual port RAM 512x18 bits	280	MHz
Distributed Memory Functions		
16x2 SP RAM	426	MHz
64x2 SP RAM	328	MHz
128x4 SP RAM	247	MHz
32x2 PDP RAM	355	MHz
64x4 PDP RAM	303	MHz

Note: The above timing numbers were generated using ispLEVER tool, exact performance may vary with design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
Timing v.0.04

Derating Logic Timing

Logic timing provided in the following sections of this data sheet and in the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best-case process can be much better than the values given in the tables. The ispLEVER design tool from Lattice can provide logic timing numbers at a particular temperature and voltage.

LatticeXP External Switching Characteristics

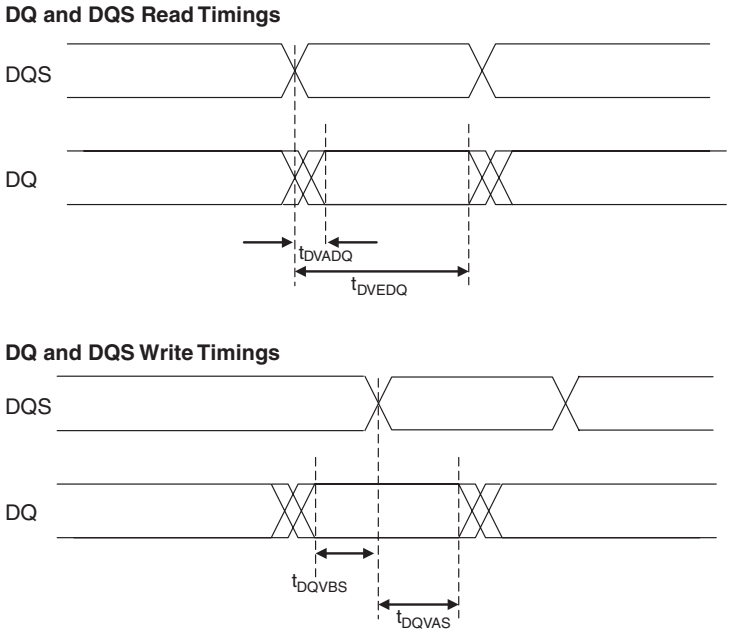
Over Recommended Operating Conditions

Parameter	Description	Device	-5		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output – PIO Output Register	LFXP10	—	5.5	—	6.6	—	7.7	ns
t_{SU}	Clock to Data Setup – PIO Input Register	LFXP10	0.0	—	0.0	—	0.0	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	LFXP10	3.4	—	4.2	—	4.9	—	ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFXP10	3.4	—	4.2	—	4.9	—	ns
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	LFXP10	0.0	—	0.0	—	0.0	—	ns
f_{MAX_IO}	Clock frequency of I/O and PFU Register	LFXP10	—		—		—		MHz
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	LFXP10	—	0.192	—	0.192	—	0.192	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	LFXP10	0.668	—	0.668	—	0.668	—	UI
t_{DQVBS}	Data Valid Before DQS	LFXP10	0.2	—	0.2	—	0.2	—	UI
t_{DQVAS}	Data Valid After DQS	LFXP10	0.2	—	0.2	—	0.2	—	UI
f_{MAX_DDR}	DDR Clock Frequency	LFXP10	95	166	95	133	95	100	MHz
Primary and Secondary Clock									
f_{MAX_PRI}	Frequency for Primary Clock Tree	LFXP10	—	375	—	338	—	304	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	LFXP10	1.19	—	1.19	—	1.19	—	ns
t_{SKEW_PRI}	Primary Clock Skew within an I/O Bank	LFXP10	—	250	—	300	—	350	ps

1. General timing numbers based on LVCMOS 2.5, 12mA.
2. DDR timing numbers based on SSTL.

Timing v.0.04

Figure 3-6. DDR Timings



LatticeXP Internal Timing Parameters[1]

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.23	—	0.28	—	0.33	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.47	—	0.56	—	0.67	ns
t_{LSR_PFU}	Set/Reset to output of PFU	—	0.48	—	0.57	—	0.69	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) input setup time		—		—		—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) input hold time		—		—		—	ns
t_{SUD_PFU}	Clock to D input setup time		—		—		—	ns
t_{HD_PFU}	Clock to D input hold time		—		—		—	ns
t_{CK2Q_PFU}	Clock to Q delay, D-type register configuration	—	0.36	—	0.43	—	0.52	ns
t_{LE2Q_PFU}	Clock to Q delay latch configuration	—	0.41	—	0.50	—	0.60	ns
t_{LD2Q_PFU}	D to Q throughput delay when latch is enabled	—	0.45	—	0.55	—	0.65	ns
PFU Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output	—	0.36	—	0.43	—	0.52	ns
t_{SUDATA_PFU}	Data Setup Time		—		—		—	ns
t_{HDATA_PFU}	Data Hold Time		—		—		—	ns
t_{SUADDR_PFU}	Address Setup Time		—		—		—	ns
t_{HADDR_PFU}	Address Hold Time		—		—		—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time		—		—		—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time		—		—		—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay	—	0.57	—	0.67	—	0.80	ns
t_{OUT_PIO}	Output Buffer Delay	—	1.58	—	1.90	—	2.22	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	—	3.70	—	4.44	—	5.33	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	—	0.63	—	0.76	—	0.91	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.97	—	1.16	—	1.39	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	—	-0.02	—	-0.03	—	-0.03	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	—	0.13	—	0.16	—	0.19	ns
t_{SULSR_PIO}	Set/Reset Setup Time		—		—		—	ns
t_{HLSR_PIO}	Set/Reset Hold Time		—		—		—	ns
EBR Timing								
t_{CO_EBR}	Clock to output from Address or Data	—	3.80	—	4.55	—	5.47	ns
t_{COO_EBR}	Clock to output from EBR output Register	—		—		—		ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.35	—	-0.42	—	-0.50	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.42	—	0.51	—	0.61	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.35	—	-0.42	—	-0.50	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.42	—	0.51	—	0.61	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.25	—	-0.30	—	-0.36	—	ns

LatticeXP Internal Timing Parameters[1] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HWREN_EBR}	Hold Write/Read Enable to PFU Memory	0.33	—	0.40	—	0.48	—	ns
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register	0.14	—	0.16	—	0.19	—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register	-0.12	—	-0.14	—	-0.17	—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register	—	0.85	—	1.02	—	1.22	ns
PLL Parameters								
t_{RSTREC}	Reset Recovery to Rising Clock	—		—		—		ns
t_{RSTSU}	Reset Signal Setup Time	—		—		—		ns
t_{RSTW}	Reset Signal Pulse Width	—		—		—		ns

1. Internal parameters are characterized but not tested on every device.

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Timing Diagrams

PFU Timing Diagrams

Figure 3-7. Slice Single/Dual Port Write Cycle Timing

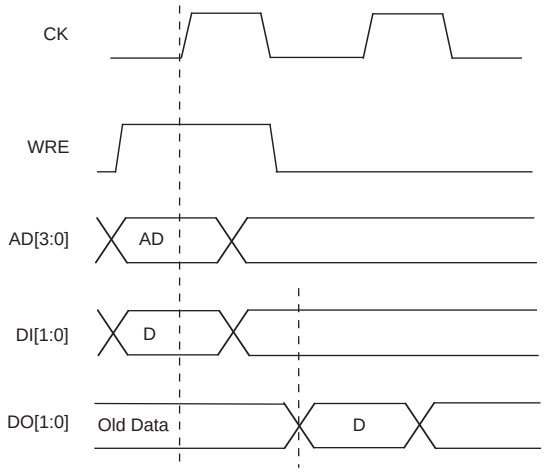
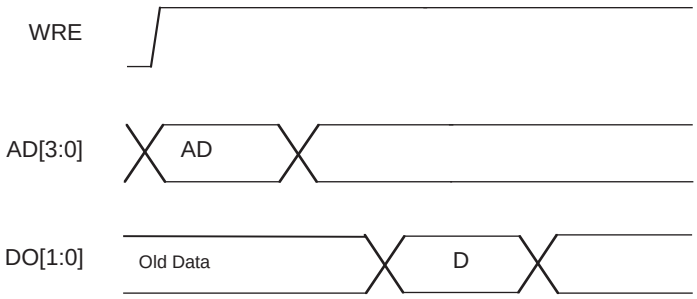
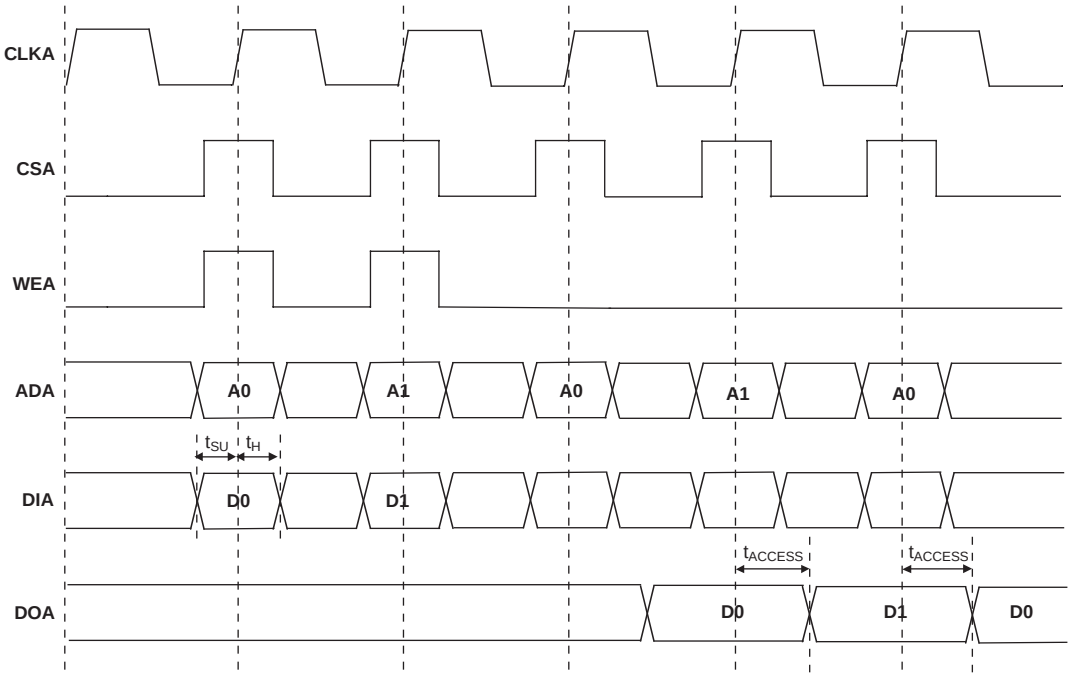


Figure 3-8. Slice Single /Dual Port Read Cycle Timing



EBR Memory Timing Diagrams

Figure 3-9. Read Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-10. Read Mode with Input and Output Registers

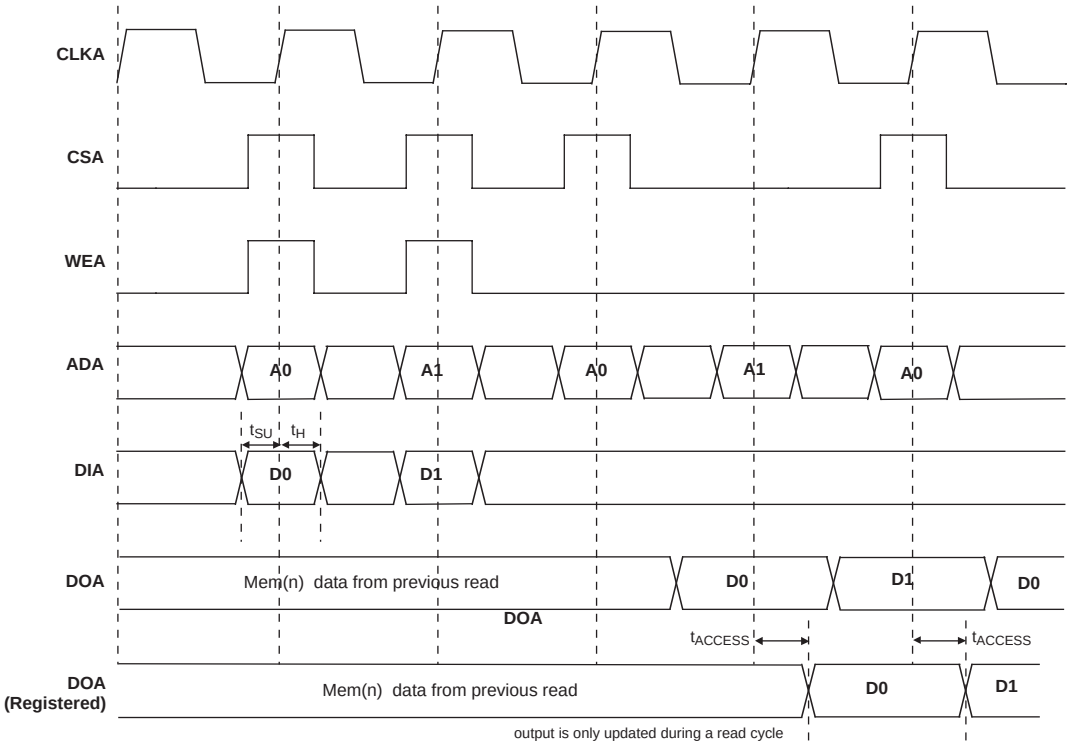
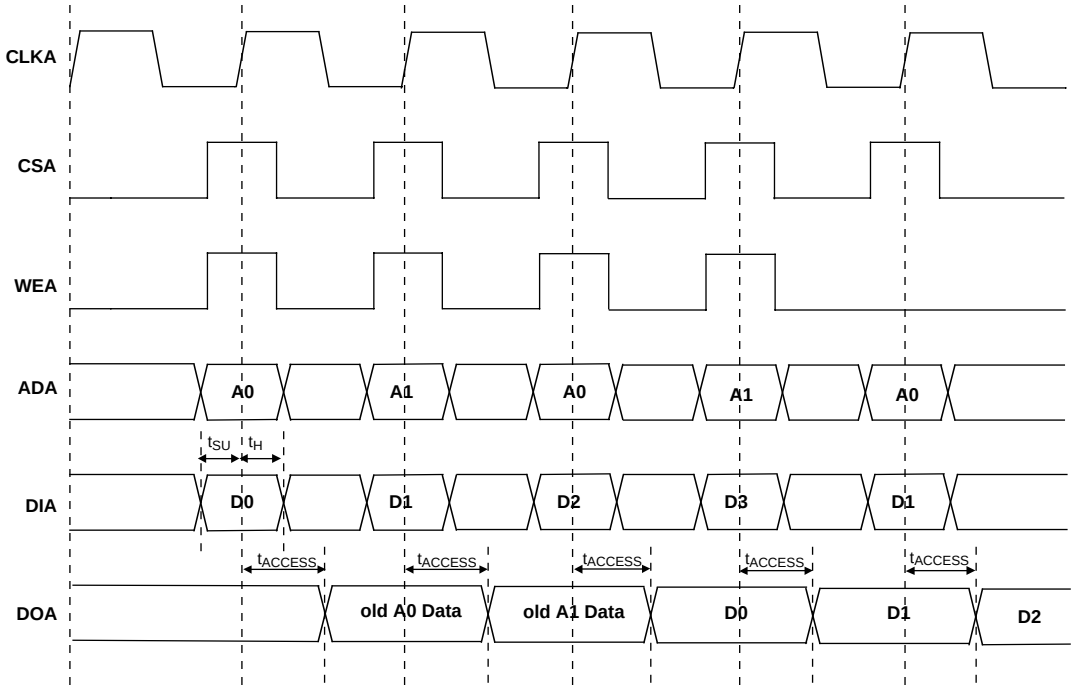
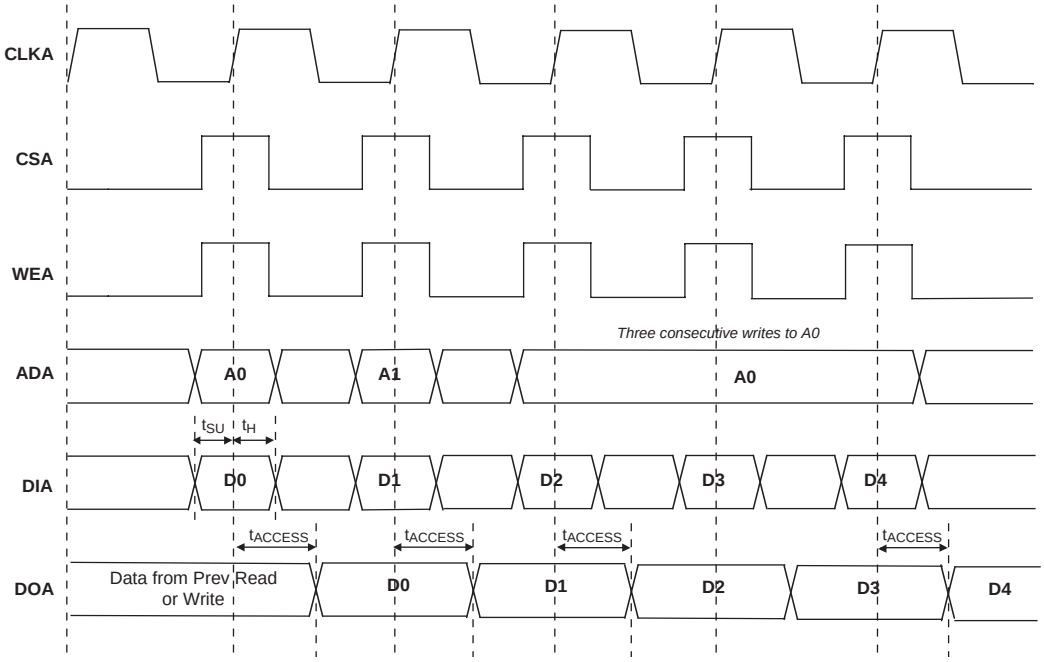


Figure 3-11. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-12. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeXP Family Timing Adders[1]

Over Recommended Operating Conditions

Buffer Type	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Adjusters								
LVDS25	LVDS 2.5	—	0.4	—	0.4	—	0.4	ns
LVDS25	LVDS 2.5 Emulated	—	0.5	—	0.5	—	0.5	ns
BLVDS25	BLVDS 2.5	—	0.5	—	0.5	—	0.5	ns
LVPECL33	LVPECL 3.3	—	0.6	—	0.6	—	0.6	ns
HSTL18_I	HSTL_18 class I	—	0.4	—	0.4	—	0.4	ns
HSTL18_II	HSTL_18 class II	—	0.4	—	0.4	—	0.4	ns
HSTL18_III	HSTL_18 class III	—	0.4	—	0.4	—	0.4	ns
HSTL18D_I	Differential HSTL 18 class I	—	0.4	—	0.4	—	0.4	ns
HSTL18D_II	Differential HSTL 18 class II	—	0.4	—	0.4	—	0.4	ns
HSTL18D_III	Differential HSTL 18 class III	—	0.4	—	0.4	—	0.4	ns
HSTL15_I	HSTL_15 class I	—	0.5	—	0.5	—	0.5	ns
HSTL15_III	HSTL_15 class III	—	0.5	—	0.5	—	0.5	ns
HSTL15D_I	Differential HSTL 15 class I	—	0.5	—	0.5	—	0.5	ns
HSTL15D_III	Differential HSTL 15 class III	—	0.5	—	0.5	—	0.5	ns
SSTL33_I	SSTL_3 class I	—	0.6	—	0.6	—	0.6	ns
SSTL33_II	SSTL_3 class II	—	0.6	—	0.6	—	0.6	ns
SSTL33D_I	Differential SSTL_3 class I	—	0.6	—	0.6	—	0.6	ns
SSTL33D_II	Differential SSTL_3 class II	—	0.6	—	0.6	—	0.6	ns
SSTL25_I	SSTL_2 class I	—	0.5	—	0.5	—	0.5	ns
SSTL25_II	SSTL_2 class II	—	0.5	—	0.5	—	0.5	ns
SSTL25D_I	Differential SSTL_2 class I	—	0.5	—	0.5	—	0.5	ns
SSTL25D_II	Differential SSTL_2 class II	—	0.5	—	0.5	—	0.5	ns
SSTL18_I	SSTL_18 class I	—	0.5	—	0.5	—	0.5	ns
SSTL18D_I	Differential SSTL_18 class I	—	0.5	—	0.5	—	0.5	ns
LVTTL33	LVTTL 3.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS33	LVCMOS 3.3	—	0.3	—	0.3	—	0.3	ns
LVCMOS25	LVCMOS 2.5	—	0.0	—	0.0	—	0.0	ns
LVCMOS18	LVCMOS 1.8	—	0.1	—	0.1	—	0.1	ns
LVCMOS15	LVCMOS 1.5	—	0.1	—	0.1	—	0.1	ns
LVCMOS12	LVCMOS 1.2	—	0.1	—	0.1	—	0.1	ns
PCI33	PCI 3.3	—	0.3	—	0.3	—	0.3	ns
Output Adjusters								
LVDS25	LVDS 2.5	—	0.1	—	0.1	—	0.1	ns
LVDS25E	LVDS 2.5 Emulated	—	0.3	—	0.3	—	0.3	ns
BLVDS25	BLVDS 2.5	—	0.3	—	0.3	—	0.3	ns
LVPECL33	LVPECL 3.3	—	0.1	—	0.1	—	0.1	ns
HSTL18_I	HSTL_18 class I	—	0.1	—	0.1	—	0.1	ns
HSTL18_II	HSTL_18 class II	—	0.1	—	0.1	—	0.1	ns
HSTL18_III	HSTL_18 class III	—	0.2	—	0.2	—	0.2	ns
HSTL18D_I	Differential HSTL 18 class I	—	0.1	—	0.1	—	0.1	ns

LatticeXP Family Timing Adders[1] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-5		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
HSTL18D_II	Differential HSTL 18 class II	—	-0.1	—	-0.1	—	-0.1	ns
HSTL18D_III	Differential HSTL 18 class III	—	0.2	—	0.2	—	0.2	ns
HSTL15_I	HSTL_15 class I	—	0.2	—	0.2	—	0.2	ns
HSTL15_III	HSTL_15 class III	—	0.2	—	0.2	—	0.2	ns
HSTL15D_I	Differential HSTL 15	—	0.2	—	0.2	—	0.2	ns
HSTL15D_III	Differential HSTL 15 class III	—	0.2	—	0.2	—	0.2	ns
SSTL33_I	SSTL_3 class I	—	0.1	—	0.1	—	0.1	ns
SSTL33_II	SSTL_3 class II	—	0.3	—	0.3	—	0.3	ns
SSTL33D_I	Differential SSTL_3	—	0.1	—	0.1	—	0.1	ns
SSTL33D_II	Differential SSTL_3 class II	—	0.3	—	0.3	—	0.3	ns
SSTL25_I	SSTL_2 class I	—	-0.1	—	-0.1	—	-0.1	ns
SSTL25_II	SSTL_2 class II	—	0.3	—	0.3	—	0.3	ns
SSTL25D_I	Differential SSTL_25 class I	—	-0.1	—	-0.1	—	-0.1	ns
SSTL25D_II	Differential SSTL_25 class II	—	0.3	—	0.3	—	0.3	ns
SSTL18_I	SSTL_2 class I	—	0.1	—	0.1	—	0.1	ns
SSTL18D_I	Differential SSTL_2	—	0.1	—	0.1	—	0.1	ns
LVTTL_4mA	LVTTL 4mA drive	—	0.8	—	0.8	—	0.8	ns
LVTTL_8mA	LVTTL 8mA drive	—	0.5	—	0.5	—	0.5	ns
LVTTL_12mA	LVTTL 12mA drive	—	0.3	—	0.3	—	0.3	ns
LVTTL_16mA	LVTTL 16mA drive	—	0.4	—	0.4	—	0.4	ns
LVTTL_20mA	LVTTL 20mA drive	—	0.3	—	0.3	—	0.3	ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive	—	0.8	—	0.8	—	0.8	ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive	—	0.5	—	0.5	—	0.5	ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive	—	0.3	—	0.3	—	0.3	ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive	—	0.4	—	0.4	—	0.4	ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive	—	0.3	—	0.3	—	0.3	ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive	—	0.7	—	0.7	—	0.7	ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive	—	0.4	—	0.4	—	0.4	ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive	—	0.0	—	0.0	—	0.0	ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive	—	0.2	—	0.2	—	0.2	ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive	—	0.4	—	0.4	—	0.4	ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive	—	0.6	—	0.6	—	0.6	ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive	—	0.4	—	0.4	—	0.4	ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	—	0.2	—	0.2	—	0.2	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive	—	0.2	—	0.2	—	0.2	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	—	0.6	—	0.6	—	0.6	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	—	0.2	—	0.2	—	0.2	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	—	0.4	—	0.4	—	0.4	ns
LVCMOS12_4mA	LVCMOS 1.2 4mA drive	—	0.4	—	0.4	—	0.4	ns
LVCMOS12_8mA	LVCMOS 1.2 8mA drive	—	0.4	—	0.4	—	0.4	ns
PCI	PCI 3.3	—	0.3	—	0.3	—	0.3	ns

1. General timing numbers based on LVCMOS 2.5, 12mA.

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		25	—	375	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		25	—	375	MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)		0.195	—	187.5	MHz
f_{VCO}	PLL VCO Frequency		420	—	750	MHz
f_{PFD}	Phase Detector Input Frequency		25	—	—	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle elected[3]	45	50	55	%
t_{PH}[4]	Output Phase Accuracy		—	—		UI
t_{OPJIT}[1]	Output Clock Period Jitter	Fout >= 100MHz	—	—	+/- 125	ps
		Fout < 100MHz	—	—	0.02	UIPP
t_{SK}	Input Clock to Output Clock skew	Divider ratio = integer	—	—	+/- 200	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	1	—	—	ns
t_{LOCK}[2]	PLL Lock-in Time		—	—	150	us
t_{PA}	Programmable Delay Unit		100	250	400	ps
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 200	ps
t_{FBKDLY}	External Feedback Delay		—	—	10	ns
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	—	ns
t_{RST}	RST Pulse Width		10	—		ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

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LatticeXP sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup time to CCLK	7	—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK	2	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	-	—	ns
t_{SUCS}	CS[0:1] Setup time to CCLK	7	—	ns
t_{HCS}	CS[0:1] Hold Time to CCLK	2	—	ns
t_{SUWD}	Write Signal Setup time to CCLK	7	—	ns
t_{HWD}	Write Signal Hold time to CCLK	2	—	ns
t_{DCB}	CCLK to BUSY Delay time	—	12	ns
t_{CORD}	Clock to out for read Data	—	12	ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave Clock Minimum High Pulse	6	—	ns
t_{BSCL}	Byte Slave Clock Minimum Low Pulse	6	—	ns
t_{BSCYC}	Byte Slave Clock Cycle Time	15	—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI (Data In) Setup time to CCLK	7	—	ns
t_{HSCDI}	DI (Data In) Hold Time to CCLK	2	—	ns
t_{CODO}	Clock to Dout in Flowthrough Mode	—	12	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave Clock Minimum High Pulse	6	—	ns
t_{SSCL}	Serial Slave Clock Minimum Low Pulse	6	—	ns
sysCONFIG POR, Initialization and Wake Up				
t_{ICFG}	Minimum Vcc to INIT high	—	50	ms
t_{VMC}	Time from tICFG to valid Master Clock	—	2	us
t_{PRGMRJ}	Program Pin Pulse Rejection	—	10	ns
t_{PRGM}	PROGRAMB Low time to start Configuration	25	—	ns
t_{DINIT}	INIT Low Time	—	1	ms
$t_{DPPINIT}$	Delay time from PROGRAMB Low to INIT Low	—	37	ns
t_{DINITD}	Delay time from PROGRAMB Low to DONE Low	—	37	ns
t_{IODISS}	User IO disable from PROGRAMB low	—	25	ns
t_{IOENSS}	User IO enabled time from CCLK edge during wake up sequence	—	25	ns
t_{MWC}	Additional Wake Master Clock Signals after Done Pin High	120	—	cycles
Configuration Master Clock (CCLK)				
Frequency		Selected Value - 30%	Selected Value + 30%	MHz
Duty Cycle		40	60	%

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JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

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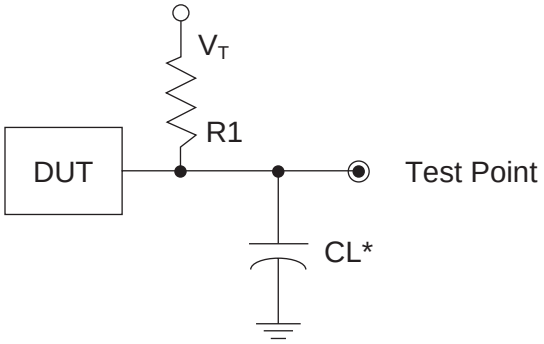
Switching Test Conditions

Figure 3-13 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Figure 3-4.

Figure 3-13. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	0pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	188	0pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)			V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

LatticeXP Family Data Sheet Pinout Information

February 2005 Advance Data Sheet

Signal Descriptions

Signal Name	I/O	Descriptions
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal. (Active low). Any I/O pin can be configured to be GSRN.
NC	—	No connect.
GND	—	GND - Ground. Dedicated Pins.
V_{CC}	—	VCC - The power supply pins for core logic. Dedicated Pins.
V_{CCAUX}	—	V_{CCAUX} - The Auxiliary power supply pin. It powers all the differential and referenced input buffers. Dedicated Pins.
V_{CCIOx}	—	V_{CCIO} - The power supply pins for I/O bank x. Dedicated Pins.
$V_{REF1(x)}$, $V_{REF2(x)}$	—	The reference supply pins for I/O bank x. Any pin in a bank can be assigned as reference supply pin.
PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_PLL[T, C]_IN_A	—	Reference clock (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_OUT_A	—	Reference clock (PLL) output Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL[T, C]_FB_A	—	Optional feedback (PLL) input Pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A, B, C...at each side.
[LOC][num]_PLL_RST	—	PLL Reset (M register) input Pads: ULM, LLM, URM, LRM, num = row from center.
PCLK[T, C]_[n:0]_[3:0]	—	Primary Clock Pads, T = true and C = complement, n per side, indexed by bank and 0,1, 2, 3 within bank.
[LOC]DQS[num]	—	DQS input Pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = Ball function number. Any pad can be configured to be DQS output.
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.

Signal Descriptions (Continued)

Signal Name	I/O	Descriptions
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
V_{CCJ}	—	V_{CCJ} - The power supply pin for JTAG Test Access Port.
Configuration Pads (used during sysCONFIG)		
CFG[1:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITB. During configuration, a pull-up is enabled. After configuration, these are user-programmable I/O pins.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY	I/O	Generally not used. After configuration it is a user-programmable I/O pin.
CSN	I	sysCONFIG chip select (Active low). During configuration, a pull-up is enabled. After configuration it is user a programmable I/O pin.
CS1N	I	sysCONFIG chip select (Active Low). During configuration, a pull-up is enabled. After configuration it is user programmable I/O pin
WRITEN	I	Write Data on Parallel port (Active low). After configuration it is a user programmable I/O pin
D[7:0]	I/O	sysCONFIG Port Data I/O. After configuration these are user programmable I/O pins.
DOUT, CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port. After configuration, it is a user-programmable I/O pin.
DI	I	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. After configuration it is a user-programmable I/O pin.
RESERVE	I	For future enhancement. This pin must be tied high.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO within PIC	Polarity	DDR Strobe (DQS) and Data (DQ) Pins
P[Edge] [n-4]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-3]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n-1]	A	True	DQ
P[Edge] [n]			
	B	Complement	DQ
P[Edge] [n+1]	A	True	[Edge]DQSn
	B	Complement	DQ
P[Edge] [n+2]	A	True	DQ
	B	Complement	DQ
P[Edge] [n+3]	A	True	DQ
	B	Complement	DQ

Notes:
1. “n” is a row/column PIC number.
2. The DDR interface is designed for memories that support one DQS strobe per eight bits of data. In some packages, all the potential DDR data (DQ) pins may not be available.
3. The definition of the PIC numbering is provided in the Signal Names column of the Signal Descriptions table in this data sheet.

LFXP10 Pin Information Summary[1]

Pin Type		Package	
		256 fpBGA	388 fpBGA
Single Ended User I/O		188	244
Differential Pair User I/O		76	104
Configuration	Dedicated	16	16
	Muxed	13	13
TAP		4	4
Dedicated (total without supplies)		11	11
V_{CC}		8	14
V_{CCAUX}		4	4
V_{CCPLL}		2	2
V_{CCIO}	Bank0	2	5
	Bank1	2	5
	Bank2	2	4
	Bank3	2	4
	Bank4	2	5
	Bank5	2	5
	Bank6	2	4
	Bank7	2	4
GND		24	50
GND_{PLL}		2	2
NC		0	24
Single Ended/ Differential I/O per Bank	Bank0	26/13	33/16
	Bank1	26/13	33/16
	Bank2	21/10	28/14
	Bank3	21/10	28/14
	Bank4	26/13	33/16
	Bank5	26/13	33/16
	Bank6	21/10	28/14
	Bank7	21/10	28/14
V_{CCJ}		1	1

1. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.

LFXP10 Power Supply and NC Connections

Signals	256 fpBGA	388 fpBGA
V_{CC}	D4, D13, E5, E12, M5, M12, N4, N13,	H9, J8, J15, K8, K15, L8, L15, M8, M15, N8, N15, P8, P15, R9
V_{CCIO0}	F7, F8	G8, G9, G10, G11, H8
V_{CCIO1}	F9, F10	G12, G13, G14, G15, H15
V_{CCIO2}	G11, H11	H16, J16, K16, L16
V_{CCIO3}	J11, K11	M16,N16, P16, R16
V_{CCIO4}	L9, L10	R15, T12, T13, T14, T15
V_{CCIO5}	L7, L8	R8, T8, T9, T10, T11
V_{CCIO6}	J6, K6	M7, N7, P7, R7
V_{CCIO7}	G6, H6	H7, J7, K7, L7
V_{CCJ}	D16	E20
V_{CCP0}	H4	M2
V_{CCP1}	J12	M21
V_{CCAUX}	E4, E13, M4, M13,	G7, G16, T7, T16,
GND[1]	A1, A16, F6, F11, G7, G8, G9, G10, H5, H7, H8, H9, H10, J7, J8, J9, J10, J13, K7, K8, K9, K10, L11, L6, T1, T16	A1, A22, H10, H11, H12, H13, H14, J9, J10, J11, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N1, N9, N10, N11, N12, N13, N14, N22, P9, P10, P11, P12, P13, P14, R10, R11, R12, R13, R14, AB1, AB22,
NC[2]	—	C2, C15, C16, C17, D4, D5, D6, D7, D16, D17, E4, E19, W3, W4, W7, W17, W18, W19, W20, Y3, Y15, Y16, AA1, AA2

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
VCCAUX	7				
PROGRAMN	7	PROGRAMN		C2	F4
CCLK	7	CCLK		C1	G4
GND	7				
PL2A	7		T		D2
GNDIO7	7				
PL2B	7		C		D1
PL3A	7	LUM0_PLLT_FB_A	T	D2	E2
PL3B	7	LUM0_PLLC_FB_A	C	D3	E3
PL4A	7		T		F3
PL4B	7		C		F2
VCCIO7	7				
PL5A	7			D1	H4
PL6B	7	VREF1_7		E2	H3
GNDIO7	7				
PL7A	7	LDQS7	T	E1	G3
PL7B	7		C	F1	G2
PL8A	7		T	E3	F1
PL8B	7		C	F4	E1
PL9A	7		T	F3	J4
VCCIO7	7				
PL9B	7		C	F2	K4
PL11A	7		T		G1
GNDIO7	7				
PL11B	7		C	G1	H2
PL12A	7	LUM0_PLLT_IN_A	T	G3	J2
PL12B	7	LUM0_PLLC_IN_A	C	G2	H1
VCC	7				
PL13A	7		T	H1	J1
PL13B	7		C	H2	K2
VCCIO7	7				
PL14A	7	VREF2_7		G4	K3
PL15B	7			G5	J3
GNDIO7	7				
PL16A	7	LDQS16	T	J1	K1
PL16B	7		C	J2	L2
PL17A	7		T		L3
PL17B	7		C		L4
PL18A	7		T	H3	L1
VCCIO7	7				
PL18B	7		C	J3	M1
VCCP0	7			H4	M2
GNDP0	6			H5	N1

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
PL19A	6		T		M3
VCCIO6	6				
PL19B	6		C		M4
PL20A	6	PCLKT6_0	T	K1	P1
PL20B	6	PCLKC6_0	C	K2	N2
PL21A	6		T		R1
PL21B	6		C		P2
GNDIO6	6				
PL22A	6			J4	N3
PL23B	6	VREF1_6		J5	N4
VCCIO6	6				
PL24A	6	LDQS24	T	L1	T1
GND	6				
PL24B	6		C	L2	R2
PL25A	6	LLM0_PLLT_IN_A	T	M1	U1
PL25B	6	LLM0_PLLC_IN_A	C	M2	T2
PL26A	6		T	K3	V1
GNDIO6	6				
PL26B	6		C	L3	U2
PL28A	6		T	L4	W1
VCCIO6	6				
PL28B	6		C		V2
PL29A	6		T	K4	P3
PL29B	6		C	K5	P4
VCC	6				
PL30A	6		T		Y1
PL30B	6		C		W2
GNDIO6	6				
PL31A	6	VREF2_6		N1	R3
PL32B	6			N2	R4
VCCIO6	6				
PL33A	6	LDQS33	T	P1	T3
PL33B	6		C	P2	T4
PL34A	6	LLM0_PLLT_FB_A	T	L5	V4
PL34B	6	LLM0_PLLC_FB_A	C	M6	V3
PL35A	6		T	M3	U4
GNDIO6	6				
PL35B	6		C	N3	U3
GND	6				
VCC	6				
VCCAUX	6				
RESERVE	5	RESERVE		P4	W5
	5				
INITN	5	INITN		P3	Y2

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
GND	5				
VCC	5				
PB2A	5				W6
GNDIO5	5				
PB3A	5		T		Y4
PB3B	5		C		Y5
PB4A	5		T		AB2
PB4B	5		C		AA3
VCCIO5	5				
PB5A	5		T		AB3
PB5B	5		C		AA4
PB6A	5		T	R4	W8
PB6B	5		C	N5	W9
GNDIO5	5				
PB7A	5	VREF1_5	T	P5	AB4
PB7B	5		C	R1	AA5
PB8A	5			N6	AB5
PB9B	5			M7	Y6
VCCIO5	5				
PB10A	5	BDQS10	T	R2	AA6
PB10B	5		C	T2	AB6
PB11A	5		T	R3	Y9
PB11B	5		C	T3	Y10
GNDIO5	5				
PB12A	5		T	T4	AA7
PB12B	5	VREF2_5	C	R5	AB7
PB13A	5		T	N7	Y7
PB13B	5		C	M8	AA8
VCCIO5	5				
PB14A	5		T	T5	AB8
PB14B	5		C	P6	Y8
PB15A	5		T	T6	AB9
PB15B	5		C	R6	AA9
GNDIO5	5				
PB16A	5			P7	W10
PB17B	5			N8	W11
PB18A	5	BDQS18	T	R7	AB10
PB18B	5		C	T7	AA10
VCCIO5	5				
PB19A	5		T	P8	AA11
PB19B	5		C	T8	AB11
PB20A	5		T	R8	Y11
PB20B	5		C	T9	Y12
GND	5				

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
VCC	5				
GND	4				
VCC	4				
PB21A	4		T	R9	AB12
GNDIO4	4				
PB21B	4		C	P9	AA12
PB22A	4	PCLKT4_0	T	T10	AB13
PB22B	4	PCLKC4_0	C	T11	AA13
PB23A	4		T	R10	AA14
VCCIO4	4				
PB23B	4		C	P10	AB14
PB24A	4			N9	W12
PB25B	4			M9	W13
PB26A	4	BDQS26	T	R12	AA15
GNDIO4	4				
PB26B	4	VREF1_4	C	T12	AB15
PB27A	4		T	P13	AA16
PB27B	4		C	R13	AB16
PB28A	4		T	M11	Y17
VCCIO4	4				
PB28B	4		C	N11	AA17
PB29A	4		T	N10	Y13
PB29B	4		C	M10	Y14
PB30A	4		T	T13	AB17
GNDIO4	4				
PB30B	4		C	P14	Y18
PB31A	4	VREF2_4	T	R11	AA18
PB31B	4		C	P12	AB18
PB32A	4			T14	Y19
VCCIO4	4				
PB33B	4			R14	AB19
PB34A	4	BDQS34	T	P11	AA19
PB34B	4		C	N12	Y20
PB35A	4		T	T15	W14
GNDIO4	4				
PB35B	4		C	R15	W15
PB36A	4		T		AB20
PB36B	4		C		AA20
PB37A	4		T		AB21
VCCIO4	4				
PB37B	4		C		AA21
PB38A	4		T		AA22
PB38B	4		C		Y21
PB39A	4				W16

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
GND	4				
VCC	4				
	4				
	4				
VCCAUX	4				
	3				
GND	3				
VCC	3				
PR35B	3		C		T20
GNDIO3	3				
PR35A	3		T		T19
PR34B	3	RLM0_PLLC_FB_A	C	P15	U19
PR34A	3	RLM0_PLLT_FB_A	T	N15	U20
PR33B	3		C	P16	V19
PR33A	3	RDQS33	T	R16	V20
VCCIO3	3				
PR32B	3			M15	R19
PR31A	3	VREF1_3		N14	R20
GNDIO3	3				
PR30B	3		C		W21
PR30A	3		T		Y22
GND	3				
PR29B	3		C	M14	P19
PR29A	3		T	L13	P20
PR28B	3		C	L15	V21
VCCIO3	3				
PR28A	3		T	L14	W22
PR26B	3		C		U21
GNDIO3	3				
PR26A	3		T	L12	V22
PR25B	3	RLM0_PLLC_IN_A	C	M16	T21
PR25A	3	RLM0_PLLT_IN_A	T	N16	U22
PR24B	3		C	K14	R21
VCC	3				
PR24A	3	RDQS24	T	K15	T22
VCCIO3	3				
PR23B	3			K12	N19
PR22A	3	VREF2_3		K13	N20
GNDIO3	3				
PR21B	3		C	L16	R22
PR21A	3		T	K16	P22
PR20B	3		C		P21
PR20A	3		T		N21
PR19B	3		C	J15	M20

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
VCCIO3	3				
PR19A	3		T	J14	M19
GNDP1	3			J13	N22
VCCP1	2			J12	M21
PR18B	2		C		M22
GNDIO2	2				
PR18A	2		T		L22
PR17B	2	PCLKC2_0	C	J16	K22
PR17A	2	PCLKT2_0	T	H16	K21
PR16B	2		C	H13	L19
PR16A	2	RDQS16	T	H12	K20
VCCIO2	2				
PR15B	2			H15	L20
PR14A	2	VREF1_2		H14	L21
GNDIO2	2				
PR13B	2		C	G15	J22
PR13A	2		T	G14	J21
GND	2				
PR12B	2	RUM0_PLLC_IN_A	C	G16	H22
PR12A	2	RUM0_PLLT_IN_A	T	F16	H21
PR11B	2		C	G13	K19
VCCIO2	2				
PR11A	2		T		J19
PR9B	2		C		J20
GNDIO2	2				
PR9A	2		T		H20
PR8B	2		C	G12	H19
PR8A	2		T	F13	G19
PR7B	2		C	B16	G22
PR7A	2	RDQS7	T	C16	G21
VCCIO2	2				
PR6B	2			F15	F20
PR5A	2	VREF2_2		E15	G20
GNDIO2	2				
PR4B	2		C	F14	F22
PR4A	2		T	E14	F21
PR3B	2	RUM0_PLLC_FB_A	C	D15	E22
PR3A	2	RUM0_PLLT_FB_A	T	C15	E21
PR2B	2		C		D22
VCCIO2	2				
PR2A	2		T		D21
VCC	2				
VCCAUX	2				
TDO	2	TDO		E16	F19

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
VCCJ	2			D16	E20
TDI	1	TDI		D14	D20
TMS	1	TMS		C14	D19
TCK	1	TCK		B14	D18
GND	1				
VCC	1				
PT39A	1				C18
GNDIO1	1				
PT38B	1		C		C19
PT38A	1		T		C20
PT37B	1		C		C21
PT37A	1		T		C22
VCCIO1	1				
PT36B	1		C		B22
PT36A	1		T		A21
PT35B	1		C	A15	D15
PT35A	1		T	B15	D14
GNDIO1	1				
PT34B	1	VREF1_1	C	D12	B21
PT34A	1	TDQS34	T	C11	A20
PT33B	1			A14	B20
PT32A	1			B13	A19
VCCIO1	1				
PT31B	1		C	F12	B19
PT31A	1		T	E11	A18
PT30B	1		C	A13	C14
PT30A	1	D0	T	C13	C13
GNDIO1	1				
PT29B	1	D1	C	C10	B18
PT29A	1	VREF2_1	T	E10	A17
PT28B	1		C	A12	B17
PT28A	1	D2	T	B12	A16
VCCIO1	1				
PT27B	1	D3	C	C12	B16
PT27A	1		T	A11	A15
PT26B	1		C	B11	B15
PT26A	1	TDQS26	T	D11	A14
GNDIO1	1				
PT25B	1			B9	D13
PT24A	1	D4		D9	D12
PT23B	1		C	A10	B14
PT23A	1	D5	T	B10	A13
VCCIO1	1				
PT22B	1	D6	C	D10	B13

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
PT22A	1		T	A9	A12
PT21B	1	D7	C	C9	B12
PT21A	1		T	C8	C12
GND	1				
VCC	1				
GND	0				
VCC	0				
PT20B	0	BUSY	C	E9	C11
GNDIO0	0				
PT20A	0	CS1N	T	B8	B11
PT19B	0	PCLKC0_0	C	A8	A11
PT19A	0	PCLKT0_0	T	A7	A10
PT18B	0		C	B7	B10
VCCIO0	0				
PT18A	0	TDQS18	T	C7	B9
PT17B	0			E8	D11
PT16A	0	DOUT		D8	D10
PT15B	0		C	A6	A9
GNDIO0	0				
PT15A	0	WRITEN	T	C6	C8
PT14B	0		C	E7	B8
PT14A	0	VREF1_0	T	D7	A8
PT13B	0		C	A5	C7
VCCIO0	0				
PT13A	0	DI	T	B5	A7
PT12B	0		C	A4	B7
PT12A	0	CSN	T	B6	C6
PT11B	0		C	E6	C10
GNDIO0	0				
PT11A	0		T	D6	C9
PT10B	0	VREF2_0	C	D5	A6
PT10A	0	TDQS10	T	A3	B6
PT9B	0			B3	A5
VCCIO0	0				
PT8A	0			B2	B5
PT7B	0		C	A2	C5
PT7A	0		T	B1	A4
PT6B	0		C	F5	D9
GNDIO0	0				
PT6A	0		T	C5	D8
PT5B	0		C		B4
PT5A	0		T		A2
PT4B	0		C		A3
VCCIO0	0				

LFXP10 Logic Signal Connections: 256 fpBGA and 388 fpBGA (Continued)

Ball Function	Bank	Dual Function	LVDS	256-Ball fpBGA	388-Ball fpBGA
PT4A	0		T		B3
PT3B	0		C		C4
PT3A	0		T		C3
PT2A	0				D3
GND	0				
VCC	0				
CFG0	0	CFG0		C4	C1
CFG1	0	CFG1		B4	B2
DONE	0	DONE		C3	B1

LatticeXP Family Data Sheet Ordering Information

February 2005 **Advance Data Sheet**

Part Number Description

LFXP XX – X – X XXXXXX X

Device Family
Lattice XP FPGA

Logic Capacity
3K LUTs = 3
6K LUTs = 6
10K LUTs = 10
15K LUTs = 15
20K LUTs = 20

Supply Voltage
C = 1.8V/2.5V/3.3V
E = 1.2V

Note: Parts dual marked per table below.

Grade
C = Commercial
I = Industrial

Package
T100 = 100-pin TQFP
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F388 = 388-ball fpBGA
F484 = 484-ball fpBGA

Speed
3 = Slowest
4
5 = Fastest

Ordering Information

Note: LatticeXP devices are dual marked. For example, the commercial speed grade LFXP10E-4F256C is also marked with industrial grade -3I (LFXP10E-3F256I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Commercial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208C	136	-3	PQFP	208	COM	3.1K
LFXP3C-4Q208C	136	-4	PQFP	208	COM	3.1K
LFXP3C-5Q208C	136	-5	PQFP	208	COM	3.1K
LFXP3C-3T144C	100	-3	TQFP	144	COM	3.1K
LFXP3C-4T144C	100	-4	TQFP	144	COM	3.1K
LFXP3C-5T144C	100	-5	TQFP	144	COM	3.1K
LFXP3C-3T100C	62	-3	TQFP	100	COM	3.1K
LFXP3C-4T100C	62	-4	TQFP	100	COM	3.1K
LFXP3C-5T100C	62	-5	TQFP	100	COM	3.1K

Commercial (Cont.)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256C	188	-3	fpBGA	256	COM	5.8K
LFXP6C-4F256C	188	-4	fpBGA	256	COM	5.8K
LFXP6C-5F256C	188	-5	fpBGA	256	COM	5.8K
LFXP6C-3Q208C	142	-3	PQFP	208	COM	5.8K
LFXP6C-4Q208C	142	-4	PQFP	208	COM	5.8K
LFXP6C-5Q208C	142	-5	PQFP	208	COM	5.8K
LFXP6C-3T144C	100	-3	TQFP	144	COM	5.8K
LFXP6C-4T144C	100	-4	TQFP	144	COM	5.8K
LFXP6C-5T144C	100	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388C	244	-3	fpBGA	388	COM	9.7K
LFXP10C-4F388C	244	-4	fpBGA	388	COM	9.7K
LFXP10C-5F388C	244	-5	fpBGA	388	COM	9.7K
LFXP10C-3F256C	188	-3	fpBGA	256	COM	9.7K
LFXP10C-4F256C	188	-4	fpBGA	256	COM	9.7K
LFXP10C-5F256C	188	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484C	300	-3	fpBGA	484	COM	15.5K
LFXP15C-4F484C	300	-4	fpBGA	484	COM	15.5K
LFXP15C-5F484C	300	-5	fpBGA	484	COM	15.5K
LFXP15C-3F388C	268	-3	fpBGA	388	COM	15.5K
LFXP15C-4F388C	268	-4	fpBGA	388	COM	15.5K
LFXP15C-5F388C	268	-5	fpBGA	388	COM	15.5K
LFXP15C-3F256C	188	-3	fpBGA	256	COM	15.5K
LFXP15C-4F256C	188	-4	fpBGA	256	COM	15.5K
LFXP15C-5F256C	188	-5	fpBGA	256	COM	15.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484C	340	-3	fpBGA	484	COM	19.7K
LFXP20C-4F484C	340	-4	fpBGA	484	COM	19.7K
LFXP20C-5F484C	340	-5	fpBGA	484	COM	19.7K
LFXP20C-3F388C	268	-3	fpBGA	388	COM	19.7K
LFXP20C-4F388C	268	-4	fpBGA	388	COM	19.7K
LFXP20C-5F388C	268	-5	fpBGA	388	COM	19.7K
LFXP20C-3F256C	188	-3	fpBGA	256	COM	19.7K
LFXP20C-4F256C	188	-4	fpBGA	256	COM	19.7K
LFXP20C-5F256C	188	-5	fpBGA	256	COM	19.7K

Commercial (Cont.)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208C	136	-3	PQFP	208	COM	3.1K
LFXP3E-4Q208C	136	-4	PQFP	208	COM	3.1K
LFXP3E-5Q208C	136	-5	PQFP	208	COM	3.1K
LFXP3E-3T144C	100	-3	TQFP	144	COM	3.1K
LFXP3E-4T144C	100	-4	TQFP	144	COM	3.1K
LFXP3E-5T144C	100	-5	TQFP	144	COM	3.1K
LFXP3E-3T100C	62	-3	TQFP	100	COM	3.1K
LFXP3E-4T100C	62	-4	TQFP	100	COM	3.1K
LFXP3E-5T100C	62	-5	TQFP	100	COM	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256C	188	-3	fpBGA	256	COM	5.8K
LFXP6E-4F256C	188	-4	fpBGA	256	COM	5.8K
LFXP6E-5F256C	188	-5	fpBGA	256	COM	5.8K
LFXP6E-3Q208C	142	-3	PQFP	208	COM	5.8K
LFXP6E-4Q208C	142	-4	PQFP	208	COM	5.8K
LFXP6E-5Q208C	142	-5	PQFP	208	COM	5.8K
LFXP6E-3T144C	100	-3	TQFP	144	COM	5.8K
LFXP6E-4T144C	100	-4	TQFP	144	COM	5.8K
LFXP6E-5T144C	100	-5	TQFP	144	COM	5.8K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388C	244	-3	fpBGA	388	COM	9.7K
LFXP10E-4F388C	244	-4	fpBGA	388	COM	9.7K
LFXP10E-5F388C	244	-5	fpBGA	388	COM	9.7K
LFXP10E-3F256C	188	-3	fpBGA	256	COM	9.7K
LFXP10E-4F256C	188	-4	fpBGA	256	COM	9.7K
LFXP10E-5F256C	188	-5	fpBGA	256	COM	9.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484C	300	-3	fpBGA	484	COM	15.5K
LFXP15E-4F484C	300	-4	fpBGA	484	COM	15.5K
LFXP15E-5F484C	300	-5	fpBGA	484	COM	15.5K
LFXP15E-3F388C	268	-3	fpBGA	388	COM	15.5K
LFXP15E-4F388C	268	-4	fpBGA	388	COM	15.5K
LFXP15E-5F388C	268	-5	fpBGA	388	COM	15.5K
LFXP15E-3F256C	188	-3	fpBGA	256	COM	15.5K
LFXP15E-4F256C	188	-4	fpBGA	256	COM	15.5K
LFXP15E-5F256C	188	-5	fpBGA	256	COM	15.5K

Commercial (Cont.)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484C	340	-3	fpBGA	484	COM	19.7K
LFXP20E-4F484C	340	-4	fpBGA	484	COM	19.7K
LFXP20E-5F484C	340	-5	fpBGA	484	COM	19.7K
LFXP20E-3F388C	268	-3	fpBGA	388	COM	19.7K
LFXP20E-4F388C	268	-4	fpBGA	388	COM	19.7K
LFXP20E-5F388C	268	-5	fpBGA	388	COM	19.7K
LFXP20E-3F256C	188	-3	fpBGA	256	COM	19.7K
LFXP20E-4F256C	188	-4	fpBGA	256	COM	19.7K
LFXP20E-5F256C	188	-5	fpBGA	256	COM	19.7K

Industrial

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP3C-3Q208I	136	-3	PQFP	208	IND	3.1K
LFXP3C-4Q208I	136	-4	PQFP	208	IND	3.1K
LFXP3C-3T144I	100	-3	TQFP	144	IND	3.1K
LFXP3C-4T144I	100	-4	TQFP	144	IND	3.1K
LFXP3C-3T100I	62	-3	TQFP	100	IND	3.1K
LFXP3C-4T100I	62	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP6C-3F256I	188	-3	fpBGA	256	IND	5.8K
LFXP6C-4F256I	188	-4	fpBGA	256	IND	5.8K
LFXP6C-3Q208I	142	-3	PQFP	208	IND	5.8K
LFXP6C-4Q208I	142	-4	PQFP	208	IND	5.8K
LFXP6C-3T144I	100	-3	TQFP	144	IND	5.8K
LFXP6C-4T144I	100	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP10C-3F388I	244	-3	fpBGA	388	IND	9.7K
LFXP10C-4F388I	244	-4	fpBGA	388	IND	9.7K
LFXP10C-3F256I	188	-3	fpBGA	256	IND	9.7K
LFXP10C-4F256I	188	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP15C-3F484I	300	-3	fpBGA	484	IND	15.5K
LFXP15C-4F484I	300	-4	fpBGA	484	IND	15.5K
LFXP15C-3F388I	268	-3	fpBGA	388	IND	15.5K
LFXP15C-4F388I	268	-4	fpBGA	388	IND	15.5K
LFXP15C-3F256I	188	-3	fpBGA	256	IND	15.5K
LFXP15C-4F256I	188	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP20C-3F484I	340	-3	fpBGA	484	IND	19.7K
LFXP20C-4F484I	340	-4	fpBGA	484	IND	19.7K
LFXP20C-3F388I	268	-3	fpBGA	388	IND	19.7K
LFXP20C-4F388I	268	-4	fpBGA	388	IND	19.7K
LFXP20C-3F256I	188	-3	fpBGA	256	IND	19.7K
LFXP20C-4F256I	188	-4	fpBGA	256	IND	19.7K

Industrial (Cont.)

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP3E-3Q208I	136	-3	PQFP	208	IND	3.1K
LFXP3E-4Q208I	136	-4	PQFP	208	IND	3.1K
LFXP3E-3T144I	100	-3	TQFP	144	IND	3.1K
LFXP3E-4T144I	100	-4	TQFP	144	IND	3.1K
LFXP3E-3T100I	62	-3	TQFP	100	IND	3.1K
LFXP3E-4T100I	62	-4	TQFP	100	IND	3.1K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP6E-3F256I	188	-3	fpBGA	256	IND	5.8K
LFXP6E-4F256I	188	-4	fpBGA	256	IND	5.8K
LFXP6E-3Q208I	142	-3	PQFP	208	IND	5.8K
LFXP6E-4Q208I	142	-4	PQFP	208	IND	5.8K
LFXP6E-3T144I	100	-3	TQFP	144	IND	5.8K
LFXP6E-4T144I	100	-4	TQFP	144	IND	5.8K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP10E-3F388I	244	-3	fpBGA	388	IND	9.7K
LFXP10E-4F388I	244	-4	fpBGA	388	IND	9.7K
LFXP10E-3F256I	188	-3	fpBGA	256	IND	9.7K
LFXP10E-4F256I	188	-4	fpBGA	256	IND	9.7K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP15E-3F484I	300	-3	fpBGA	484	IND	15.5K
LFXP15E-4F484I	300	-4	fpBGA	484	IND	15.5K
LFXP15E-3F388I	268	-3	fpBGA	388	IND	15.5K
LFXP15E-4F388I	268	-4	fpBGA	388	IND	15.5K
LFXP15E-3F256I	188	-3	fpBGA	256	IND	15.5K
LFXP15E-4F256I	188	-4	fpBGA	256	IND	15.5K

Part Number	I/Os	Grade	Package	Pins	Temp.	LUTs
LFXP20E-3F484I	340	-3	fpBGA	484	IND	19.7K
LFXP20E-4F484I	340	-4	fpBGA	484	IND	19.7K
LFXP20E-3F388I	268	-3	fpBGA	388	IND	19.7K
LFXP20E-4F388I	268	-4	fpBGA	388	IND	19.7K
LFXP20E-3F256I	188	-3	fpBGA	256	IND	19.7K
LFXP20E-4F256I	188	-4	fpBGA	256	IND	19.7K

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For Further Information

A variety of technical notes for the LatticeXP family are available on the Lattice web site at www.latticesemi.com.

- *LatticeECP/EC and LatticeXP sysIO Usage Guide* (TN1056)
- *Lattice ispTRACY Usage Guide* (TN1054)
- *LatticeECP/EC and LatticeXP sysCLOCK PLL Design and Usage Guide* (TN1049)
- *Memory Usage Guide for LatticeECP/EC and LatticeXP Devices* (TN1051)
- *LatticeECP/EC and XP DDR Usage Guide* (TN1050)
- *Estimating Power Using Power Calculator for LatticeECP/EC and LatticeXP Devices* (TN1052)
- *LatticeXP sysCONFIG Usage Guide* (TN1082)
- *IEEE 1149.1 Boundary Scan Testability in Lattice Devices*

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com