ispXPLD™ 5000MX Family

3.3V, 2.5V and 1.8V In-System Programmable
eXpanded Programmable Logic Device XPLD™ Family

July 2003 **Data Sheet**

Features

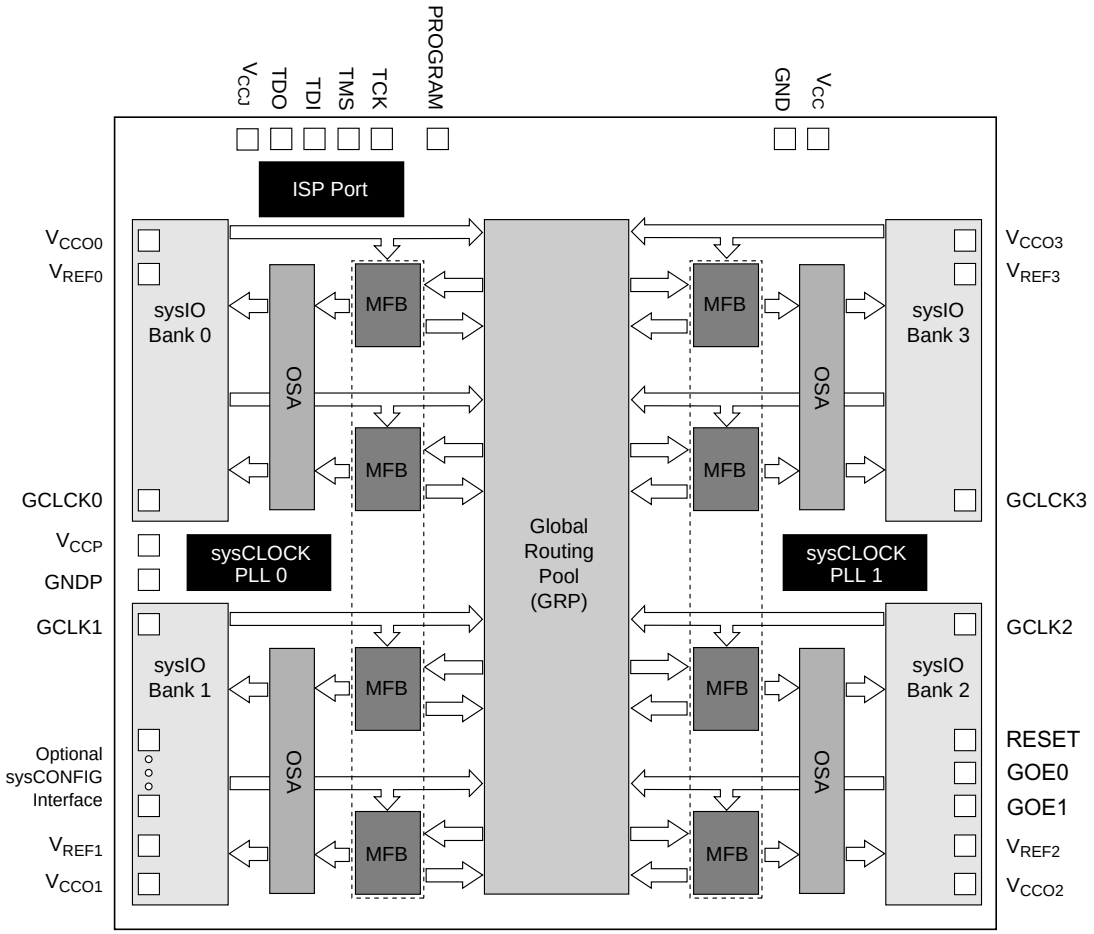
- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
  - LVTTL
- **Expanded In-System Programmability (ispXP™)**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
  - Design security
- **High Speed Operation**
  - 4.0ns pin-to-pin delays, 300MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Static power: 20 to 50mA (1.8V)
    30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
  - 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
  - IEEE 1149.1 interface for boundary scan testing
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.2ns
t_S (Register Set-up Time)	2.2ns	2.9ns	3.0ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.8ns	3.8ns
f_{MAX} (Maximum Operating Frequency)	300MHz	250MHz	240MHz	235MHz
System Gates	75K	150K	225K	300K
I/Os	141	149/193/253	193/317	317/381
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Note: ispXPLD 5256MX/5512MX/51024MX information is preliminary. ispXPLD 5768MX information is advance.

Figure 1. ispXPLD 5000MX Block Diagram



Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up time, and operating frequency up to 300MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

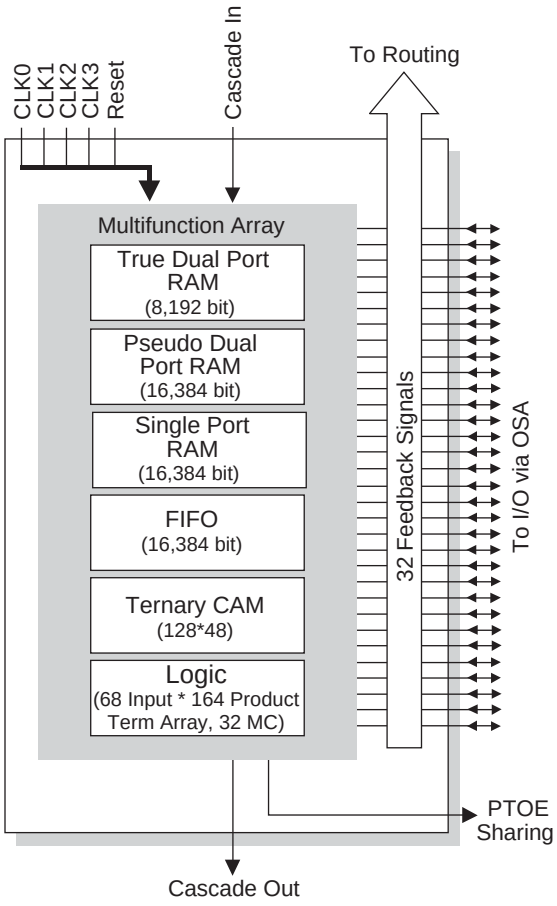
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram



Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width support.

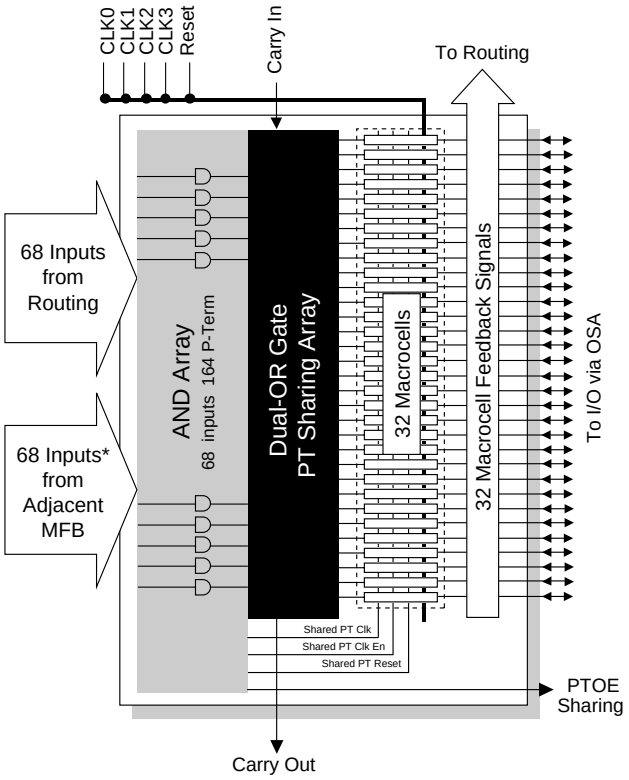
Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	E → F → G → H
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

SuperWIDE Logic Mode

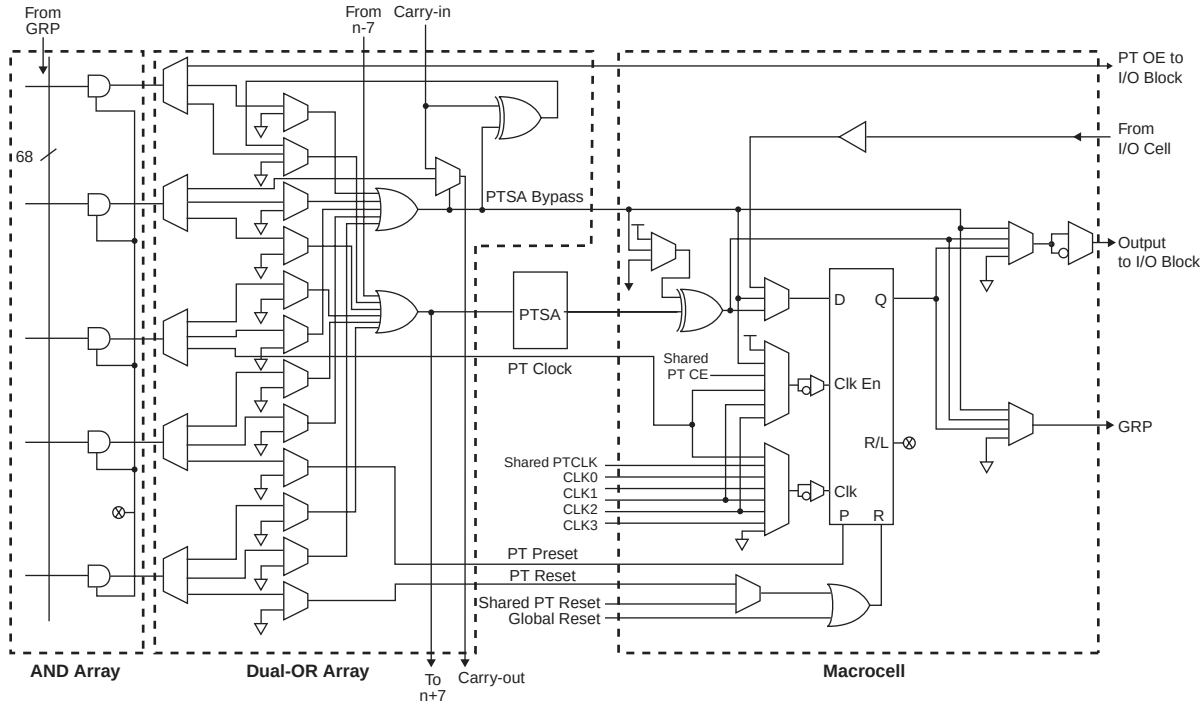
In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

Figure 3. MFB in SuperWIDE Logic Mode



*Note: These inputs are used for width expansion when more inputs are needed for CPLD or Memory mode. Single MFB consists of 68 inputs.

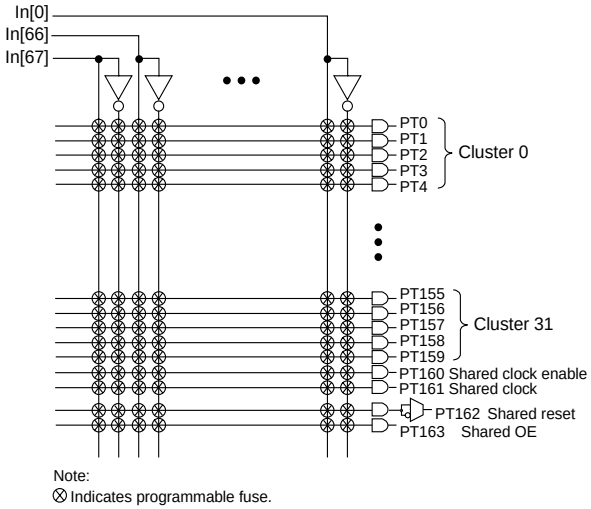
Figure 4. Macrocell Slice in Logic Mode AND-Array



AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array

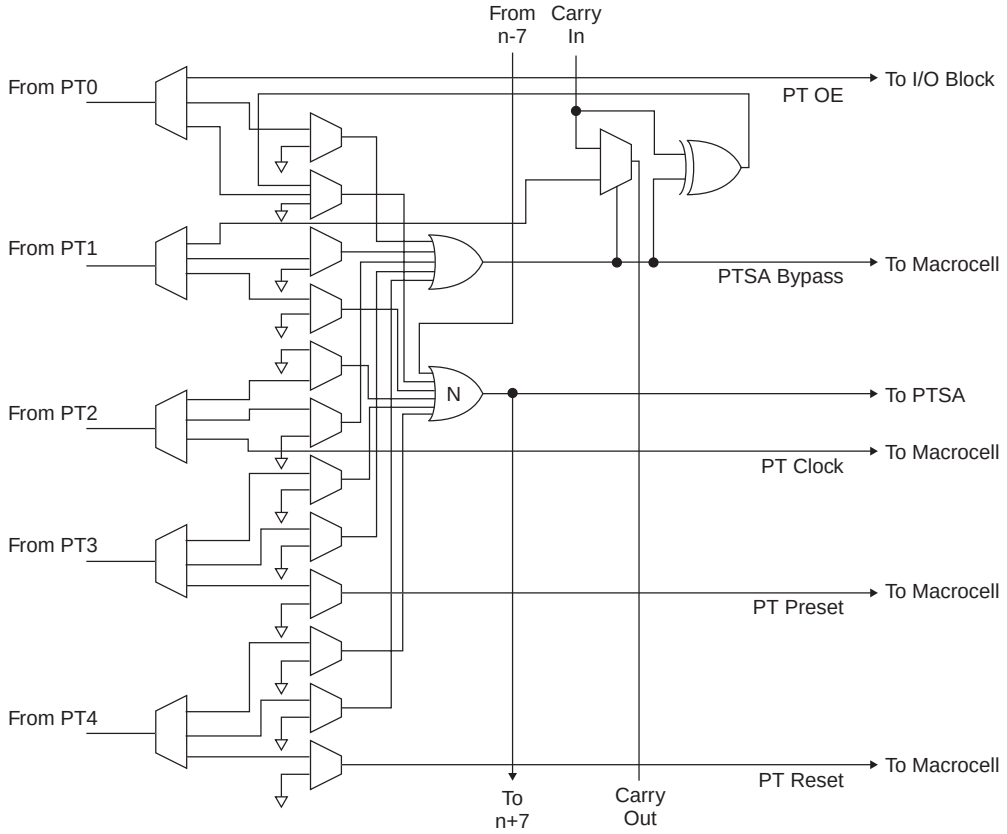


Dual-OR Array (Including Arithmetic Support)

The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

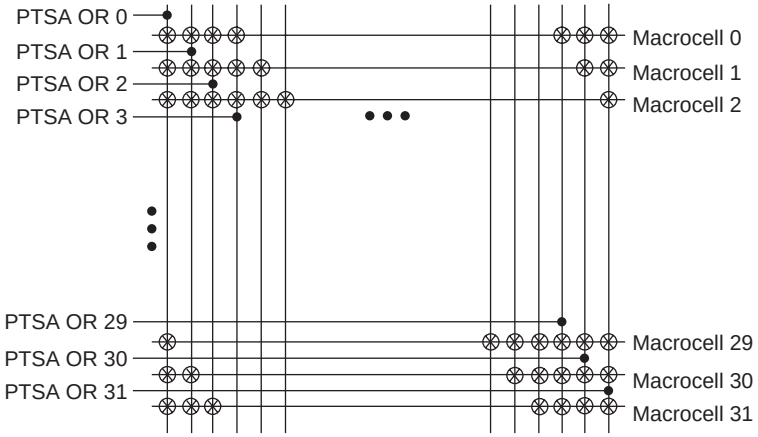
Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

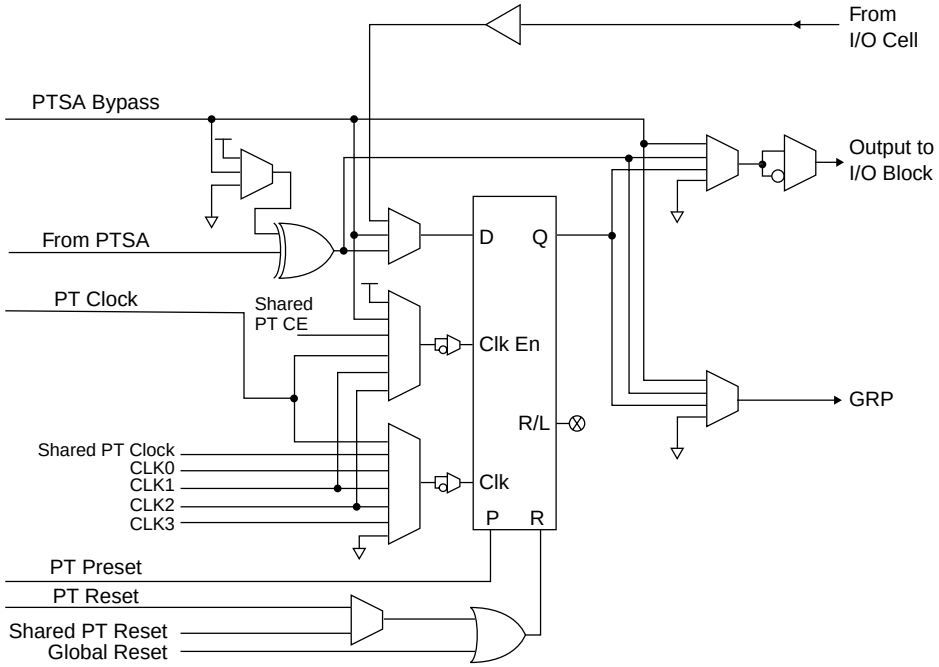
Figure 7. Product Term Sharing Array (PTSA)



Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in technical note number TN1030, *Using Memory in ispXPLD 5000MX Devices.*

Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size[1]
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output
The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation
In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width
Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching
All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

True Dual-Port SRAM Mode

In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two independent read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are supported by the MFB. Figure 9 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Resets are asynchronous. All inputs on the same port share the same clock, clock enable, and reset selections. All outputs on the same port share the same clock, clock enable, and reset selections. Selections may be made independently between both inputs and outputs and ports. Table 5 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 9. Dual-Port SRAM Block Diagram

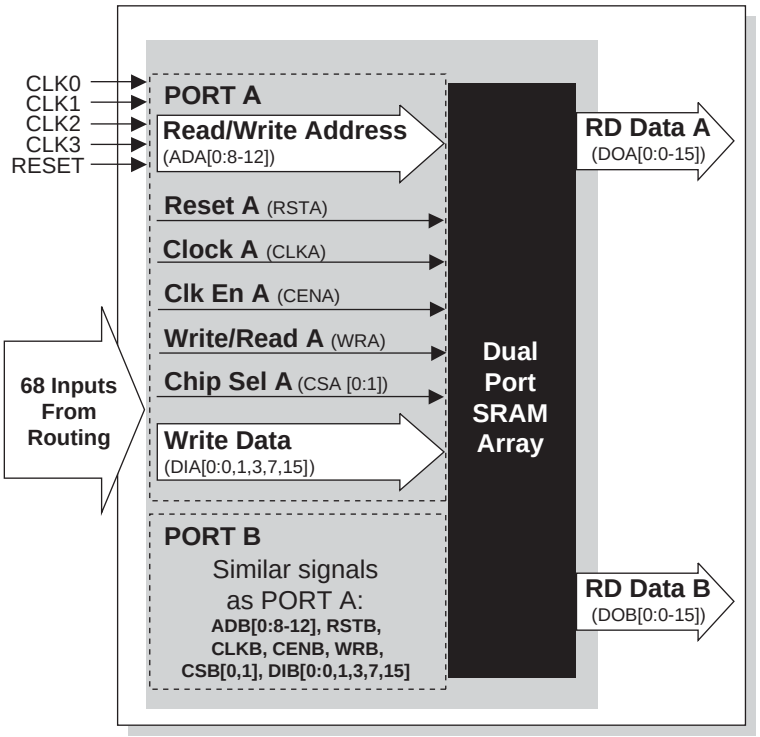


Table 5. Register Clock, Clock Enable, and Reset in Dual-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLKA (CLKB) or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	CENA (CENB) or one of the global clocks (CLK1 - CLK 2). The selected signal can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RSTA (RSTB). RSTA (RSTB) can be inverted is desired.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

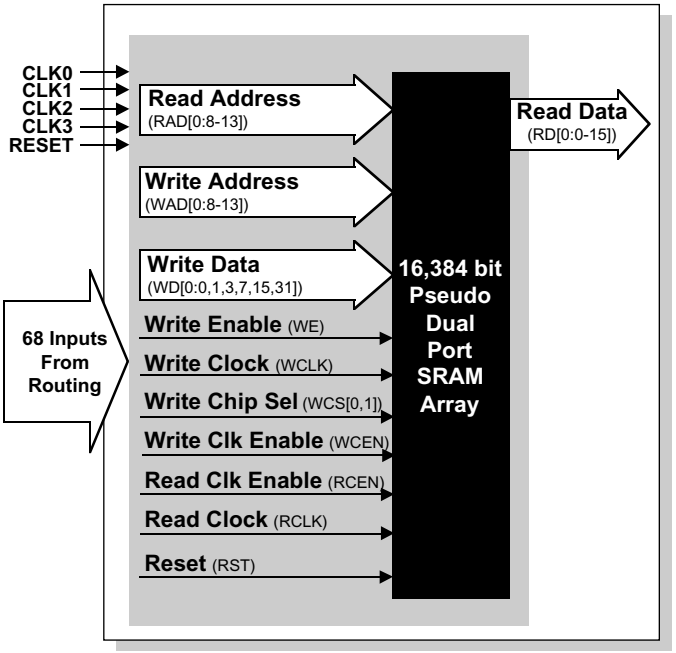


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

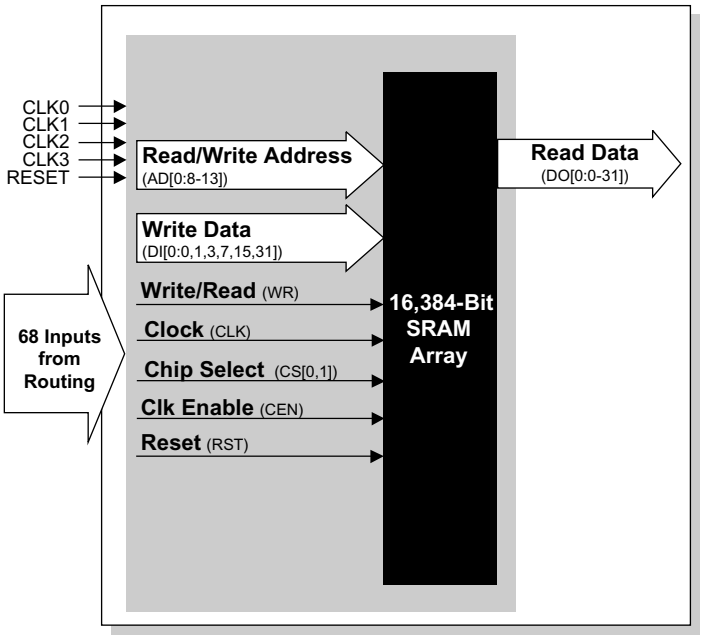


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

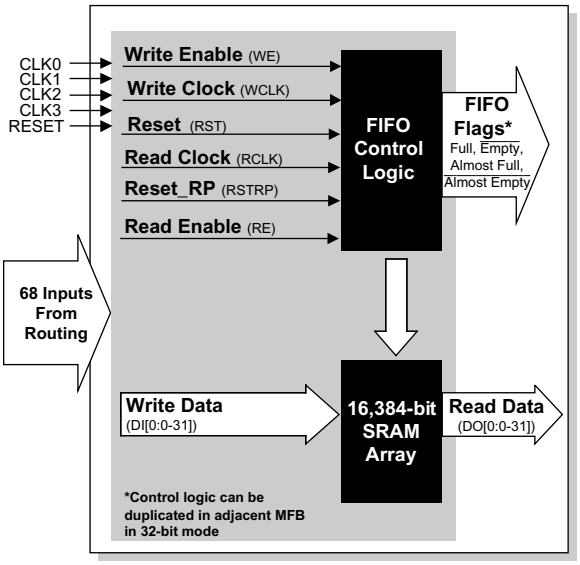


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

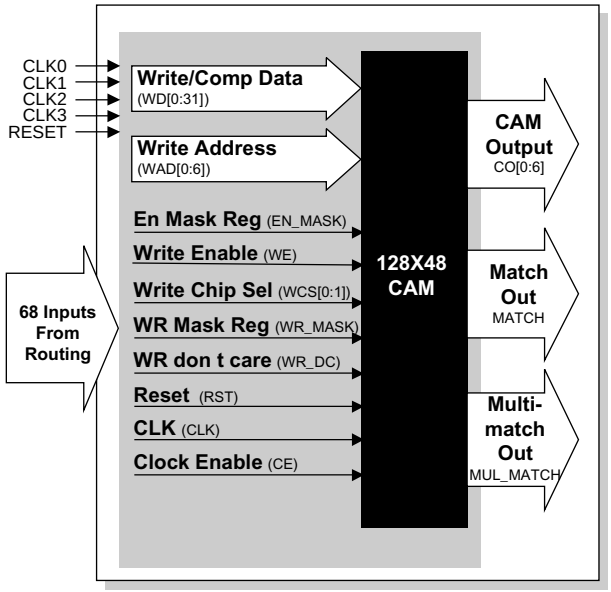


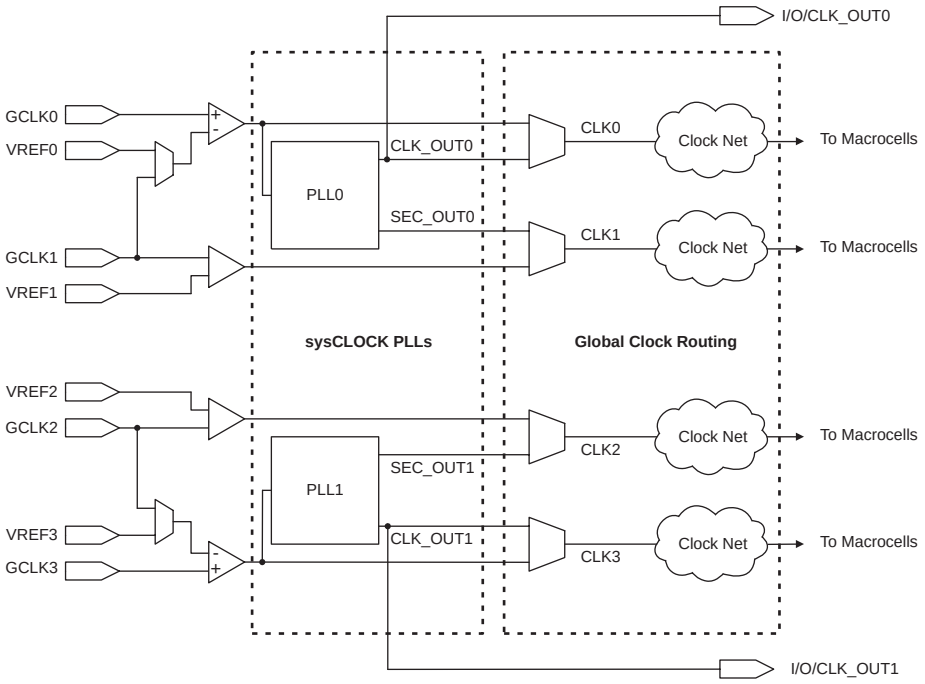
Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Figure 15. PLL Block Diagram

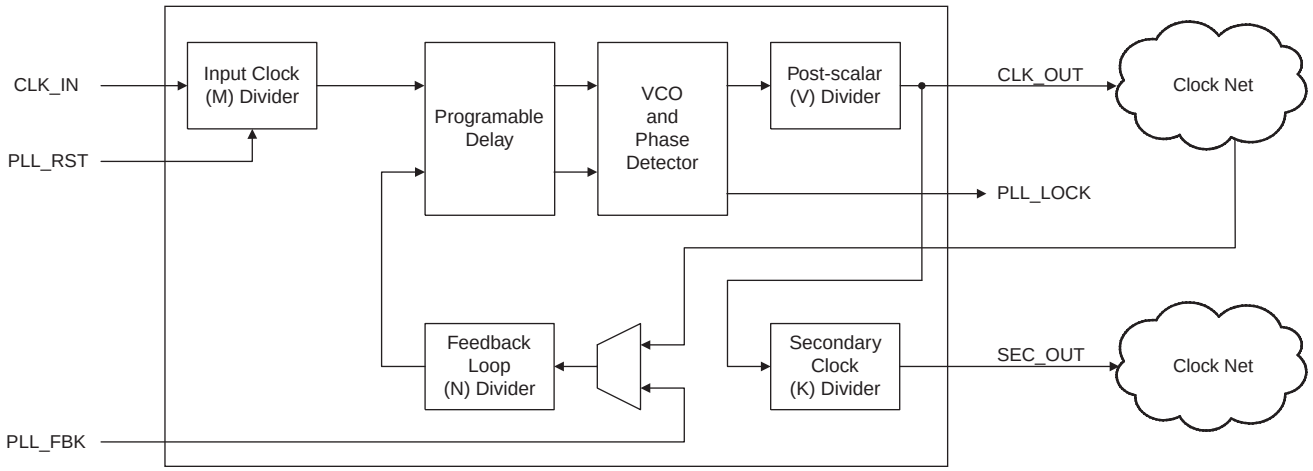
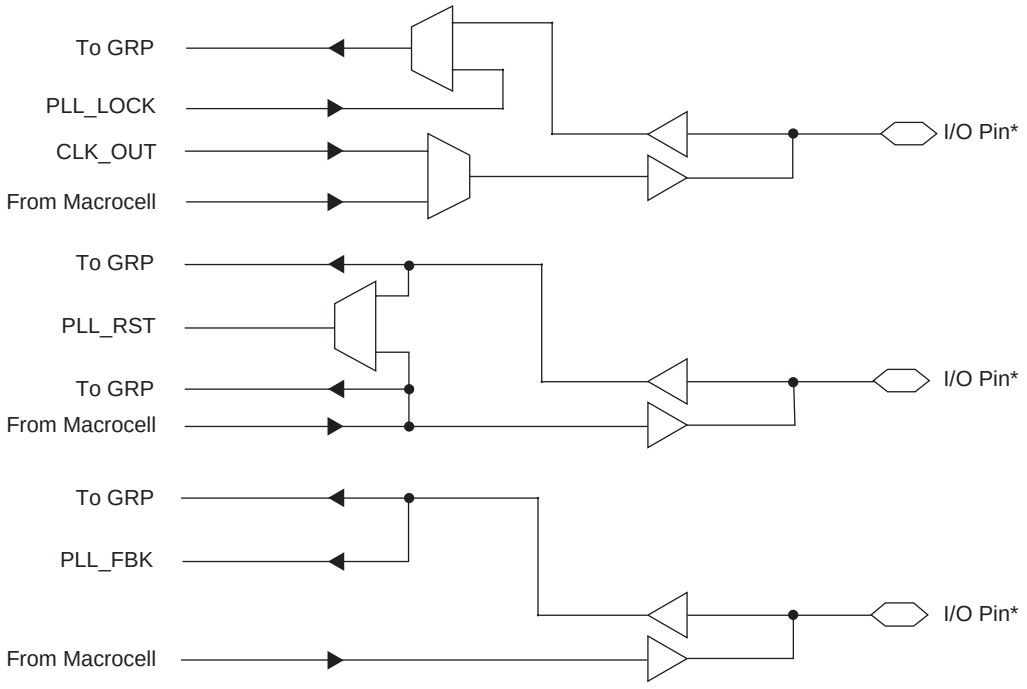


Figure 16. Connection of Optional PLL Inputs and Outputs



*See pinout table for details

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to Lattice technical note number TN1003, *Lattice sysCLOCK PLL Usage Guidelines.*

Output Sharing Array (OSA)

A number of I/O pads are available in each sysIO bank to route the selected number of macrocells from the MFB outputs directly to the I/O pads in logic mode. In the ispXPLD 5000MX, the large number of inputs and PTs to the MFB as well as the presence of the PTSA can cover most routing flexibility of signals to I/O cells. The Output Sharing Array gives additional routing capability and I/O access to an MFB when a wide output function takes up the whole MFB and cannot be easily divided across multiple MFBs. By using the OSA, the wide output function, such as 32-bit FIFO, can have all of its output signals from the one MFB routed to I/O cells. In a given I/O block, the wide output functions must share the I/O pads with other logic functions.

The OSA bypass option routes the MFB signal directly to the I/O cell, allowing a direct connection to the I/O cell. The logic functions use the option to provide faster speed to the outputs. The Logic Signal Connection tables list the OSA bypass as the primary macrocell and OSA options as alternate macrocells. Similarly, the Alternate Input listing in the table shows the alternate macrocell input connection for a given I/O pin. Figure 17 shows the alternate macrocell connections in an I/O cell.

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedback line to its associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The MFBs are grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PTOE signal is derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

Figure 17. I/O Cell

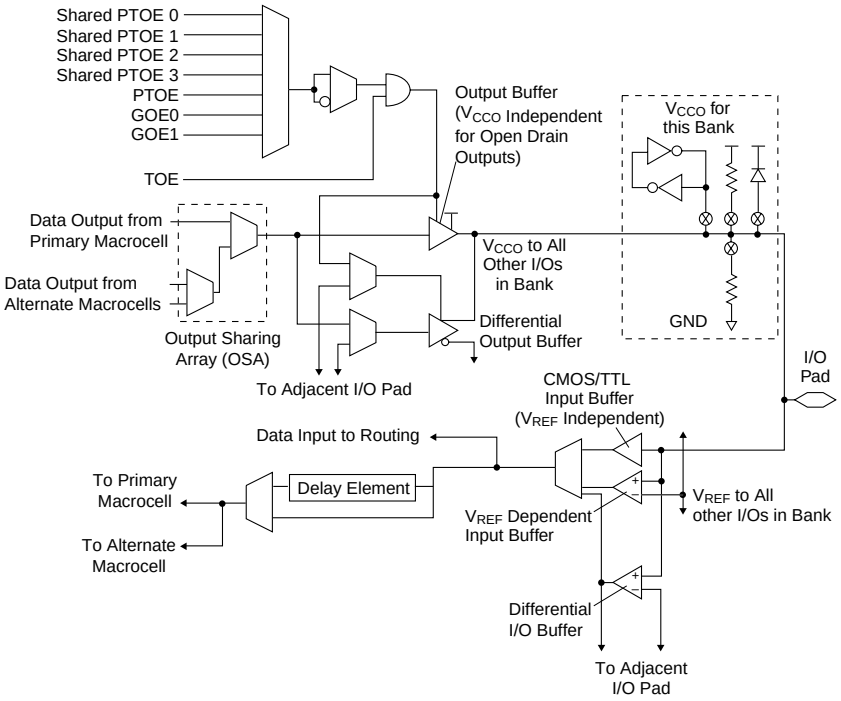


Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 12 lists the sysIO standards with the typical values for $V_{CCO,}$ V_{REF} and $V_{TT.}$ For more information on the sysIO capability, please refer to Lattice technical note number TN1000, *sysIO Usage Guidelines for Lattice Devices,* available at www.latticesemi.com.

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to Lattice technical note TN1000, *sysIO Usage Guidelines for Lattice Devices,* available at www.latticesemi.com.

Control, Clock, and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE, JTAG TAP pins, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

Programmable Slew Rate

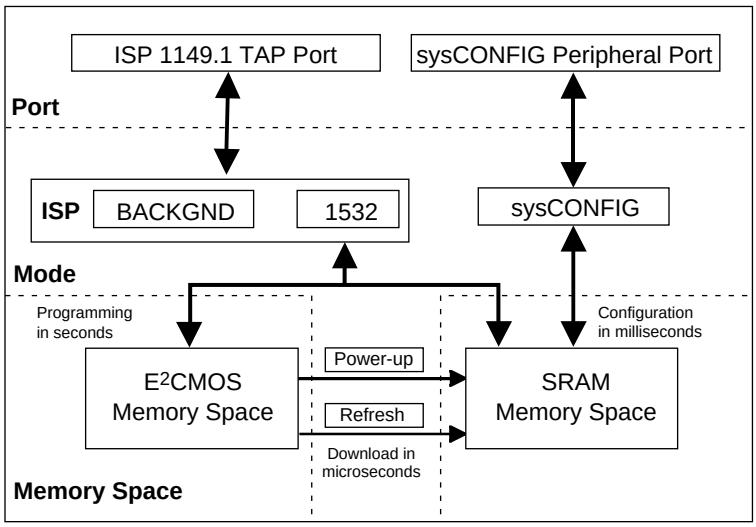
The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices support two slew rates. This allows system noise and performance to be balanced in a design.

Programmable Bus-Maintenance
All general-purpose inputs have programmable bus maintenance circuitry. These are intended to maintain a valid logic level into a device when driving devices go into the tri-state mode. Four options are available for users: pull-up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device. Figure 18 shows the different ports and modes that are used in the configuration and programming of the ispXPLD 5000MX devices.

Figure 18. ispXP Block Diagram



IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfiguration of the SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during the testing of a circuit board.

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor style interface (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more information on the sysCONFIG capability, please refer to technical note number TN1026, *ispXP Configuration Usage Guidelines.*

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For information on estimating power consumption, please refer to Lattice technical note number TN1031, *Power Estimation in ispXPLD 5000MX Devices.*

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings[1, 2, 3]

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IHMAX} +2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95	V
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7	V
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6	V
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95	V
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7	V
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6	V
T_J	Junction Temperature (Commercial Operation)	0	90	C
	Junction Temperature (Industrial Operation)	-40	105	C

E²CMOS Erase Reprogram Specifications

Parameter	Min.	Max.	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	0 ≤ V_{IN} ≤ 3.0V	—	+/-50	+/-800	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CCO}) ≤ 3.6V.
2. 0 ≤ V_{CC} ≤ V_{CC} (MAX), 0 ≤ V_{CCO} ≤ V_{CCO} (MAX)
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.
4. LVTTL, LVCMOS only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCO} - 0.2V)$	—	—	10	µA
		$(V_{CCO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40	µA
I_{IH}[4]	Input High Leakage Current	$3.6V < V_{IN} \le 5.5V$ and $3.0V \le V_{CCO} \le 3.6V$	—	—	3	mA
I_{PU}[3]	I/O Active Pullup Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	-30	—	-150	µA
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	µA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	$V_{CCO} * 0.35$	—	$V_{CCO} * 0.65$	µA
C1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz
3. I_{PU} on JTAG pins has a maximum of -175µA for 5512MX devices.
4. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \le V_{CCO} \le 3.6V$. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 5256						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CC} = 3.3V, f = 1.0MHz, unloaded	—	3	—	mA
		V_{CC} = 2.5V, f = 1.0MHz, unloaded	—	3	—	mA
		V_{CC} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCOP}	PLL Power Supply Current (per PLL Bank)	V_{CC} = 3.3V, f = 10MHz	—	6	—	mA
		V_{CC} = 2.5V, f = 10MHz	—	6	—	mA
		V_{CC} = 1.8V, f = 10MHz	—	6	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	0.75	—	mA
		V_{CCJ} = 2.5V	—	0.5	—	mA
		V_{CCJ} = 1.8V	—	0.25	—	mA
ispXPLD 5512						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CC} = 3.3V, f = 1.0MHz, unloaded	—	3	—	mA
		V_{CC} = 2.5V, f = 1.0MHz, unloaded	—	2	—	mA
		V_{CC} = 1.8V, f = 1.0MHz, unloaded	—	2	—	mA
I_{CCOP}	PLL Power Supply Current (per PLL Bank)	V_{CC} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CC} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CC} = 1.8V, f = 10MHz	—	8	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	2	—	mA
		V_{CCJ} = 2.5V	—	1.5	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA
ispXPLD 5768						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—		—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—		—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—		—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CC} = 3.3V, f = 1.0MHz, unloaded	—		—	mA
		V_{CC} = 2.5V, f = 1.0MHz, unloaded	—		—	mA
		V_{CC} = 1.8V, f = 1.0MHz, unloaded	—		—	mA
I_{CCOP}	PLL Power Supply Current (per PLL Bank)	V_{CC} = 3.3V, f = 10MHz	—		—	mA
		V_{CC} = 2.5V, f = 10MHz	—		—	mA
		V_{CC} = 1.8V, f = 10MHz	—		—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—		—	mA
		V_{CCJ} = 2.5V	—		—	mA
		V_{CCJ} = 1.8V	—		—	mA

Supply Current (Continued)

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.	Units
ispXPLD 51024						
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	75	—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—	75	—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—	55	—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CC} = 3.3V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CC} = 2.5V, f = 1.0MHz, unloaded	—	4	—	mA
		V_{CC} = 1.8V, f = 1.0MHz, unloaded	—	3	—	mA
I_{CCOP}	PLL Power Supply Current (per PLL Bank)	V_{CC} = 3.3V, f = 10MHz	—	11	—	mA
		V_{CC} = 2.5V, f = 10MHz	—	11	—	mA
		V_{CC} = 1.8V, f = 10MHz	—	10	—	mA
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	2	—	mA
		V_{CCJ} = 2.5V	—	1.5	—	mA
		V_{CCJ} = 1.8V	—	1	—	mA

1. Device configured with 16-bit counters.
2. ICC varies with specific device configuration and operating frequency.
3. T_A = 25°C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[2]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	—	—	—
LVCMOS 2.5	2.3	2.5	2.7	—	—	—
LVCMOS 1.8[1]	1.65	1.8	1.95	—	—	—
LVTTL	3.0	3.3	3.6	—	—	—
PCI 3.3	3.0	3.3	3.6	—	—	—
AGP-1X	3.15	3.3	3.45	—	—	—
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	—	0.9	—
HSTL Class IV	1.4	1.5	1.6	—	0.9	—
GTL+	1.4	—	3.6	0.882	1.0	1.122
LVDS	2.3	2.5/3.3	3.6	—	—	—

1. Design tools default setting.
2. Inputs are independent of V_{CCO} setting. However, V_{CCO} must be set within the valid operating range for one of the supported standards.

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} and V_{IH} = 0.65 * V_{CC}.
4. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8.

sysIO Differential DC Electrical Characteristics

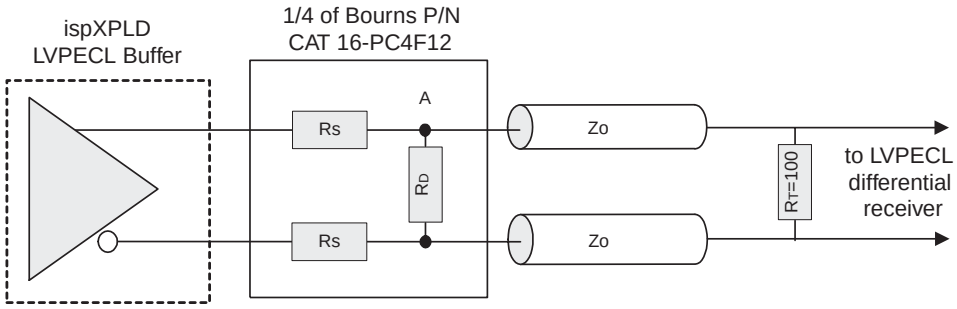
Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS					
V_{INP}	Input Voltage		0V	—	2.4V
V_{THD}	Differential Input Threshold	$0.2 \le V_{CM} \le 1.8V$	+/-100mV	—	—
I_{IN}	Input Current	Power On	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM})$, R_T = 100 Ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50mV
V_{OS}	Output Voltage Offset	$(V_{OP} - V_{OM})/2$, R_T = 100 Ohm	1.125V	1.20V	1.375V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—	24mA

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input voltage	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 19). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for $0.2 \le V_{CM} \le 1.8V$

Figure 19. LVPECL Driver with Three Resistor Pack



ispXPLD 5000MX Family External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data propagation delay, 5-PT bypass	—	4.0	—	4.5	—	5.0	ns
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	ns
t_S	MFB register setup time before clock, 5-PT bypass	2.2	—	2.9	—	2.8	—	ns
t_{S_PTSA}	MFB register setup time before clock	2.5	—	3.3	—	3.1	—	ns
t_{SIR}	MFB register setup time before clock, input register path	1.0	—	1.0	—	1.3	—	ns
t_H	MFB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB register hold time before clock	0.0	—	0.0	—	0.0	—	ns
t_{HIR}	MFB register hold time before clock, input reg. path	0.5	—	0.5	—	0.6	—	ns
t_{CO}	MFB register clock-to-output delay	—	2.8	—	3.0	—	3.5	ns
t_R	External reset pin to output delay	—	4.0	—	4.5	—	5.0	ns
t_{RW}	Reset pulse duration	1.8		1.8	—	2.3	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/ disable	—	6.0	—	7.0	—	7.5	ns
$t_{SPTOE/DIS}$	Input to output shared product term output enable/disable	—	6.0	—	7.0	—	7.5	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.5	—	5.5	—	5.6	ns
t_{CW}	Clock width, high or low	1.5	—	1.5	—	1.9	—	ns
t_{GW}	Gate width low (for low transparent) or high (for high transparent)	1.5	—	1.5	—	1.9	—	ns
t_{WIR}	Input register clock width, high or low	1.5	—	1.5	—	1.9	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.6	—	0.6	—	0.8	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	300	—	250	—	240	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback,1/ (t_S + t_{CO})	—	189	—	159	—	151	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	—	333	—	333	—	267	MHz
f_{MAX} (CAMC)[5]	Clock frequency to CAM (Configure mode)	—	280	—	280	—	224	MHz
f_{MAX} (CAM)[5]	Clock frequency to CAM (Compare mode)	—	150	—	150	—	120	MHz
f_{MAX} (RAM)[5]	Clock frequency to RAM in:							
	- Single port mode[6]	—	155	—	155	—	124	MHz
	- Dual port mode[6]	—	155	—	155	—	124	MHz
	- Pseudo dual port mode	—	180	—	180	—	144	MHz
f_{MAX} (FIFO)[5]	Clock frequency to FIFO	—	225	—	220	—	180	MHz
t_{PWR_ON}	Power-on time from E^2 mode to SRAM mode	—	200	—	200	—	200	µs

ispXPLD 5256MX - Timing v.1.0
ispXPLD 5512MX - Timing v.1.2
ispXPLD 51024MX - Timing v.1.0

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM fMAX specification used shared PT Clk.
6. Based on write-through mode when available.

ispXPLD 5000MX Family External Switching Characteristics[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Parameter	Description	-52		-75		Units
		Min.	Max.	Min.	Max.	
t_{PD}	Data propagation delay, 5-PT bypass	—	5.2	—	7.5	ns
t_{PD_PTSA}	Data propagation delay	—	6.5	—	9.5	ns
t_S	MFB register setup time before clock, 5-PT bypass	3.0	—	4.9	—	ns
t_{S_PTSA}	MFB register setup time before clock	3.7	—	5.5	—	ns
t_{SIR}	MFB register setup time before clock, input register path	0.5	—	1.7	—	ns
t_H	MFB register hold time before clock, 5-PT bypass	0.0	—	0.0	—	ns
t_{H_PTSA}	MFB register hold time before clock	0.0	—	0.0	—	ns
t_{HIR}	MFB register hold time before clock, input reg. path	1.0	—	1.3	—	ns
t_{CO}	MFB register clock-to-output delay	—	3.8	—	5.0	ns
t_R	External reset pin to output delay	—	5.0	—	7.5	ns
t_{RW}	Reset pulse duration	2.0	—	3.0	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/ disable	—	8.5	—	11.6	ns
$t_{SPTOE/DIS}$	Input to output shared product term output enable/disable	—	8.5	—	11.7	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	6.5	—	9.2	ns
t_{CW}	Clock width, high or low	1.8	—	2.5	—	ns
t_{GW}	Gate width low (for low transparent) or high (for high transparent)	1.8	—	2.5	—	ns
t_{WIR}	Input register clock width, high or low	1.8	—	2.5	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.6	—	1.0	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	235	—	150	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback,1/ ($t_S + t_{CO}$)	—	147	—	95	MHz
f_{MAX} (Tog.)	Clock frequency max Toggle	—	278	—	200	MHz
f_{MAX} (CAMC)[5]	Clock frequency to CAM (Configure mode)	—	230	—	168	MHz
f_{MAX} (CAM)[5]	Clock frequency to CAM (Compare mode)	—	135	—	90	MHz
f_{MAX} (RAM)[5]	Clock frequency to RAM in:					
	- Single port mode[6]	—	155	—	93	MHz
	- Dual port mode[6]	—	155	—	93	MHz
	- Pseudo dual port mode	—	160	—	108	MHz
f_{MAX} (FIFO)[5]	Clock frequency to FIFO	—	210	—	132	MHz
t_{PWR_ON}	Power-on time from E^2 mode to SRAM mode	—	200	—	200	µs

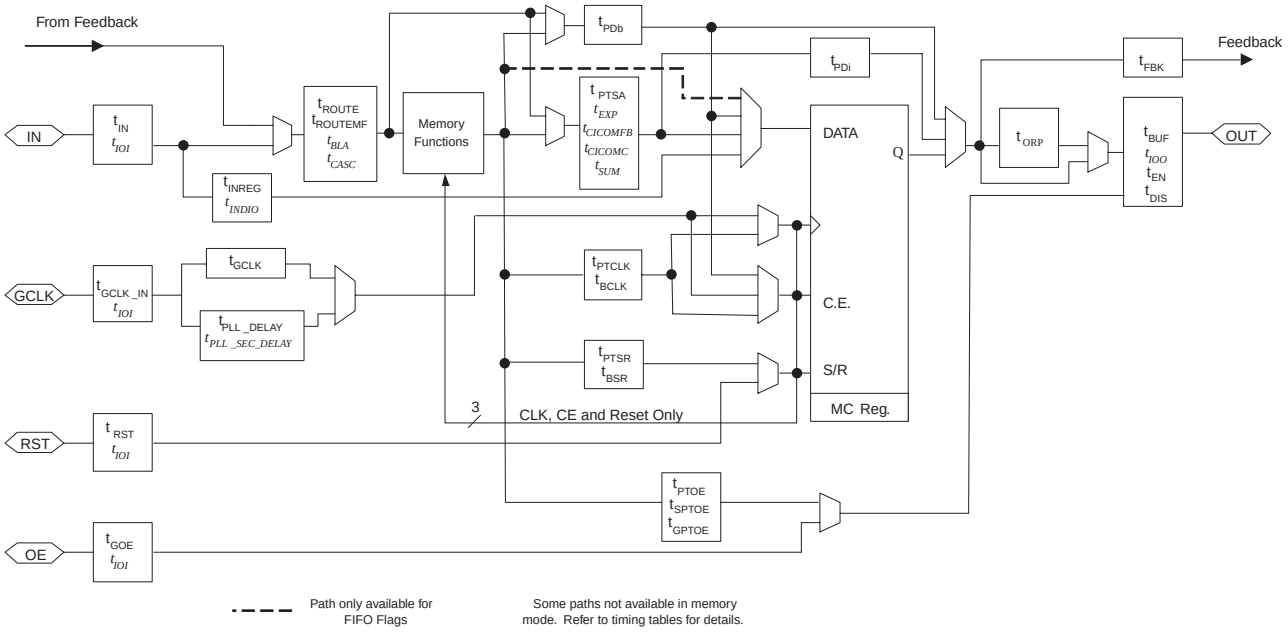
ispXPLD 5256MX - Timing v.1.0
ispXPLD 5512MX - Timing v.1.2
ispXPLD 51024MX - Timing v.1.0

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM fMAX specification used shared PT Clk.
6. Based on write-through mode when available.

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 20 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
In/Out Delays									
t_{IN}	Input Buffer Delay	—	—	0.70	—	0.61	—	0.87	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.40	—	0.57	—	0.50	ns
t_{RST}	Global RESET Pin Delay	—	—	3.77	—	4.31	—	4.71	ns
t_{GOE}	Global OE Pin Delay	—	—	1.98	—	2.35	—	2.48	ns
t_{BUF}	Delay through Output Buffer	—	—	1.16	—	1.34	—	1.45	ns
t_{EN}	Output Enable Time	—	—	2.52	—	3.17	—	3.15	ns
t_{DIS}	Output Disable Time	—	—	1.92	—	2.14	—	2.40	ns
Routing Delays									
t_{ROUTE}	Delay through SRP	—	—	1.95	—	2.17	—	2.44	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.87	—	0.87	—	1.08	ns
t_{PTSA}	Product Term Sharing Array Delay	—	—	0.50	—	0.72	—	0.63	ns
t_{FBK}	Internal Feedback Delay	—	—	0.18	—	0.02	—	0.23	ns
t_{GCLK}	Global Clock Tree Delay	—	—	0.52	—	0.47	—	0.65	ns
t_{BCLK}	Block PT Clock Delay	—	—	0.12	—	1.42	—	0.15	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	—	0.12	—	0.92	—	0.15	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.30	—	0.38	ns
t_{BSR}	Block PT Reset Delay	—	—	0.72	—	0.80	—	0.90	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	—	0.60	—	0.67	—	0.75	ns
t_{PTOE}	Macrocell PT OE Delay	—	—	0.83	—	1.02	—	1.04	ns
t_{SPTOE}	Segment PT OE Delay	—	—	0.83	—	1.04	—	1.04	ns
t_{OSA}	Output Sharing Array Delay	—	—	0.80	—	0.80	—	1.00	ns
t_{PTOE}	Global PT OE Delay	—	—	0.83	—	1.02	—	1.04	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	—	0.20	—	0.35	—	0.25	ns
t_{PDi}	Macrocell Propagation Delay	—	—	0.50	—	0.84	—	0.63	ns
Registered Delays									
t_S	D-Register Setup Time, Global Clock	—	0.28	—	0.83	—	0.35	—	ns
t_{S_PT}	D-Register Setup Time, PT Clock	—	-0.13	—	-0.13	—	-0.10	—	ns
t_H	D-Register Hold Time	—	1.20	—	0.20	—	1.50	—	ns
t_{COi}	Register Clock to OSA Time	—	0.72	—	0.63	—	0.90	—	ns
t_{CESi}	Clock Enable Setup Time	—	1.07	—	0.84	—	1.33	—	ns
t_{CEHi}	Clock Enable Hold Time	—	0.00	—	0.00	—	0.00	—	ns
t_{SIR}	D-Input Register Setup Time, Global Clock	—	0.36	—	0.60	—	0.29	—	ns
t_{SIR_PT}	D-Input Register Setup Time, PT Clock	—	0.42	—	0.42	—	0.34	—	ns
t_{HIR}	D-Input Register Hold Time, Global Clock	—	1.14	—	0.90	—	0.91	—	ns
t_{HIR_PT}	D-Input Register Hold Time, PT Clock	—	0.00	—	0.00	—	0.00	—	ns
Latched Delays									
t_{SL}	Latch Setup Time, Global Clock	—	0.18	—	0.18	—	0.23	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SL_PT}	Latch Setup Time, PT Clock	—	0.18	—	0.18	—	0.23	—	ns
t_{HL}	Latch Hold Time	—	-0.06	—	-0.06	—	-0.04	—	ns
t_{GOi}	Latch Gate to OSA Time	—	—	0.07	—	0.07	—	0.08	ns
t_{PDLi}	Propagation Delay through Latch to OSA Transparent	—	—	0.52	—	0.52	—	0.65	ns
Reset and Set Delays									
t_{SRi}	Asynchronous Reset or Set to OSA Delay	—	—	0.23	—	0.19	—	0.29	ns
t_{SRR}	Asynchronous Reset or Set Recovery	—	—	0.42	—	0.42	—	0.53	ns
eXtended Function Routing Delays									
$t_{ROUTEMF}$	Delay through SRP when Implimenting Memory Functions	—	—	2.00	—	2.00	—	2.51	ns
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.71	—	0.89	ns
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.12	—	0.44	ns
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.08	—	0.13	ns
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.62	—	3.27	ns
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	2.57	—	3.21	ns
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	0.80	—	1.05	—	1.00	ns
Optional Adjusters									
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.04	—	0.05	ns
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.53	—	0.66	ns
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.50	—	0.97	—	0.63	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.91	—	0.92	—	0.91	ns
Input and Output Buffer Delays									
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables						ns
t_{IOO}	Secondary PLL Output Delay	t_{BUF}							ns
FIFO									
$t_{FIFOWCLKS}$	Write Data Setup Before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{FIFOWCLKH}$	Write Data Hold After Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	3.08	—	3.71	—	3.86	—	ns
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	3.08	—	3.71	—	3.86	—	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	3.08	—	3.71	—	3.86	—	ns
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	3.08	—	3.71	—	3.86	—	ns
$t_{FIFOWES}$	Write-Enable setup Before Write Clock	—	2.33	—	2.33	—	2.91	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{FIFOWEH}$	Write-Enable hold After Write Clock	—	-2.95	—	-2.95	—	-2.36	—	ns
$t_{FIFORES}$	Read-Enable setup Before Read Clock	—	2.69	—	2.33	—	3.36	—	ns
$t_{FIFOREH}$	Read-Enable hold After Read Clock	—	-3.17	—	-3.17	—	-2.53	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	ns
CAM – Update Mode									
t_{CAMMSS}	Memory Select Setup Before CLK	—	2.09	—	2.54	—	2.62	—	ns
t_{CAMMSH}	Memory Select Hold After CLK	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time Before CLK	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time After CLK	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMADDS}$	Address Setup Time Before Clock	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{CAMADDH}$	Address Hold Time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMDATAS}$	Data Setup Time Before Clock	—	-0.41	—	-0.27	—	-0.33	—	ns
$t_{CAMDATAH}$	Data Hold Time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMDCS}	“Don’t Care” Setup Time Before Clock	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{CAMDCH}	“Don’t Care” Hold Time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMRWS}	R/W Setup Time Before Clock	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{CAMRWH}	R/W Enable Hold Time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{CAMCES}	Clock Enable Setup Time Before Clock	—	1.55	—	1.55	—	1.94	—	ns
t_{CAMCEH}	Clock Enable Hold Time After Clock	—	-2.95	—	-2.95	—	-2.36	—	ns
$t_{CAMWMSKS}$	Write Mask Register Setup Time Before Clock	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time After Clock	—	-0.01	--	-0.01	—	-0.01	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	ns
CAM – Compare Mode									
$t_{CAMDATAS}$	Data Setup Time Before Clock	—	-0.41	—	-0.27	—	-0.33	—	ns
$t_{CAMDATAH}$	Data Hold Time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time Before Clock	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.18	—	5.50	—	7.73	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.18	—	5.50	—	7.73	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.88	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	ns
Single Port RAM									
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	7.46	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{SPMSH}	Memory Select Hold time After Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCES}	Clock Enable Setup Before Clock Time	—	2.30	—	2.33	—	2.88	—	ns
t_{SPCEH}	Clock Enable Hold time After Clock Time	—	-2.95	—	-2.95	—	-2.36	—	ns
t_{SPADDS}	Address Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{SPADDH}	Address Hold time After Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPRWS}	R/W Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{SPRWH}	R/W Hold time After Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{SPDATAS}$	Data Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{SPDATAH}$	Data Hold time After Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.27	—	7.47	ns
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	ns
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	ns
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	ns
Pseudo Dual Port RAM									
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{PDPMSH}	Memory Select Hold time After Clock	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPRCES}$	Clock Enable Setup Before Read Clock Time	—	2.33	—	2.33	—	2.91	—	ns
$t_{PDPRCEH}$	Clock Enable Hold time After Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	ns
$t_{PDPWCES}$	Clock Enable Setup Before Write Clock Time	—	1.87	—	2.33	—	2.34	—	ns
$t_{PDPWCEH}$	Clock Enable Hold time After Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	ns
$t_{PDPRADDS}$	Read Address Setup Before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{PDPRADDH}$	Read Address Hold After Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPWADDS}$	Write Address Setup Before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{PDPWADDH}$	Write Address Hold After Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{PDPRWS}	R/W Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{PDPRWH}	R/W Hold time After Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{PDPDATAS}$	Data Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{PDPDATAH}$	Data Hold time After Clock Time	—	-0.01	—	-0.01	—	-0.01	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	4.37	—	6.35	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	ns
Dual Port RAM									
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{DPMSAH}	Memory Select Hold time After R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEAS}	Clock Enable A Setup Before Clock A Time	—	3.72	—	2.33	—	4.65	—	ns
t_{DPCEAH}	Clock Enable A Hold time After Clock A Time	—	-2.95	—	-2.95	—	-2.36	—	ns
$t_{DPADDAS}$	Address A Setup Before Clock A Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{DPADDAH}$	Address A Hold time After Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWAS}	R/W A Setup Before Clock A Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{DPRWAH}	R/W A Hold time After Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATAAS}$	Write Data A Setup Before Clock A Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{DPDATAAH}$	Write Data A Hold time After Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{DPMSBH}	Memory Select Hold time After R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPCEBS}	Clock Enable B Setup Before Clock B Time	—	2.33	—	2.33	—	2.91	—	ns
t_{DPCEBH}	Clock Enable Hold B After Clock B Time	—	-2.95	—	-2.95	—	-2.36	—	ns
$t_{DPADDBS}$	Address B Setup Before Clock B Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{DPADDBH}$	Address B Hold time After Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	ns
t_{DPRWBS}	R/W B Setup Before Clock B Time	—	-0.27	—	-0.27	—	-0.22	—	ns
t_{DPRWBH}	R/W B Hold time After Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPDATABS}$	Write Data B Setup Before Clock B Time	—	-0.27	—	-0.27	—	-0.22	—	ns
$t_{DPDATABH}$	Write Data B Hold After Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	ns
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	5.97	—	5.27	—	7.47	ns
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	5.16	—	5.27	—	6.45	ns
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	ns
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	--	4.13	ns
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	ns

ispXPLD 5256MX - Timing v.1.0
ispXPLD 5512MX - Timing v.1.2
ispXPLD 51024MX - Timing v.1.0

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
In/Out Delays							
t_{IN}	Input Buffer Delay	—	—	1.21	—	1.02	ns
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.95	—	0.95	ns
t_{RST}	Global RESET Pin Delay	—	—	4.81	—	7.18	ns
t_{GOE}	Global OE Pin Delay	—	—	2.68	—	3.92	ns
t_{BUF}	Delay through Output Buffer	—	—	1.35	—	2.24	ns
t_{EN}	Output Enable Time	—	—	3.83	—	5.29	ns
t_{DIS}	Output Disable Time	—	—	2.14	—	3.56	ns
Routing Delays							
t_{ROUTE}	Delay through SRP	—	—	1.54	—	3.62	ns
t_{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.46	—	1.45	ns
t_{PTSA}	Product Term Sharing Array Delay	—	—	1.80	—	1.20	ns
t_{FBK}	Internal Feedback Delay	—	—	0.02	—	0.03	ns
t_{GCLK}	Global Clock Tree Delay	—	—	0.70	—	0.78	ns
t_{BCLK}	Block PT Clock Delay	—	—	1.42	—	2.36	ns
t_{PTCLK}	Macrocell PT Clock Delay	—	—	0.92	—	1.54	ns
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.50	ns
t_{BSR}	Block PT Reset Delay	—	—	0.80	—	1.34	ns
t_{PTSR}	Macrocell PT Set/Reset Delay	—	—	0.67	—	1.12	ns
t_{PTOE}	Macrocell PT OE Delay	—	—	1.95	—	1.70	ns
t_{SPTOE}	Segment PT OE Delay	—	—	1.96	—	1.73	ns
t_{OSA}	Output Sharing Array Delay	—	—	0.80	—	1.33	ns
t_{PTOE}	Global PT OE Delay	—	—	1.95	—	1.70	ns
t_{PDB}	5-PT Bypass Propagation Delay	—	—	1.10	—	0.59	ns
t_{PDi}	Macrocell Propagation Delay	—	—	0.60	—	1.40	ns
Registered Delays							
t_{S}	D-Register Setup Time, Global Clock	—	0.80	—	1.38	—	ns
t_{S_PT}	D-Register Setup Time, PT Clock	—	-0.13	—	-0.08	—	ns
t_{H}	D-Register Hold Time	—	0.20	—	0.34	—	ns
t_{COi}	Register Clock to OSA Time	—	0.80	—	1.05	—	ns
t_{CESi}	Clock Enable Setup Time	—	1.26	—	1.40	—	ns
t_{CEHi}	Clock Enable Hold Time	—	0.00	—	0.00	—	ns
t_{SIR}	D-Input Register Setup Time, Global Clock	—	0.53	—	0.36	—	ns
t_{SIR_PT}	D-Input Register Setup Time, PT Clock	—	0.42	—	0.25	—	ns
t_{HIR}	D-Input Register Hold Time, Global Clock	—	1.01	—	0.54	—	ns
t_{HIR_PT}	D-Input Register Hold Time, PT Clock	—	0.00	—	0.00	—	ns
Latched Delays							
t_{SL}	Latch Setup Time, Global Clock	—	0.18	—	0.30	—	ns
t_{SL_PT}	Latch Setup Time, PT Clock	—	0.18	—	0.30	—	ns
t_{HL}	Latch Hold Time	—	-0.06	—	-0.03	—	ns
t_{GOi}	Latch Gate to OSA Time	—	—	0.07	—	0.11	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
t_{PDLi}	Propagation Delay through Latch to OSA Transparent	—	—	0.52	—	0.86	ns
Reset and Set Delays							
t_{SRi}	Asynchronous Reset or Set to OSA Delay	—	—	0.19	—	0.32	ns
t_{SRR}	Asynchronous Reset or Set Recovery	—	—	0.42	—	0.70	ns
eXtended Function Routing Delays							
$t_{ROUTEMF}$	Delay through SRP when Implimenting Memory Functions	—	—	2.00	—	3.34	ns
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	1.18	ns
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.12	—	0.20	ns
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.08	—	0.14	ns
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	4.36	ns
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	4.28	ns
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	1.05	—	1.75	ns
Optional Adjusters							
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.06	ns
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.88	ns
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.97	—	1.62	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.92	—	0.92	ns
Input and Output Buffer Delays							
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables				ns
t_{IOO}	Secondary PLL Output Delay	t_{BUF}					ns
FIFO							
$t_{FIFOWCLKS}$	Write Data Setup Before Write Clock Time	—	-0.20	—	-0.16	—	ns
$t_{FIFOWCLKH}$	Write Data Hold After Write Clock Time	—	-0.01	—	0.00	—	ns
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	--	2.34	ns
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	3.97	—	6.19	—	ns
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	3.97	—	6.19	—	ns
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	3.97	—	6.19	—	ns
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	3.97	—	6.19	—	ns
$t_{FIFOWES}$	Write-Enable setup Before Write Clock	—	2.33	—	3.88	—	ns
$t_{FIFOWEH}$	Write-Enable hold After Write Clock	—	-2.95	—	-1.77	—	ns
$t_{FIFORES}$	Read-Enable setup Before Read Clock	—	2.33	—	3.88	—	ns
$t_{FIFOREH}$	Read-Enable hold After Read Clock	—	-3.17	—	-1.90	—	ns
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	5.50	ns
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	2.00	—	ns
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.24	—	ns
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	6.21	ns
CAM – Update Mode							
t_{CAMMSS}	Memory Select Setup Before CLK	—	3.34	—	4.23	—	ns
t_{CAMMSH}	Memory Select Hold After CLK	—	-0.01	—	0.00	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
$t_{CAMENMSKS}$	Enable Mask Register Setup Time Before CLK	—	-0.27	—	-0.16	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time After CLK	—	-0.01	—	0.00	—	ns
$t_{CAMADDS}$	Address Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
$t_{CAMADDH}$	Address Hold Time After Clock	—	-0.01	—	0.00	—	ns
$t_{CAMDATAS}$	Data Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
$t_{CAMDATAH}$	Data Hold Time After Clock	—	-0.01	—	0.00	—	ns
t_{CAMDCS}	“Don’t Care” Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
t_{CAMDCH}	“Don’t Care” Hold Time After Clock	—	-0.01	—	0.00	—	ns
t_{CAMRWS}	R/W Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
t_{CAMRWH}	R/W Enable Hold Time After Clock	—	-0.01	—	0.00	—	ns
t_{CAMCES}	Clock Enable Setup Time Before Clock	—	1.55	—	2.59	—	ns
t_{CAMCEH}	Clock Enable Hold Time After Clock	—	-2.95	—	-1.77	—	ns
$t_{CAMWMSKS}$	Write Mask Register Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
$t_{CAMWMSKH}$	Write Mask Register Setup Time After Clock	—	-0.01	—	0.00	—	ns
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	--	5.50	ns
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	2.00	—	ns
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.24	—	ns
CAM – Compare Mode							
$t_{CAMDATAS}$	Data Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
$t_{CAMDATAH}$	Data Hold Time After Clock	—	-0.01	—	0.00	—	ns
$t_{CAMENMSKS}$	Enable Mask Register Setup Time Before Clock	—	-0.27	—	-0.16	—	ns
$t_{CAMENMSKH}$	Enable Mask Register Setup Time After Clock	—	-0.01	—	0.00	—	ns
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.66	ns
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	5.50	—	9.17	ns
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	5.50	—	9.17	ns
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	9.17	ns
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	5.27	ns
Single Port RAM							
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	9.95	ns
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.16	—	ns
t_{SPMSH}	Memory Select Hold time After Clock Time	—	-0.01	—	0.00	—	ns
t_{SPCES}	Clock Enable Setup Before Clock Time	—	2.33	—	3.88	—	ns
t_{SPCEH}	Clock Enable Hold time After Clock Time	—	-2.95	—	-1.77	—	ns
t_{SPADDS}	Address Setup Before Clock Time	—	-0.27	—	-0.16	—	ns
t_{SPADDH}	Address Hold time After Clock Time	—	-0.01	—	0.00	—	ns
t_{SPRWS}	R/W Setup Before Clock Time	—	-0.27	—	-0.16	—	ns
t_{SPRWH}	R/W Hold time After Clock Time	—	-0.01	—	0.00	—	ns
$t_{SPDATAS}$	Data Setup Before Clock Time	—	-0.27	—	-0.16	—	ns
$t_{SPDATAH}$	Data Hold time After Clock Time	—	-0.01	—	0.00	—	ns
t_{SPCLKO}	Clock to Output Delay	—	—	4.56	—	8.78	ns
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	5.50	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	2.00	—	ns
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.24	—	ns
Pseudo Dual Port RAM							
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.16	—	ns
t_{PDPMSH}	Memory Select Hold time After Clock	—	-0.01	—	0.00	—	ns
$t_{PDPRCES}$	Clock Enable Setup Before Read Clock Time	—	2.33	—	3.88	—	ns
$t_{PDPRCEH}$	Clock Enable Hold time After Read Clock Time	—	-2.95	—	-1.77	—	ns
$t_{PDPWCES}$	Clock Enable Setup Before Write Clock Time	—	2.33	—	3.88	—	ns
$t_{PDPWCEH}$	Clock Enable Hold time After Write Clock Time	—	-2.95	—	-1.77	—	ns
$t_{PDPRADDS}$	Read Address Setup Before Read Clock Time	—	-0.27	—	-0.16	—	ns
$t_{PDPRADDH}$	Read Address Hold After Read Clock Time	—	-0.01	—	0.00	—	ns
$t_{PDPWADDS}$	Write Address Setup Before Write Clock Time	—	-0.27	—	-0.16	—	ns
$t_{PDPWADDH}$	Write Address Hold After Write Clock Time	—	-0.01	—	0.00	—	ns
t_{PDPRWS}	R/W Setup Before Clock Time	—	-0.27	—	-0.16	—	ns
t_{PDPRWH}	R/W Hold time After Clock Time	—	-0.01	—	0.00	—	ns
$t_{PDPDATAS}$	Data Setup Before Clock Time	—	-0.27	—	-0.16	—	ns
$t_{PDPDATAH}$	Data Hold time After Clock Time	—	-0.01	—	0.00	—	ns
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	4.34	—	7.29	ns
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	2.34	—	ns
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	5.50	ns
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	2.00	—	ns
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.24	—	ns
Dual Port RAM							
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.16	—	ns
t_{DPMSAH}	Memory Select Hold time After R/W A Time	—	-0.01	—	0.00	—	ns
t_{DPCEAS}	Clock Enable A Setup Before Clock A Time	—	2.33	—	3.88	—	ns
t_{DPCEAH}	Clock Enable A Hold time After Clock A Time	—	-2.95	—	-1.77	—	ns
$t_{DPADDAS}$	Address A Setup Before Clock A Time	—	-0.27	—	-0.16	—	ns
$t_{DPADDAH}$	Address A Hold time After Clock A Time	—	-0.01	—	0.00	—	ns
t_{DPRWAS}	R/W A Setup Before Clock A Time	—	-0.27	—	-0.16	—	ns
t_{DPRWAH}	R/W A Hold time After Clock A Time	—	-0.01	—	0.00	—	ns
$t_{DPDATAAS}$	Write Data A Setup Before Clock A Time	—	-0.27	—	-0.16	—	ns
$t_{DPDATAAH}$	Write Data A Hold time After Clock A Time	—	-0.01	—	0.00	—	ns
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.16	—	ns
t_{DPMSBH}	Memory Select Hold time After R/W B Time	—	-0.01	—	0.00	—	ns
t_{DPCEBS}	Clock Enable B Setup Before Clock B Time	—	2.33	—	3.88	—	ns
t_{DPCEBH}	Clock Enable Hold B After Clock B Time	—	-2.95	—	-1.77	—	ns
$t_{DPADDBS}$	Address B Setup Before Clock B Time	—	-0.27	—	-0.16	—	ns
$t_{DPADDBH}$	Address B Hold time After Clock B Time	—	-0.01	—	0.00	—	ns
t_{DPRWBS}	R/W B Setup Before Clock B Time	—	-0.27	—	-0.16	—	ns
t_{DPRWBH}	R/W B Hold time After Clock B Time	—	-0.01	—	0.00	—	ns

ispXPLD 5000MX Family Internal Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
$t_{DPDATABS}$	Write Data B Setup Before Clock B Time	—	-0.27	—	-0.16	—	ns
$t_{DPDATABH}$	Write Data B Hold After Clock B Time	—	-0.01	—	0.00	—	ns
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	4.56	—	8.78	ns
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	4.56	—	8.78	ns
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	2.34	—	ns
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	5.50	ns
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	2.00	—	ns
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.24	—	ns

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ispXPLD 51024MX - Timing v.1.0

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IOH} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5v	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3v	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	ns
t_{IDO} Output Adjusters – Output Signal Modifiers									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	ns
t_{IDO} Output Adjusters – Output Configurations									
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Parameter	-4		-45		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_33_20mA_out	Using 3.3v CMOS Standard, 20mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
CTT25_out	Using CTT 2.5v	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3v	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5v, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5v, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
HSTL_IV_out	Using HSTL 2.5v, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
SSTL2_I_out	Using SSTL 2.5v, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	ns
SSTL2_II_out	Using SSTL 2.5v, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3v, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
SSTL3_II_out	Using SSTL 3.3v, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	ns

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ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
t_{IOH} Input Adjusters							
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5v	t_{IOIN}	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3v	t_{IOIN}	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	ns
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	ns
t_{IDO} Output Adjusters – Output Signal Modifiers							
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	ns
t_{IDO} Output Adjusters – Output Configurations							
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	ns
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	ns
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	ns
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	ns
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
LVCMOS_33_20mA_out	Using 3.3v CMOS Standard, 20mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	ns
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
CTT25_out	Using CTT 2.5v	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	ns
CTT33_out	Using CTT 3.3v	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	ns

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Parameter	-52		-75		Units
			Min.	Max.	Min.	Max.	
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
HSTL_I_out	Using HSTL 2.5v, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
HSTL_III_out	Using HSTL 2.5v, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
HSTL_IV_out	Using HSTL 2.5v, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	ns
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	ns
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	ns
SSTL2_I_out	Using SSTL 2.5v, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	ns
SSTL2_II_out	Using SSTL 2.5v, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	ns
SSTL3_I_out	Using SSTL 3.3v, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	ns
SSTL3_II_out	Using SSTL 3.3v, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	ns

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sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	Output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 250	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 150	ps
$T_{JIT(PERIOD)}$[2]	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 300	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 150	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	600	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		—	1.8	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay (t_{PLL_DELAY})		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specification.
2. Accumulated jitter measured over 10,000 waveform samples.
3. Internal timing for reference only.

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.	Units
sysCONFIG Write Cycle Timing				
t_{SUCS}	Input setup time of CS to CCLK rise	10	—	ns
t_{HCS}	Hold time of CS to CCLK rise	1	—	ns
t_{SUWD}	Input setup time of write data to CCLK rise	10	—	ns
t_{HWD}	Hold time of write data to CCLK rise	0	—	ns
t_{PRGM}	Low time to reset device SRAM	5	50	ns
t_{DINIT}	INIT delay time	—	5	ms
t_{IODISS}	User I/O disable	—	—	ns
t_{IOENSS}	User I/O enable	—	—	ns
t_{WH}	Write clock High pulse width	18	—	ns
t_{WL}	Write clock Low pulse width	18	—	ns
f_{MAXW}	Write f_{MAX}	—	27	MHz
sysCONFIG Read Cycle Timing				
t_{HREAD}	Hold time of READ to CCLK rise	1	—	ns
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—	ns
t_{RH}	READ clock high pulse width	18	—	ns
t_{RL}	READ clock low pulse width	18	—	ns
f_{MAXR}	Read f_{MAX}	—	27	MHz
t_{CORD}	Clock to out for read data	—	25	ns

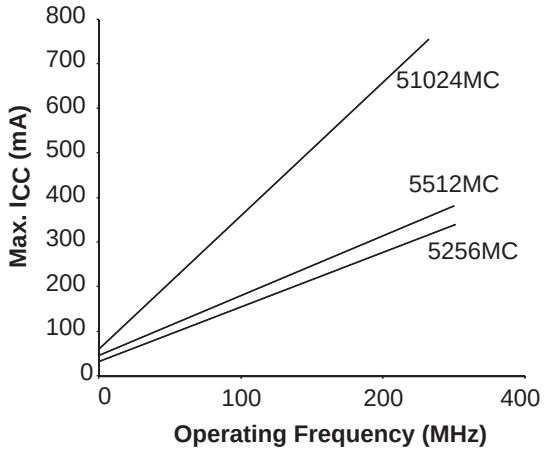
Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

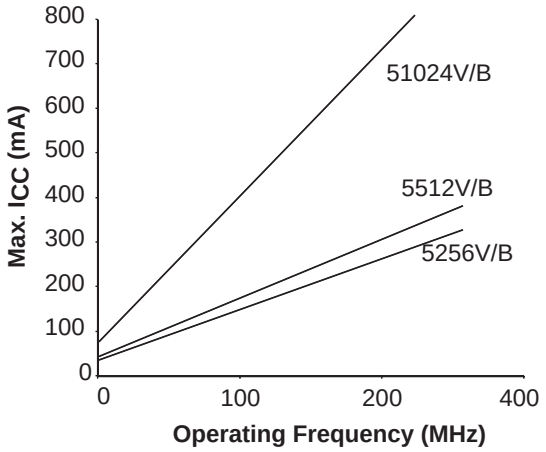
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC	
									ispXPLD 5000MC	ispXPLD 5000MV/B
ispXPLD 5256	2.2	8.4	3.2	7.8	70	0.1379	0.0433	6.476	16	24
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	25
ispXPLD 5768	—	—	—	—	—	—	—	—	—	—
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	43

Note: For further information about the use of these coefficients, refer to technical note TN1031, *Power Estimation in ispXPLD 5000MX Devices.*

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	—	—	—	—
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)

- K10 = Current per row decoder (µA/MHz)
- K11 = Current per column driver (µA/MHz)

Power Estimation Equations

ICC = ICC_DC + IMFB_CPLD + IMFB_ SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL_D

ICC_DC
Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) from the data sheet.

IMFB_CPLD
= ((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** * CPLD GRP from IFB) * AF+ **K4**) * FREQ / 1000µA/mA

IMFB_CAM
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

IMFB_ SRAM/PDPRAM/FIFO
= (WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (**K1** + 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * SRAM/PDPRAM/FIFO Memory MFBs * FREQ / 1000µA/mA

IMFB_ DPRAM
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs * FREQ / 1000µA/mA

IPLL_D
= **K5** * PLL_FREQ * number of PLLs used. IPPL_D is the PLL digital component of the VCC supply current.

Analog portion of PLL supply current consumption, from PLL power pin:

IPLL_A = (**K6** * PLL_FREQ + **K7**) * number of PLLs used

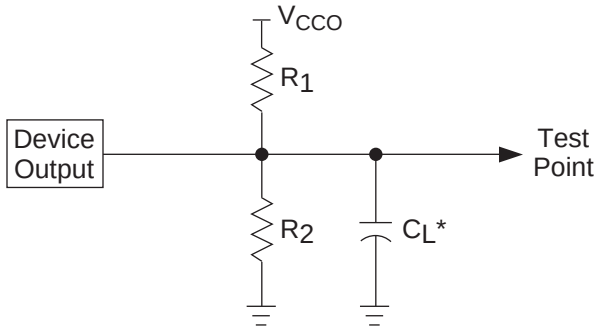
Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the IEEE 1149.1 state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data out.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the registers in the device. The global polarity (active high or active low) for this pin is selectable on a global basis.
yzz	Input/Output – These are the general purpose I/O used by the logic array. *y* is the MFB reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs (see Figure 14 for differential pairing).
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GNDP	GND – Ground for PLLs.
V_{CCP}	V_{CC} – The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG interface.
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2CMOS or IEEE 1149.1 TAP.
PROGRAMB	Input – Controls the programming of SRAM. Hold high for normal operation. Toggle low to reload SRAM from E^2 memory.
CCLK	Input – Clock for sysCONFIG interface. Reads and writes occur on the rising edge of the clock.
READ	Input – Drive high to perform reads from the sysCONFIG interface.
INITB	I/O – Indicates status of configuration. Can be driven low to inhibit configuration.
DONE	Output (open drain) – Indicates status of configuration.

ispXPLD 5000MX Power Supply and NC Connections[1]

Signals	208 PQFP	256 fpBGA	484 fpBGA	672 fpBGA
VCC	10, 49, 76, 114, 153, 180	D4, D13, F6, F11, L6, L11, N4, N13	A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4	AA21, AA6, F21, F6, G20, G7, J13, J14, K13, K14, L13, L14, M13, M14, N10, N11, N12, N15, N16, N17, N18, N9, P10, P11, P12, P15, P16, P17, P18, P9, R13, R14, T13, T14, U13, U14, V13, V14, Y20, Y7
VCCO0	5, 17, 189, 204	A1, F7, G6	B9, C3, G8, G9, H7, J2, J7, P4	H10, H11, H8, H9, J8, J9, K8, L8, M8, N8
VCCO1	42, 57, 72	K6, L7, T1	AA9, R7, T3, T8, Y3	P8, R8, T8, U8, V8, V9, W10, W11, W8, W9
VCCO2	85, 100, 107, 121	K11, L10, T16	AA14, R16, T15, T20, Y20	P19, R19, T19, U19, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19
VCCO3	146, 161, 176	A16, F10, G11	B14, C20, G14, G15, H16, J16, J21, P19	H12, H13, H14, H15, H16, H17, H18, H19, J18, J19, K19, L19, M19, N19
VCCP	136	J16	M22	N25
VCCJ	27	J1	M1	N4
GND	15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174	K1, C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3	N1, A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8	A11, A16, A2, A25, AE1, AE2, AE25, AE26, AF11, AF16, AF2, AF25, B1, B2, B25, B26, J10, J11, J12, J15, J16, J17, K10, K11, K12, K15, K16, K17, K18, K9, L1, L10, L11, L12, L15, L16, L17, L18, L26, L9, M10, M11, M12, M15, M16, M17, M18, M9, N13, N14, P13, P14, R10, R11, R12, R15, R16, R17, R18, R9, T1, T10, T11, T12, T15, T16, T17, T18, T26, T9, U10, U11, U12, U15, U16, U17, U18, U9, V10, V11, V12, V15, V16, V17
GNDP	134	K16	N22	P26
NC[2]	—	**5256MX**: A2, A11, A12, A15, B2, B12, B15, B16, C4, C12, C15, C16, D1, D11, D14, D15, D16, E1, E4, E10, E11, E13, E14, F4, F5, F12, F13, L1, L4, M3, M7, M13, N2, N6, P1, P2, P5, P6, P13, P14, P15, P16, R1, R2, R4, R5, R6, R16, T2, T3, T4, T5, T6 **5512MX**: L1	**5512MX**: P1, AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6 **51024MX**: None	A12, A13, A14, A15, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA7, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AD11, AD12, AD13, AD14, AD15, AD16, AE11, AE12, AE13, AE14, AE15, AE16, AF12, AF13, AF14, AF15, B11, B12, B13, B14, B15, B16, C11, C12, C13, C14, C15, C16, C3, D10, D11, D12, D13, D14, D15, D16, D17, E10, E11, E12, E13, E14, E15, E16, E17, E6, E7, E8, F10, F11, F12, F13, F14, F15, F16, F17, G10, G11, G12, G13, G14, G15, G16, G17, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, VCC or GND.

ispXPLD 5256MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
0	61N	H30	G17	H17	H31	B1
0	61P	H28	G16	H16	H29	C1
0	62N	H26	G15	H15	H27	D3
0	62P	H24	G14	H14	H25	C2
0	63N	H22	G13	H13	H23	E3
0	63P	H21	G12	H12	-	D2
-	-	VCC	-	-	-	VCC
0	64N	H20	G11	H11	-	E2
0	64P	H18/CLK_OUT0	G10	H10	H19	F2
0	65N	H16	G9	H9	H17	F1
0	65P	H14	G8	H8	H15	G1
-	-	GND	-	-	-	GND
0	66N	H12	G7	H7	H13	F3
-	-	VCCO0	-	-	-	VCCO0
0	66P	H10	G6	H6	H11	G5
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	67N	H8/PLLRSTK0	G5	H5	H9	H5
0	67P	H6/PLL_RST0	G4	H4	H7	G4
0	68N	H5	-	-	-	G3
0	68P	H4/PLL_FBK0	-	-	-	H3
0	69N	H2	-	-	H3	G2
0	69P	H0	-	-	H1	H1
-	GCLK0P	GCLK0	-	-	-	H2
-	-	VCCJ	-	-	-	J1
-	GCLK0N	GCLK1	-	-	-	J2
-	-	GND	-	-	-	GND
-	-	TDI	-	-	-	H6
-	-	TMS	-	-	-	H4
-	-	TCK	-	-	-	J6
-	-	TDO	-	-	-	K2
1	0P	A0/DATA0	A0	B0	A1	K3
1	0N	A2/DATA1	A1	B1	A3	J3
1	1P	A4/DATA2	A2	B2	-	J5
1	1N	A5/DATA3	A3	B3	-	J4
1	2P	A6/DATA4	A4	B4	A7	L2
1	2N	A8/DATA5	A5	B5	A9	M1
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	3P	A10/DATA6	A6	B6	A11	K4
-	-	VCCO1	-	-	-	VCCO1
1	3N	A12/DATA7	A7	B7	A13	L3
-	-	GND	-	-	-	GND
1	4P	A14/INITB	A8	B8	A15	K5

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
1	4N	A16/CSB	A9	B9	A17	L5
1	5P	A18/READ	A10	B10	A19	N1
1	5N	A20/CCLK	A11	B11	A21	M2
-	-	VCC	-	-	-	VCC
-	-	DONE	-	-	-	M4
1	6P	A22	A12	B12	A23	N3
1	6N	A24	A13	B13	A25	P4
1	7P	A26	A14	B14	A27	N5
1	7N	A28	A15	B15	A29	M6
-	-	PROGRAMB	-	-	-	R3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
-	-	VCCO1	-	-	-	VCC01
-	-	CFG0	-	-	-	L8
1	8P	B2	A16	B16	B3	T7
1	8N	B4	A17	B17	-	R7
1	9P	B5	A18	B18	-	N7
1	9N	B6	A19	B19	B7	P7
1	10P	B8	A20	B20	B9	T8
1	10N	B10	A21	B21	B11	R8
1	11P	B12	A22	B22	B13	M8
1	11N	B14	A23	B23	B15	P8
1	-	B16/VREF1	-	-	B17	L9
1	12P	B18	A24	B24	B19	N8
1	12N	B20	A25	B25	-	M9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)
1	13P	B21	A26	B26	-	N10
-	-	VCCO1	-	-	-	VCCO1
1	13N	B22	A27	B27	B23	T9
1	14P	B24	A28	B28	B25	T10
1	14N	B26	A29	B29	B27	R9
-	-	VCC	-	-	-	VCC
1	15P	B28	A30	B30	B29	P9
1	15N	B30	A31	B31	B31	N9
2	16P	C0	C0	D0	C1	T11
2	16N	C2	C1	D1	C3	T12
-	-	GND	-	-	-	NC
2	17P	C4	C2	D2	-	P10
2	17N	C5	C3	D3	-	R10
2	18P	C6	C4	D4	C7	R11
-	-	VCCO2	-	-	-	VCCO2
2	18N	C8	C5	D5	C9	M10
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	19P	C10	C6	D6	C11	M11

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
2	19N	C12	C7	D7	C13	T13
2	20P	C14	-	-	C15	P11
2	20N	C16/VREF2	-	-	C17	T14
2	21P	C18	C8	D8	C19	R12
2	21N	C20	C9	D9	-	R13
2	22P	C21	C10	D10	-	N11
2	22N	C22	C11	D11	C23	T15
2	23P	C24	C12	D12	C25	R14
2	23N	C26	C13	D13	C27	N12
2	24P	C28	C14	D14	C29	P12
2	24N	C30	C15	D15	C31	R15
-	-	VCCO2	-	-	-	VCCO2
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	25P	D0	-	-	D1	N15
2	25N	D2	-	-	D3	N14
2	26P	D4	C16	D16	-	N16
2	26N	D5	C17	D17	-	M16
2	27P	D6	C18	D18	D7	M14
2	27N	D8	C19	D19	D9	M15
-	-	VCC	-	-	-	VCC
2	28P	D10	C20	D20	D11	L13
2	28N	D12	C21	D21	D13	L12
2	29P	D14	C22	D22	D15	L15
2	29N	D16	C23	D23	D17	L16
-	-	GND	-	-	-	GND
2	30P	D18	C24	D24	D19	L14
-	-	VCCO2	-	-	-	VCCO2
2	30N	D20	C25	D25	-	K15
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)
2	31P	D21	C26	D26	-	K14
2	31N	D22	C27	D27	D23	K12
2	32P	D24	C28	D28	D25	K13
2	32N	D26	C29	D29	D27	J13
2	33P	D28	C30	D30	D29	J14
2	33N	D30	C31	D31	D31	J12
-	-	TOE	-	-	-	J15
-	-	RESET	-	-	-	J11
-	-	GOE0	-	-	-	H11
-	-	GOE1	-	-	-	H13
-	-	GNDP	-	-	-	K16
-	GCLK3N	GCLK2	-	-	-	H15
-	-	VCCP	-	-	-	J16
-	GCLK3P	GCLK3	-	-	-	H16

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	34N	E30	-	-	E31	H14
3	34P	E28	-	-	E29	G16
3	35N	E26	-	-	E27	G15
3	35P	E24/PLL_FBK1	-	-	E25	F15
3	36N	E22/PLL_RST1	E27	F27	E23	H12
3	36P	E21/PLLRSTK1	E26	F26	-	G14
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	37N	E20	E25	F25	-	F16
-	-	VCCO3	-	-	-	VCCO3
3	37P	E18	E24	F24	E19	E16
-	-	GND	-	-	-	GND
3	38N	E16	E23	F23	E17	G13
3	38P	E14	E22	F22	E15	G12
3	39N	E12	E21	F21	E13	F14
3	39P	E10/CLK_OUT1	E20	F20	E11	E15
-	-	VCC	-	-	-	VCC
3	40N	E8	E19	F19	E9	D12
3	40P	E6	E18	F18	E7	B14
3	41N	E5	E17	F17	-	C13
3	41P	E4	E16	F16	-	A14
3	42N	E2	E31	F31	E3	A13
3	42P	E0	E30	F30	E1	B13
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
-	-	VCCO3	-	-	-	VCCO3
3	43N	F30	E15	F15	F31	B11
3	43P	F28	E14	F14	F29	C11
3	44N	F26	E13	F13	F27	B10
3	44P	F24	E12	F12	F25	A10
3	45N	F22	E11	F11	F23	C10
3	45P	F21	E10	F10	-	D10
3	46N	F20	E9	F9	-	C9
3	46P	F18	E8	F8	F19	E9
3	47N	F16/VREF3	E29	F29	F17	D9
3	47P	F14	E28	F28	F15	F9
3	48N	F12	E7	F7	F13	A9
3	48P	F10	E6	F6	F11	F8
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)
3	49N	F8	E5	F5	F9	E8
-	-	VCCO3	-	-	-	VCCO3
3	49P	F6	E4	F4	F7	A8
3	50N	F5	E3	F3	-	B9
3	50P	F4	E2	F2	-	D8
-	-	VCC	-	-	-	VCC

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	256 fpBGA Ball Number
			Macrocell 1	Macrocell 2		
3	51N	F2	E1	F1	F3	B8
3	51P	F0	E0	F0	F1	C8
0	52N	G30	G31	H31	G31	B7
0	52P	G28	G30	H30	G29	A7
-	-	GND	-	-	-	NC
0	53N	G26	G29	H29	G27	D7
0	53P	G24	G28	H28	G25	C7
0	54N	G22	G27	H27	G23	B6
-	-	VCCO0	-	-	-	VCCO0
0	54P	G21	G26	H26	-	E7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)
0	55N	G20	G25	H25	-	E6
0	55P	G18	G24	H24	G19	A6
0	56N	G16/VREF0	G3	H3	G17	A5
0	56P	G14	G2	H2	G15	A4
0	57N	G12	G23	H23	G13	B5
0	57P	G10	G22	H22	G11	A3
0	58N	G8	G21	H21	G9	B4
0	58P	G6	G20	H20	G7	B3
0	59N	G5	G19	H19	-	C5
0	59P	G4	G18	H18	-	C6
0	60N	G2	G1	H1	G3	D5
0	60P	G0	G0	H0	G1	D6
-	-	VCCO0	-	-	-	VCCO0
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	B4
0	109P	O28	O10	P16	O29	1	E4	A4
0	110N	O26	M17	O17	O27	2	B1	B3
0	110P	O24	M16	O16	O25	3	C1	A3
0	111N	O22	M15	O15	O23	4	D3	F5
—	—	V_{CCO0}	—	—	—	5	V_{CCO0}	V_{CCO0}
0	111P	O20	M14	O14	O21	6	C2	G6
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	GND (Bank 0)
0	112N	O18	M13	O13	O19	8	E3	H6
0	112P	O16	M12	O12	O17	9	D2	G5
0	113N	O14	O9	P14	O15	NC	NC	D3
0	113P	O12	O8	P12	O13	NC	NC	D2
0	114N	O10	O7	P10	O11	NC	NC	E4
0	114P	O8	O6	P8	O9	NC	NC	E3
0	115N	O6	O5	P6	O7	NC	NC	F4
0	115P	O4	O4	P4	O5	NC	NC	G4
0	116N	O2	O3	P2	O3	NC	NC	C2
—	—	V_{CCO0}	—	—	—	NC	V_{CCO0}	V_{CCO0}
0	116P	O0	O2	P0	O1	NC	NC	C1
—	—	GND (Bank 0)	—	—	—	NC	GND (Bank 0)	GND (Bank 0)
0	117N	P30	O1	—	P31	NC	D1	F3
0	117P	P28	O0	—	P29	NC	E1	G3
0	118N	P26	O31	—	P27	NC	F4	H4
—	—	V_{CC}	—	—	—	10	V_{CC}	V_{CC}
0	118P	P24	O30	—	P25	NC	F5	J4
0	119N	P22	M11	O11	P23	11	E2	H5
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	J5
0	120N	P18	M9	O9	P19	13	F1	E2
0	120P	P16	M8	O8	P17	14	G1	F2
—	—	GND	—	—	—	15	GND	GND
0	121N	P14	M7	O7	P15	16	F3	D1
—	—	V_{CCO0}	—	—	—	17	V_{CCO0}	V_{CCO0}
0	121P	P12	M6	O6	P13	18	G5	E1
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	GND (Bank 0)
0	122N	P10	M5	O5	P11	20	H5	J3
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	H2
0	123N	P6	—	—	P7	22	G3	G2
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	G1
0	124N	P2	—	—	P3	24	G2	H1
0	124P	P0	—	—	P1	25	H1	J1
—	GCLK0P	GCLK0	—	—	—	26	H2	N7
—	—	V_{CCJ}	—	—	—	27	J1	M1
—	GCLK0N	GCLK1	—	—	—	28	J2	P7

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
—	—	GND	—	—	—	29	GND	GND
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	V_{CCO1}
1	3N	A14/DATA7	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	NC	NC	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	NC	P1[1]	V3
1	7P	A28	—	—	A29	NC	M3	Y2
1	7N	A30	—	—	A31	NC	L4	W3
1	8P	B0	A0	—	B1	NC	N2	U5
1	8N	B2	A2	—	B3	NC	P2	T5
—	—	GND (Bank 1)	—	—	—	NC	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	NC	R1	U4
—	—	V_{CCO1}	—	—	—	NC	V_{CCO1}	V_{CCO1}
1	9N	B5	A6	—	—	NC	R2	V4
1	10P	B6	A8	—	B7	NC	T2	AA3
1	10N	B8	A10	—	B9	NC	T3	AB3
1	—	B10	A12	—	B11	NC	NC	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	NC	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)
1	13P	B24	A16	—	B25	NC	T4	V6

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	NC	T5	V7
1	14P	B28	A20	—	B29	NC	R4	Y5
1	14N	B30	A22	—	B31	NC	N6	AA5
1	15P	C0	—	—	C1	NC	R5	Y6
1	15N	C2	—	—	C3	NC	P6	Y7
1	16P	C4	—	—	C5	NC	NC	AA6
1	16N	C8	—	—	C9	NC	NC	AA7
1	17P	C10	—	—	C11	NC	NC	W7
1	17N	C12	—	—	C13	NC	M7[1]	V8
1	18P	C16	—	—	C17	NC	T6	W8
1	18N	C18	—	—	C19	NC	R6	U9
—	—	GND0 (Bank 1)	—	—	—	NC	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	NC	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	NC	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	V_{CCO2}

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
2	29N	E10	F5	H5	E11	86	M10	U12
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	GND (Bank 2)
2	30P	E12	F6	H6	E13	88	M11	AB13
2	30N	E16	F7	H7	E17	89	T13	Y13
2	31P	E18	—	—	E19	90	P11	V13
2	31N	E20/V_{REF2}	—	—	E21	91	T14	W13
2	32P	E22	F8	H8	E23	92	R12	V14
2	32N	E24	F9	H9	E25	93	R13	W14
2	33P	E26	F10	H10	E27	94	N11	Y14
2	33N	E28	F11	H11	E29	95	T15	AB14
2	34P	F0	F12	H12	F1	96	R14	AB15
2	34N	F2	F13	H13	F3	97	N12	AA15
2	35P	F4	F14	H14	F5	98	P12	U13
—	—	V_{CCO2}	—	—	—	NC	V_{CCO2}	V_{CCO2}
2	35N	F6	F15	H15	F7	99	R15	U14
—	—	GND (Bank 2)	—	—	—	NC	GND (Bank 2)	GND (Bank 2)
2	36P	F8	E0	—	F9	NC	NC	W15
2	36N	F10	E2	—	F11	NC	NC	W16
2	37P	F12	E4	—	F13	NC	NC	Y16
2	37N	F16	E6	—	F17	NC	NC	AA16
2	38P	F18	E8	—	F19	NC	NC	AB16
2	38N	F20	E10	—	F21	NC	NC	AA17
2	39P	F22	E12	—	F23	NC	NC	Y17
2	39N	F24	E16	—	F25	NC	NC	AA18
2	40P	F26	E20	—	F27	NC	NC	W17
2	40N	F28	E22	—	F29	NC	NC	W18
2	41P	G0	—	—	G1	NC	NC	V15
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	V_{CCO2}
2	41N	G2	—	—	G3	NC	NC	U15
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	GND (Bank 2)
2	42P	G4	—	—	G5	102	P13	Y18
2	42N	G6	—	—	G7	103	P15	V17
2	43P	G8	—	—	G9	NC	M13	V16
2	43N	G10	—	—	G11	NC	P14	U16
2	44P	G12	—	—	G13	NC	NC	AB18
2	44N	G14	—	—	G15	NC	NC	AB19
2	45P	G16	—	—	G17	NC	NC	U18
2	45N	G18	—	—	G19	NC	NC	T17
2	46P	G20	—	—	G21	104	R16	AB20
2	46N	G22	—	—	G23	105	P16	AA20
2	47P	G24	—	—	G25	106	N15	Y19
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	V_{CCO2}
2	47N	G26	—	—	G27	108	N14	V19

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	NC	NC	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	NC	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	134	K16	N22
—	GCLK3N	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	136	J16	M22
—	GCLK3P	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND
3	61N	I14	I23	K23	I15	149	G13	D22

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
3	61P	I12	I22	K22	I13	150	G12	D21
3	62N	I10	I21	K21	I11	151	F14	J20
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	J19
3	63N	I6	K31	—	I7	NC	F12	E20
—	—	V_{CC}	—	—	—	153	VCC	VCC
3	63P	I4	K30	L30	I5	NC	F13	F20
3	64N	I2	K29	L28	I3	NC	D16	H17
3	64P	I0	K28	L26	I1	NC	D15	H18
—	—	GND (Bank 3)	—	—	—	NC	GND (Bank 3)	GND (Bank 3)
3	65N	J30	K27	—	J31	NC	NC	J18
—	—	V_{CCO3}	—	—	—	NC	V_{CCO3}	V_{CCO3}
3	65P	J28	K26	—	J29	NC	NC	H19
3	66N	J26	K25	—	J27	NC	NC	G20
3	66P	J24	K24	—	J25	NC	NC	G19
3	67N	J22	K23	—	J23	NC	NC	C22
3	67P	J20	K22	—	J21	NC	NC	C21
3	68N	J18	K21	—	J19	NC	NC	D20
3	68P	J16	K20	—	J17	NC	NC	C19
3	69N	J14	K19	—	J15	NC	C16	F19
3	69P	J12	K18	—	J13	NC	B16	E19
—	—	GND (Bank 3)	—	—	—	NC	GND (Bank 3)	GND (Bank 3)
3	70N	J10	K17	—	J11	NC	C15	G18
—	—	V_{CCO3}	—	—	—	NC	V_{CCO3}	V_{CCO3}
3	70P	J8	K16	—	J9	NC	B15	F18
3	71N	J6	K15	—	J7	NC	E14	B20
3	71P	J4	K14	—	J5	NC	D14	B19
3	72N	J2	K13	—	J3	NC	E13	A20
3	72P	J0	K12	—	J1	NC	A15	A19
3	73N	K30	I19	K19	K31	154	D12	D18
3	73P	K28	I18	K18	K29	155	B14	C18
3	74N	K26	I17	K17	K27	156	C13	G17
3	74P	K24	I16	K16	K25	157	A14	F16
3	75N	K22	I31	K31	K23	158	A13	E17
3	75P	K21	I30	K30	—	159	B13	D17
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	GND (Bank 3)
3	76N	K20	K11	L21	—	NC	D11	B18
—	—	V_{CCO3}	—	—	—	161	V_{CCO3}	V_{CCO3}
3	76P	K18	K10	L20	K19	NC	B12	A18
3	77N	K16	K9	L18	K17	NC	C12	C17
3	77P	K14	K8	L16	K15	NC	E11	B17
3	78N	K12	K7	L12	K13	NC	NC	C16
3	78P	K10	K6	L10	K11	NC	NC	B16
3	79N	K8	K5	L8	K9	NC	NC	F13

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
3	79P	K6	K4	L6	K7	NC	NC	F15
3	80N	K5	K3	L5	—	NC	NC	D16
3	80P	K4	K2	L4	—	NC	E10[1]	E16
3	81N	K2	K1	L2	K3	NC	A12	A16
3	81P	K0	K0	L0	K1	NC	A11	A15
—	—	GND (Bank 3)	—	—	—	NC	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	NC	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	—	167	D10	F14
3	85N	L20	I9	K9	—	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	VCC	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	NC	GND
—	—	GND	—	—	—	NC	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10
0	96N	M12	M23	O23	M13	196	B5	A10

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
0	96P	M10	M22	O22	M11	197	A3	A9
0	97N	M8	M21	O21	M9	198	B4	C9
0	97P	M6	M20	O20	M7	199	B3	D9
0	98N	M5	M19	O19	—	200	C5	F9
0	98P	M4	M18	O18	—	201	C6	E9
0	99N	M2	M1	O1	M3	202	D5	A8
—	—	V_{CCO0}	—	—	—	NC	V_{CCO0}	V_{CCO0}
0	99P	M0	M0	O0	M1	203	D6	B8
—	—	GND (Bank 0)	—	—	—	NC	GND (Bank 0)	GND (Bank 0)
0	100N	N30	O29	—	N31	NC	NC	A7
0	100P	N28	O28	—	N29	NC	NC	B7
0	101N	N26	O27	—	N27	NC	NC	A5
0	101P	N24	O26	—	N25	NC	NC	B5
0	102N	N22	O25	—	N23	NC	NC	B6
0	102P	N21	O24	—	—	NC	NC	C7
0	103N	N20	O23	—	—	NC	NC	E8
0	103P	N18	O22	—	N19	NC	NC	E7
0	104N	N16	O21	—	N17	NC	NC	E6
0	104P	N14	O20	—	N15	NC	NC	D6
0	105N	N12	O19	—	N13	NC	NC	D8
—	—	V_{CCO0}	—	—	—	204	V_{CCO0}	V_{CCO0}
0	105P	N10	O18	—	N11	NC	NC	F8
—	—	GND (Bank 0)	—	—	—	205	GND (Bank 0)	GND (Bank 0)
0	106N	N8	O17	—	N9	NC	NC	F7
0	106P	N6	O16	—	N7	NC	NC	D7
0	107N	N5	O15	—	—	206	A2	C6
0	107P	N4	O14	—	—	207	B2	C5
0	108N	N2	O13	—	N3	NC	NC	C4
0	108P	N0	O12	—	N1	NC	NC	D5

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 51024MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	159N	AA22	AA11	AB18	AA23	B4	C2
0	159P	AA20	AA10	AB16	AA21	A4	C1
0	160N	AA18	Y17	AA17	AA19	B3	D4
0	160P	AA16	Y16	AA16	AA17	A3	D3
0	161N	AA14	Y15	AA15	AA15	F5	D2
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	161P	AA12	Y14	AA14	AA13	G6	D1
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	162N	AA10	Y13	AA13	AA11	H6	E5
0	162P	AA8	Y12	AA12	AA9	G5	E4
0	163N	AA6	AA9	AB14	AA7	D3	E3
0	163P	AA4	AA8	AB12	AA5	D2	E2
0	164N	AA2	AA7	AB10	AA3	E4	E1
-	-	VCC	-	-	-	VCC	VCC
0	164P	AA0	AA6	AB8	AA1	E3	F2
-	-	GND	-	-	-	GND	GND
0	165N	AB30	AA5	AB6	AB31	F4	F5
0	165P	AB28	AA4	AB4	AB29	G4	G6
0	166N	AB26	AA3	AB2	AB27	C2	F4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	166P	AB24	AA2	AB0	AB25	C1	F3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	167N	AB22	AA1	-	AB23	F3	F1
0	167P	AB20	AA0	-	AB21	G3	G1
0	168N	AB18	AA31	-	AB19	H4	G5
-	-	VCC	-	-		VCC	VCC
0	168P	AB16	AA30	-	AB17	J4	G4
0	169N	AB14	Y11	AA11	AB15	H5	H7
0	169P	AB12/CLK_OUT0	Y10	AA10	AB13	J5	J7
0	170N	AB10	Y9	AA9	AB11	E2	G3
0	170P	AB8	Y8	AA8	AB9	F2	G2
-	-	GND	-	-	-	GND	GND
0	171N	AB6	Y7	AA7	AB7	D1	H6
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	171P	AB4	Y6	AA6	AB5	E1	J6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	172N	AB2	Y5	AA5	AB3	J3	H5
0	172P	AB0/PLL_RST0	Y4	AA4	AB1	H2	H4
0	173N	AC30	AC31	AE31	AC31	G2	H3
0	173P	AC28/PLL_FBK0	AC30	AE30	AC29	G1	H2
0	174N	AC26	AC29	AE29	AC27	J6	H1
0	174P	AC24	AC28	AE28	AC25	K4	J1

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	J5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	175P	AC20	AC26	AE26	AC21	K3	J4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	176N	AC18	AC25	AE25	AC19	K5	K7
0	176P	AC16	AC24	AE24	AC17	K2	L7
0	177N	AC14	AC23	AE23	AC15	L5	J3
0	177P	AC12	AC22	AE22	AC13	K1	J2
0	178N	AC10	AC21	AE21	AC11	L6	K6
0	178P	AC8	AC20	AE20	AC9	L1	L6
0	179N	AC6	AC19	AE19	AC7	M5	K5
0	179P	AC4	AC18	AE18	AC5	L2	K4
0	180N	AC2	AC17	AE17	AC3	N5	K3
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	180P	AC0	AC16	AE16	AC1	L3	K2
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	181N	AE30	AC15	AE15	AE31	M6	K1
0	181P	AE28	AC14	AE14	AE29	M2	L2
0	182N	AE26	AC13	AE13	AE27	P5	L5
-	-	VCC	-	-	-	VCC	VCC
0	182P	AE24	AC12	AE12	AE25	P6	L4
0	183N	AE22	AC11	AE11	AE23	M3	L3
0	183P	AE20	AC10	AE10	AE21	N6	M3
0	184N	AE18	AC9	AE9	AE19	N2	M7
0	184P	AE16	AC8	AE8	AE17	P1	N7
-	-	GND	-	-	-	GND	GND
0	185N	AE14	AC7	AE7	AE15	N3	M5
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	185P	AE12	AC6	AE6	AE13	M8	M4
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	186N	AE10	AC5	AE5	AE11	N8	M6
0	186P	AE8	AC4	AE4	AE9	P2	N6
0	187N	AE6	AC3	AE3	AE7	P8	M2
0	187P	AE4	AC2	AE2	AE5	N4	M1
0	188N	AE2	AC1	AE1	AE3	H1	N1
0	188P	AE0	AC0	AE0	AE1	J1	N2
-	GCLK0P	GCLK0	-	-	-	N7	N5
-	-	VCCJ	-	-	-	M1	N4
-	GCLK0N	GCLK1	-	-	-	P7	N3
-	-	GND	-	-	-	GND	GND
-	-	TDI	-	-	-	R1	P4
-	-	TMS	-	-	-	R2	P5
-	-	TCK	-	-	-	T1	P3

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	TDO	-	-	-	V1	P2
1	0P	A30	A0	C0	A31	NC	P1
1	0N	A28	A1	C1	A29	NC	R1
1	1P	A26	A2	C2	A27	NC	P6
1	1N	A24	A3	C3	A25	NC	R6
1	2P	A22	A4	C4	A23	NC	P7
1	2N	A20	A5	C5	A21	NC	R7
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	3P	A18	A6	C6	A19	NC	R4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	3N	A16	A7	C7	A17	NC	R5
-	-	GND	-	-	-	GND	GND
1	4P	A14	A8	C8	A15	NC	R3
-	-	VCC	-	-	-	VCC	VCC
1	4N	A12	A9	C9	A13	NC	R2
1	5P	A10	A10	C10	A11	NC	T2
1	5N	A8	A11	C11	A9	NC	T3
1	6P	A6	A12	C12	A7	NC	T4
1	6N	A4	A13	C13	A5	NC	T5
1	7P	A2	A14	C14	A3	NC	U2
1	7N	A0	A15	C15	A1	NC	U3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	8P	C30	A16	C16	C31	NC	U4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	8N	C28	A17	C17	C29	NC	U5
1	9P	C26	A18	C18	C27	NC	T6
1	9N	C24	A19	C19	C25	NC	U6
1	10P	C22	A20	C20	C23	NC	T7
1	10N	C20	A21	C21	C21	NC	U7
1	11P	C18	A22	C22	C19	NC	U1
1	11N	C16	A23	C23	C17	NC	V1
1	12P	C14	A24	C24	C15	NC	V2
1	12N	C12	A25	C25	C13	NC	V3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	13P	C10	A26	C26	C11	NC	V5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	13N	C8	A27	C27	C9	NC	V4
-	-	GND	-	-	-	GND	GND
1	14P	C6	A28	C28	C7	NC	W2
-	-	VCC	-	-	-	VCC	VCC
1	14N	C4	A29	C29	C5	NC	W3
1	15P	C2	A30	C30	C3	NC	W4
1	15N	C0	A31	C31	C1	NC	W5

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	16P	E30/DATA0	G0	E0	E31	W1	W1
1	16N	E28/DATA1	G1	E1	E29	Y1	Y1
1	17P	E26/DATA2	G2	E2	E27	P3	V6
1	17N	E24/DATA3	G3	E3	E25	R3	W6
1	18P	E22/DATA4	G4	E4	E23	T2	Y2
1	18N	E20/DATA5	G5	E5	E21	U2	Y3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	19P	E18/DATA6	G6	E6	E19	V2	Y4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	19N	E16/DATA7	G7	E7	E17	W2	Y5
-	-	GND	-	-	-	GND	GND
1	20P	E14/INITB	G8	E8	E15	R4	V7
1	20N	E12/CSB	G9	E9	E13	T4	W7
1	21P	E10/READ	G10	E10	E11	R6	AA1
1	21N	E8/CCLK	G11	E11	E9	R5	AA2
1	22P	E6	-	-	E7	U3	AA3
-	-	VCC	-	-	-	VCC	VCC
1	22N	E4	-	-	E5	V3	AA4
1	23P	E2	-	-	E3	Y2	Y6
1	23N	E0	-	-	E1	W3	AA5
1	24P	F30	H0	-	F31	U5	AB2
1	24N	F28	H2	-	F29	T5	AB3
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	25P	F26	H4		F27	U4	AB4
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	25N	F24	H6	-	F25	V4	AB5
1	26P	F22	H8	-	F23	AA3	AB1
1	26N	F20	H10	-	F21	AB3	AC2
1	-	F18	H12	-	F19	Y4	AC3
-	-	DONE	-	-	-	AA4	AC4
1	27P	F14	-	-	F15	AB2	AC1
1	27N	F12	-	-	F13	U6	AD1
-	-	GNDIO1	-	-	-	GNDIO1	GNDIO1
1	28P	F10			F11	V5	AD2
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	28N	F8			F9	W6	AD3
1	29P	F6	G12	E12	F7	AB4	Y8
1	29N	F4	G13	E13	F5	AB5	Y9
1	30P	F2	G14	E14	F3	T6	AA8
1	30N	F0	G15	E15	F1	U7	AA9
-	-	PROGRAMB	-	-	-	W5	AB8
1	-	G28	H14	-	G29	U8	AB9
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
1	31P	G26	H16	-	G27	V6	AB7
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	31N	G24	H18	-	G25	V7	AC7
-	-	GND	-	-	-	GND	GND
1	32P	G22	H20	-	G23	Y5	AB6
-	-	VCC	-	-	-	VCC	VCC
1	32N	G20	H22	-	G21	AA5	AC6
1	33P	G18	-	-	G19	Y6	AC8
1	33N	G16	-	-	G17	Y7	AC9
1	34P	G14	-	-	G15	AA6	AC5
1	34N	G12	-	-	G13	AA7	AD4
1	35P	G10	-	-	G11	W7	AD5
1	35N	G8	-	-	G9	V8	AD6
1	36P	G6	-	-	G7	W8	AD7
1	36N	G4	-	-	G5	U9	AD8
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
-	-	CFG0	-	-	-	U10	AE3
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	37P	G0	G16	E16	G1	AB7	AD9
1	37N	H30	G17	E17	H31	AA8	AD10
1	38P	H28	G18	E18	H29	AB8	AE4
1	38N	H26	G19	E19	H27	AB9	AE5
1	39P	H24	G20	E20	H25	W9	AE6
1	39N	H22	G21	E21	H23	Y9	AE7
1	40P	H20	G22	E22	H21	AB10	AE8
1	40N	H18	G23	E23	H19	AA10	AE9
1	-	H16/VREF1	-	-	H17	W10	AE10
1	41P	H14	G24	E24	H15	Y10	AF3
1	41N	H12	G25	E25	H13	Y11	AF4
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	GND (Bank 1)
1	42P	H10	G26	E26	H11	V9	AF5
-	-	VCCO1	-	-	-	VCCO1	VCCO1
1	42N	H8	G27	E27	H9	V10	AF6
1	43P	H6	G28	E28	H7	AA11	AF7
-	-	GND	-	-	-	GND	GND
1	43N	H4	G29	E29	H5	AB11	AF8
-	-	VCC	-	-	-	VCC	VCC
1	44P	H2	G30	E30	H3	U11	AF9
1	44N	H0	G31	E31	H1	V11	AF10
2	45P	I0	J0	L0	I1	AB12	AF17
-	-	VCC	-	-	-	VCC	VCC
2	45N	I2	J1	L1	I3	AA12	AF18
-	-	GND	-	-	-	GND	GND

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	46P	I4	J2	L2	I5	Y12	AF19
2	46N	I6	J3	L3	I7	AA13	AF20
2	47P	I8	J4	L4	I9	V12	AF21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	47N	I10	J5	L5	I11	U12	AF22
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	48P	I12	J6	L6	I13	AB13	AF23
2	48N	I14	J7	L7	I15	Y13	AF24
2	49P	I16	L0	-	I17	V13	AE17
2	49N	I18/VREF2	L1	-	I19	W13	AE18
2	50P	I20	J8	L8	I21	V14	AE19
2	50N	I22	J9	L9	I23	W14	AE20
2	51P	I24	J10	L10	I25	Y14	AE21
2	51N	I26	J11	L11	I27	AB14	AE22
2	52P	I28	J12	L12	I29	AB15	AE23
2	52N	I30	J13	L13	I31	AA15	AE24
2	53P	J0	J14	L14	J1	U13	AD17
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	53N	J2	J15	L15	J3	U14	AD18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	54P	J4	L2	I0	J5	W15	AD19
2	54N	J6	L3	I2	J7	W16	AD20
2	55P	J8	L4	I4	J9	Y16	AD21
2	55N	J10	L5	I6	J11	AA16	AD22
2	56P	J12	L6	I8	J13	AB16	AD23
2	56N	J14	L7	I10	J15	AA17	AD24
2	57P	J16	L8	I12	J17	Y17	AC22
2	57N	J18	L9	I16	J19	AA18	AC21
2	58P	J20	L10	I20	J21	W17	AC18
-	-	VCC	-	-	-	VCC	VCC
2	58N	J22	L11	I22	J23	W18	AC19
-	-	GND	-	-	-	GND	GND
2	59P	J24	L12	-	J25	V15	AC20
-	-	VCCO2		-	-	VCCO2	VCCO2
2	59N	J26	L13	-	J27	U15	AB21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	60P	J28	L14	-	J29	Y18	AB18
2	60N	J30	L15	-	J31	V17	AB19
2	61P	K0	L16	-	K1	V16	AB20
2	61N	K2	L17	-	K3	U16	AA20
2	62P	K4	L18	-	K5	AB18	AA19
2	62N	K6	L19	-	K7	AB19	Y19
2	63P	K8	L20	-	K9	AA19	AA18

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	63N	K10	L21	-	K11	U17	Y18
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	64P	K12	L22	-	K13	V18	AD25
2	64N	K14	L23	-	K15	AB21	AD26
2	65P	K16	L24	-	K17	U18	AC23
2	65N	K18	L25	-	K19	T17	AC24
2	66P	K20	L26	-	K21	AB20	AC25
2	66N	K22	L27	-	K23	AA20	AC26
2	67P	K24	L28	-	K25	Y19	AB22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	67N	K26	L29	-	K27	V19	AB23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	68P	K28	J16	L16	K29	T18	AB24
2	68N	K30	J17	L17	K31	R17	AB25
2	69P	L0	J18	L18	L1	U19	AB26
2	69N	L2	J19	L19	L3	T19	AA26
2	70P	L4	L30	I24	L5	V20	AA22
-	-	VCC	-	-	-	VCC	VCC
2	70N	L6	L31	I26	L7	U20	Y21
2	71P	L8	J20	L20	L9	W20	AA23
2	71N	L10	J21	L21	L11	Y21	AA24
2	72P	L12	J22	L22	L13	R18	AA25
2	72N	L14	J23	L23	L15	R19	Y26
-	-	GND	-	-	-	GND	GND
2	73P	L16	J24	L24	L17	W21	Y22
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	73N	L18	J25	L25	L19	Y22	Y23
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	74P	L20	J26	L26	L21	R20	W20
2	74N	L22	J27	L27	L23	P20	V20
2	75P	L24	J28	L28	L25	T21	W21
2	75N	L26	J29	L29	L27	R21	V21
2	76P	L28	J30	L30	L29	U21	Y24
2	76N	L30	J31	L31	L31	V21	Y25
2	77P	N0	P0	N0	N1	NC	W22
2	77N	N2	P1	N1	N3	NC	W23
2	78P	N4	P2	N2	N5	NC	W24
-	-	VCC	-	-	-	VCC	VCC
2	78N	N6	P3	N3	N7	NC	W25
-	-	GND	-	-	-	GND	GND
2	79P	N8	P4	N4	N9	NC	W26
-	-	VCCO2	-	-	-	VCCO2	VCCO2

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
2	79N	N10	P5	N5	N11	NC	V26
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	80P	N12	P6	N6	N13	NC	V22
2	80N	N14	P7	N7	N15	NC	V23
2	81P	N16	P8	N8	N17	NC	V24
2	81N	N18	P9	N9	N19	NC	V25
2	82P	N20	P10	N10	N21	NC	U20
2	82N	N22	P11	N11	N23	NC	T20
2	83P	N24	P12	N12	N25	NC	U26
2	83N	N26	P13	N13	N27	NC	U25
2	84P	N28	P14	N14	N29	NC	U21
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	84N	N30	P15	N15	N31	NC	T21
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	85P	P0	P16	N16	P1	NC	U22
2	85N	P2	P17	N17	P3	NC	U23
2	86P	P4	P18	N18	P5	NC	U24
2	86N	P6	P19	N19	P7	NC	T24
2	87P	P8	P20	N20	P9	NC	T23
2	87N	P10	P21	N21	P11	NC	T22
2	88P	P12	P22	N22	P13	NC	T25
-	-	VCC	-	-	-	VCC	VCC
2	88N	P14	P23	N23	P15	NC	R26
-	-	GND	-	-	-	GND	GND
2	89P	P16	P24	N24	P17	NC	R25
-	-	VCCO2	-	-	-	VCCO2	VCCO2
2	89N	P18	P25	N25	P19	NC	R24
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	GND (Bank 2)
2	90P	P20	P26	N26	P21	NC	R21
2	90N	P22	P27	N27	P23	NC	P21
2	91P	P24	P28	N28	P25	NC	R22
2	91N	P26	P29	N29	P27	NC	R23
2	92P	P28	P30	N30	P29	NC	R20
2	92N	P30	P31	N31	P31	NC	P20
-	-	TOE	-	-	-	W22	P25
-	-	RESETB	-	-	-	V22	P24
-	-	GOE0	-	-	-	T22	P23
-	-	GOE1	-	-	-	R22	P22
-	-	GNDP	-	-	-	N22	P26
-	GCLK3N	GCLK2	-	-	-	P16	N26
-	-	VCCP	-	-	-	M22	N25
-	GCLK3P	GCLK3	-	-	-	N16	N24
3	93N	R0	T31	R31	R1	J22	N23

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	93P	R2	T30	R30	R3	H22	N22
3	94N	R4	T29	R29	R5	N19	M26
3	94P	R6	T28	R28	R7	P15	M25
3	95N	R8	T27	R27	R9	P21	M23
3	95P	R10	T26	R26	R11	N15	M22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	96N	R12	T25	R25	R13	M15	N20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	96P	R14	T24	R24	R15	N20	M20
-	-	GND	-	-	-	GND	GND
3	97N	R16	T23	R23	R17	P22	N21
3	97P	R18	T22	R22	R19	N21	M21
3	98N	R20	T21	R21	R21	N17	M24
3	98P	R22	T20	R20	R23	M20	L24
3	99N	R24	T19	R19	R25	P17	L23
-	-	VCC	-	-	-	VCC	VCC
3	99P	R26	T18	R18	R27	P18	L22
3	100N	R28	T17	R17	R29	M21	L25
3	100P	R30	T16	R16	R31	M17	K26
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	101N	T0	T15	R15	T1	L20	K25
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	101P	T2	T14	R14	T3	N18	K24
3	102N	T4	T13	R13	T5	L21	K23
3	102P	T6	T12	R12	T7	M18	K22
3	103N	T8	T11	R11	T9	L22	J25
3	103P	T10	T10	R10	T11	L17	J24
3	104N	T12	T9	R9	T13	K22	L21
3	104P	T14	T8	R8	T15	L18	K21
3	105N	T16	T7	R7	T17	K21	L20
3	105P	T18	T6	R6	T19	K18	K20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	106N	T20	T5	R5	T21	K20	J23
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	106P	T22	T4	R4	T23	K17	J22
3	107N	T24	T3	R3	T25	K19	J26
3	107P	T26	T2	R2	T27	J17	H26
3	108N	T28	T1	R1	T29	E22	H25
3	108P	T30/PLL_FBK1	T0	R0	T31	E21	H24
3	109N	U0/PLL_RST1	X27	V27	U1	G22	H23
3	109P	U2	X26	V26	U3	F21	H22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	110N	U4	X25	V25	U5	H21	J21

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	110P	U6	X24	V24	U7	G21	H21
-	-	GND	-	-	-	GND	GND
3	111N	U8	X23	V23	U9	D22	G25
3	111P	U10	X22	V22	U11	D21	G24
3	112N	U12	X21	V21	U13	J20	G23
3	112P	U14/CLK_OUT1	X20	V20	U15	J19	G22
3	113N	U16	V31	-	U17	E20	J20
-	-	VCC	-	-	-	VCC	VCC
3	113P	U18	V30	U30	U19	F20	H20
3	114N	U20	V29	U28	U21	H17	G26
3	114P	U22	V28	U26	U23	H18	F25
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	115N	U24	V27	-	U25	J18	F24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	115P	U26	V26	-	U27	H19	F23
3	116N	U28	V25	-	U29	G20	G21
3	116P	U30	V24	-	U31	G19	F22
-	-	GND	-	-	-	GND	GND
3	117N	V0	V23	-	V1	C22	F26
-	-	VCC	-	-	-	VCC	VCC
3	117P	V2	V22	-	V3	C21	E26
3	118N	V4	V21	-	V5	D20	E25
3	118P	V6	V20	-	V7	C19	E24
3	119N	V8	V19	-	V9	F19	E23
3	119P	V10	V18	-	V11	E19	E22
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	120N	V12	V17	-	V13	G18	D26
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	120P	V14	V16	-	V15	F18	D25
3	121N	V16	V15	-	V17	B20	D24
3	121P	V18	V14	-	V19	B19	D23
3	122N	V20	V13	-	V21	A20	C26
3	122P	V22	V12	-	V23	A19	C25
3	123N	V24	X19	V19	V25	D18	G19
3	123P	V26	X18	V18	V27	C18	F19
3	124N	V28	X17	V17	V29	G17	G18
3	124P	V30	X16	V16	V31	F16	F18
3	125N	W0	X31	V31	W1	E17	F20
3	125P	W2	X30	V30	W3	D17	E20
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	126N	W4	V11	U21	W5	B18	E19
-	-	VCCO3	-	-	-	VCCO3	VCCO3

ispXPLD 51024MX Logic Signal Connections (Continued)

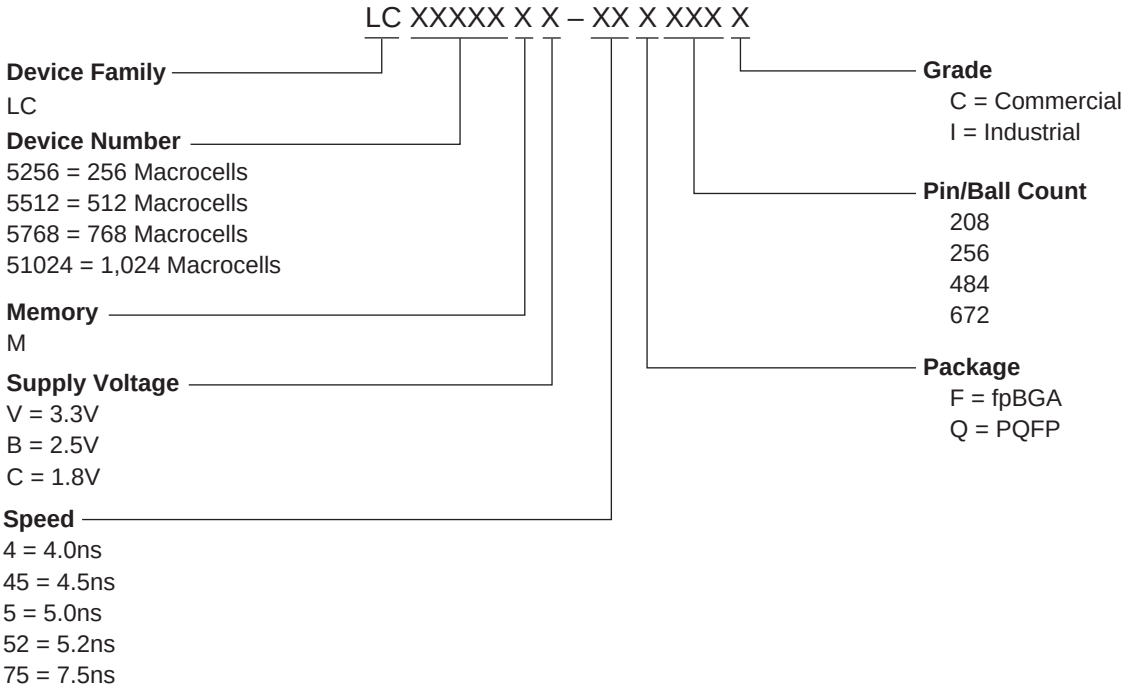
sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
3	126P	W6	V10	U20	W7	A18	E18
-	-	GND	-	-	-	GND	GND
3	127N	W8	V9	U18	W9	C17	C24
-	-	VCC	-	-	-	VCC	VCC
3	127P	W10	V8	U16	W11	B17	C23
3	128N	W12	V7	U12	W13	C16	D22
3	128P	W14	V6	U10	W15	B16	D21
3	129N	W16	V5	U8	W17	F13	E21
3	129P	W18	V4	U6	W19	F15	D20
3	130N	W20	V3	U5	W21	D16	D19
3	130P	W22	V2	U4	W23	E16	D18
3	131N	W24	V1	U2	W25	A16	C22
3	131P	W26	V0	U0	W27	A15	C21
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	132N	W28	X15	V15	W29	B15	C20
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	132P	W30	X14	V14	W31	A14	C19
3	133N	X0	X13	V13	X1	D15	C18
3	133P	X2	X12	V12	X3	E15	C17
3	134N	X4	X11	V11	X5	D14	B24
3	134P	X6	X10	V10	X7	F14	B23
3	135N	X8	X9	V9	X9	A13	B22
3	135P	X10	X8	V8	X11	B13	B21
3	136N	X12/VREF3	X29	V29	X13	C14	B20
3	136P	X14	X28	V28	X15	E14	B19
3	137N	X16	X7	V7	X17	E13	B18
3	137P	X18	X6	V6	X19	F12	B17
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	GND (Bank 3)
3	138N	X20	X5	V5	X21	D13	A24
-	-	VCCO3	-	-	-	VCCO3	VCCO3
3	138P	X22	X4	V4	X23	C13	A23
3	139N	X24	X3	V3	X25	E12	A22
-	-	GND	-	-	-	GND	GND
3	139P	X26	X2	V2	X27	C12	A21
-	-	VCC	-	-	-	VCC	VCC
3	140N	X28	X1	V1	X29	B12	A20
3	140P	X30	X0	V0	X31	A12	A19
0	141N	Y30	Y31	AA31	Y31	E11	A18
-	-	VCC	-	-	-	VCC	VCC
0	141P	Y28	Y30	AA30	Y29	C11	A17
-	-	GND	-	-	-	GND	GND
0	142N	Y26	Y29	AA29	Y27	B11	A10
0	142P	Y24	Y28	AA28	Y25	A11	A9

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocel/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	672 fpBGA Ball Number
			Macrocell 1	Macrocell 2			
0	143N	Y22	Y27	AA27	Y23	F11	A8
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	143P	Y20	Y26	AA26	Y21	F10	A7
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	144N	Y18	Y25	AA25	Y19	E10	A6
0	144P	Y16	Y24	AA24	Y17	C10	A5
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	A4
0	145P	Y12	Y2	AA2	Y13	B10	A3
0	146N	Y10	Y23	AA23	Y11	A10	B10
0	146P	Y8	Y22	AA22	Y9	A9	B9
0	147N	Y6	Y21	AA21	Y7	C9	B8
0	147P	Y4	Y20	AA20	Y5	D9	B7
0	148N	Y2	Y19	AA19	Y3	F9	B6
0	148P	Y0	Y18	AA18	Y1	E9	B5
0	149N	Z30	Y1	AA1	Z31	A8	B4
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	149P	Z28	Y0	AA0	Z29	B8	B3
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	150N	Z26	AA29	-	Z27	A7	C10
0	150P	Z24	AA28	-	Z25	B7	C9
0	151N	Z22	AA27	-	Z23	A5	C8
0	151P	Z20	AA26	-	Z21	B5	C7
0	152N	Z18	AA25	-	Z19	B6	C6
0	152P	Z16	AA24	-	Z17	C7	C5
0	153N	Z14	AA23	-	Z15	E8	C4
0	153P	Z12	AA22	-	Z13	E7	D5
0	154N	Z10	AA21	-	Z11	E6	D9
-	-	VCC	-	-	-	VCC	VCC
0	154P	Z8	AA20	-	Z9	D6	D8
-	-	GND	-	-	-	GND	GND
0	155N	Z6	AA19	-	Z7	D8	D7
-	-	VCCO0	-	-	-	VCCO0	VCCO0
0	155P	Z4	AA18	-	Z5	F8	D6
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	GND (Bank 0)
0	156N	Z2	AA17	-	Z3	F7	F9
0	156P	Z0	AA16	-	Z1	D7	E9
0	157N	AA30	AA15	-	AA31	C6	F7
0	157P	AA28	AA14	-	AA29	C5	F8
0	158N	AA26	AA13	-	AA27	C4	G8
0	158P	AA24	AA12	-	AA25	D5	G9

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

Part Number Description



Ordering Information

Note: For all but the slowest commercial speed grade, the speed grades on these devices are dual marked. For example, the commercial speed grade -45XXXXC is also marked with the industrial grade -75I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial grade only.

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	141	C
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	141	C
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	141	C
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	149	C
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	149	C
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	193	C
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	193	C
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	253	C
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	253	C
LC51024MC	LC51024MC-52F484C	1024	1.8	5.2	fpBGA	484	317	C
	LC51024MC-75F484C	1024	1.8	7.5	fpBGA	484	317	C
	LC51024MC-52F672C	1024	1.8	5.2	fpBGA	672	381	C
	LC51024MC-75F672C	1024	1.8	7.5	fpBGA	672	381	C

ispXPLD 5000MB (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-4F256C	256	2.5	4.0	fpBGA	256	141	C
	LC5256MB-5F256C	256	2.5	5.0	fpBGA	256	141	C
	LC5256MB-75F256C	256	2.5	7.5	fpBGA	256	141	C
LC5512MB	LC5512MB-45Q208C	512	2.5	4.5	PQFP	208	149	C
	LC5512MB-75Q208C	512	2.5	7.5	PQFP	208	149	C
	LC5512MB-45F256C	512	2.5	4.5	fpBGA	256	193	C
	LC5512MB-75F256C	512	2.5	7.5	fpBGA	256	193	C
	LC5512MB-45F484C	512	2.5	4.5	fpBGA	484	253	C
	LC5512MB-75F484C	512	2.5	7.5	fpBGA	484	253	C
LC51024MB	LC51024MB-52F484C	1024	2.5	5.2	fpBGA	484	317	C
	LC51024MB-75F484C	1024	2.5	7.5	fpBGA	484	317	C
	LC51024MB-52F672C	1024	2.5	5.2	fpBGA	672	381	C
	LC51024MB-75F672C	1024	2.5	7.5	fpBGA	672	381	C

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141	C
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141	C
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141	C
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149	C
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149	C
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193	C
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193	C
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253	C
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253	C
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317	C
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317	C
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381	C
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381	C

ispXPLD 5000MC (1.8V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MC	LC5256MC-5F256I	256	1.8	5.0	fpBGA	256	141	I
	LC5256MC-75F256I	256	1.8	7.5	fpBGA	256	141	I
LC5512MC	LC5512MC-75Q208I	512	1.8	7.5	PQFP	208	149	I
	LC5512MC-75F256I	512	1.8	7.5	fpBGA	256	193	I
	LC5512MC-75F484I	512	1.8	7.5	fpBGA	484	253	I
LC51024MC	LC51024MC-75F484I	1024	1.8	7.5	fpBGA	484	317	I
	LC51024MC-75F672I	1024	1.8	7.5	fpBGA	672	381	I

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	141	I
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	141	I
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149	I
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193	I
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253	I
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317	I
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381	I

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O	Grade
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141	I
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141	I
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149	I
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193	I
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253	I
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317	I
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381	I

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- sysIO Usage Guidelines for Lattice Devices (TN1000)
- Lattice sysCLOCK PLL Design and Usage Guidelines (TN1003)
- Power Estimation in ispXPLD 5000MX Devices (TN1031)
- Using Memory in ispXPLD 5000MX Devices (TN1030)
- ispXP Configuration Usage Guidelines (TN1026)