KAF-4301E

2084(H) x 2084(V) Pixel

Enhanced Response
Full-Frame CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650

Revision 2
September 23, 2002

Eastman Kodak Company - Image Sensor Solutions
For the most current information regarding this product:
Phone: (585) 722-4385 Fax: (585) 722-4947 Web: www.kodak.com/go/imagers E-mail: imagers@kodak.com

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1.1 Features

- **Front Illuminated Full-Frame Architecture with Blue Plus Transparent Gate True Two Phase Technology**
- **24µm(H) x 24µm(V) Pixel Size**
- **2084(H) x 2084(V) Photosensitive Pixels**
- **50.02 mm x 50.02 mm Photo active Area**
- **100% Fill FactorTwo**
- **Clock Selectable Outputs**
  - **High Gain Output (11 µV/e⁻)**
  - **High Dynamic Range Output (2.0 µV/e⁻)**
- **Low Dark Current (<15 pA/cm^2 @ T=25^{o}C)**

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1.2 Functional Description

The KAF-4301E is a high performance silicon charge-coupled device (CCD) designed for a wide range of image sensing applications in the 0.4µm to 1.1µm wave-length band. Common applications include medical, scientific, military, machine and industrial vision.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400 nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

The clock selectable on-chip output amplifiers have been specially designed to meet two different needs. The first is a high sensitivity 2-stage output with 11µV/e- charge to voltage conversion ratio. The second is a single stage output with 2µV/e- charge to voltage conversion

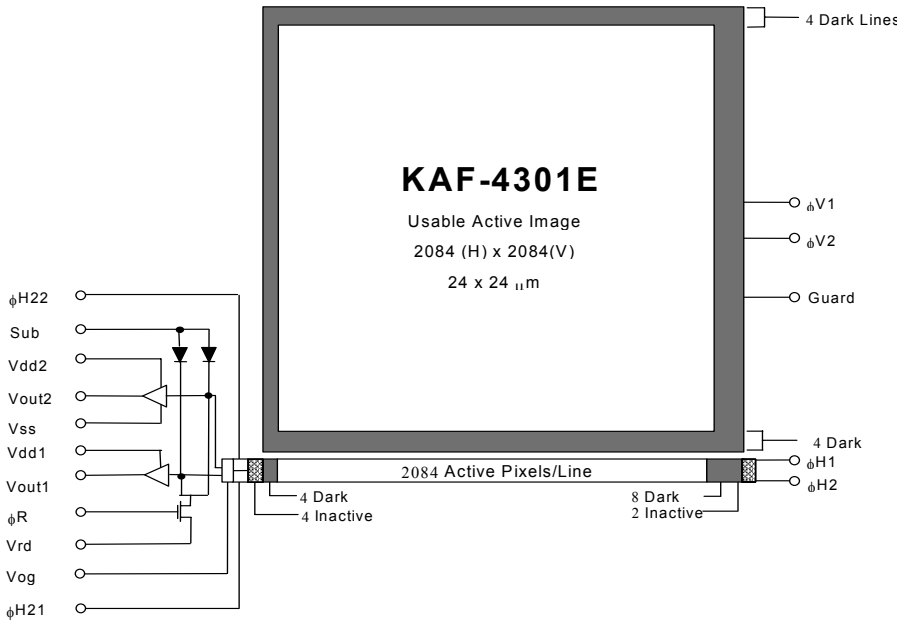


Figure 1 - Functional Block Diagram

Shaded areas represent 8 non-imaging pixels at the beginning and 10 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

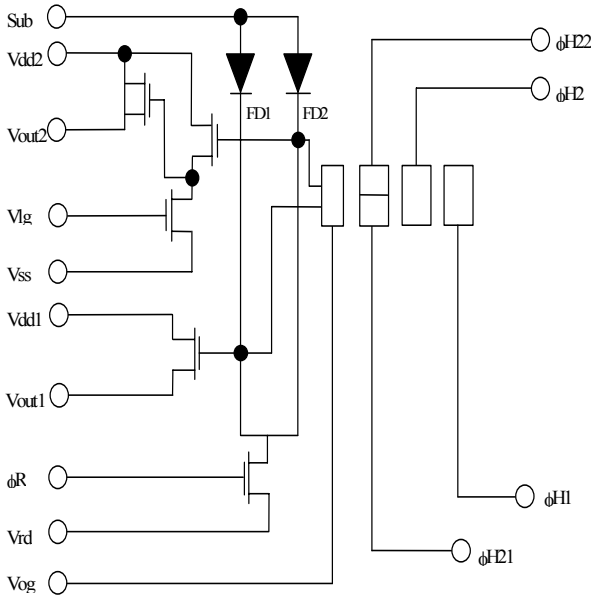


Figure 2 - Output Structure

1.3 Architecture

Refer to the block diagram in Figure 1 - Functional Block Diagram The KAF-4301E consists of 2092 vertical (parallel) CCD shift registers, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. Both registers incorporate two level polysilicon and true two-phase buried channel technology. The vertical registers contain 24 µm x 24 µm photocapacitor sensing elements (pixels) that also serves as the transport mechanism. The pixels are arranged in a 2084(H) x 2084(V) array; an additional 8 columns (4 at the left and 4 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. This device must be synchronized with strobe illumination or shuttered during readout because there is no storage array.

1.4 Image Acquisition

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines (ϕV1, ϕV2). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

1.5 Charge Transport

Integrated charge is transported to the output in a two-step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram, integration of charge is performed with ϕV1 and ϕV2 held low. Transfer to horizontal CCD begins when ϕV1 is brought high causing charge from the ϕV1 and ϕV2 gates to combine under the ϕV1 gate. ϕV1 and ϕV2 now reverse their polarity causing the charge packets to 'spill' forward under the ϕV2 gate of the next pixel. The rising edge of ϕV2 also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the ϕV1 electrode of the next pixel. The sequence completes when ϕV1 is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary

clocking (using ϕH1 and ϕH2 pins) as shown. The falling edge of ϕH2 forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) that controls the output amplifier. The cycle repeats until all lines are read.

1.6 Output Structure

The final gate of the horizontal register is split into two sections, ϕH21 and ϕH22 as shown in Figure 2 - Output Structure The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), tie ϕH22 to a negative voltage to block charge transfer, and tie ϕH21 to ϕH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), tie ϕH21 to a negative voltage and ϕH22 to ϕH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $\Delta V_{fd}=\Delta Q/C_{fd}$. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

1.7 Pin Description

Pin Number	Symbol	Description	Notes
1, 2, 27, 39, 40	ϕV2	Vertical (Parallel) CCD Clock - Phase 2	1
3, 4, 28, 37, 38	ϕV1	Vertical (Parallel) CCD Clock - Phase 1	2
5, 10, 20, 21, 29, 36	VSUB	Substrate	3
9, 22, 30	VGUARD	Guard Ring	4
11	VDD2	High Sensitivity Two-Stage Amplifier Supply	
12	VOUT2	Video Output from High Sensitivity Two-Stage Amplifier	
13	VLG	First Stage Load Transistor Gate for Two-Stage Amplifier	
14	VSS	High Sensitivity Two-Stage Amplifier Return	
15	VRD	Reset Drain	
16	ϕR	Reset Clock	
17	VDD1	High Dynamic Range Single-Stage Amplifier Supply	
18	VOUT1	Video Output from High Dynamic Range Single-Stage Amplifier	
19	VOG	Output Gate	
23	ϕH21	Last Horizontal (Serial) CCD Phase - Split Gate	
24	ϕH22	Last Horizontal (Serial) CCD Phase - Split Gate	
25	ϕH2	Horizontal (Serial) CCD Clock - Phase 1	
26	ϕH1	Horizontal (Serial) CCD Clock - Phase 2	
6, 7, 8, 31, 32, 33, 34, 35	N/C	No Connect	

Notes: 1 - Pins 1, 2, 27, 39 and 40 must be connected together - only one Phase 2-clock driver is required
2 - Pins 3, 4, 28, 37 and 38 must be connected together - only one Phase 1-clock driver is required
3 - Pins 5, 10, 20, 21, 29 and 36 should be connected to a common potential
4 - Pins 9, 22 and 30 should be connected to a common potential

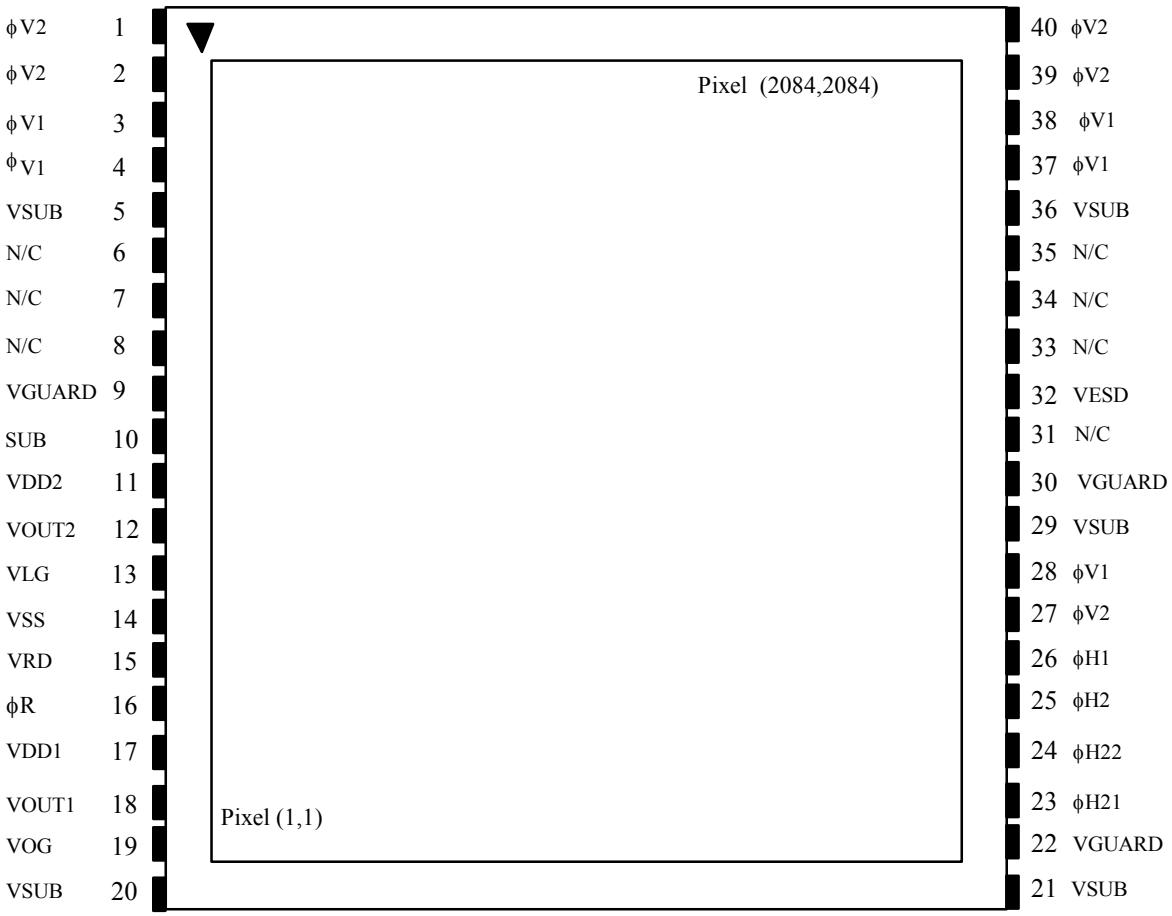


Figure 3 - Pinout Diagram

2.0 Performance

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to a voltage, multiply by the amplifier sensitivity, Vout/Ne-.

2.1 Electro-Optical

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
F F	Optical Fill Factor		100		%	
PRNU	Photoresponse Non-uniformity				% rms	Full Array
QE	Quantum Efficiency (450, 550, 650 nm)					See Figure 4 - Spectral Response

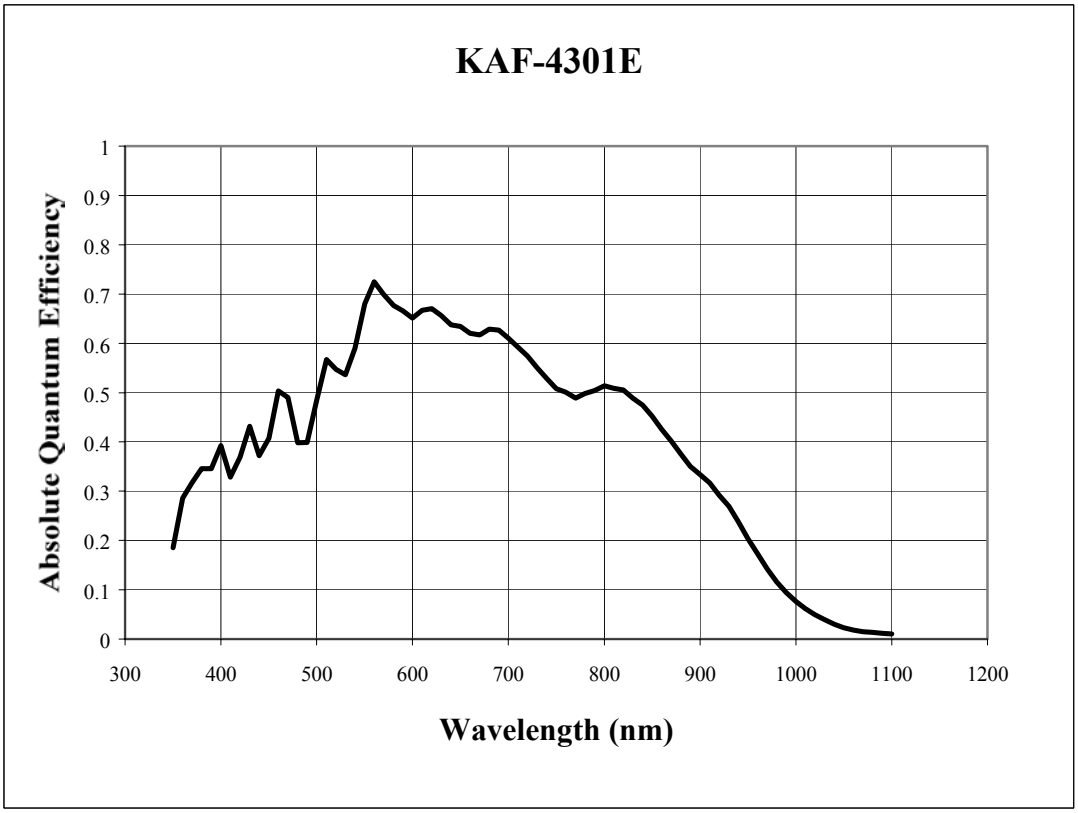


Figure 4 - Spectral Response

2.2 CCD Parameters

2.2.1 CCD Parameters Common To both Outputs

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
N_{e^-sat}	Sat. Signal - Vccd register	510	570		ke	Note 2
J_d	Dark Current		4.2 150	15 540	pA/cm^2 e^-pixel/sec	25ºC (mean of all pixels)
DCDR	Dark Current Doubling Temp	5	6	7	^oC	
DSNU	Dark Signal Non-uniformity			540	e-/pix/sec	Note 4
CTE	Charge Transfer Efficiency		.99999			Note 5
T_{VH}	V-H CCD Transfer Time		32		µs	Note 6, 7,1 0
Bs	Blooming Suppression		none			

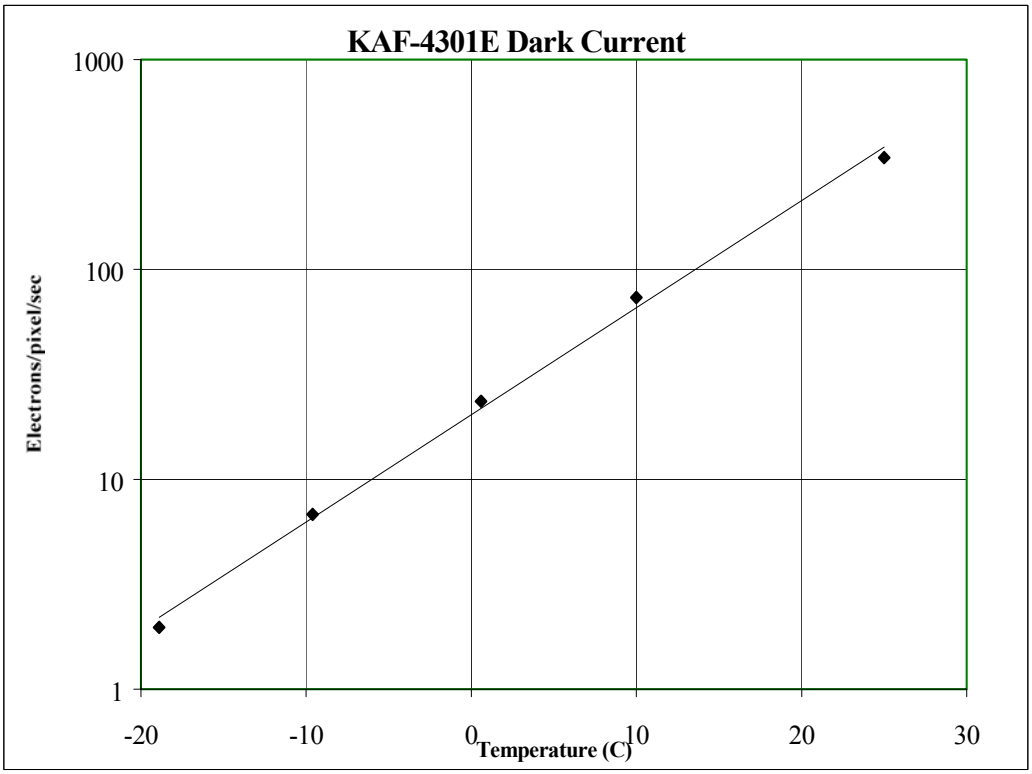


Figure 5 - Dark current

2.2.2 CCD Parameters Specific to High Gain Output Amplifier

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
Vout/Ne-	Output Sensitivity	9	11.5		uV/electron	
N_{e^-sat}	Sat. Signal	130	150	180	ke^-	Note 1
n_{e^-total}	Total Sensor Noise		13	20	e^- rms	Note 8
F_H	Horizontal CCD Frequency:		1	2.5	MHz	Note 6
DR	Dynamic Range :	79	81		dB	Note 9

2.2.3 CCD Parameters Specific to Low Gain (high dynamic range) Output Amplifier

Symbol	Parameter	Min.	Nom.	Max.	Units	Condition
Vout/Ne-	Output Sensitivity	1.7	2		uV/electron	
N_{e^-sat}	Sat. Signal	1400	1500	1800	ke^-	Note 3
n_{e^-total}	Total Sensor Noise		22	30	e^- rms	Note 8
F_H	Horizontal CCD Frequency:		0.5	2	MHz	Note 6
DR	Dynamic Range :	89	87		dB	Note 9

Notes:

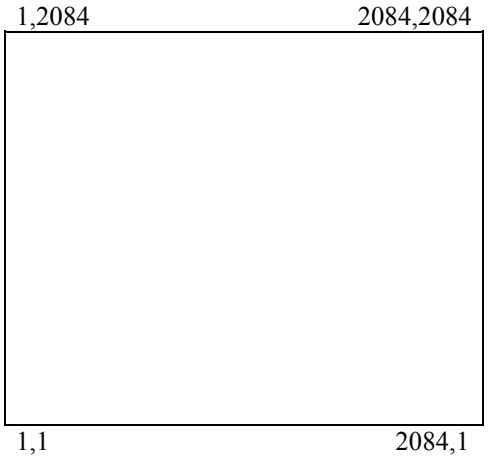
1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 256 sub arrays (128 x 128) exceed the maximum dark current specification.
5. For 2MHz data rate and T = 30ºC to -40ºC.
6 Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance
7. Time between the rising edge of ϕV1 and the first falling edge of ϕH1
8. At $T_{integration}$ = 0; data rate = 1 MHz; temperature = -30ºC
9. Uses 20LOG($N_{e^- sat}$ / $n_{e^- total}$) where $N_{e^- sat}$ refers to the appropriate saturation signal.
10. CTE corresponds to a signal level of 3500-5500 e^-/pix at 25°C and ϕH1, ϕH2 of 1MHz

2.3 Cosmetic Specification

Grade	Point Defects	Cluster Defects	Column Defects	Double Columns
C1	≤50	≤20	0	0
C2	≤50	≤20	≤4	0
C3	≤100	≤50	≤20	0
C4	≤1000	≤200	≤40	≤20

Dark Defect	A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation
Bright Defect	A pixel whose dark current exceeds 4500 electrons/pixel/second at 25ºC
Cluster Defect	A grouping of not more than 5 adjacent point defects.
Column Defect	1) A grouping point defects along a single column. (Dark Column) 2) A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25 C. (Bright Column) 3) A column that does not exhibit the minimum charge capacity specification. (Low charge capacity) 4) A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)
Neighboring Pixels	The surrounding 128 x 128 pixels of ± 64 columns/rows

Cluster defects are separated by no less than 2 pixels from other column and cluster defects.
Column defects are separated by no less than 5 pixels from other column defects.



3.0 Operation

3.1 Absolute Minimum/Maximum Ratings

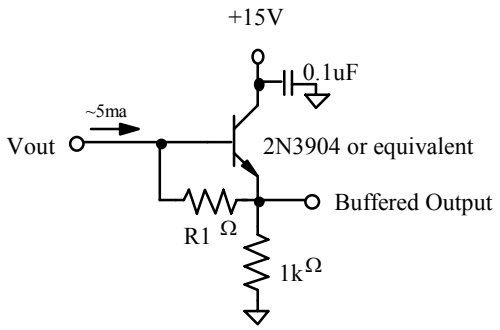
		Min.	Max.	Units	Conditions
Temperature	Storage	-100	+80	C	At Device
	Operating	-70	+50		
Voltage	All Clocks	-16	+16	V	VSUB = OV
	VOG, VLG	0	+8		
	VRD, VSS, VDD, GUARD	0	+20		
Current	Output Bias Current (IDD)		10	mA	
Capacitance	Output Load Capacitance (CLOAD)		10	pF	
Frequency/Time	ϕV1, ϕV2 Pulse Width	70		µs	
	ϕH1, ϕH2		2.5	MHz	
	ϕR Pulse Width	20		ns	

Warning: For maximum performance, built-in gate protection has been added only to the VOG and VLG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage.

3.2 DC Operating Conditions

		Min.	Nom.	Max.	Units	Pin Impedance
VSUB	Substrate	0.0	0.0	0.0	V	Common
VDD	Output Amplifier Supply	15.0	+17.0	17.5	V	5 pf, 2KΩ
VSS	Output Amplifier Return	1.4	+2.0	2.1	V	5 pf, 2KΩ
VRD	Reset Drain	11.5	+12	12.5	V	5 pf, 1MΩ
VOG	Output Gate	4.5	5.0	5.25	V	5 pf, 10MΩ
VGUARD	Guard Ring	9.0	+10.0	15.0	V	350 pF, 10MΩ
VLG	Load Gate	Vss-1.0	Vss	Vss+1.0	V	

Notes:
1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.



The value of R1 depends on the desired output current according the following formula: R1 = 0.7 / Iout
The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5 mA is recommended for capacitance of 12 pF and pixel rates up to 20 MHz.

Figure 6 - Typical Output Structure Load Diagram
(For operation of up to 10 MHz)

3.3 AC Clock Level Conditions

			Min.	Nom.	Max.	Units	Pin Impedance
ϕV1	Vertical Clock - Phase 1	Low	-8.5	-8.0	-7.8	V	700 nf, 10MΩ
		High	1.0	1.0	2.0	V	
ϕV2	Vertical Clock - Phase 2	Low	-8.5	-8.0	-7.8	V	800 nf, 10MΩ
		High	1.0	1.0	2.0	V	
ϕH1	Horizontal Clock - Phase 1	Low	-2.2	-2.0	-1.8	V	1200 pf, 10MΩ
		High	7.8	+8.0	8.2	V	
ϕH2	Horizontal Clock - Phase 2	Low	-2.2	-2.0	-1.8	V	1200 pf, 10MΩ
		High	7.8	+8.0	8.2	V	
ϕR	Reset Clock	Low	2.0	3.0	3.5	V	10 pF, 10MΩ
		High	9.5	10.0	11.0	V	

			Using the High Gain Output (Vout 2)			Using the High Dynamic Range Output (Vout1)				
			Min.	Nom.	Max.	Min.	Nom.	Max.	Units	Pin Impedance
ϕH21	Horizontal Clock - Phase 1	Low	-4	ϕH2 low	ϕH2 low		ϕH2		V	10 pF, 10MΩ
		High	-4	ϕH2 low	ϕH2 low		ϕH2		V	
ϕH22	Horizontal Clock - Phase 2	Low		ϕH2		-4	ϕH2 low	ϕH2 low	V	10 pF, 10MΩ
		High		ϕH2		-4	ϕH2 low	ϕH2 low	V	

Note: When using Vout1 ϕH21 is clocked identically with ϕH2 while ϕH22 is held at a static level. When using Vout2 ϕH21 and ϕH22 are exchanged so that ϕH22 is identical to ϕH2 and ϕH21 is held at a static level. The static level should be the same voltage as ϕH2 low.

Note: The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.

Note: ϕV1,2 and ϕH 1,2 capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.

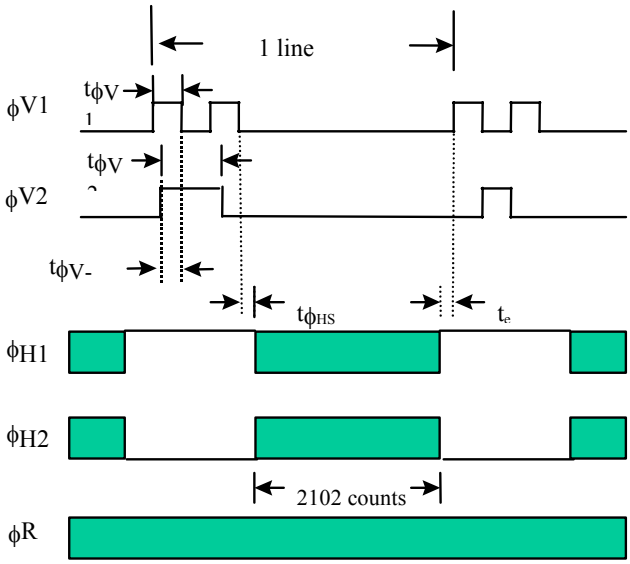
Note: This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

3.4 AC Timing Chart

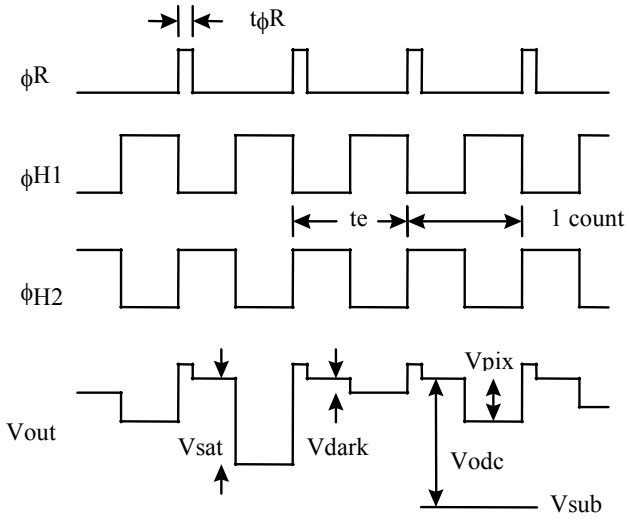
Description	Symbol	Min.	Nom.	Max.	Units	Notes
fH1, fH2 Clock Frequency	f_H		1	2.5	MHz	1, 2, 3
Pixel Period	t_{pix}	400	1000		ns	
fH1, fH2 Setup Time	$t_{\phi HS}$	0.5	1		µs	
fV1 Clock Pulse Width	$t_{\phi V1}$		100		µs	2
fV2 Clock Pulse Width	$t_{\phi V2}$		150		µs	2
fV2, V1 Clock Pulse Overlap	$t_{\phi V2}$		150		µs	2
Reset Clock Pulse Width	$t_{\phi R}$	20	60		ns	4
Readout Time	$t_{readout}$	1751	5320		ms	5

Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously
5. $t_{readout} = (2092 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 2102 * t_{pix} + t_{pix}$

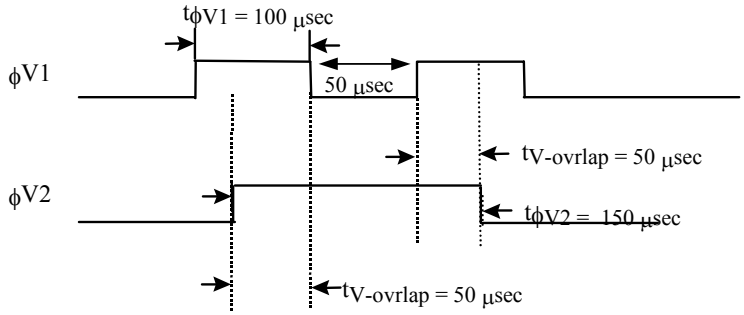
Line Timing Detail



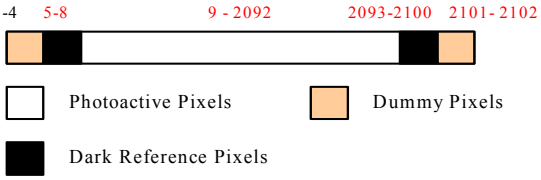
Pixel Timing Detail



Vertical Clock Timing Detail



Line Content



Vsat	Saturated pixel video output signal
Vdark	Video output signal in no light situation, not zero due to Jdark
Vpix	Pixel video output signal level, more electrons =more
Vodc	Video level offset with respect to vsub
Vsub	Analog Ground

* See Image Aquisition section

Figure 7 - Timing diagrams

4.0 Storage and Handling

4.1 Storage Conditions

Image sensors with temporary cover glass should be stored at room temperature (nominally 25ºC.) in dry nitrogen.

4.2 ESD

CAUTION:
This device contains limited protection against Electrostatic Discharge (ESD). This device is rated as Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test.)
Devices should be handled in accordance with strict ESD protection procedures.

For more information see Application Note MTD/PS-0224, Electrostatic Discharge Control.

5.0 Quality Assurance and Reliability

5.1 Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

5.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

5.3 Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer

5.4 Liability of the Customer: Damage from mechanical (scratches or breakage), electrical (ESD), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

5.5 Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note DS 00-009, Cover Glass Cleaning, for further information.

5.6 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

5.7 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

5.8 Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

5.9 Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

6.0 Mechanical Drawings and Specifications.

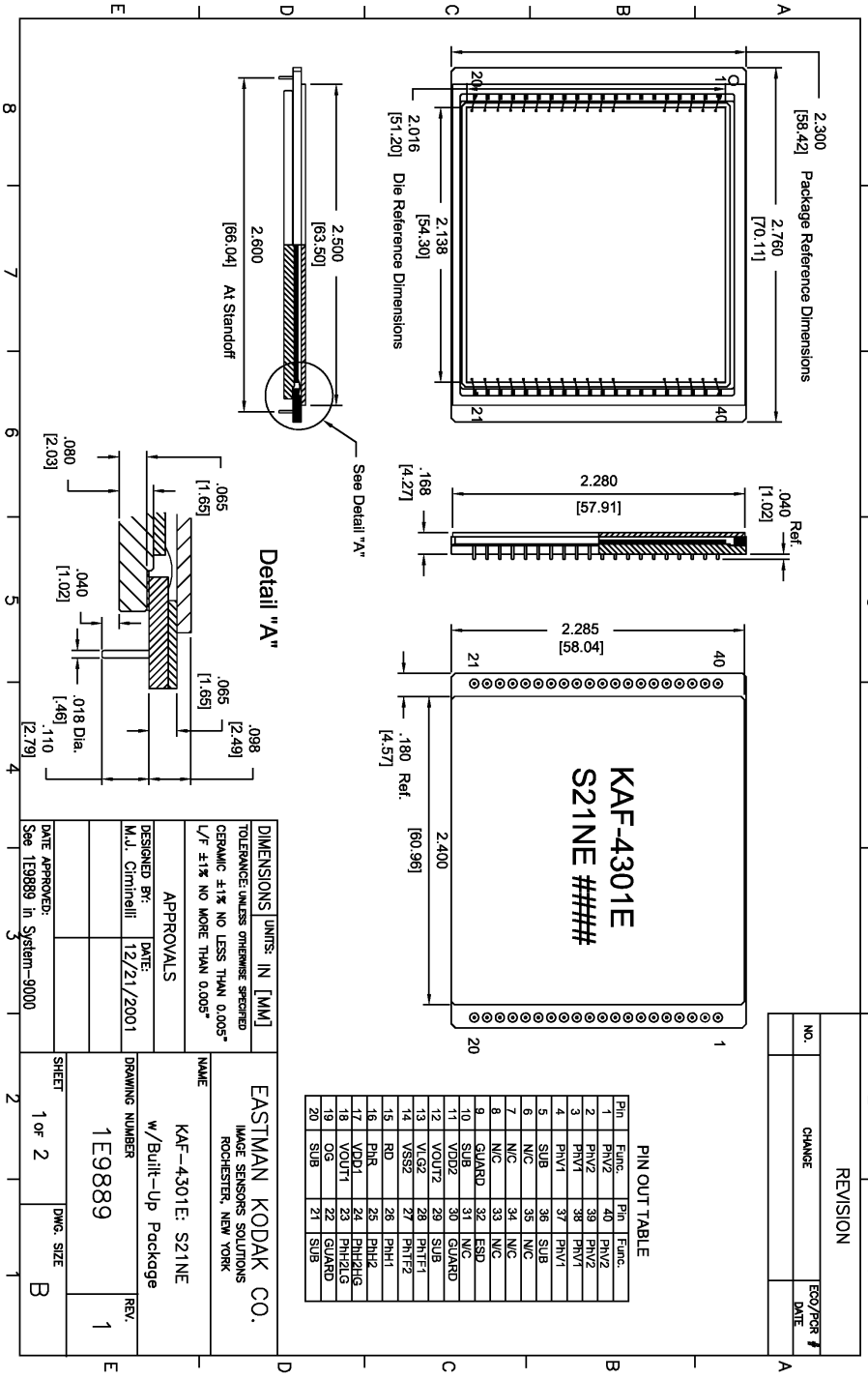


Figure 8 - Package Mechanical Drawing - Page 1

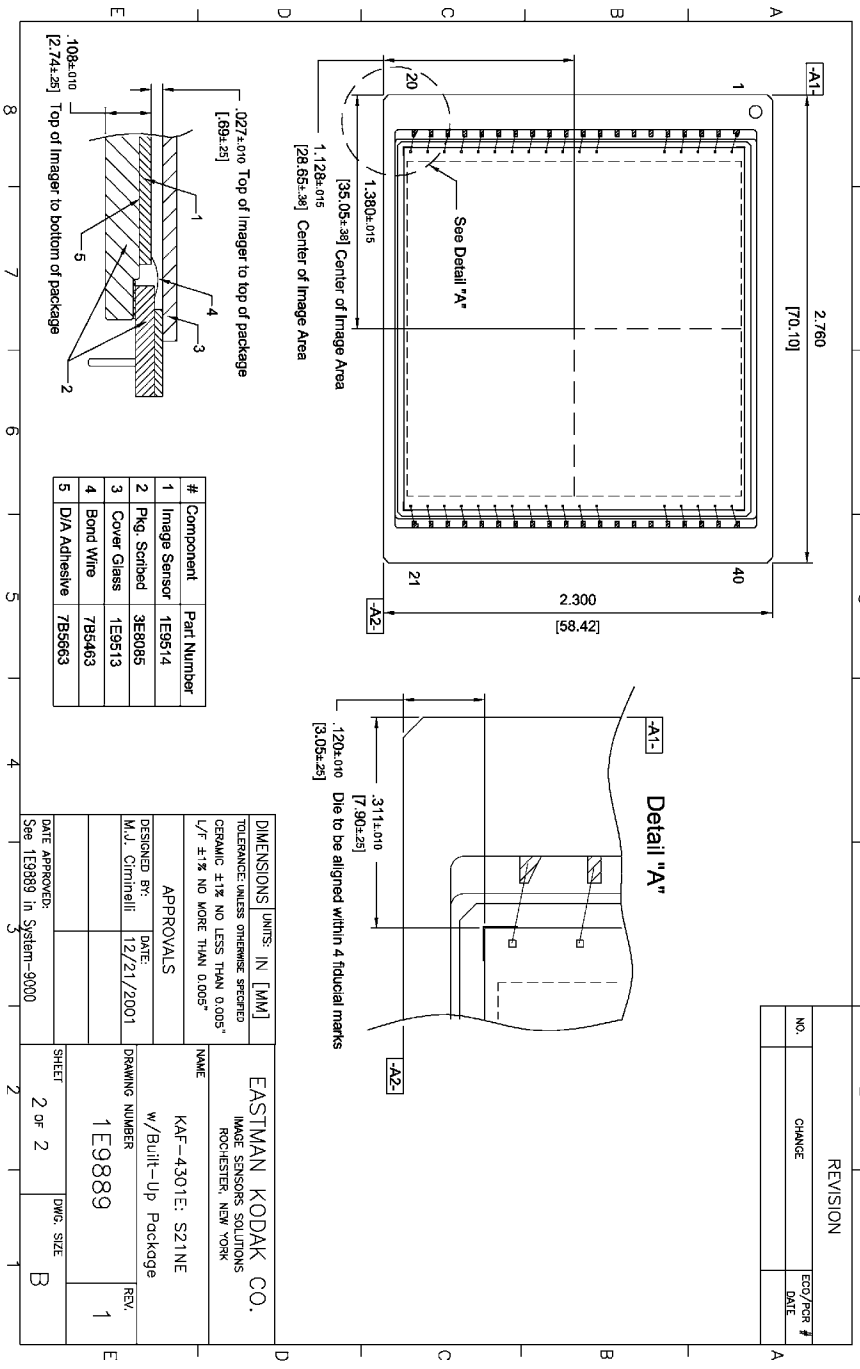


Figure 8 - Package Mechanical Drawing - Page 2

6.1 Imager Flatness

The flatness of the die is defined as a peak-to-peak distortion in the image sensor surface. The parallelism between the image sensor surface and any of the package components is not specified or guaranteed. The non-parallelism is removed when measuring the distortion in the image sensor surface.

		Minimum	Nominal	Maximum	Unit
Die Flatness	Peak-to-Peak distortion	-	8.0	12.0	microns

Some examples of profiles from typical image sensors surfaces are shown below.

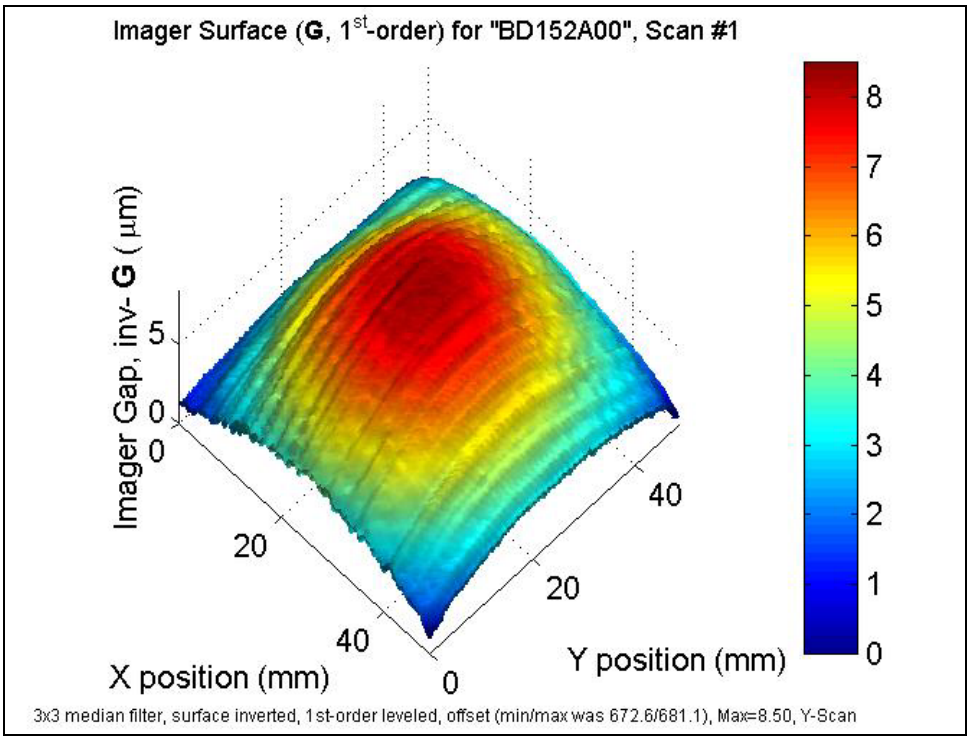


Figure 9 - Surface Profile of Image Sensor Surface

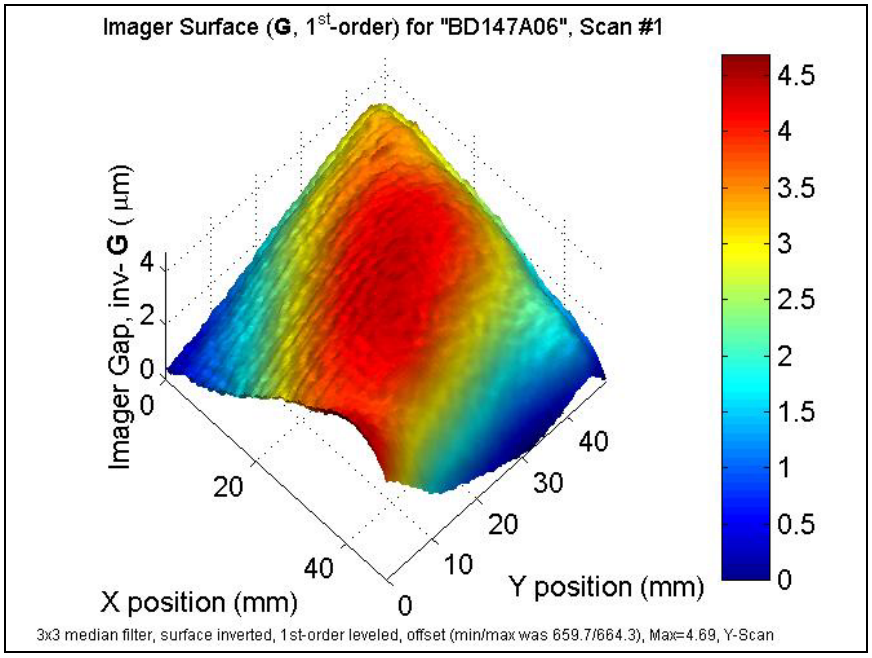


Figure 10 - Surface Profile of Image Sensor Surface

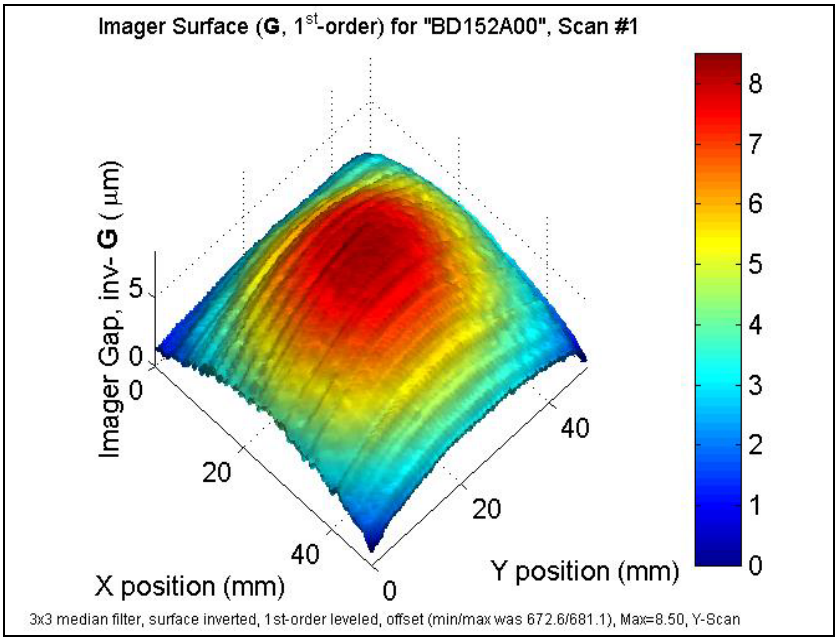


Figure 11 - Surface Profile of Image Sensor Surface

7.0 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
E-mail: imagers@Kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Image Sensor Solutions, Eastman Kodak Company products are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

Appendix 1:

Revision Changes:

Revision No.	Date	Changes
1	3/12/02	Initial formal version
2	9/19/02	Added Section 6.1 Imager Flatness