KL5KUSB111

USB to HomePNA

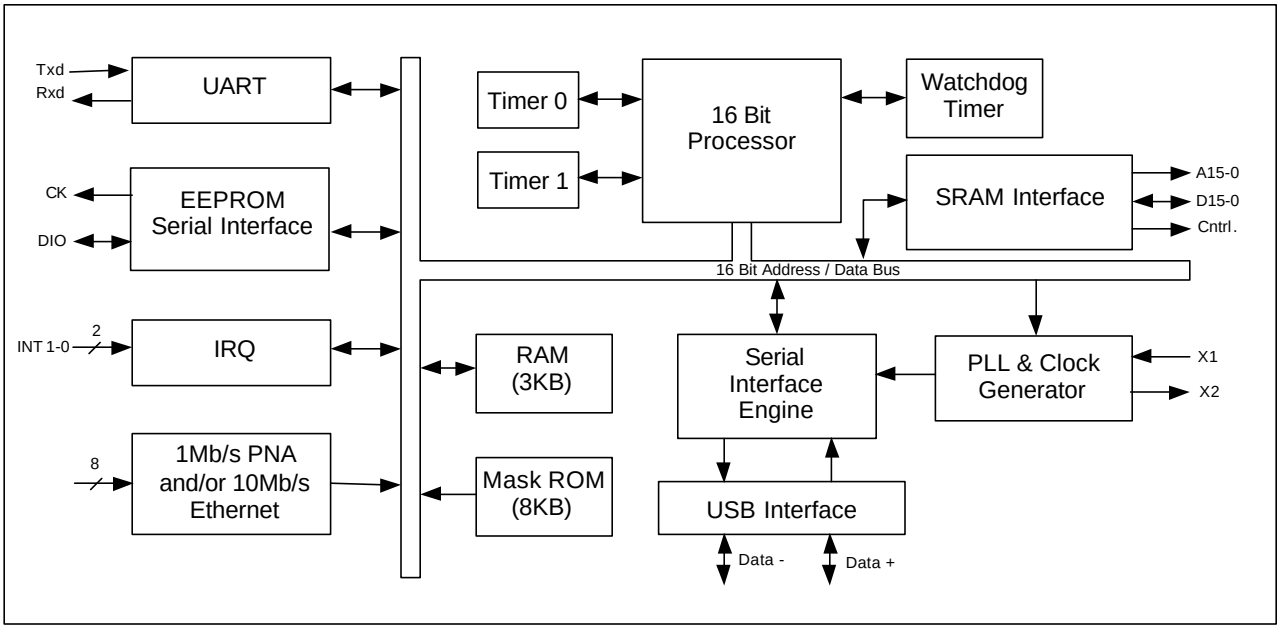
General Description

The Kawasaki KL5KUSB111 Controller is a unique single chip solution developed to interface the Universal Serial Bus (USB) to HomePNA-Networks and standard 10base-T Networks. The KL5KUSB111 has been specifically designed to provide a simple solution to communicate with Home Networking Applications at 1 Mb/s and/or 10 Mb/s Ethernet. By utilizing the Kawasaki's USB to Ethernet technology that has been used throughout the industry. The USB controller consists of a central 16-bit processor, mask ROM, RAM buffer, clock generator, HomePNA / Ethernet interface, UART, IRQ, Watchdog Timer, Serial interface, External Memory Interface and Debug UART. The SIE (Serial Interface Engine) is fully compatible with the USB specification. The Kawasaki USB to HomePNA controller enables the advantages of Home Networking such as Shared Internet access, Printer/peripheral sharing, File and application sharing and Networked gaming.

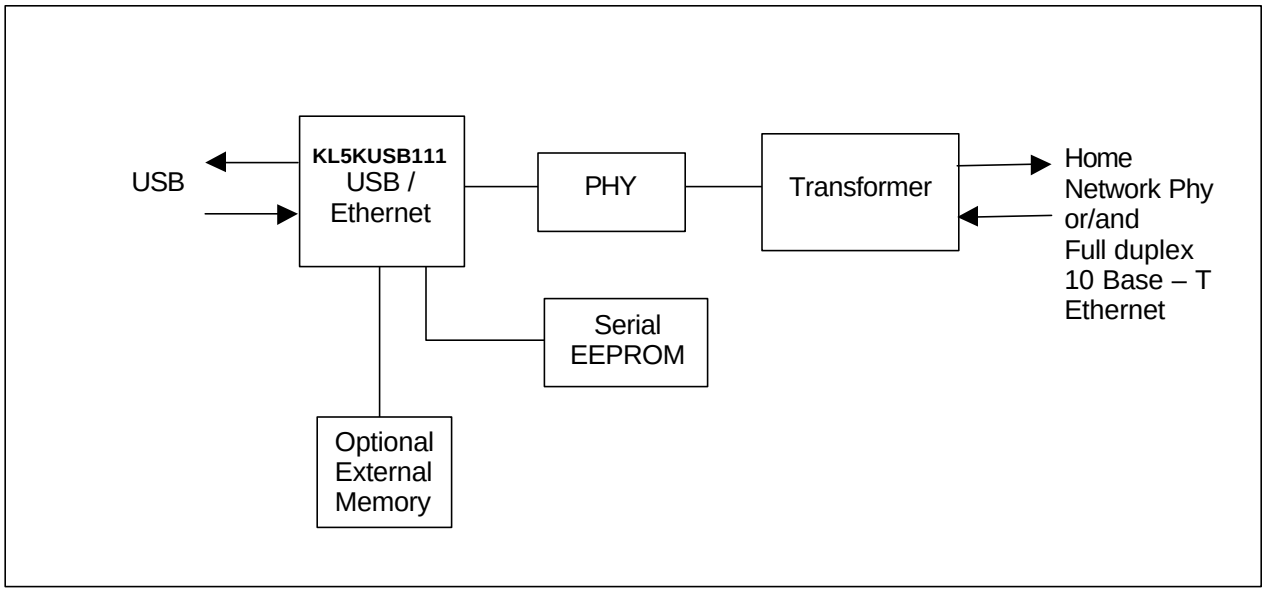
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- USB interface ver. 1.0/1.1 compliant
- Integrated Transceivers and SIE (Serial Interface Engine)
- Internal Clock Generation
- Utilizes low cost external crystal circuitry
- 1.5K x 16 Internal RAM buffer
- Serial Interface for external EEPROM
- HomePNA compliant for 1Mb/sec.
- Fully IEEE 802.3 compliant 10 Mbit/sec Ethernet MAC Layer. Interfaces serially of an external ENDEC PHY.
- Debug UART
- External memory interface
- Compatible with most HomePNA PHY's
- Watchdog timer
- 100 pin LQFP package

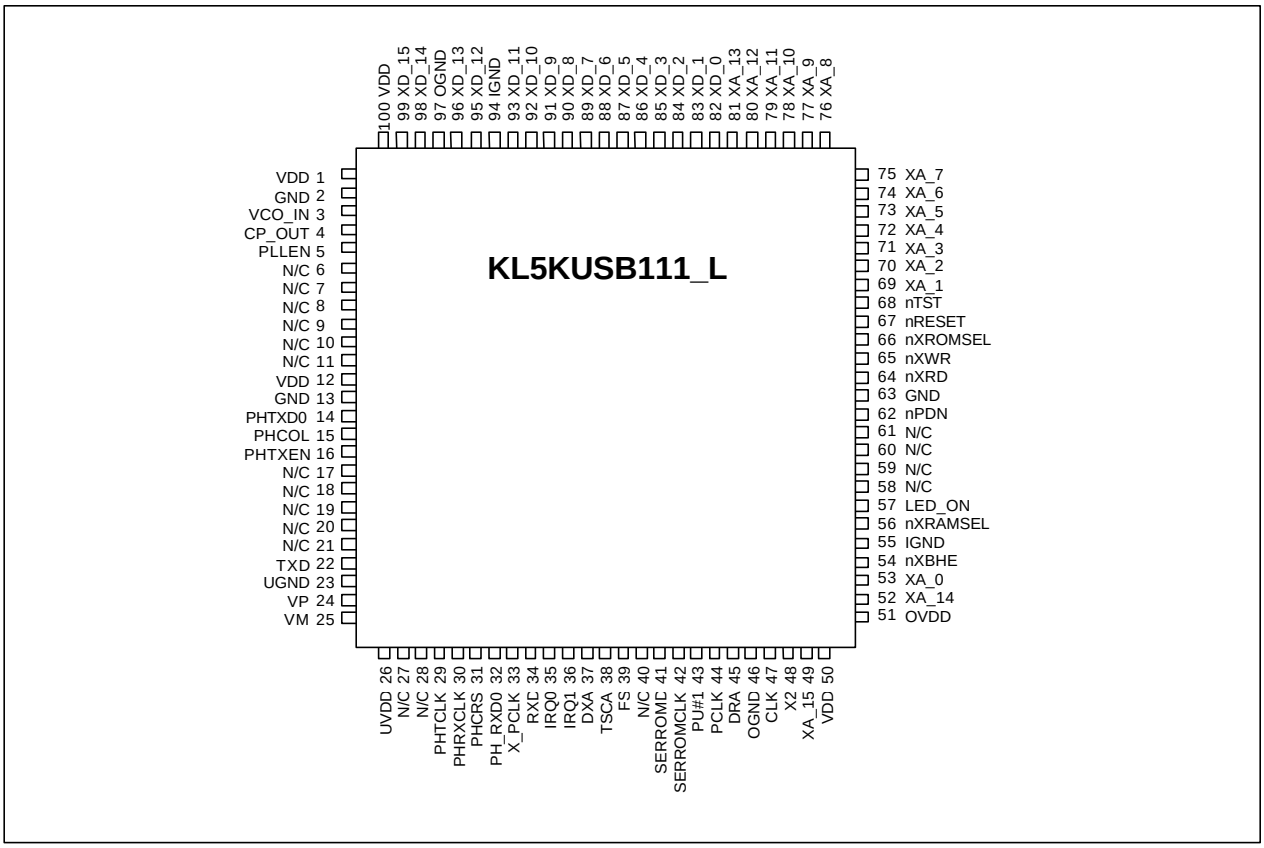
Block Diagram



KL5KUSB111 Application Block Diagram



Pin Diagram 100LQFP



Pin Description

Pin # LQFP	I/O	Pin Name	Description
1	IN	0VDD	VDD
2	IN	GND	GND
3	IN	VCO_IN	PLL VCO IN
4	OUT	CP_OUT	PLL VCO OUT
5	IN	PLLEN	PLL Enable
6	NC	NC	NC
7	NC	NC	NC
8	NC	NC	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	IN	VDD	VDD
13	IN	GND	GND
14	OUT	PHTXD0	Transmit data to PHY
15	IN	PHCOL	Collision input from PHY
16	OUT	PHTXEN	Transmit Enable to PHY
17	NC	NC	NC
18	NC	NC	NC
19	NC	NC	NC
20	NC	NC	NC
21	NC	NC	NC
22	IN/OUT	TXD	UART TXD
23	IN	UGND	USB GND
24	IN/OUT	VP	USB+ Pin
25	IN/OUT	VM	USB- Pin
26	IN	UVDD	USB VDD
27	NC	NC	NC
28	NC	NC	NC
29	IN	PHTXCLK	PHY Transmit Clock
30	IN	PHRXCLK	PHY Receive Clock
31	IN	PHCRS	PHY Carrier Sense
32	IN	PH_RXD0	PHY Serial Receive Data
33	IN/OUT	X_PCLK	External PCLK
34	IN/OUT	RXD	UART RXD
35	IN	IRQ0	IRQ or GPIO10
36	IN	IRQ1	IRQ or GPIO11
37	OUT	DXA	Sport Mode or GPIO7
38	IN	TSCA	Sport Mode or GPIO8
39	IN/OUT	FS	Sport Mode or GPIO9
40	NC	NC	NC
41	IN/OUT	SERROMD	Serial ROM data
42	OUT	SERROMCLK	Serial ROM clk
43	IN/OUT	PU#1	Pull up to USB + Pin for High Speed

Pin # LQFP	I/O	Pin Name	Description
44	IN	PCLK	Sport Mode or GPIO5
45	IN	DRA	Sport Mode or GPIO6
46	IN	OGND	GND
47	IN	CLK	12MHz Clock/Crystal Input
48	OUT	X2	12MHz Crystal Output
49	OUT	XA_15	External Address Pin
50	IN	VDD	VDD
51	IN	0VDD	VDD
52	OUT	XA_14	External Address Pin
53	OUT	XA_0	External Address Pin
54	OUT	nXBHE	SRAM Byte High Enable
55	IN	IGND	GND
56	OUT	nXRAMSEL	SRAM Byte Low Enable
57	IN/OUT	LED_ON	Turns on 3.3V to TX LED
58	NC	NC	NC
59	NC	NC	NC
60	NC	NC	NC
61	NC	NC	NC
62	IN/OUT	nPDN	Powerdown to PHY(active LO)
63	IN	GND	GND
64	OUT	nXRD	External Memory Read (active LO)
65	OUT	nXWR	External Memory Write (active LO)
66	OUT	nXROMSEL	External ROM CS (active LO)
67	IN	nRESET	Reset Pin
68	IN	nTST	Test Pin, NC for Normal Operation
69	OUT	XA_1	External Address Pin
70	OUT	XA_2	External Address Pin
71	OUT	XA_3	External Address Pin
72	OUT	XA_4	External Address Pin
73	OUT	XA_5	External Address Pin
74	OUT	XA_6	External Address Pin
75	OUT	XA_7	External Address Pin
76	OUT	XA_8	External Address Pin
77	OUT	XA_9	External Address Pin
78	OUT	XA_10	External Address Pin
79	OUT	XA_11	External Address Pin
80	OUT	XA_12	External Address Pin
81	OUT	XA_13	External Address Pin
82	IN/OUT	XD_0	External Data Pin
83	IN/OUT	XD_1	External Data Pin
84	IN/OUT	XD_2	External Data Pin
85	IN/OUT	XD_3	External Data Pin
86	IN/OUT	XD_4	External Data Pin
87	IN/OUT	XD_5	External Data Pin
88	IN/OUT	XD_6	External Data Pin
89	IN/OUT	XD_7	External Data Pin
90	IN/OUT	XD_8	External Data Pin
91	IN/OUT	XD_9	External Data Pin
92	IN/OUT	XD_10	External Data Pin

Pin # LQFP	I/O	Pin Name	Description
93	IN/OUT	XD_11	External Data Pin
94	IN	IGND	GND
95	IN/OUT	XD_12	External Data Pin
96	IN/OUT	XD_13	External Data Pin
97	IN	OGND	GND
98	IN/OUT	XD_14	External Data Pin
99	IN/OUT	XD_15	External Data Pin
100	IN	VDD	VDD

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (4K X 16) in the KL5KUSB111 or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of USB peripherals.

The processor supports prioritized vectored hardware interrupts. In addition, as many as 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

The Processor – Divide/Multiply function

The processor's divide/multiply function contains all the instructions of the base processor that additionally includes integer divide and multiply instructions. A signed multiply instruction takes two 16-bit operands and returns a 32-bit result. A signed divide instruction divides a 32-bit operand by a 16-bit operand.

RAM Buffer

The USB controller contains a 3K byte (1.5K X 16) internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal 48MHz clock requirements. This circuitry is designed to allow use of a low cost 12 MHz external crystal which is connected to the USB3 pins X1 and X2. If an external 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit and connected directly to the X1 input pin.

USB Interface

The USB controller meets the Universal Serial Bus (USB) specification ver 1.0. The transceiver is capable of transmitting and receiving serial data at the USB's full speed, 12 Mbits/sec data rate. The driver portion of the transceiver is differential, while the receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally, the transceiver connects to the physical layer of the USB.

1Mb/sec HomePNA Interface

The KL5KUSB111 Controller has a built in 1 Mbit/sec interface to a variety of Home Networking Phys.

10Mb/sec Ethernet Interface

The KL5KUSB111 Controller has a built in 10 Mbit/sec 10-base T Ethernet MAC (Media Access Controller) which is fully compliant with the IEEE 802.3 Ethernet standard. The KL5KUSB111 connects externally to a 10 Base -T ENDEC PHY. The KL5KUSB111 Controller 16-bit processor has direct access to the registers of the MAC.

UART Interface

Supports a transfer rate of 900 to 115.2K baud.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface can support a variety of serial EEPROM formats.

SRAM Interface

An address port and 16-bit data port has been provided to interface to an external SRAM.

DC CHARACTERISTICS

U2E is implemented with Kawasaki's 0.5um CMOS CBA and Embedded Memory KZ300EM Technology. The followings are the description of chip electric characteristics.

1. Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vdd	–0.3 ~ 4.0	V
Input Voltage	Vin	–0.3 ~ 7.3	V
DC Output Current	Iout	±15	mA
Storage Temperature	Tstg	–55 ~ 125	°C

2. Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage	Vdd	3.0	–	3.6	V
Operating ambient temperature	Ta	0	–	70	°C

3. I/O Electrical DC Characteristics (Over Recommended Range)

Table 3.1 DC Characteristics (over recommended range)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	VIL	–	–	0.8	V	
Input high voltage	VIH	2.0	–	–	V	
Input low current	IIL	–10	–	10	uA	VIN = Gnd
Input high current	IIH	–10	–	10	uA	VIN = Vdd
Output low voltage	VOL	–	–	0.4	V	IOL = 4mA
Output high voltage	VOH	2.4	–	–	V	IOH = –4mA
3-state leak current	IOZ	–10	–	10	uA	VOH = Gnd or VOL = Vdd
Active pull-up current	IPU	–25	–66	–160	uA	VIN = Gnd or VOH = Gnd
Standby current	IDDS	–	80	100	uA	VIN = Gnd or Vdd No inputs are cycling. Outputs open.
Suspend current	ISUSP	–	350	450	uA	Same conditions as IDDS except for CLKI input buffer 48MHz toggling.
dynamic operating current	IDDOP1 (in busy)	–	80	100	mA	Outputs open. Vdd = Max. FCLKI = FMAX (48MHz)
	IDDOP2 (in idle)	–	40	50	mA	
Input capacitance	CIN	–	–	15	pF	Fpin=1MHz, VIN = Gnd. Vin = 100 mVrms
Output capacitance	COUT	–	–	15	pF	