WT6561F

USB Embedded Controller with Hub

(Flash Type)

Preliminary Specification v.099h

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1 Features

GENERAL DESCRIPTION

WT6561F is an embedded flash memory type and micro-controller based Full Speed USB device with 2 down stream Hub. It contains an 8051 CPU, 16K bytes Flash, 512 bytes SRAM, 12 channels of 12 bits AD converter, 4 PWMs, and I^2C Interface. It is suitable for the combination of USB peripheral functions with Hub, such as X-Box game pad/joystick, USB game controller, and USB keyboard hub , etc.

FEATURES

- **8-bit 8051 compatible CPU with 24 MHz operating frequency**
- **16K bytes Flash, 512 bytes SRAM**
- **6MHz crystal oscillator**
- **Universal Serial Bus (USB) hub with one upstream port, two external downstream ports, and one internal downstream port for embedded function.**
- **Complete Universal Serial Bus specification 1.1 compatible**

- **USB hub**
  - Connectivity behavior
  - Power management, including suspend / resume
  - Device connect / disconnect detection
  - Bus fault detection and recovery
  - Full / Low speed device support
  - Gang mode downstream port power enable
  - Gang mode over-current detection

- **USB Embedded function:**
  - Support USB1.1 Full Speed Functions
  - Compliant to USB Human Interface Devices (HID) specification 1.0 and XID specification.
  - 1 control endpoint, IN/OUT each with 64 Bytes (8/16/32/64 bytes programmable) FIFO
  - 1 Interrupt IN endpoint, with 64 Bytes(8/16/32/64 bytes programmable) FIFO
  - 2 Generic endpoints (IN/OUT programmable) each with 64 Bytes(8/16/32/64

bytes programmable) FIFO

- **12 channels 12-bit AD converter**
- **4 channels 8 bits PWM**
- **14 GPIO(minimum), (Maximum 34 programmable I/O pin)**
- **Low V_{DD} reset**
- **Fast mode master/slave I^2C interface (support 50/100/200 up to 400KHz)**
- **One Watch-dog timer (programmable ranged from 10ms ~ 640ms)**
- **Two 16bit programmable timer**

ORDERING INFORMATION

Package Type	Part Number
48-pin LQFP	WT6561F-LQ48
48-pin DIP	WT6561F-N48
Die	WT6561F-Die

2 Pin Assignment and Package Types

Pin	Name
1	V33
2	DP0
3	DM0
4	DP1
5	DM1
6	DP2
7	DM2
8	VDDA
9	VSSA
10	PB0/AD0
11	PB1/AD1
12	PB2/AD2
13	PB3/AD3
14	PB4/AD4
15	PB5/AD5
16	PB6/AD6

Pin	Name
17	PB7/AD7
18	PD0/AD8
19	PD1/AD9
20	PD2/AD10
21	PD3/AD11/ADvref
22	PD4/PWM0
23	PD5/PWM1
24	PD6/PWM2
25	PD7/PWM3
26	PA0/EXINT0
27	PA1/EXINT1
28	PA2/EXINT2
29	PA3/EXINT3
30	PA4/EXINT4
31	PA5/EXINT5
32	PA6/EXINT6

Pin	Name
33	PA7/EXINT7
34	PC0
35	PC1
36	PC2
37	PC3
38	PC4/SCL
39	PC5/SDA
40	PC6
41	PC7
42	VDD
43	XTAL1
44	XTAL2
45	VSS
46	RESET
47	PE0/NUPE
48	PE1/NOVI

Table 1. WT6561F 48 Signals Arranged by Pin Number

2.1 Pin Description

Pin Description (48 PDIP & 48 LQFP Package)

DIP Pin	LQFP Pin	Signal Name	Type	Description
7	1	V33	PWR	3.3Volts output, Must be connected to a 1μF capacitor (or larger) to ensure proper operation of the differential line drivers. The other lead of the capacitor must be connected to GND.
8	2	DP0	I/O	USB plus data line of USB upstream port. An internal 1.5KΩ ± 5% pull-up resistor is connected between this lead and V33 to select full-speed USB operation. The internal 1.5 KΩ resistor is controlled by DPEN.
9	3	DM0	I/O	USB minus data line of USB upstream port.
10	4	DM1	I/O	USB plus data lines of USB downstream ports. An external 15KΩ ± 5% pull-down resistor must be connected to each of these leads.
11	5	DP1	I/O	USB minus data lines of USB downstream ports. An external 15KΩ ± 5% pull-down resistor must be connected to each of these leads.
12	6	DP2	I/O	USB plus data lines of USB downstream ports. An external 15KΩ ± 5% pull-down resistor must be connected to each of these leads.
13	7	DM2	I/O	USB minus data lines of USB downstream ports. An external 15KΩ ± 5% pull-down resistor must be connected to each of these leads.
14	8	VDDA	PWR	+5V supply voltage, for analog circuit
15	9	VSSA	PWR	Ground for analog circuit
16	10	PB1/AD0	I/O	Option 1: GPIO Port, With Schmitt-trigger and 30KΩ **programmable** pull-up resistor in input mode. Option 2: Input of AD converter.
17	11	PB1/AD1	I/O	
18	12	PB2/AD2	I/O	
19	13	PB3/AD3	I/O	
20	14	PB4/AD4	I/O	
21	15	PB5/AD5	I/O	
22	16	PB6/AD6	I/O	
23	17	PB7/AD7	I/O	

24	18	PD0/AD8	I/O	
25	19	PD1/AD9	I/O	Note: For Pin 19 (PD3/AD11/ADVref). If it is programmed as the reference AD voltage (ADVref), then only 11 channels of AD can be used (i.e. AD[10:0]). Or otherwise, when 12 channels will be used, the reference voltage is VDDA.
26	20	PD2/AD10	I/O	
27	21	PD3/AD11/ ADVref	I/O	
28	22	PD4 /PWM0	I/O	Option 1: GPIO Port, With Schmitt-trigger and 30KΩ **programmable** pull-up resistor in input mode. Option 2: 8-bit PWM.
29	23	PD5/PWM1	I/O	
30	24	PD6/PWM2	I/O	
31	25	PD7/PWM3	I/O	
32	26	PA0/EXINT0	I/O	Option 1: GPIO Port, With Schmitt-trigger and 30KΩ pull-up resistor in input mode. Option 2: External interrupt.
33	27	PA1/EXINT1	I/O	
34	28	PA2/EXINT2	I/O	
35	29	PA3/EXINT3	I/O	
36	30	PA4/EXINT4	I/O	
37	31	PA5/EXINT5	I/O	
38	32	PA6/EXINT6	I/O	
39	33	PA7/EXINT7	I/O	
40	34	PC0	I/O	GPIO Port, With Schmitt-trigger and 30KΩ pull-up resistor in input mode.
41	35	PC1	I/O	
42	36	PC2	I/O	
43	37	PC3	I/O	
44	38	PC4/SCL	I/O	Option 1: GPIO Port, With Schmitt-trigger and 30KΩ pull-up resistor in input mode. Option 2: Hardware I^2C interface
45	39	PC5/SDA	I/O	
46	40	PC6	I/O	GPIO Port, With Schmitt-trigger and 30KΩ pull-up resistor in input mode.
47	41	PC7	I/O	
48	42	VDD	PWR	+5V power supply voltage.
1	43	XTAL1	I	Crystal oscillator input
2	44	XTAL2	O	Crystal oscillator output.
3	45	VSS	PWR	Ground

4	46	RESET	I	Reset input. Active high. This pin has an internal pull-down resister connected.
5	47	PE0/NUPE	I/O	Option 1: GPIO Port, With Schmitt-trigger and 30KΩ pull-up resistor in input mode. Option 2: Downstream port power enable, low active and internal pull-up.
6	48	PE1/NOVI	I/O	Option 1: GPIO Port, With Schmitt-trigger and 30KΩ pull-up resistor in input mode. Option 2: Downstream port over-current detection, low active and internal pull-up.
		VPP	I/O	High Voltage pin used in test mode and operating in 0~15V (not bonded)
		TM[1:0]	I/O	Analog pins used in test mode and operating in 0~VDD. (not bonded)

Note:

1. For flash programming purpose, a total of 18 pins are used. They are PB[7:0], PC[2:0], PD[7], PE[1:0], XTAL1, RESET, VDD, VSS.
2. PE[7:2] shown in the core pad map are simply GPIO ports with Schmitt-trigger and 30KΩ pull-up resistor in input mode.

Table 2. WT6561F Signal Description

2.2 Pin Configuration

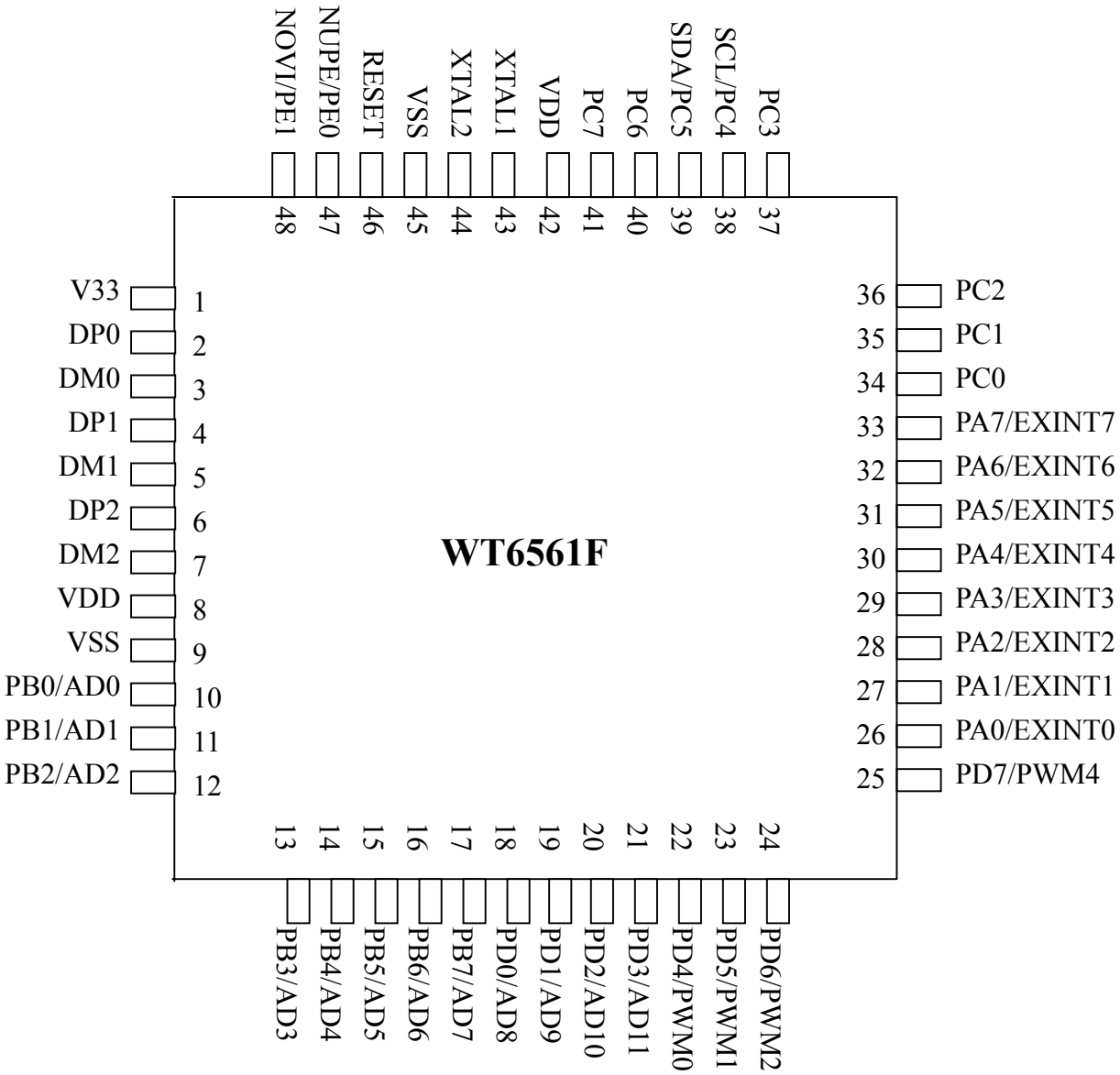


Figure 1. WT6561F 48-Pin QFP Package

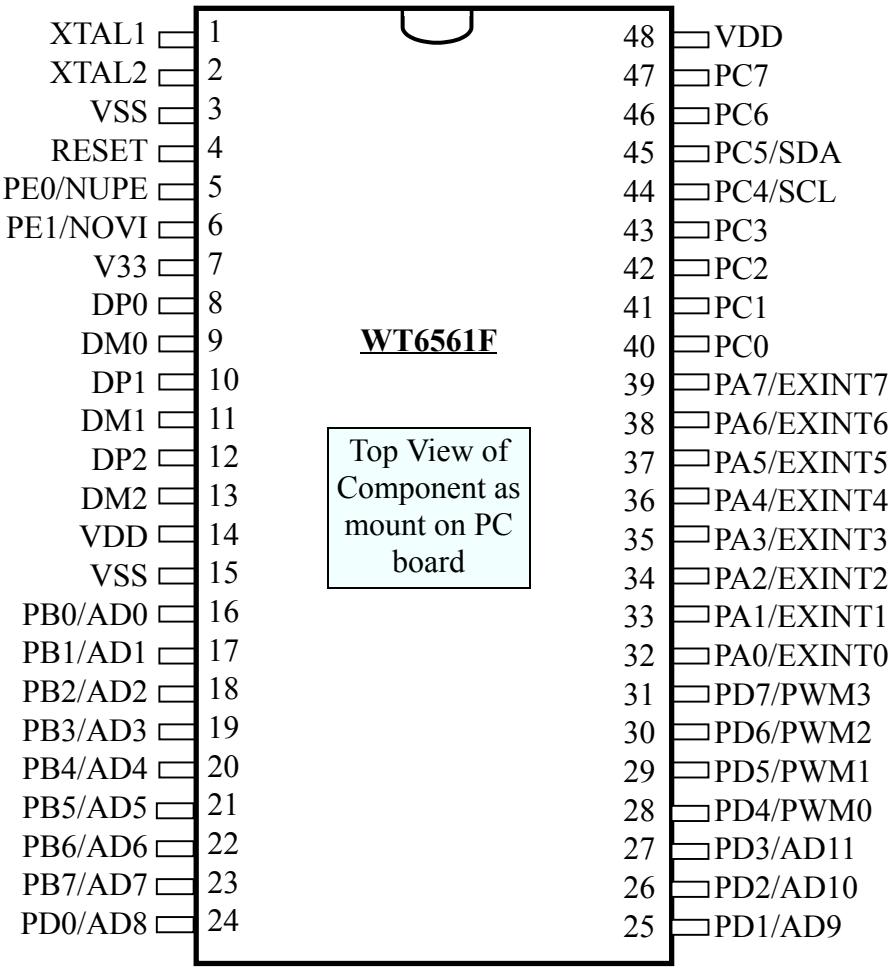


Figure 2. WT6561F 48-Pin DIP Package

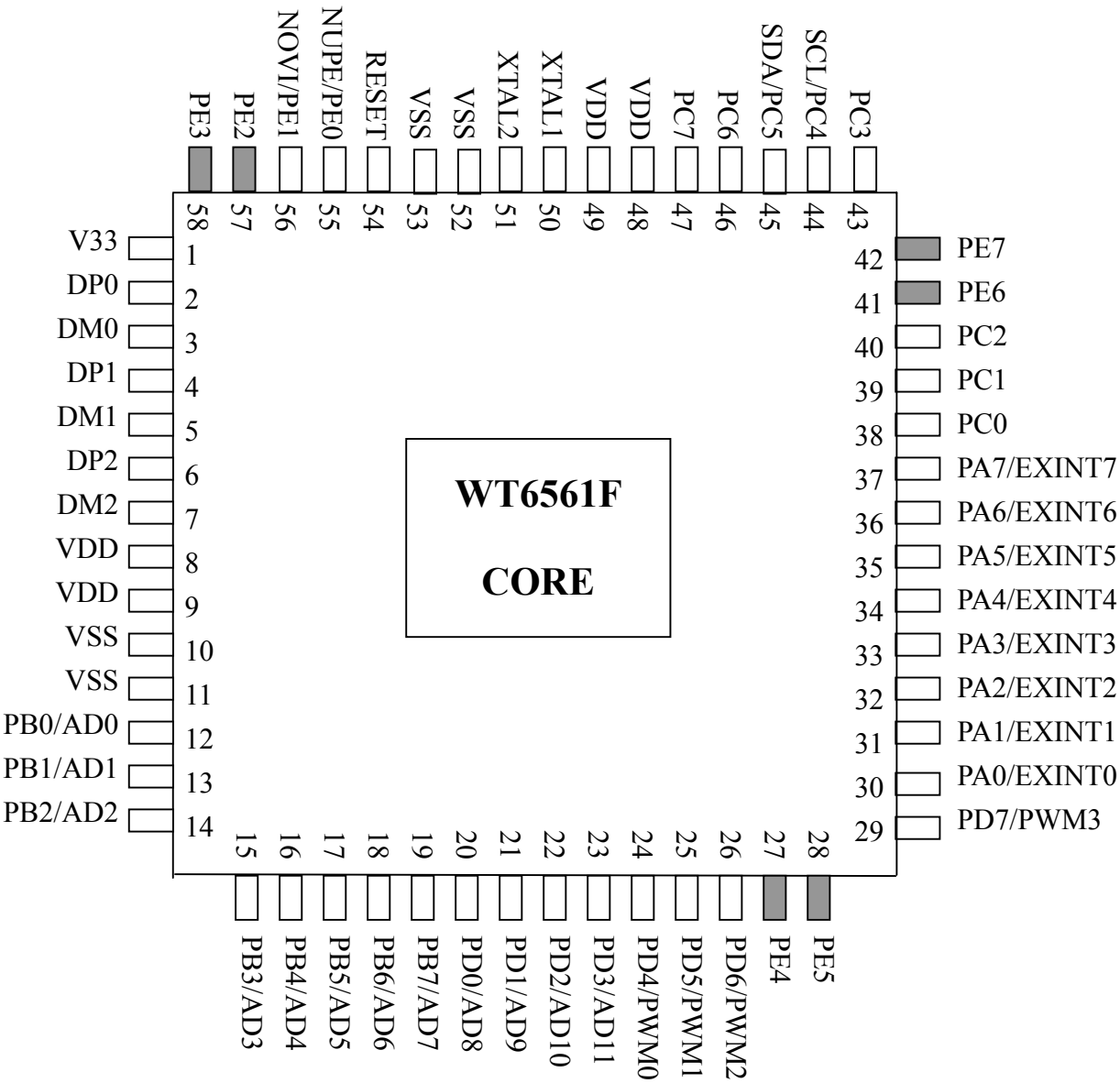


Figure 3. WT6561F Core Pads Map

Note: Three pads, TM[0], TM[1] and VPP for foundry usage, is not shown in the figure.

3 Functional Description

The WT6561F is a physical entity that conjoins a device and 2 downstream USB interface to a compound device with USB interface. It functions as an USB device with an 2-port hub. Operations of the USB interface and device function are controlled through the use of external function registers (XFRs) , special function registers (SFRs) , SIE, HIU, SIL, FIFOs and 8051 micro-controller that are described in the following sections.

3.1 WT6561F USB Module

The USB function interface manages communications between the Host and the USB function. The WT6561F interface consists of the USB full / low speed transceiver, the serial bus engine (SIE), the hub interface unit (HIU), the system interface logic (SIL), and the transmit / receive FIFOs. The USB transceiver in WT6561F provides a physical interface to USB lines. The SIE handles communication protocol of USB. The HIU manages data transmission between upstream and downstream ports. The SIL handles data transfers and provides the interface among the SIE, the 8051 CPU and the function FIFOs.

The main blocks in the USB module are:

1. **Full / Low Speed USB Transceiver:** This is an on-chip transceiver having one differential driver to transmit the USB data onto the USB bus and single ended receivers on the D+ and D- lines as well as a differential receiver to receive the USB data signal on the USB bus.

2. **Serial Bus Interface Engine (SIE):** The SIE does all the front-end functions of USB protocol such as clock/data separation, sync-field identification, NRZI-NRZ conversion, token packet decoding, bit stripping, bit stuffing, NRZ-NRZI conversion, CRC5 checking and CRC16 generation and checking. Besides, it manages detecting of reset, suspend and resume signals on the upstream port of the WT6561F to wakeup the system from the suspend state. It also provides serial-to-parallel conversion for the serial packet from the full speed USB transceiver to 8 bit parallel data to the system interface logic

and for 8 bit parallel data from the system interface logic to serial packet to the full speed USB transceiver.

3. **Hub Interface Unit (HIU):** The HIU processes all the USB packets transmission, it detects SOP / EOP for each packet and enable / disable USB data line to send packets in both direction.

4. **System Interface Logic (SIL):** The SIL operates in conjunction with the 8051 CPU to provide the capabilities of controlling the operation of the FIFOs. The SIL also monitors the status of the data transactions, transfers event control to the 8051 CPU through interrupt requests at the appropriate moment, initiate resume signaling to USB bus while the WT6561F is in power-down mode. Operation of the SIL is controlled through the use of external function registers.

5. **Device Function / Hub-Function FIFOs:** The WT6561F device function interface has four endpoints that can support three types of USB data transfer: control, interrupt and bulk transfer. Transmit FIFOs are written by 8051 CPU, then read by SIL for transmission. Receive FIFO is written by the SIL following reception, then read by the 8051 CPU. Endpoint 0 supports control transfer for configuration / command / status type communication flows between client software and function. Endpoint 1/2/3 supports interrupt/bulk transfer. The hub function has 2 endpoints supporting two types of USB data transfer: control and interrupt. Endpoint 0 contains **two** FIFO for transmit and receive while endpoint 1 is used as hub status-change notification and only a byte register is used.

3.2 Micro-controller

The 8051 CPU is a high performance 8-bit on-chip micro-controller running the firmware associated with the operation of the function. As shown in Figure -(TBD), it features 16K-byte Flash, 512-byte RAM and two 16 bit timers. In addition, the 8051 has two power saving modes enabling further power reduction.

1. **16-bit Timer:** The WT6561F has two timers that can be clocked by oscillator. It can be programmed for applications such as periodically generating interrupt requests and serving as a firmware watchdog timer.
2. **8051 On-Chip Memory:** The 8051 provides on-chip program memory beginning at location 0000H where, following chip reset, the first instruction is fetched and executed from. The 8051 CPU also provides on-chip data RAM beginning at location 00H. Locations 00H-7FH can be accessed with direct, indirect addressing while locations 80H-FFH can only be accessed with indirect addressing. Locations 20H-2FH are bit addressable.

3.3 WT6561F Address Space Mapping

The WT6561F has five address spaces : a program memory space, an internal data memory space, a special function register space, an external function register space, and a register file. Table 3 shows the addressing mapping of the WT6561F.

Memory Type	Size	Location	Data Addressing
Code	8K bytes	0000H-1FFFH	Indirect using MOVC instruction
External Function Register	64 bytes	00H-3FH	Indirect using MOVX instruction
Embedded External RAM	192bytes	40H-FFH	Indirect using MOVX instruction
Internal Data	128 bytes	00H-7FH	Direct, Indirect
	128 bytes	80H-FFH	Indirect
SFRs	128 bytes	80H-FFH	Direct
Register File (1)	8 bytes	R0-R7	Register

Note:

Direct: Direct Byte Addressing

Indirect: Indirect Byte Addressing

Table 3. Addressing Mapping

3.3.1 WT6561F Special Function Register Address Space

The special function registers (SFRs) reside in this optimized 8051 micro-controller core. Table 4 lists the location of all the WT6561F SFRs. Please refer to the 8051 data sheet for bit definition of each SFR.

Data Address	Register Name	Description
80H	P0	Port 0
81H	SP	Stack Point
82H	DPL	Data Point Low
83H	DPH	Data Point High
87H	PCON	Power Control Register
88H	TCON	Timer Control Register
89H	TMOD	Timer Mode Register
8AH	TL0	Timer 0 Low Order
8CH	TH0	Timer 0 High Order
90H	P1	Port 1 (As PB)
A0H	P2	Port 2 (As PC)
A8H	IE	Interrupt Enable Register
B0H	P3	Port 3
B8H	IP	Interrupt Priority Register
D0H	PSW	Program Status Word
E0H	ACC	Accumulator
F0H	B	B Register

Table 4. WT6561F Special Function Register Layout

3.3.2 External Function Register Address Space

The external function registers (XFRs) reside inside the USB module. The 8051 is connected to one of these registers when the register is addressed by the contents of registers R0 or R1 in the internal data memory. Two instructions, MOVX @Rr, A and MOVX A, @Rr can be used for data movement between the XFRs and accumulator of the 8051.Table 9 lists the location of all the XFRs. When the instruction, MOVX @Rr, A or MOVX A, @Rr, is executed, the address contained in R0 or R1 registers is latched by ALE signal and then the direction of data movement between the XFRs and the 8051 can be controlled by the signals $\overline{WR}$ or $\overline{RD}$ subsequently generated by the 8051.

3.4 Clock Unit

The WT6561F can use an external clock or an on-chip oscillator with crystal or ceramic resonator as its clock source. The timing waveform at XTAL1 can be provided by:

- an on-chip oscillator employing an external crystal / resonator connected across XTAL1 and XTAL2
- an external clock source connected to XTAL1

The frequency of clock is 6MHz in normal operation, and is used as the internal X8 PLL input, then the PLL output 48MHz clock (4 times of full-speed USB bit-rate and internal CPU clock).

As shown in Figure 4, the clock to CPU control section is stopped where "1" is set in bit 0 (IDL) of the power control register (PCON) in firmware, thereby the CPU operation is halted in idle mode. Idle mode freezes the clocks to the CPU at known states while the peripherals continue to be clocked. The CPU status before entering idle mode is preserved. The contents of the SFRs, XFRs and RAM are also retained. Idle mode can be used while the device is in un-enumerated state following chip reset. Activation of an enabled interrupt and a logic high on chip reset are the ways to exit the idle mode.

The clock to where the CPU controlled section and peripherals that including some portions of USB function is stopped at where bit 1 (PD) of the power control register (PCON) is set in firmware. Therefore both oscillator and CPU operation are halted in power-down mode. The CPU status before entering power-down mode is preserved. In addition, the contents of the SFRs, XFRs and RAM are also retained. For suspend, firmware must put the WT6561F into power-down mode to meet the USB limitation of 500 μA. Activation of an enabled interrupt and a logic high on chip reset are the ways to exit the power-down mode.

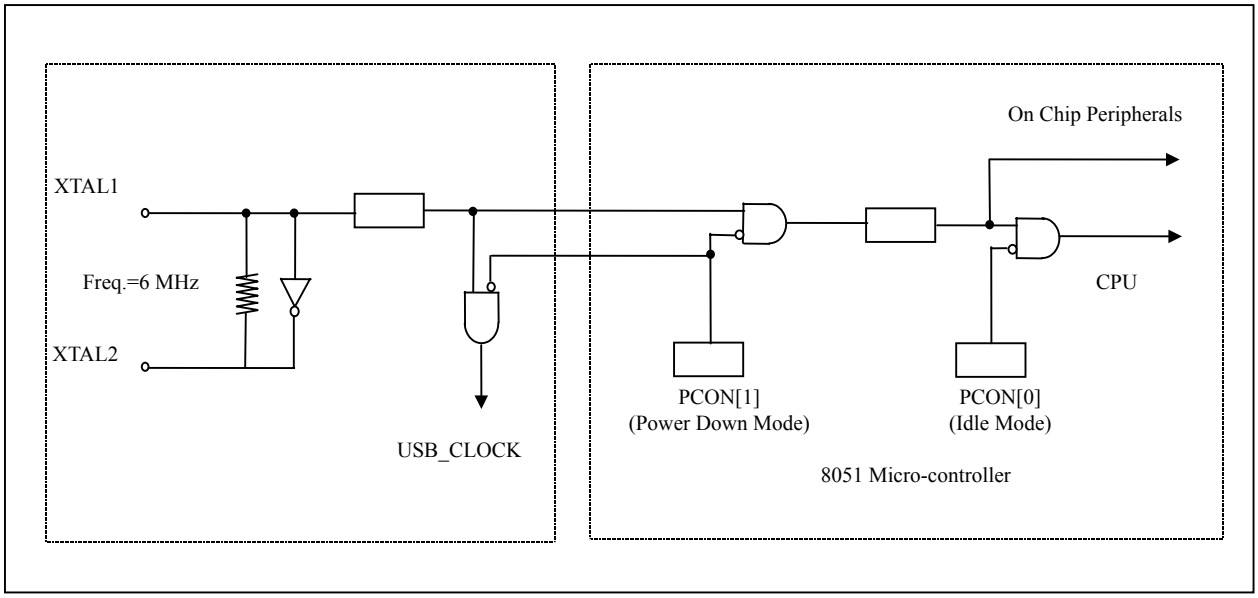


Figure 4. Clock Circuit

3.5 Reset

Chip reset can be initiated by the built-in power on reset (low voltage reset) or an USB-initiated reset, or a high level of signal on the RESET pin for at least 100us while the oscillator is running.

Built-in power on reset circuit can generate a pulse to reset the entire chip.

A ”low” voltage (VCC ≤ V_{LVR}) causes a reset condition for entire chip to prevent the chip from being placed at unknown state.

3.6 Power-down Mode and Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the idle mode is activated. Once in the idle mode the CPU status is preserved in its entirety. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware and then the idle mode is terminated.

The instruction that sets PCON.1 is the last executed prior to entering power-down mode. Once in the power-down mode, the oscillator is stopped. The contents of the on-chip RAM, the Special Function Registers and USB External Function Registers are saved. Hardware reset and activation of any enabled interrupt is the ways of exiting the power-down mode. Power-down mode should be used for USB suspend operation. PCON.1 has to be set in the ISR of interrupt caused by active SUSPEND signal.

The WT6561F can initiate resume signaling to the USB host through remote wakeup of the USB function while it is in power-down mode. While in power-down mode, remote wakeup has to be initiated through assertion of an enabled interrupt. In the ISR for the interrupt activated by active SUSPEND signal, the interrupt should be enabled in firmware prior to entering power-down mode which can be terminated by activation of an enabled interrupt signal or an enabled USB resume interrupt signal (RESUME). In the ISR, interrupt signal should be disable before escaping from power-down mode. Upon completion of the ISR, program execution continues with the instruction immediately following the instruction that activated the power-down.

Note: Add two “NOP” instructions after set power-down instruction in F/W to avoid code execution error.

3.7 Interrupt

There are 13 interrupt sources share two external interrupt inputs of the 8051:

Interrupt 0 This interrupt is connected to the external hardware interrupt input 0 of the 8051. In WT6561F, this interrupt is used by hub function interrupts (include suspend / resume processing), The interrupt vector is 03H.

Interrupt 1 This interrupt is connected to the external hardware interrupt input 1 of the 8051. In WT6561F, The device function interrupts and port-3 bit interrupts use it to operate. In normal operation, interrupt is disabled. In power-down mode to support remote wakeup, interrupt is enabled to terminate the power-down mode (suspend state). and its interrupt vector is 13H.

3.8 Function Endpoint

The WT6561F supports four device function endpoints. Endpoint 0 contains a FIFO each for transmit and receive. Endpoint 1, endpoint 2 and 3 can be programmed to transmit or receive. Endpoint 0 handles control data transfer. Endpoint 1, endpoint 2 and 3 can be interrupt or bulk transfer. The EPINDEX register selects the endpoint for any given data transaction.

The WT6561F supports two hub function endpoints. Endpoint 0 contains a FIFO each for transmit and receive control data while endpoint 1 is used as hub status-change and only a byte register is available.

3.9 Transmit FIFOs

3.9.1 Transmit FIFOs Features

The transmit FIFOs are data buffers with the following features (See Figure 5):

- support for one data set of not greater than 8/16/32/64 bytes (programmable by counter setting)
- a byte count register to store the number of bytes in the data set
- protection against overwriting data in a full FIFO
- capable to retransmit the current data set

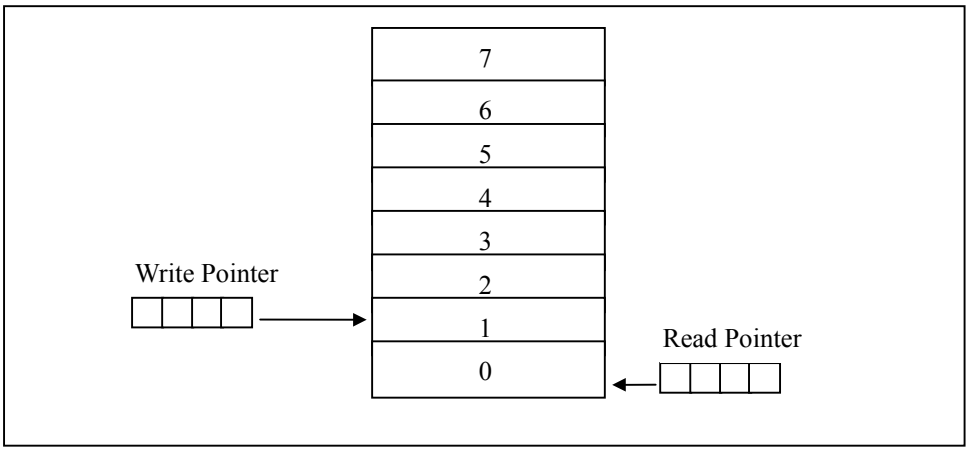


Figure 5. Transmit FIFO Outline (example for 8 bytes FIFO)

The 8051 CPU writes to the FIFO location specified by the write pointer also used as the byte-counter to indicate how many bytes have been written and not yet read by the SIL. The write pointer automatically increments by one after a write and decrements by one after a read. The read pointer points the next FIFO location to be read by the SIL. The read pointer automatically increments by one after a read. The transmit FIFO is inhibited to be read by the SIL when it is empty or before a data set has been successfully written into it.

3.12.2 Transmit Data Set Management

TXFULL = 1 in the TXFLG register, indicates data set has been written into the FIFO and is ready for transmission. Following reset, TXFULL = 0 and TXEMP = 1, signifying an empty FIFO. Only the first eight bytes of the data set which size is greater than eight are written into the FIFO. In this case, TXFULL is not set until a write to TXCNT. In the case of TXFULL = 1 farther writing to TXDAT or TXCNT are ignored. Please note that the content of TXCNT determines the number of bytes transmitted over the USB lines. Discrepancy between the byte number written to TXCNT and number of bytes actually written to the FIFO will cause an unexpected result. Read the FIFO is prohibited when the FIFO is empty or TXFULL = 0.

Two events cause the TXFULL to be updated:

- A new data set is written to the FIFO: The CPU writes bytes to the FIFO via TXDAT and writes the number of bytes to TXCNT. TXFULL is only set after the write to TXCNT. Set TXCNT=0 indicates a zero length transmission. In this case, TXFULL is set and TXEMP remains unchanged to indicate the FIFO is still empty. This process is illustrated in Table 5.

- A data set in the FIFO is successfully transmitted: The SIL reads the data set from the FIFO for transmission. When a good transmission is acknowledged, the TXFULL is cleared and TXEMP is set.

TX FULL	TX EMP	Zero Length Transmission	Write bytes to TXDATx	Data Set Written	TX FULL	TX EMP
0	0	No		Yes	1	0
0	1	No		Yes	1	0
0	1	Yes	Write byte count to	No	1	1
1	-	-	TXCNTx	Write Ignored	1	-

Table 5. Writing to the Byte Count Register

When a good transmission is completed, both read pointer and write pointer is advanced to

the start point of the FIFO to set up for transmitting the next data set. When a bad transmission is encountered, the read pointer is reversed to the start point of the FIFO to enable the SIL to re-read the last data set for retransmission. The pointer reversal and advance are accomplished automatically by hardware. Table 6 summarizes how actions following a transmission depend on TXERR and TXACK.

TXERR	TXACK	Action at End of Transfer Cycle
0	0	No operation
0	1	Read Pointer and Write Pointer both are set to the start point of FIFO
1	0	Read Pointer is set to the start point of FIFO

Table 6. Truth Table for Transmit FIFO Management

3.12.3 Transmit FIFO Registers

TXDAT, the transmit FIFO data register (see Table 17)
TXCNT, the transmit FIFO byte count register (see Table 20)
TXCON, the transmit FIFO control register (see Table 18)
TXFLG, the transmit FIFO flag register (see Table 19)

These registers are endpoint indexed. They are used as a set to control the operation of the transmit FIFO, associated with the current endpoint specified by the EPINDEX register

3.13 Receive FIFOs

The WT6561F has two receive FIFO for Device / hub endpoint 0. This FIFO is shared with the transmit FIFO. Detail operating is described in section 5.15 .

3.13.1 Receive FIFO Features

The receive FIFO is a data buffer with the following features (see Figure 6):

- support for one data set of not greater than eight bytes
- a byte count register accesses the number of bytes in the data set
- flag to signal a full FIFO and an empty FIFO
- capability to re-receive the last data set

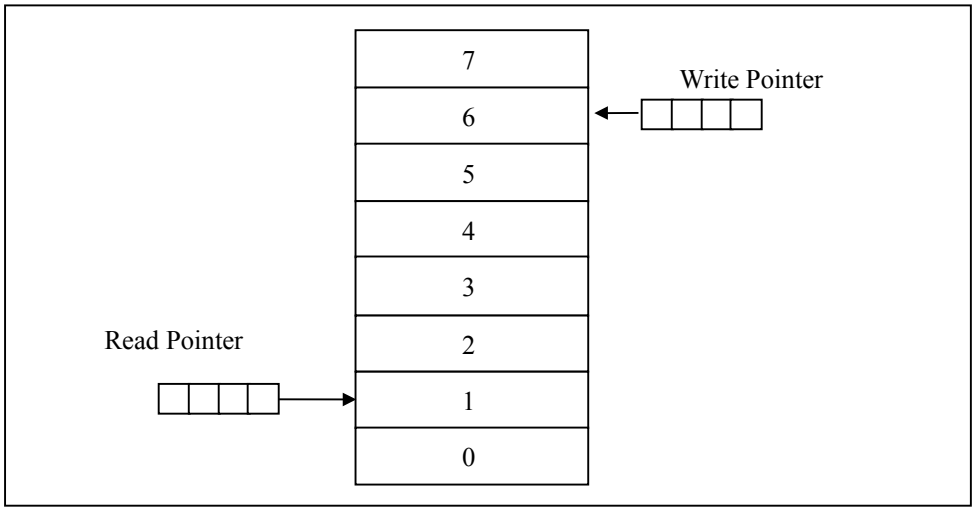


Figure 6. Receive FIFO Outline(example for 8 bytes FIFO)

The SIL writes to the FIFO location specified by the write pointer also used as the byte-counter to indicate how many bytes have been written and not yet read by the 8051 CPU. The write pointer automatically increments by one after a write and decrements by one after a read. The read pointer points the next FIFO location to be read by the 8051 CPU. The read pointer automatically increments by one after a read. The receive FIFO is inhibited to be read by the 8051 CPU when it is empty or before a data set has been successfully written into it.

When a SETUP token is detected by the SIL, the SIL flushes the FIFO even if the FIFO is being read by the 8051 CPU.

3.13.2 Receive Data Set Management

RXFULL = 1 in the RXFLG register, indicates the data set has been written into the FIFO and is ready for reception. Following reset, RXFULL = 0 and RXEMP = 1, signifying an empty FIFO. Only the first eight bytes of the data set which size is greater than eight are written into FIFO. RXFULL is however not set until reception is done and successfully acknowledged. RXFULL is cleared by setting the FFRC bit of RXCON in firmware to indicate the data set has successfully read by CPU. In the case of RXFULL = 1 farther writes to FIFO are ignored. Please note that the content of RXCNT should be read by 8051 CPU to determine the numbers of bytes need to be read from FIFO by 8051 CPU. Further reading from an empty FIFO is ignored.

RXFULL	RXEMP	Status
0	0	Data set is being written to FIFO
0	1	Empty
1	0	Data set already written to FIFO
1	1	Zero length packet received

Table 7. Status of the Receive FIFO Data Set

When a good reception is completed and the data set has been successfully read by the 8051, firmware must set the FFRC bit of RXCON to advance the write pointer and read pointer to the start point of the FIFO to set up for receiving the next data set. When a bad reception is completed, the write pointer can be reversed to the position of the start point of the FIFO to enable the SIL to re-write the last data set for re-reception. The pointer advance and reversal are accomplished automatically by hardware. Table 8 summarizes how actions following a reception depend on RXERR and RXACK.

RXERR	RXACK	Action at End of Transfer Cycle
0	0	No operation
0	1	Read Pointer and Write Pointer are set to the start point of FIFO when firmware sets the FFRC bit of RXCON

1	0	Write Pointer is set to the start point of FIFO

Table 8. Truth Table for Receive FIFO Management

3.13.3 Receive FIFO Registers

RXDAT, the receive FIFO data register (see Table 33)
RXCNT, the receive FIFO byte count register (see Table 36)
RXCON, the receive FIFO control register (see Table 34)
RXFLG, the receive FIFO flag register (see Table 35)

These registers are endpoint indexed. They are used as a set to control the operation of the receive FIFO associated with the current endpoint specified by the EPINDEX register.

3.14 Setup Token Receive FIFO Handling

SETUP tokens received by the endpoint zero must be acknowledged, even if the receive FIFO is not empty. As described in section 5.14, when a SETUP token is detected by the SIL, the SIL flushes the FIFO and sets the STOVW bit of RXSTAT for reset and locking the read pointer. These prevent RXURF bit of RXFLG and the read pointer from being set if the receive FIFO flush occurs in the middle of an 8051 CPU data read cycle. The STOVW bit is cleared and the EDOVW bit is set when a SETUP packet has been successfully acknowledged. The read pointer will remain locked until both the STOVW and EDOVW bits are cleared. For SETUP packets only, firmware must clear EDOVW before reading data from the FIFO. If this is not done, data read from the FIFO will be invalid. After processing a SETUP packet, firmware should always check the STOVW and EDOVW flags before setting the RXFFRC bit. When a SETUP packet either has been or is being received, setting of RXFFRC has no effect if either STOVW or EDOVW is set.

3.15 Suspend and Resume

In order to reduce the power consumption, WT6561F automatically enters the suspend state when it has observed no bus traffic for 3 ms. When in suspend, the 8051 CPU and its peripherals are in power down mode, an interrupt is enabled to support remote wakeup. The entire chip consumes less than 500 μA in suspended state.

WT6561F exits suspend mode when there is bus activity. A USB device may also request the host exits from suspend or selective suspend by using electrical signaling to indicate remote wakeup. The ability of a device to signal remote wakeup is optional. WT6561F allows the host to enable or disable this capability. Device states are described in Figure 7.

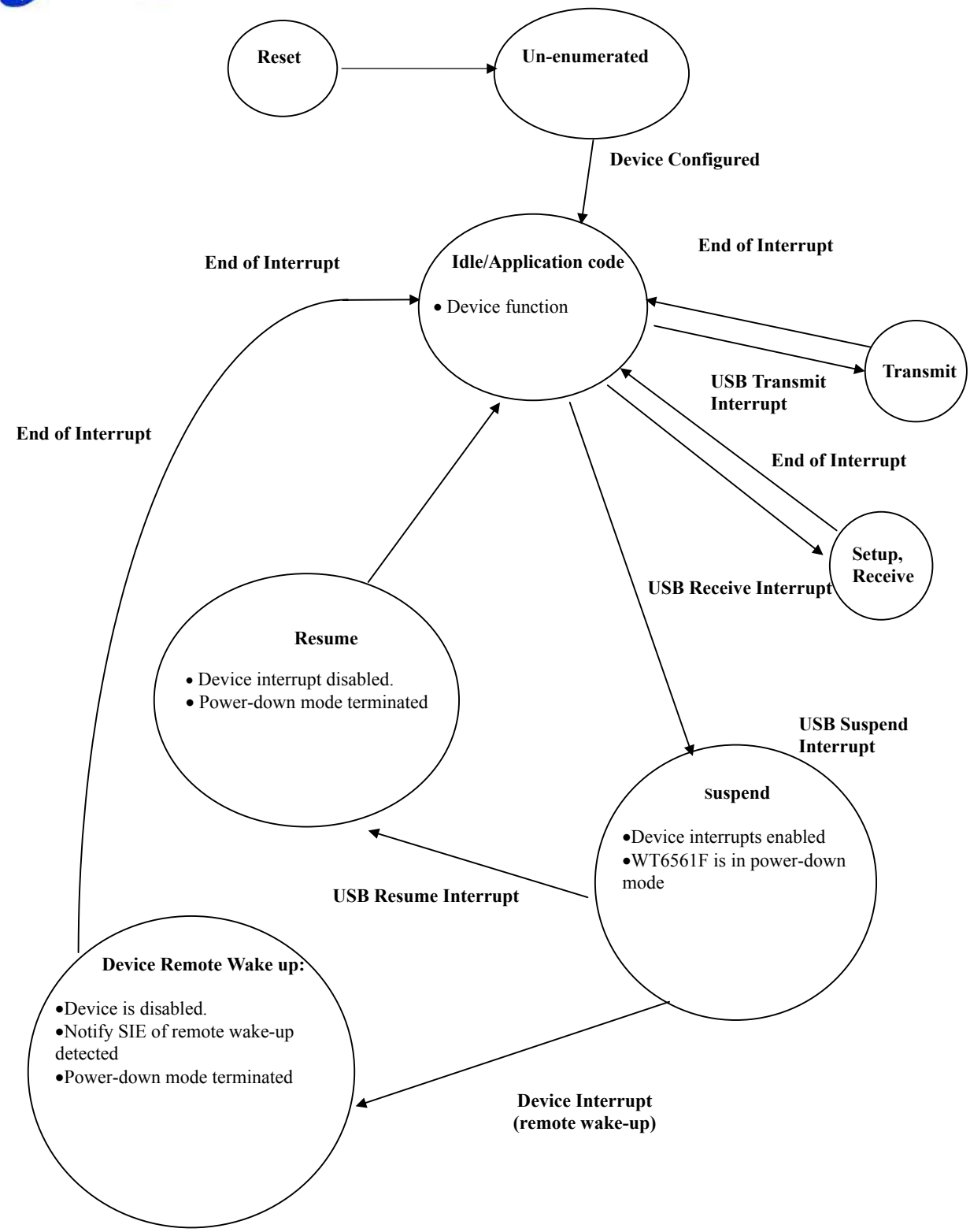


Figure 7. Suspend and Resume State Diagram

4 USB External Function Registers

Data Address	Register Name	Description
00H	FADDR	Function Address Register
01H	USBFI	USB Function Interrupt Register
02H	USBFIE	USB Function Interrupt Enable Register
03H	SIEI	SIE Interface Register
04H	(TEST)	Reserved for Testing
05H	EPINDEX	Endpoint Index Register
06H	EPCON	Endpoint Data-flow Control Register
07H	WDTRST	Watchdog Timer Reset Register
08H	TXDAT	Transmit FIFO Data Register
09H	TXCON	Transmit FIFO Control Register
0AH	TXFLG	Transmit FIFO Flag Register
0BH	TXCNT	Transmit FIFO Byte Count Register
0CH	TXSTAT	Endpoint Transmit Status Register
0DH	HPBSTAT	Hub Port Bus Status Register
0EH	HPSC	Hub Port Status Change Register
0FH	NOTEBOOK	Notebook Register
10H	HADDR	Hub Address Register
11H	USBHI	USB Hub Interrupt Register
12H	USBHIE	USB Hub Interrupt Enable Register
13H	HSTAT	Hub Status and Configuration Register
14H	HEPSC	Hub Endpoint 1 Status Change Register
15H	HPINDEX	Hub Port Index Register
16H	HPCON	Hub Port Control Register
17H	HPSTAT	Hub Port Status Register
18H	RXDAT	Receive FIFO Data Register
19H	RXCON	Receive FIFO Control Register
1AH	RXFLG	Receive FIFO Flag Register
1BH	RXCNT	Receive FIFO Byte Count Register
1CH	RXSTAT	Endpoint Receive Status Register
1DH	PA	Port A (corresponding P0) data
1EH	PD	Port D (corresponding P3) data
1FH	PE	Port E (corresponding P4) data

Data Address	Register Name	Description
20H	EXINTD	Rising/Falling Trigger Control for External Intr.
21H	EXINTEN	Enable/Disable Control for External Interrupts
22H	WDTEXT	Extension of watch-dog timer
23H	RMPEN	Enable/Disable port Remote wakeup
24H	PWM0	PWM data 0
25H	PWM1	PWM data 1
26H	PWM2	PWM data 2
27H	PWM3	PWM data 3
28H	PWMEN	Enable of PWMs
29H	ADL	AD data lower 8 bits
2AH	ADH	AD data upper 4 bits
2BH	AD_C	AD control bits
2CH	PUCTRLB	**PB programmable pull-up**
2DH	PUCTRLD	**PD programmable pull-up**
2EH	ADCHENL	ADC Channel enable select, bit 7:0
2FH	ADCHENH	ADC Channel enable select, bit 11:8
30H	PSWEN	Power Switch Control
31H	PAOE	PA Output Enable
32H	PDOE	PD Output Enable
33H	PEOE	PE Output Enable
34H	I2CCON	I2C Function Control (For Firmware I2C only)
35H (R)	**I2CSTA**	**I2C Interface Status Register**
35H (W)	**I2CCON2**	**I2C Interface Control Register**
36H (W)	**I2CTX**	**I2C Interface Transmit Buffer Register**
36H (R)	**I2CRX**	**I2C Interface Receive Buffer Register**
37H (W)	**I2CADR**	**I2C Interface Address Register**

Table 9. External Function Register Layout

FADDR

Address: 00H
Reset State: 0000 0000B

Function Address Register. This XFR holds the address for the USB function. During bus enumeration, it is written with a unique value assigned by the host.

7							0
---	FA6:0						

Bit Number	Bit Mnemonic	Function
7	---	Reserved: Write zero to this bit.
6:0	FA6:0	7-bit Programmable Function Address: This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only.

Table 10. Function Address Register

USBFI

Address: 01H
Reset State: x000 0000B

USB Function Interrupt Register. A '1' indicates that an interrupt is actively pending. All bits are cleared after a read.

7							0
RMPINT	ADINT	EXINT	USBx 3INT	USBx 2INT	USBx 1INT	USBRx 0INT	USBTx 0INT

Bit Number	Bit Mnemonic	Function
7	RMPINT	(Remote wake up interrupt enable) During suspend, if any of the enabled port (see RMPEN) detects "low", then RMPINT is set and remote-wakeup is processed
6	ADINT	AD Converter Interrupt flag. This bit is set when the AD data was converted
5	EXINT	External Interrupt 1: Interrupt detected (Only occurs when any of EXINTEN is set to '1' 0: No interrupt
4	USBx3INT	Function Transmit/Receive Dong Flag for endpoint 3
3	USBx2INT	Function Transmit/Receive Dong Flag for endpoint 2
2	USBx1INT	Function Transmit/Receive Dong Flag for endpoint 1
1	USBRx0INT	Function Receive Dong Flag for endpoint 0
0	USBTx0INT	Function Transmit Done Flag for endpoint 0.

Table 11. USB Function Interrupt Register

USBFIE

Address: 02H
Reset State: x000 0000B

USB Function Interrupt Enable Register.

7							0
---	ADINT_IE	---	USBx 3INT_IE	USBx 2INT_IE	USBx 1INT_IE	USBRx 0INT_IE	USBTx 0INT_IE

Bit Number	Bit Mnemonic	Function
7	Reserved	
6	ADINT_IE	ADINT Interrupt Enable
5	Reserved	
4	USBx3INT_IE	Function Transmit/Receive Dong Interrupt Enable 3: Enable USBx3INT
3	USBx2INT_IE	Function Transmit/Receive Done Interrupt Enable 2: Enable function transmit/receive done interrupt for endpoint 2 (USBx2INT).
2	USBx1INT_IE	Function Transmit/Receive Done Interrupt Enable 1: Enable function transmit/receive done interrupt for endpoint 1 (USBx1INT).
1	USBRx0INT_IE	Function Transmit Receive Done Interrupt Enable 0: Enable function transmit receive done interrupt for endpoint 0 (USBRx0INT).
0	USBTx0INT_IE	Function Transmit Done Interrupt Enable 0: Enable function transmit done interrupt for endpoint 0 (USBTx0INT).

Table 12. USB Function Interrupt Enable Register

For all bits, a ‘1’ means the interrupt is enabled and will cause an interrupt to be signaled to the micro-controller. A ‘0’ means the associated interrupt source is disabled and cannot cause an interrupt.

SIEI

Address: 03H
Reset State: xxxx x000B

USB SIE Interface Register.

7							0
---	---	---	---	----	USBRSTEN	DPEN	WAKEUP

Bit Number	Bit Mnemonic	Function
7:3	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
2	USBRSTEN	USB Reset Enable: Set this bit to enable USB reset. This bit should be set at least 500μs after DPEN is set. This bit is not reset by USB reset.
1	DPEN	DP0 Enable: When this bit is cleared, CEXT does not provide 3.3V output and is in high impedance state. In this case, the 1.5KΩ resistor does not connect to the DP0 line and the upstream port of the device is disconnected. Set this bit for normal operation. This bit is not reset by USB reset.
0	WAKEUP	Wakeup: This bit is used by the USB function to initiate a remote wakeup. Set by firmware to drive resume signaling on the USB lines to the host or upstream hub. Cleared by hardware when resume signaling is done.

Table 13. USB SIE Interface Register

EPINDEX

Address: 05H
Reset State: 1xxx xx00B

Endpoint Index Register. This Register identifies the endpoint pair. Its contents select the transmit and receive FIFO pair and serve as an index to endpoint-specific XFRs**.**

7							0
HORF	---	---	---	---	---	EPINX1	EPINX0

Bit Number	Bit Mnemonic	Function
7	HORF	Hub/function Bit: 1 = Hub. Selects USB hub FIFOs and XFRs. 0 = Function. Selects USB function FIFOs and XFRs.
6:2	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
1:0	EPINX1:0	Endpoint Index: 00 = Endpoint 0. 01 = Endpoint 1. 10 = Endpoint 2. 11 = Endpoint 3.

Table 14. Endpoint Index Register

The value in this register selects the associated bank of endpoint-indexed XFRs including TXDAT, TXCON, TXFLG, TXCNT, TXSTAT, RXDAT, RXCON, RXFLG, RXCNT, RXSTAT and EPCON.

EPCON Address: 06H
(Endpoint-indexed) Reset State: Endpoint 0 001x 0101B
Hub Endpoint 1 x0xx xx00B
Function Endpoint 1,2,3 x0xx xx00B

Endpoint Control Register. This XFR configures the operation of the endpoint specified by EPINDEX.

7							0
RXSTL	TXSTL	CTLEP	---	RXIE	RXEPEN	TXOE	TXEPEN

Bit Number	Bit Mnemonic	Function
7	RXSTL	Stall Receive Endpoint: Set this bit to stall the receive endpoint. Clear this bit only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and RXSETUP is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP token by a control endpoint.
6	TXSTL	Stall Transmit Endpoint: Set this bit to stall the transmit endpoint. This bit should be cleared only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid IN token. When this bit is set and RXSETUP is set, the receive endpoint will NAK.
5	CTLEP	Control Endpoint: Set this bit to configure the endpoint as a control endpoint. Only control endpoint is capable of receiving SETUP tokens.
4	---	Reserved: Value read from this bit is indeterminate. Write zero to this bit.
3	RXIE	Receive Input Enable: Set this bit to enable data from the USB to be written into the receive FIFO. If cleared, the endpoint will not write the received data into the receive FIFO and at the end of reception, but will return a NAK handshake on a valid OUT token if the RXSTL bit is not set. This bit does not affect a valid SETUP token. A valid SETUP token and packet overrides this bit if it is cleared, and place the receive data in the FIFO.
2	RXEPEN	Receive Endpoint Enable: Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to valid OUT or SETUP token. This bit is hardware read-only and has the highest priority among RXIE and RXSTL. Note that endpoint 0 is enabled for reception upon reset.
1	TXOE	Transmit Output Enable: This bit is used to enable the data in TXDAT to be transmitted. If cleared, the endpoint returns a NAK handshake to a valid IN token if the TXSTL bit is not set.
0	TXEPEN	Transmit Endpoint Enable: This bit is used to enable the transmit endpoint. When disabled, the endpoint does not response to a valid IN token. This bit is hardware read-only. Note that endpoint 0 is enabled for transmission upon reset.

Table 15. Endpoint Control Register

WDTRST Address: 07H
Reset State: xxxx xxxxB

Watchdog Timer Reset Register. After device reset, the hardware watchdog is cleared and disabled. Write AAH to WDTRST register can clear and enable the watchdog timer. The watchdog timer overflows in 10.9 ms. If the WDT overflows, it initiates a device reset. Firmware should write AAH to WDTRST to clear the WDT before it overflows.

7							0
WDTRST7:0							

Bit Number	Bit Mnemonic	Function
7:0	WDTRST7:0	Watchdog Timer Reset (write-only): Write AAH to clear and enable the WDT.

Table 16. Watchdog Timer Reset Register

TXDAT Address: 08H
(Endpoint-indexed) Reset State: xxxx xxxx B

Transmit FIFO Data Register. Data to be transmitted by the FIFO specified by EPINDEX is first written to this register.

7							0
TXDAT7:0							

Bit Number	Bit Mnemonic	Function
7:0	TXDAT7:0	Transmit Data Byte (write-only): To write data to the transmit FIFO, write to this register. The write pointer is incremented automatically after a write.

Table 17. Transmit FIFO Data Register

TXCON Address: 09H
(Endpoint-indexed) Reset State: 0xxx xxxxB

Transmit FIFO Control Register. Controls the transmit FIFO specified by EPINDEX.

7							0
TXCLR	---	---	---	---	---	---	---

Bit Number	Bit Mnemonic	Function
7	TXCLR	Transmit Clear: Setting this bit flushes the transmit FIFO, resets all the read/write pointers, sets the EMPTY bit in TXFLG, and clears all other bits in TXFLG. After the flush, hardware clears this bit.
6:0	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.

Table 18. Transmit FIFO Control Register

TXFLG Address: 0AH
(Endpoint-indexed) Reset State: xxxx 1000B

Transmit FIFO Flag Register. These flags indicate the status of data packets in the transmit FIFO specified by EPINDEX.

7							0
---	---	---	---	TXEMP	TXFULL	TXURF	TXOVF

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
3	TXEMP	Transmit FIFO Empty Flag (read-only): Hardware sets this bit when the data set has been read out of the transmit FIFO by SIL. Hardware clears this bit when the empty condition no longer exists. This bit always tracks the current transmit FIFO status. This flag is also set when a zero-length data packet is transmitted.
2	TXFULL	Transmit FIFO Full Flag (read-only): This flag indicates the data set is present in the transmit FIFO. This bit is set after write to TXCNT to reflect the condition of the data set. Hardware clears this bit when the data set has been successfully transmitted.
1	TXURF	Transmit FIFO Under-run Flag (read-, clear-only)*: Hardware sets this flag when an addition byte is read from an empty transmit FIFO. This is a sticky bit that must be cleared through firmware by writing a '0' to this bit. When the transmit FIFO under-runs, the read pointer will not advance -- it remains locked in the empty position.
0	TXOVF	Transmit FIFO Overrun Flag (read-, clear-only)*: This bit is set when an additional byte is written to a FIFO with TXFULL = 1. This is a sticky bit that must be cleared through firmware by writing a '0' to this bit. When the transmit FIFO overruns, the write pointer will not advance -- it remains locked in the full position.

Table 19. Transmit FIFO Flag Register

* When set, all transmission are NAKed.

TXCNT Address: 0BH
(Endpoint-indexed) Reset State: 0000 0000B

Transmit FIFO Byte Count Register. This register stores the number of bytes for the data packet in the transmit FIFO specified by EPINDEX.

7				0
---	---	TXCNT5	TXCNT4	TXCNT3:0

Bit Number	Bit Mnemonic	Function
7:6	---	Reserved: Write zeros to these bits.
5:0	TXCNT[5:0]	Transmit Byte Count (write-only): The number of bytes in the data set written to the transmit FIFO. When this register is written, TXFULL is set. Write the byte count to this register after writing data set to TXDAT.

Table 20. Transmit FIFO Byte Count Register

To send a status stage after a control write or no data control command or a null packet, write 0 to TXCNT.

TXSTAT Address: 0CH
(Endpoint-indexed) Reset State: 0000 0000B

Endpoint Transmit Status Register. Contains the current endpoint status of the transmit FIFO specified by EPINDEX.

7							0
TXSEQ	---	---	---	---	TXVOID	TXERR	TXACK

Bit Number	Bit Mnemonic	Function
7	TXSEQ	Transmit Current Sequence Bit (read, clear-only): This bit will be transmitted in the next PID and toggled on a valid ACK handshake. This bit is toggled by hardware on a valid SETUP token. The SIE will handle all sequence bit tracking. This bit should only be used when initializing a new configuration or interface.
6:3	---	Reserved: Write zeros to these bits.
2	TXVOID	Transmit Void (read-only): A void condition has occurred in response to a valid IN token. Transmit void is closely associated with the NAK/STALL handshake returned by the function after a valid IN token, due to the conditions that cause the transmit FIFO to be unable or not ready to transmit. Use this bit to check any NAK/STALL handshake returned by the function. This bit does not affect the USBTx*x*INT, TXERR or TXACK bit. This bit is updated by hardware at the end of a non-isochronous transaction in response to a valid IN token.
1	TXERR	Transmit Error (read-only): An error condition has occurred with the transmission. Complete or partial data has been transmitted. The error can be one of the following: 1. Data transmitted successfully but no handshake received. 2. Transmit FIFO goes into underrun condition while transmitting. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXACK bit at the end of data transmission (this bit is mutually exclusive with TXACK).
0	TXACK	Transmit Acknowledge (read-only): Data transmission completed and acknowledged successfully. The corresponding transmit done bit is set when active. This bit is updated by hardware along with the TXERR bit at the end of data transmission (this bit is mutually exclusive with TXERR).

Table 21. Endpoint Transmit Status Register

HPBSTAT Address: 0DH
(Port-indexed) Reset State: xxxx xxxxB

Hub port bus status register. This register indicates the current status of a port bus DP/DM status.

7							0
---	---	---	---	---	---	DPSTAT	DMSTAT

Bit Number	Bit Mnemonic	Function
7:2	---	Reserved: Values read from these bits are indeterminate.
1	DPSTAT	DP Status (read-only): Value of DP for the port at end of last frame. Set and cleared by hardware at the EOF2 point near the end of a frame
0	DMSTAT	DM Status (read-only): Value of DM for the port at end of last frame. Set and cleared by hardware at the EOF2 point near the end of a frame

Table 22. Hub Port Bus Status Register

HPSC Address: 0EH
(Port-indexed) Reset State: xxx0 0000B

Hub Port Status Change Register. This register indicates a change in status for a port, including reset, over-current, suspend, enable and connect status

7							0
---	---	---	RSTSC	OVISC	PSSC	PESC	PCSC

Bit Number	Bit Mnemonic	Function
7:5	---	Reserved: Write zeros to these bits.
4	RSTSC	Reset Status Change (read-, clear-only): '1' indicates reset of port complete. '0' indicates no change. This bit is set by hardware approximately 10 msec after receipt of a port reset and enable commend.
3	POVISC	Over-Current Indicator Status Change (read-, clear-only): This bit will be set to '1' by hardware if change is detected in the over-current status, even if the condition goes away before it is detected by firmware. Always '0' when selecting the ganged over-current report mode.
2	PSSC	Port Suspend Status Change (read-, clear-only): '1' indicates resume process complete. '0' indicates no change. This bit is set by hardware upon completion of the firmware-initiated resume process.
1	PESC	Port Enable/Disable Status Change (read-, clear-only): '1' indicates port enabled/disabled status change. '0' indicates no change. This bit is set by hardware due to hardware events only. This bit indicates the port was disabled due to port error condition.
0	PCSC	Port Connect Status Change (read-, clear-only): '1' indicates connect status change. '0' indicates no change. This bit is set by hardware due to hardware connects and disconnects.

Table 23. Hub Port Status Change Register

NOTEBOOK

Address: 0FH
Reset State: 0000 0000B

Notebook Register. For firmware test purposes.

7							0
NOTEBOOK							

Bit Number	Bit Mnemonic	Function
7:0	NOTEBOOK	Notebook Register: This register can be write and read at any time. It is not reset by USB reset.

Table 24. Notebook Register

HADDR

Address: 10H
Reset State: 0000 0000B

Hub Address Register. This XFR holds the address for the USB hub. During bus enumeration, it is written with a unique value assigned by the host.

7		0
---	HA6:0	

Bit Number	Bit Mnemonic	Function
7	---	Reserved: Write zero to this bit.
6:0	HA6:0	7-bit Programmable Hub Address: This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only.

Table 25. Hub Address Register

USBHI

Address: 11H
Reset State: 0000 0000B

USB Hub Interrupt Register. Contains start of frame, USB suspend, USB resume, USB Hub Transmit and Receive Done interrupt flags. A '1' indicates that an interrupt is actively pending. All bits are cleared after a read.

7							0
---	SOF	RESUME	SUSPEND	---	---	HUBRx 0INT	HUBTx 0INT

Bit Number	Bit Mnemonic	Function
7	---	Reserved: Write zero to this bit.
6	SOF	This bit is set by hardware to indicate that the reception of an actual SOF packet or from an internally generated SOF from the frame timer.
5	RESUME	USB SIE has detected a RESUME signaling on the USB lines. This interrupt is used to terminate the power-down mode.
4	SUSPEND	USB SIE has detected a SUSPEND signaling on the USB lines. The corresponding ISR should put the whole chip into power-down mode.
3	---	Reserved.
2	---	Reserved: Write zeros to these bits.
1	HUBRx0INT	Hub Receive Done Flag for endpoint 0.
0	HUBTx0INT	Hub Transmit Done Flag for endpoint 0.

Table 26. USB Hub Interrupt Register

USBHIE

Address: 12H
Reset State: 0000 xx00B

USB Hub Interrupt Enable Register.

7							0
NAKINT_IE	SOF_IE	RESUME_IE	SUSPEND_IE	---	---	HRx0INT_IE	HTx0INT_IE

Bit Number	Bit Mnemonic	Function
7	NAKINT_IE	NAK Interrupt Enable: Set this bit to enable USB interrupt for hub and ~~keyboard~~ function even if NAK or STALL handshake is returned.
6	SOF_IE	SOF Interrupt Enable.
5	RESUME_IE	RESUME Interrupt Enable.
4	SUSPEND_IE	SUSPEND Interrupt Enable.
3	---	Reserved.
2	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
1	HRx0INT_IE	Hub Receive Done Interrupt Enable 0: Enable hub receive done interrupt for endpoint 0 (HUBRx0INT).
0	HTx0INT_IE	Hub Transmit Done Interrupt Enable 0: Enable hub transmit done interrupt for endpoint 0 (HUBTx0INT).

Table 27. USB Hub Interrupt Enable Register

For all bits, a '1' means the interrupt is enabled and will cause an interrupt to be signaled to the micro-controller. A '0' means the associated interrupt source is disabled and cannot cause an interrupt.

HSTAT

Address: 13H
Reset State: 0011 0x0xB

Hub Status and Configuration Register. This XFR contains bits for configuration, remote wakeup, status and status change indicators for over-current.

7							0
HCONFIG	HRWUPE	GANGP	GANGI	OVISC	---	OVI	---

Bit Number	Bit Mnemonic	Function
7	HCONFIG	Hub Configuration: This bit indicates whether the value of the hub configuration is zero. While it is zero, the hub will drive SE0 on all downstream ports. Set this bit when the hub receives a SetConfiguration() request with a configuration value other than zero.
6	HRWUPE	Hub Remote Wakeup Enable: Set if the suspended hub is enabled to request remote wakeup on connect/disconnect event or resume event when any bit is set in HEPSC. When '0', the suspended hub blocks resume signaling for connect / disconnect detected on downstream ports.
5	GANGP	Individual / Gang power control mode selection. Set this bit for the ganged power control mode, clear this bit for the individual power control mode. Write one to this bit.
4	GANGI	Individual / Gang over-current report mode selection. Set this bit for the ganged over-current report mode, clear this bit for the individual over-current report mode. Write one to this bit.
3	OVISC	Over-current Indicator Status Change (read-, clear-only): Set to '1' if change is detected in the over-current status, even if the condition goes away before it is detected by firmware.
2	---	Reserved: Value read from this bit is indeterminate. Write zero to this bit.
1	OVI	Over-current Indicator (read-only): Hardware sets and clears this bit via the OVI# input pin. '1' indicates an over-current condition. '0' indicates normal power operation.
0	---	Reserved: Value read from this bit is indeterminate. Write zero to this bit.

Table 28. Hub Status and Configuration Register

HEPSC

Address: 14H
Reset State: 0000 0000B

Hub Endpoint 1 Status Change Register.

7							0
---	---	---	---	HEPSC3	HEPSC2	HEPSC1	HEPSC0

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Always zeros.
3:0	HEPSC3:0	Hub Endpoint 1 Status Change (read-only): Hardware communicates status changes to the host by setting the appropriate bit: HEPSC0: hub status change HEPSC1: port 1 status change HEPSC2: port 2 status change HEPSC3: port 3 status change A '1' indicates a status change and '0' indicates no status change. When endpoint 1 is addressed via an IN token, the entire byte is sent if at least one bit is '1'. If all bits are zeros, a NAK handshake is returned.

Table 29. Hub Endpoint 1 Status Change Register

Setting any bit in port *x*'s HPSC results in the hardware setting the corresponding bit in HEPSC. Bits can be cleared indirectly in firmware by clearing the condition that caused the status change.

HPINDEX

Address: 15H
Reset State: xxxx xx00B

Hub Port Index Register. This register contains the binary value of the port whose HPSC, HPSTAT and HPCON registers are to be accessed.

7							0
---	---	---	---	---	---	HPIDX1	HPIDX0

Bit Number	Bit Mnemonic	Function
7:2	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
1:0	HPIDX1:0	Port Index Select: 01 = Port 1 (internal port) 10 = Port 2 11 = Port 3

Table 30. Hub Port Index Register

HPCON Address: 16H
(Port-indexed) Reset State: xxxx x000B

Hub Port Control Register. Firmware writes to this register to power-off, power-on, disable, reset, suspend and resume a port.

7							0
---	---	---	---	---	HPCON2	HPCON1	HPCON0

Bit Number	Bit Mnemonic	Function
7:3	---	Reserved: Write zeros to these bits.
2:0	HPCON2:0	Encoded Hub Port Control Commands: 000 = Power-off port 001 = Power-on port 010 = Disable port 011 = Reset and enable port 100 = Suspend port 101 = Resume port

Table 31. Hub Port Control Register

HPSTAT Address: 17H
(Port-indexed) Reset State: x000 0000B

Hub Port Status Register. This register indicates the current status of a port, including power, reset, suspend, low-speed device, enable, connect, over-current (valid when select individual power mode).

7							0
---	LSSTAT	PPSTAT	PRSTAT	POSTAT	PSSTAT	PESTAT	PCSTAT

Bit Number	Bit Mnemonic	Function
7	---	Reserved: Values read from these bits are indeterminate.
6	LSSTAT	Low-speed Device Attach Status (read-only): Set and cleared by hardware upon detection of the presence or absence of a low-speed device. '1' = low-speed device is attached. '0' = full-speed device is attached.
5	PPSTAT	Port Power Status (read-only): Set and cleared by hardware based on the present power status of the port, as controlled either by firmware using the HPCON register, or by an over-current condition in hardware. '1' = port is powered on. '0' = port is powered off.
4	PRSTAT	Port Reset Status (read-only): Set and cleared by hardware as a result of initiating a port reset by writing to HPCON. '1' = reset signaling is currently asserted. '0' = reset signaling is not asserted.
3	POSTAT	Port Over-Current Status (read-only): Hardware sets and clears this bit via the OVI(1/2) input pin. '1' indicates an over-current condition. '0' indicates normal power operation. Always '0' when select the ganged over-current report mode.
2	PSSTAT	Port Suspend Status (read-only): Set and cleared by hardware as controlled by firmware via HPCON. '1' = port is currently suspended. '0' = not suspended.
1	PESTAT	Port Enable/Disable Status (read-only): Set and cleared by hardware as controlled by firmware via HPCON. '1' = port is currently enabled. '0' = port is disabled.
0	PCSTAT	Port Connect Status (read-only): Set and cleared by hardware to reflect the connect state of the port. '1' = device is present on port. '0' = device is not present.

Table 32. Hub Port Status Register

RXDAT Address: 18H
(Endpoint-indexed) Reset State: xxxx xxxxB

Receive FIFO Data Register. Receive FIFO data specified by EPINDEX is stored and read from this register.

7							0
RXDAT7:0							

Bit Number	Bit Mnemonic	Function
7:0	RXDAT7:0	Receive Data Byte (read-only): To write data to the receive FIFO, the SIL writes to this register. To read data from the receive FIFO, the 8051 CPU reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively.

Table 33. Receive FIFO Data Register

RXCON Address: 19H
(Endpoint-indexed) Reset State: 0xx0 xxxxB

Receive FIFO Control Register. Controls the receive FIFO specified by EPINDEX.

7							0
RXCLR	---	---	RXFFRC	---	---	---	---

Bit Number	Bit Mnemonic	Function
7	RXCLR	Clear the Receive FIFO: Set this bit to flush the entire receive FIFO. All flags in RXFLG revert to their reset states (RXEMP is set; all other flags clear). Hardware clears this bit when the flush operation is complete.
6:5	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
4	RXFFRC	FIFO Read Complete: Set this bit to release the receive FIFO when a data set read is complete. Setting this bit clears the RXFULL bit (in the RXFLG register) corresponding to the data set that was just read. Hardware clears this bit after the RXFULL bit is cleared. All data from this data set must have been read. Note that FIFO Read Complete only works if STOVW and EDOVW are cleared.
3:0	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.

Table 34. Receive FIFO Control Register

RXFLG Address: 1AH
(Endpoint-indexed) Reset State: xxxx 1000B

Receive FIFO Flag Register. These flags indicate the status of data packets in the Receive FIFO specified by EPINDEX.

7							0
---	---	---	---	RXEMP	RXFULL	RXURF	RXOVF

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved: Values read from these bits are indeterminate. Write zeros to these bits.
3	RXEMP	Receive FIFO Empty Flag (read-only): Hardware sets this bit when the data set has been read out of the receive FIFO. Hardware clears this bit when the empty condition no longer exists. This is not a sticky bit and always tracks the current status. This flag is also set when a zero-length packet is received.
2	RXFULL	Receive FIFO Full Flag (read-only): This flag indicates the data set is present in the receive FIFO. Hardware sets this bit when the data set has been successfully received. This bit is cleared after write to RXCNT to reflect the condition of the data set. Likewise, this bit is cleared after setting of the RXFFRC bit.
1	RXURF	Receive FIFO Under-run Flag (read-, clear-only)*: Hardware sets this bit when an additional byte is read from an empty receive FIFO. This bit is cleared through firmware by writing a '0' to this bit. When the receive FIFO under-runs, the read pointer will not advance -- it remains locked in the empty position.
0	RXOVF	Receive FIFO Overrun Flag (read-, clear-only)*: This bit is set when the SIL writes an additional byte to a receive FIFO with RXFULL = 1. This is a sticky bit that must be cleared through firmware by writing a '0' to this bit, although it can be cleared by hardware if a SETUP packet is received after an RXOVF error had already occurred. When the receive FIFO overruns, the write pointer will not advance -- it remains locked in the full position.

Table 35. Receive FIFO Flag Register

* When set, all transmissions are NAKed.

RXCNT Address: 1BH
(Endpoint-indexed) Reset State: 0000 0000B

Receive FIFO Byte Count Register. This register is used to store the number of byte for the data packed received in the receive FIFO specified by EPINDEX.

7				0
---	---	RXCNT5	RXCNT4	RXCNT3:0

Bit Number	Bit Mnemonic	Function
7:6	---	Reserved: Always zeros.
5:0	RXCNT[5:0]	Byte Count (read-only): The number of bytes in data set written to the receive FIFO. When this register is written, RXFULL is not set until reception is successfully acknowledged. After the SIL writes a data set to the RXFIFO, it writes the byte count to this register. The 8051 CPU reads the byte count from this register to determine how many bytes to read from the RXFIFO.

Table 36. Receive FIFO Byte Count Register

RXSTAT Address: 1CH
(Endpoint-indexed) Reset State: 0000 0000B

Endpoint Receive Status Register. Contains the current endpoint status of the receive FIFO specified by EPINDEX.

7							0
RXSEQ	RXSETUP	STOVW	EDOVW	---	RXVOID	RXERR	RXACK

Bit Number	Bit Mnemonic	Function
7	RXSEQ	Receive Endpoint Sequence Bit (read, clear-only): This bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit will be set (or created) by hardware after reception of SETUP token. The SIE will handle all sequence bit tracking. This bit should only be used when initializing a new configuration or interface. If you don't want to change sequence bit, set this bit to '1' when you write this register.
6	RXSETUP	Receive Setup Token (read-, clear-only): This bit is set by hardware when a valid SETUP token has been received. When set, this bit causes received IN or OUT token to be NAKed until the bit is cleared to allow a control transaction. IN or OUT token is NAKed even if the endpoint is stalled (RXSTL or TXSTL) to allow a control transaction to clear a stalled endpoint. Clear this bit upon detection of a SETUP token after the firmware is ready to complete the setup stage of control transaction.
5	STOVW	Start Overwrite Flag (read-only): Set by hardware upon receipt of SETUP token for any control endpoint to indicate that the receive FIFO is being overwritten with new SETUP data. When set, the FIFO state (RXFULL and read pointer) resets and is locked for this endpoint until EDOVW is set. This prevents a prior, ongoing firmware read from corrupting the read pointer as the receive FIFO is being cleared and new data is being written into it. This bit is cleared by hardware at the end of wazzu handshake phase transmission of the setup stage. This bit is used only for control endpoint.

Bit Number	Bit Mnemonic	Function
4	EDOVW	End Overwrite Flag (read-, clear-only): This flag is set by hardware during the handshake phase of a SETUP stage. It is set after every SETUP packet is received and must be cleared prior to reading the contents of the FIFO. When set, the FIFO state (RXFULL and read pointer) remains locked for this endpoint until this bit is cleared. This prevents a prior, ongoing firmware read from corrupting the read pointer after the new data has been written into the receive FIFO. This bit is only used for control endpoint. **Note:** Make sure the EDOVW bit is cleared prior to reading the contents of the receive FIFO.
3	---	Reserved: Write zero to this bit.
2	RXVOID	Receive Void Condition (read-only): This bit is set when no valid data is received in response to a SETUP or OUT token due to one of the following conditions: 1. The receive FIFO is still locked. 2. The EPCON register's RXSTL bit is set. This bit is set and cleared by hardware. This bit is updated by hardware at the end of the transaction in response to a valid OUT token.
1	RXERR	Receive Error (read-only): Set when an error condition has occurred with the reception. Complete or partial data has been written into the receive FIFO. No handshake is returned. The error can be one of the following conditions: 1. Data failed CRC check. 2. Bit stuffing error. 3. A receive FIFO goes into overrun or underrun condition while receiving. This bit is updated by hardware at the end of a valid SETUP or OUT token transaction. The corresponding receive done bit is set when active. This bit is updated with the RXACK bit at the end of data reception and is mutually exclusive with RXACK.
0	RXACK	Receive Acknowledged (read-only): This bit is set when data is received completely into a receive FIFO and an ACK handshake is sent. This read-only bit is updated by hardware at the end of valid SETUP or OUT token transaction. The corresponding receive done bit set when active. This bit is updated with the RXERR bit at the end of data reception and is mutually exclusive with RXERR.

Table 37. Endpoint Receive Status Register

PA

Address: 1DH
Reset State: 0000 0000B

PA (corresponding P0) read/write data

7							0
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Bit Number	Bit Mnemonic	Function
7:0	PA[7:0]	PA data

Table 38. PA Register

PD

Address: 1EH
Reset State: 0000 0000B

PD (corresponding P3) read/write data

7							0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Bit Number	Bit Mnemonic	Function
7:0	PD[7:0]	PD data

Table 39. PD Register

PE

Address: 1FH
Reset State: 0000 0000B

PE (corresponding P4) read/write data

7							0
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0

Bit Number	Bit Mnemonic	Function
7:0	PE[1:0]	PE data

Table 40. PE Register

EXINTD

Address: 20H
Reset State: 0000 0000B

External Interrupt Rising/Falling Trigger direction

7							0
EXINTD7	EXINTD6	EXINTD5	EXINTD4	EXINTD3	EXINTD2	EXINTD1	EXINTD0

Bit Number	Bit Mnemonic	Function
7:0	EXINTD[7:0]	1: Rising edge trigger 0: Falling edge trigger

Table 41. External Interrupt Direction Register

EXINTEN

Address: 21H
Reset State: 0000 0000B

External Interrupt Enable/Disable direction

7							0
EXINTEN 7	EXINTEN 6	EXINTEN 5	EXINTEN 4	EXINTEN 3	EXINTEN 2	EXINTEN 1	EXINTEN 0

Bit Number	Bit Mnemonic	Function
7:0	EXINTEN[7:0]	1: Enable the corresponding external interrupt EXINT 0: Disable the corresponding external interrupt EXINT

Table 42. External Interrupt Enable Register

WDTEXT

Address: 22H
Reset State: xx00 0000B

Extension of the Watch-Dog Timer

7							0
---	---	WDTEXT 5	WDTEXT 4	WDTEXT 3	WDTEXT 2	WDTEXT 1	WDTEXT 0

Bit Number	Bit Mnemonic	Function
7:6	---	Reserved
5:0	WDTEXT[5:0]	111111:Extend the watchdog timer by 63 times 111110:Extend the watchdog timer by 62 times | 000011:Extend the watchdog timer by 3 times 000010:Extend the watchdog timer by 2 times 000001:Extend the watchdog timer by 1 times 000000: No watchdog timer extension.

Table 43. Watch-Dog Timer Extension Register

RMPEN

Address: 23H
Reset State: xxx0 0000B

Port Remote wakeup Enable Control

7							0
---	---	RMPEN4	RMPEN3	RMPEN2H	RMPEN2L	RMPEN1	RMPEN0

Bit Number	Bit Mnemonic	Function
7:6	---	Reserved
5	RMPEN4	Port E Remote-wakeup Enable 1: Enable 0: Disable
4	RMPEN3	Port D Remote-wakeup Enable 1: Enable 0: Disable
3	RMPEN2H	Port C High nibble Remote-wakeup Enable 1: Enable 0: Disable
2	RMPEN2L	Port C Low nibble Remote-wakeup Enable 1: Enable 0: Disable
1	RMPEN1	Port B Remote-wakeup Enable 1: Enable 0: Disable
0	RMPEN0	Port A Remote-wakeup Enable 1: Enable 0: Disable

Table 44. Port Remote Wakeup Enable Register

PWM0

Address: 24H
Reset State: 0000 0000B

PWM0 Duty Control

7							0
PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Bit Number	Bit Mnemonic	Function
7:0	PWM0[7:0]	Select 0/256 to 255/256 duty cycles and extended pulse. Each cycle is 1/12MHz width. 00000000: Duty cycle = 0 00000001: Duty cycle = 1/256 00000010: Duty cycle = 2/256 00000011: Duty cycle = 3/256 …. 11111110: Duty cycle = 254/256 11111111: Duty cycle = 255/256

Table 45. PWM0 Duty Control Register

PWM1

Address: 25H
Reset State: 0000 0000B

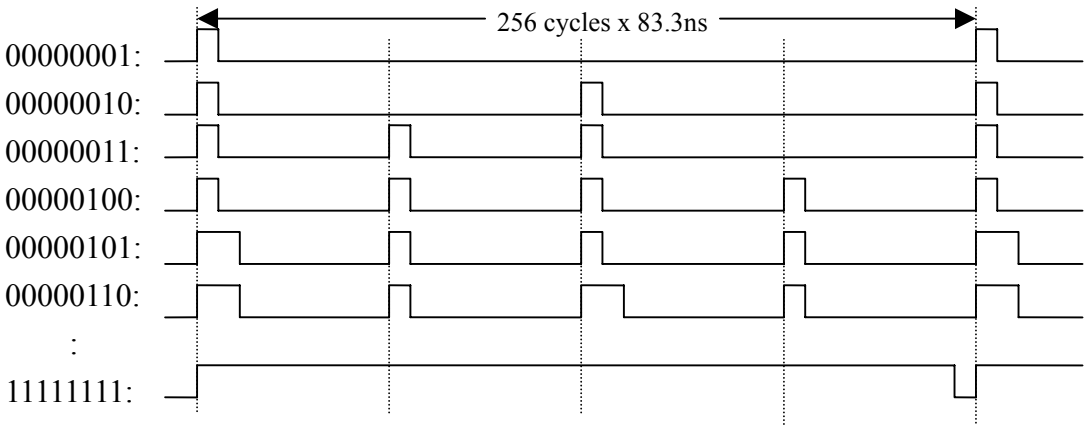
PWM2

Address: 26H
Reset State: 0000 0000B

PWM3

Address: 27H
Reset State: 0000 0000B

Function of PWM1, PWM2, PWM3 are the same as PWM0.



PWMEN

Address: 28H
Reset State: xxxx 0000B

Port Remote wakeup Enable Control

7							0
---	---	---	---	PWMEN3	PWMEN2	PWMEN1	PWMEN0

Bit Number	Bit Mnemonic	Function
7:4	---	Reserved
3	PWMEN3	PWM3 Enable 1: Enable 0: Disable
2	PWMEN2	PWM2 Enable 1: Enable 0: Disable
1	PWMEN1	PWM1 Enable 1: Enable 0: Disable
0	PWMEN0	PWM0 Enable 1: Enable 0: Disable

When any of the PWMEN bit is set, the corresponding bit from PDOE(7:4) is ignored and the corresponding pin from PD(7:4) is set to output always.

Table 46. PWM Enable Register

ADL

Address: 29H
Reset State: 0000 0000B

ADC Lower Byte Data

7							0
ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0

Bit Number	Bit Mnemonic	Function
7:0	ADB[7:0]	ADC Lower Data Byte

Table 47. ADC Lower Byte Register

ADH

Address: 2AH
Reset State: 0000 0000B

ADC Lower Byte Data

7							0
---	---	---	---	ADB11	ADB10	ADB9	ADB8

Bit Number	Bit Mnemonic	Function
7:0	ADB[11:8]	ADC Upper Data

Table 48. ADC Upper Byte Register

AD_C

Address: 2BH
Reset State: 0000 0000B

ADC Lower Byte Data

7							0
ADON	ADEN	ADSEL3	ADSEL2	ADSEL1	ADSEL0	ADVREF_C	---

Bit Number	Bit Mnemonic	Function
7	ADON	0: Disable ADC for power-down mode 1: Turn on ADC
6	ADEN	0: Disable ADC function 1: Enable ADC function
5:2	ADSEL[3:0]	0000: Select AD0 input pin 0001: Select AD1 input pin 0010: Select AD2 input pin 0011: Select AD3 input pin 0100: Select AD4 input pin 0101: Select AD5 input pin 0110: Select AD6 input pin 0111: Select AD7 input pin 1000: Select AD8 input pin 1001: Select AD9 input pin 1010: Select AD10 input pin 1011: Select AD11 input pin Others: Invalid
1	ADVREF_C	0: Select VDD to be the reference voltage of ADC circuit 1: Select ADREF (AD11) pin as the reference input voltage of ADC circuit
0	---	Reserved

Note:

1. If ADVref_C is set, then only 10 AD channels can be used.
2. The conversion time for one AD channel is 125KHz x 26 clock cycles.
3. The conversion range for AD is from 50mV to (VDD – 50mV).

Table 49. ADC Lower Byte Register

PUPCTRLB

Address: 2CH
Reset State: 1111 1111B

PB Enable/Disable of Pull-up resisters

0: Disable

1: Enable

7							0
PUAD7	PUAD6	PUAD5	PUAD4	PUAD3	PUAD2	PUAD1	PUAD0

Bit Number	Bit Mnemonic	Function
7	PUAD7	Enable/Disable corresponding pull-up resisters to pin PB7/AD7
6	PUAD6	Enable/Disable corresponding pull-up resisters to pin PB6/AD6
5	PUAD5	Enable/Disable corresponding pull-up resisters to pin PB5/AD5
4	PUAD4	Enable/Disable corresponding pull-up resisters to pin PB4/AD4
3	PUAD3	Enable/Disable corresponding pull-up resisters to pin PB3/AD3
2	PUAD2	Enable/Disable corresponding pull-up resisters to pin PB2/AD2
1	PUAD1	Enable/Disable corresponding pull-up resisters to pin PB1/AD1
0	PUAD0	Enable/Disable corresponding pull-up resisters to pin PB0/AD0

Table 50. Enable/Disable of pull-up PUPCTRLA Register

PUPCTRLD

Address: 2DH
Reset State: 1111 1111B

PD Enable/Disable of Pull-up resisters

0: Disable

1: Enable

7							0
PUPD7	PUPD6	PUPD5	PUPD4	PUAD11	PUAD10	PUAD9	PUAD8

Bit Number	Bit Mnemonic	Function
7	PUPD7	Enable/Disable corresponding pull-up resisters to pin PD7/PWM3
6	PUPD6	Enable/Disable corresponding pull-up resisters to pin PD6/PWM2
5	PUPD5	Enable/Disable corresponding pull-up resisters to pin PD5/PWM1
4	PUPD4	Enable/Disable corresponding pull-up resisters to pin PD4/PWM0
3	PUAD11	Enable/Disable corresponding pull-up resisters to pin PD3/AD11/ADVref
2	PUAD10	Enable/Disable corresponding pull-up resisters to pin PD2/AD10
1	PUAD9	Enable/Disable corresponding pull-up resisters to pin PD1/AD9
0	PUAD8	Enable/Disable corresponding pull-up resisters to pin PD0/AD8

Table 51. Enable/Disable of pull-up PUPCTRLB Register

ADCHENL

Address: 2EH
Reset State: 0000 0000B

AD channel Enable/Disable

0: Disable

1: Enable

7							0
ADCHEN 7	ADCHEN 6	ADCHEN 5	ADCHEN 4	ADCHEN 3	ADCHEN 2	ADCHEN 1	ADCHEN 0

Bit Number	Bit Mnemonic	Function
7	ADCHEN7	Enable/Disable AD channel 7
6	ADCHEN6	Enable/Disable AD channel 6
5	ADCHEN5	Enable/Disable AD channel 5
4	ADCHEN4	Enable/Disable AD channel 4
3	ADCHEN3	Enable/Disable AD channel 3
2	ADCHEN2	Enable/Disable AD channel 2
1	ADCHEN1	Enable/Disable AD channel 1
0	ADCHEN0	Enable/Disable AD channel 0

Table 52. Enable/Disable AD low byte channel Register

ADCHENH

Address: 2FH
Reset State: 0000 0000B

AD channel Enable/Disable

0: Disable

1: Enable

7 0

---	---	---	---	ADCHEN 11	ADCHEN 10	ADCHEN 9	ADCHEN 8

Bit Number	Bit Mnemonic	Function
7	---	Reserved
6	---	Reserved
5	---	Reserved
4	---	Reserved
3	ADCHEN11	Enable/Disable AD channel 11
2	ADCHEN10	Enable/Disable AD channel 10
1	ADCHEN9	Enable/Disable AD channel 9
0	ADCHEN8	Enable/Disable AD channel 8

When an ADCHENH bit is enabled, the corresponding bit from PDOE(3:0) is ignored and the corresponding pin from PD(3:0) is set the input mode always.

Table 53. Enable/Disable AD high byte channel Register

PSWEN

Address: 30H
Reset State: 0000 0000B

Power-Switch Pins Enable/Disable

0: Disable

1: Enable

7							0
---	---	---	---	---	---	---	PSWEN

Bit Number	Bit Mnemonic	Function
7	---	Reserved
6	---	Reserved
5	---	Reserved
4	---	Reserved
3	---	Reserved
2	---	Reserved
1	---	Reserved
0	OVIEN	Enable/Disable OVI and UPE Pin. 0: Disable OVI and UPE pin function, Pin is configured to GPIO 1: Enable OVI and UPE function, pin is input mode only

When PSWEN bit is set, the corresponding bit from PEOE(1:0) is ignored. As the result that PE(0) and PE(1) are set to output and input mode, respectively.

Table 54. Enable/Disable Power Switch Pins Register

PAOE Address: 31H
Reset State: 0000 0000B

PA output enable

7							0
PA7OE	PA6OE	PA5OE	PA4OE	PA3OE	PA2OE	PA1OE	PA0OE

Bit Number	Bit Mnemonic	Function
7:0	PAxOE	PA output enable 0: Corresponding GPIO bit is set to input 1: Corresponding GPIO bit is set to output

PDOE Address: 32H
Reset State: 0000 0000B

PEOE Address: 33H
Reset State: 0000 0000B

Function of PDOE and PEOE are the same as PAOE.

Table 55. PA,PD,PE output enable Register

I2CCON

Address: 34H
Reset State: 0000 0000B

Power-Switch Pins Enable/Disable

0: Disable

1: Enable

7							0
---	---	---	---	---	---	I2CINTEN	I2CINT

Bit Number	Bit Mnemonic	Function
7	---	Reserved
6	---	Reserved
5	---	Reserved
4	---	Reserved
3	---	Reserved
2	---	Reserved
1	I2CINTEN	Enable/Disable I2C Interrupt 0: Disable 1: Enable
0	I2CINT	I2C Interrupt 0: No Interrupt 1: Interrupt

Table 56. I2C Control Register

I2CSTA Address: 35H
Read Only Reset State: 0010 0010B

I2C Interface Status Register

7							0
---	---	BB	SFIRST	SSTOP	SRW	RXNAK2	I2CRDY

Bit Number	Bit Mnemonic	Function
7	---	Reserved
6	---	Reserved
5	BB	1: Bus busy 0: Bus idle. Both SDA and SCL pins keep in high level for 5 us after STOP condition
4	SFIRST	This bit is set when received START and first byte in slave mode
3	SSTOP	This bit is set when received STOP condition in slave mode
2	SRW	Received R/W bit in slave mode 1: Read command is received 0: Write command is received
1	RXNAK2	1: NACK is received 0: ACK is received
0	I2CRDY	This bit is set when a byte is received, transmitted or STOP condition is detected

Table 57. I2C Interface Status Register

I2CCON2 Address: 35H
Write Only Reset State: 0000 0010B

I2C Interface Status Register

7							0
ENI2C	MCLK1	MCLK0	MSTR	MSTOP	I2CRW	TXNAK2	SLAVE

Bit Number	Bit Mnemonic	Function
7	ENI2C	Enable/Disable SCL and SDA Pin 1: Enable SCL and SDA function 0: Disable SCL and SDA pin function, Pins are configured to GPIO
6:5	MCLK1 MCLK0	Select SCL clock is master mode 00: 400KHz 01: 100KHz 10: 50KHz 11: 200KHz
4	MSTR	Output START condition in master mode when this bit is set
3	MSTOP	Output STOP condition is master mode when this bit is set
2	I2CRW	Master mode: 0: Transmitter 1: Receiver Slave Mode 0: Receiver 1: Transmitter
1	TXNAK2	1: Output NACK 0: Output ACK. It will pull low the SDA2 pin on acknowledge bit
0	SLAVE	1: Slave Mode 0: Master Mode

Table 58. I2C Interface Control Register

I2CTX (Write Only) Address: 36H
I2CRX (Read Only) Address: 36H
Reset State: xxxx xxxx B

I2C Interface Transmit/Receive Buffer Register

7							0
MTX7	MTX6	MTX5	MTX4	MTX3	MTX2	MTX1	MTX0
MRX7	MRX6	MRX5	MRX4	MRX3	MRX2	MRX1	MRX0

Bit Number	Bit Mnemonic	Function
7:0	MTX[7:0] MRX[7:0]	Master Transmit/Receive Data

Table 59. I2C Transmit/Receive Buffer Register

I2CADR Address: 37H
Write Only Reset State: xxxx xxxx B

I2C Interface Address Register

7							0
SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	SAR1	SAR0

Bit Number	Bit Mnemonic	Function
7:0	SAR[7:0]	Slave Address

Table 60. I2C Interface Address Register

5 Target AC and DC Specification

(VCC=5V, GND=0V, TA=25°C, F_{osc}=6MHz, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Active current	I_{CC}			10	mA	
Power-down current	I_{PD}		0.3	0.5	mA	
Input high voltage (except XTAL1, RESET)	V_{IH}	0.2VCC+0.9		VCC+0.5	V	
Input high voltage (XTAL1, RESET)	V_{IH1}	0.7VCC		VCC+0.5	V	
Input low voltage (except RESET)	V_{IL}	-0.5		1.2	V	
Input low voltage (RESET)	V_{IL1}	0		2.4	V	
Output high voltage	V_{OH}	VCC-0.3			V	I_{OH}=-25μA *(Note)*
		VCC-0.7			V	I_{OH}=-65μA *(Note)*
		VCC-1.5			V	I_{OH}=-100μA *(Note)*
Output low voltage	V_{OL}			0.45	V	I_{OL}=4mA *(Note)*
Low voltage reset	V_{LVR}	3.1	3.4	3.7	V	
Input high leakage current	I_{IH}			300	nA	V_{IH}=5V
RESET pull-down resistor	R_{RST}	50		200	KΩ	
Input pull-up resistor	R_I		10		KΩ	V_{IL}=0V
I/O pin capacitor (except XTAL1, XTAL2, RESET)	C_{IO}			15	pF	

Note : Needs external 10KΩ pull-up resistor

Table 61. DC Electrical Characteristics

DC supply voltage	-0.3V to +7.0V
Input / Output voltage	GND-0.2V to VCC +0.2V
Operating ambient temperature	-0°C to +70°C
Storage temperature	-55°C to +125°C
Operating voltage (VCC)	+4.0V to 5.25V

Table 62. Absolute Maximum Rating

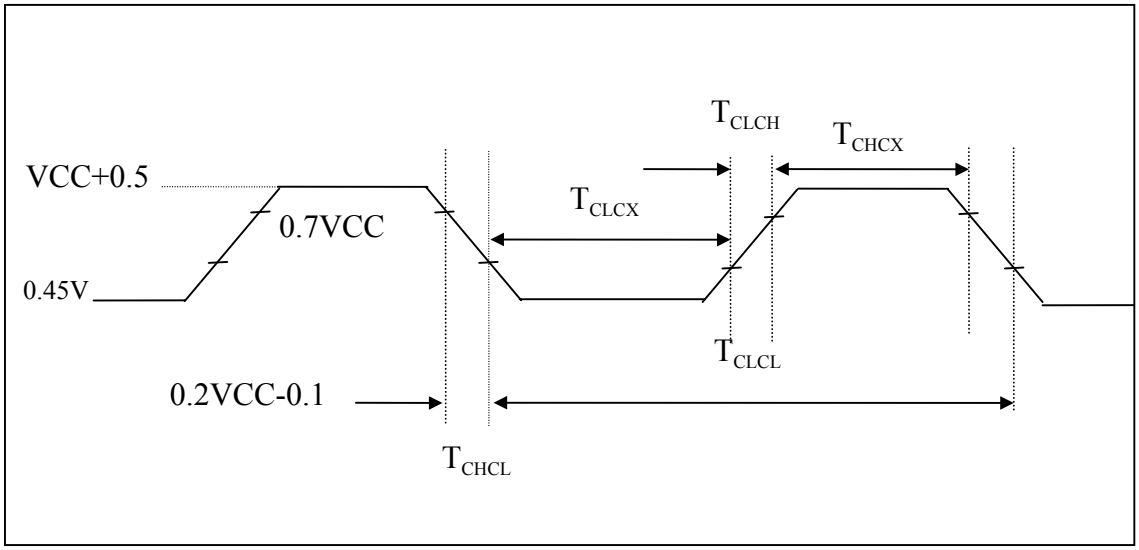


Figure 8. External Clock Drive Waveform

Symbol	Parameter	Min.	Max.	Units
$1/T_{CLCL}$	Oscillator frequency	5.94	6.06	MHz
T_{CHCX}	High time	0.35 T_{CLCL}	0.65 T_{CLCL}	nS
T_{CLCX}	Low time	0.35 T_{CLCL}	0.65 T_{CLCL}	nS
T_{CLCH}	Rise time		20	nS
T_{CHCL}	Fall time		20	nS
T_{POR}	Power on reset internal high time	30		µS

Note : 10 KΩ pull-up resistor, C=50pF

Table 63. AC Electrical Characteristics