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Command Mode Flash

Preliminary Target Specification

Product Name	Command Mode Flash Memory		
JESS Doc. No.	HF88F04.doc	JESS Product. No.	HF88F04

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1. General Description

The HF88F04 is a command mode flash device. It features parallel and serial bi-directional dual access modes. Multiple device array can be accessed with only minimal additional device select pin. Simple exclusive or checksum provides error detection during data transfer between MCU and the device. The interface logic and protocol include setting up the starting address for data transfer, writing data into Flash Memory, as well as read it back for verification, and error checking by Exclusive OR checksum. It can be used for non-volatile memory extension for all JESS's MCUs.

Chip Select pins allows array of HF88F04 devices are used simultaneously for both parallel and serial transfer mode. In the serial mode, the HF88F04 is connected in daisy chain configuration to minimize the I/O pin required to use multi-chip array, while in parallel mode, the devices share most of the control pins and data bus except the chip select pins.

2. Features

- ✓ Dual (parallel and serial) command access modes.
- ✓ Address automatically increment with each Read/Write data access.
- ✓ Page erase mode and erase verify mode.
- ✓ Exclusive or checksum error detection
- ✓ Multiple chip array is allowed with easy addressing logic
- ✓ Read access voltage range 2.2V ~ 3.6V
- ✓ Organization
  - Memory Cell Array: 512K x 8
- ✓ Package – Dice form

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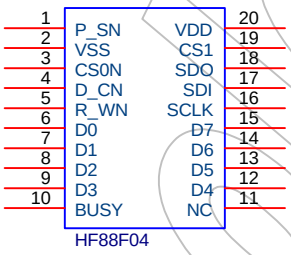
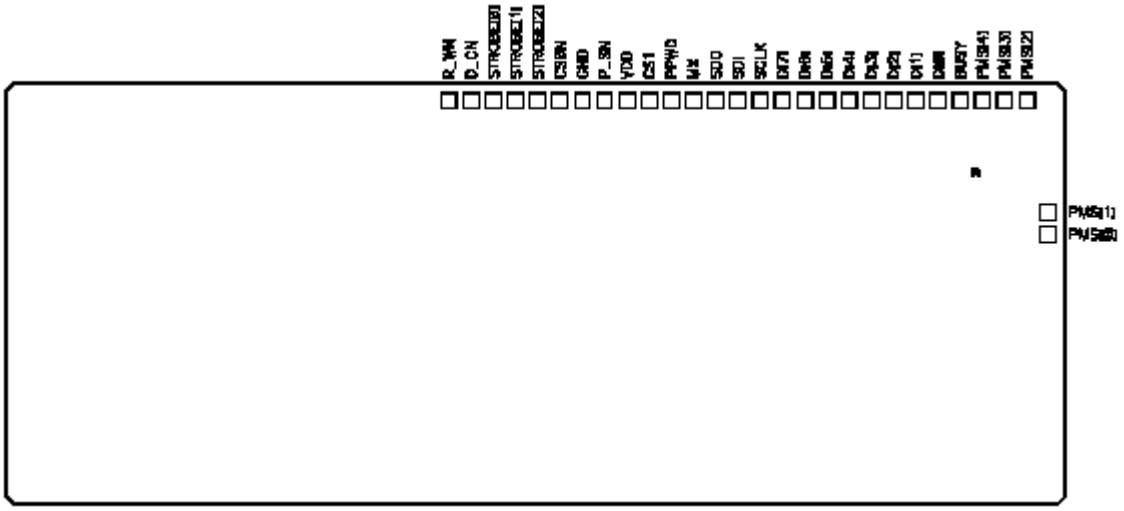
3. Pin Description



Symbol	Pin No.	I/O	Description
P_Sn		I	Input to select either parallel (when '1') or serial (when '0') interface is used for transferring data.
VSS		I	Negative power supply of the device
CS0n		I	CS0n is active low chip select input pin. The device is selected when CS1 is high and CS0n is low simultaneously. Otherwise, it is deselected.
D_Cn		I	Input to select either the FLASH memory or Registers (TPP, TPH, TPL, Mode or Checksum).
R_Wn		I	Input to select either a Read operation (when '1') or a write operation (when '0') is to be performed.
Busy		O	Busy indicator output. When high, it indicates the FLASH is occupied in internal process.
D0 ~ D7		I/O	Bi-directional data bus for parallel transfer mode.
SCLK/ Strobe		I	This pin is shared between parallel and serial modes. In serial mode, this pin is serial clock SCLK for transferring the data from/to SDI/SDO. In parallel mode, it is the strobe signal used to write the registers and FLASH as well as read the checksum and contents of FLASH memory. This pin is equipped with Schmidt type input structure to prevent the input from chattering due to slow rising clock source transition.
SDI		I	Serial Data Input for writing to either Registers or Flash Memory.
SDO		O	Serial Data Output for reading data from either Checksum Register or Flash Memory.
CS1		I	CS1 is active high chip select input. The device is selected when CS1 is high and CS0n is low simultaneously. Otherwise, it is deselected.
VDD		I	Positive power supply of the device

Command Mode Flash

4. Pad Diagram



5. Pad Coordinates

Pin Number	Pin Name	X Coordinate	Y Coordinate	Pin Number	Name	X Coordinate	Y Coordinate
1	P_SN	340.5	1022.7	16	D[1]	1950.51	1022.7
2	GND	225.5	1022.7	17	D[2]	1835.51	1022.7
3	CS0N	110.5	1022.7	18	D[3]	1720.51	1022.7
4	STROBE[2]	-4.5	1022.7	19	D[4]	1605.51	1022.7
5	STROBE[1]	-119.5	1022.7	20	D[5]	1490.51	1022.7
6	STROBE[0]	-234.5	1022.7	21	D[6]	1375.51	1022.7
7	D_CN	-349.5	1022.7	22	D[7]	1260.51	1022.7
8	R_WN	-464.5	1022.7	23	SCLK	1145.51	1022.7
9	PMS[0]	2632.97	332.41	24	SDI	1030.51	1022.7
10	PMS[1]	2632.61	448.7	25	SDO	915.51	1022.7
11	PMS[2]	2525.51	1022.7	26	MX	800.5	1022.7
12	PMS[3]	2410.51	1022.7	27	PPWD	685.5	1022.7
13	PMS[4]	2295.51	1022.7	28	CS1	570.5	1022.7
14	BUSY	2180.51	1022.7	29	VDD	455.5	1022.7
15	D[0]	2065.51	1022.7				

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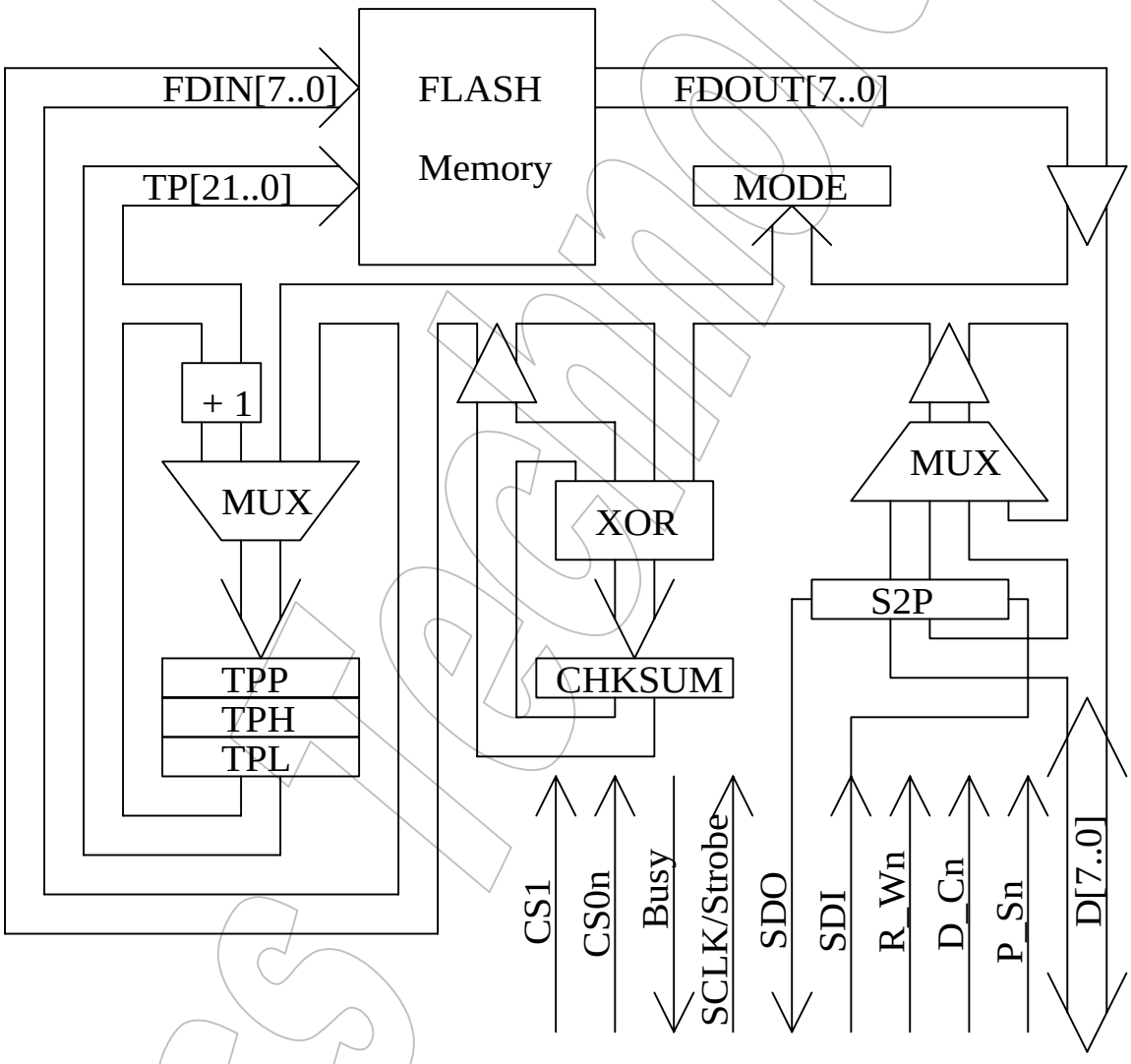
6. Function Block Diagram

Several registers are used in the interface logic. The functions of the registers are described below and their initial values are as indicated in the following table.



Register	Type	Description	Initial Value
TPL	W	Address register 0 for A7 ~ A0	"--------"
TPH	W	Address register 1 for A15 ~ A8	"--------"
TPP	W	Address register 2 for A21 ~ A16	"------"
Mode	W	Mode Control Register	"-----000"
Checksum	R	XOR checksum of data	"--------"

The Table Pointer register keeps the address of FLASH memory being written to or read from. It will automatically increment by one at the completion of each read/write access.

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The Checksum Register keeps the Exclusive OR checksum of the data bytes as they are written to/read from FLASH memory. The Checksum register cannot be written but it is cleared by any access to the TPP, TPH, TPL or Mode Register.

The Mode register is 3-bit register, which is used to control the operation modes of FLASH memory. There are five modes for the FLASH module: Power down, Read, Byte program, Page Erase and Erase verify operations. Read and Erase Verify modes need a read data operation to execute. Byte program and Page Erase modes are performed through Write Data operation. To enter the Power down mode, just fill "000" to mode register is sufficient, not extra data read or write operation is required.

	Mode2	Mode1	Mode0	Operation	Description
1.	0	0	0	None	Power down mode
2.	0	0	1	Read	Read mode
3.	0	1	0	Write	Byte program mode
4.	0	1	1	Write	Page erase mode
5.	1	0	0	Read	Erase verify mode

After Page erase operation, the user may perform blank checking by executing Erase verify mode. If the erasure is incomplete, then the user may page erase again. If the page is still not totally blank after 20 erasures, then the device may be already worn out.

7. Parallel Mode

When in parallel mode, an 8-bit data bus D[7..0] is used to transfer information between MCU and Flash memory. The advantage of parallel transfer mode is that higher speed can be achieved. To operate in parallel mode, drive the P_Sn pin with high level.

7.1. Parallel Write Command Mode

Loading of addresses and Mode register in parallel mode are by asserting the Strobe (going low and then high) in write command mode (both R_Wn and D_Cn are low), which will also clear the CHKSUM register at the same time. After the previous data transfer or when the device is just selected (CS1 is high and CS0n is low), the command data will be written to registers in the order of TPL, TPH, TPP, then Mode, TPL… So when unsure, a dummy data read or deselect and select the device again will reset the register select.

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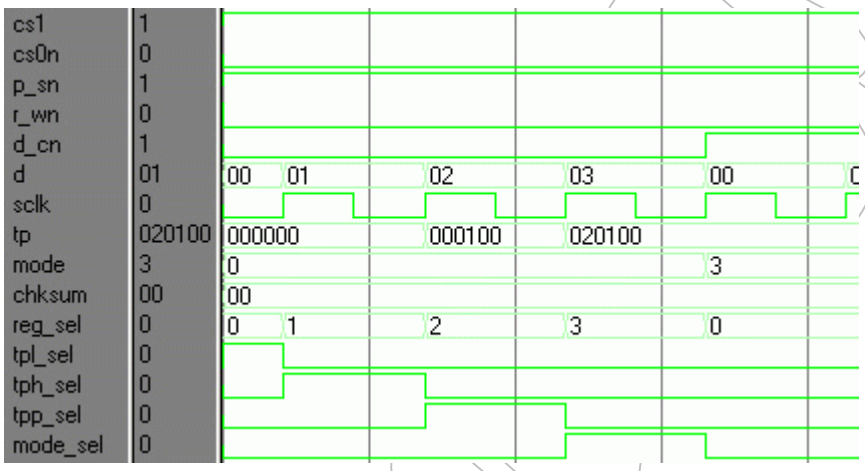
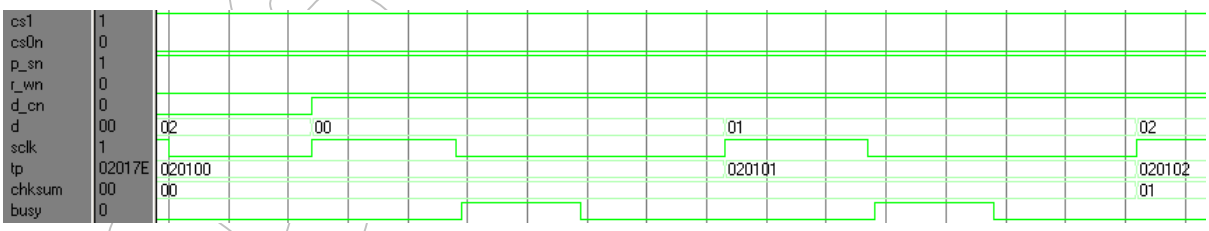


7.2. Parallel Write Data Mode

To write to Flash memory, assert Strobe in Data Write Mode (D_Cn @ Vih and R_Wn at Vil) with proper mode code in Mode register. There are two Flash Write modes – Byte Program and Page Erase mode. The control timing is similar, only the mode codes are different.

When writing data to Flash memory in any of the two modes, the Busy signal will go high after assertion (turning low) of Strobe signal. The mode select pins (D_Cn, P_Sn, R_Wn) should be held steady and Strobe must remain asserted (held at low level) until Busy signal falls. Additionally, in the Byte Programming mode, the Data on D[7..0] should be held stable before Busy signal goes low.

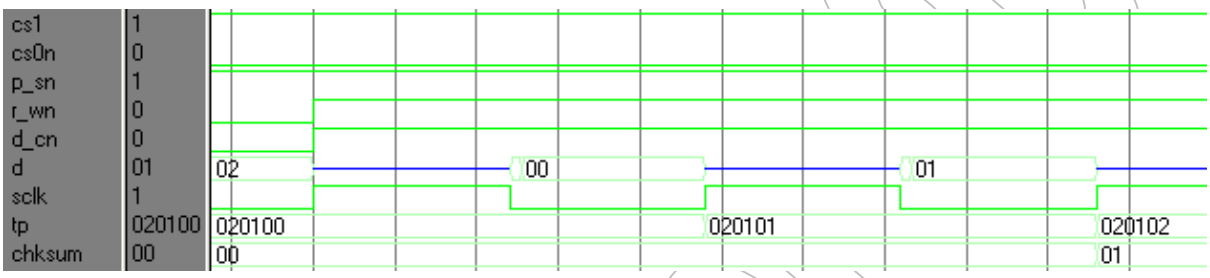
The checksum register will be updated, and the TP register will be incremented with the rising edge of Strobe signal.



7.3. Parallel Read Data Mode

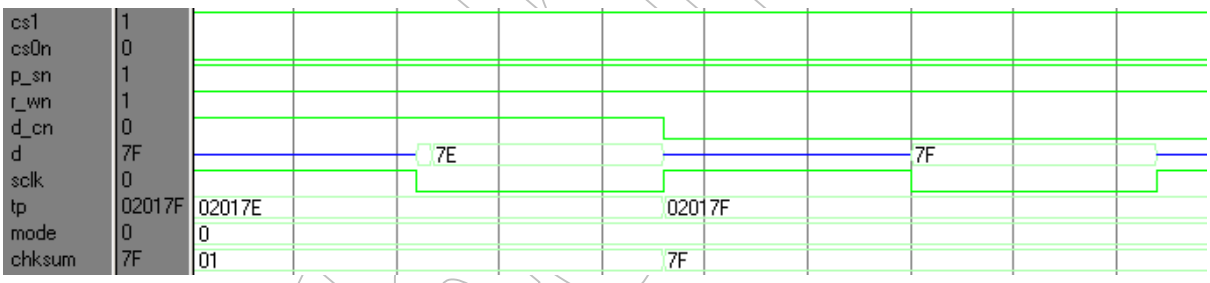
In Flash Mode 1 (Read Flash mode) and Mode 4 (Erase verify mode), the contents of Flash memory can be read by asserting the Strobe in Read Data mode (R_Wn is high and D_Cn low). The data will appear on the Data bus after proper access time. The TP will increment and Checksum will

update at the rising edge of Strobe. Register select will be reset by read data operation.



7.4. Parallel Read Checksum Mode

To read the checksum result from previous data transfer (either from Flash or to Flash), assert the Strobe signal in Read Command mode (R_Wn is high and D_Cn low).



8. Serial Mode

The serial interface is preferable to parallel interface in applications where I/O pins are limited. The interface logic circuit is basically the same as the parallel mode except that an internal shift register and bit counter are used to facilitate transferring serial data from/to external MCU.

Multiple devices array can also be used in serial mode. The chip array is connected in daisy chain manner. The MCU's serial data output pin drives the SDI pin of the first device. The SDO pin of the device then, in turn, drives the SDI pin of the next device in the chain. The SDO pin of the last device then connects back to the MCU's SDI pin to complete the loop.

There could be only one active device in the array at one time, while the other device must be deselected.

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8.1. Bi-directional Synchronous Serial Data Interface

The Serial interface is a Bi-directional Synchronous Serial Interface. Data can be written to Registers (such as TPL, TPH, TPP, Mode registers) as well as Flash memory through the serial interface. The Checksum and Flash memory contents can also be read through Serial Interface, too.

The Serial Data Input SDI pin is connected to LSB of internal shift register. With each rising edge of SCLK pin, the SDI input is shifted into the shift register. At the eighth rising edge of SCLK, the content of shift register is transferred from/to registers or Flash memory depending on the status of D_Cn and R_Wn.

If R_Wn is at “high” state at the eighth rising edge of SCLK then either the contents of Checksum Register (if D_Cn is “low”) or Flash memory been addressed (if D_Cn is “high”) will be latched into the internal shift register. Then the contents of shift register can be shifted out with the next eight rising edges of SCLK.

So one thing important should be noted here when using the Serial Data Interface to read checksum register or FLASH data is that one dummy read should be performed before the real data can be shifted out from SDO pin.

8.2. Serial Write Command Mode

The sequence of setting up addresses for data transfer and mode is similar to the parallel mode. The register pointer will be reset by accesses to FLASH data in the same way as the parallel mode does. So immediately after completion of previous data transfers or when the device is just selected, the command writes will be made to TPL, TPH, TPP then Mode registers and then wrap around. If unsure any time during the transfer, a dummy data read can be made to reset the register select.

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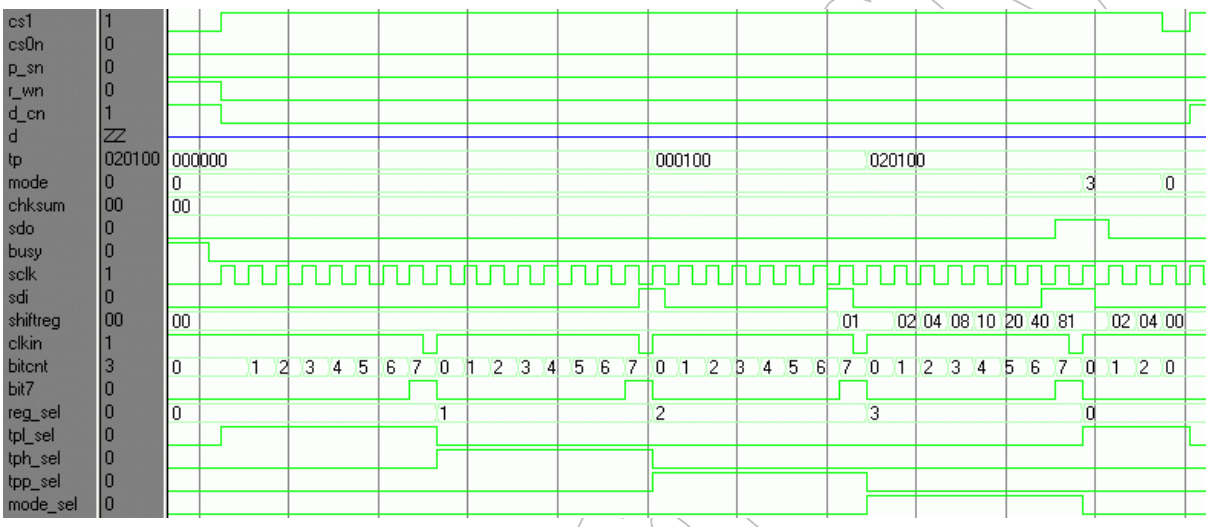
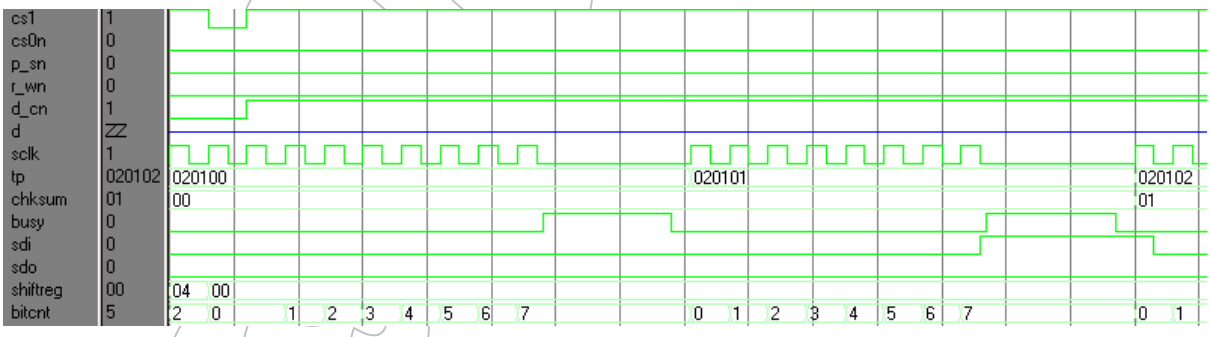


8.3. Serial Write Data Mode

With each rising edge of SCLK signal in the serial data write mode, the Data on the SDI pin will be shifted into the internal shift register. The Busy signal will go high after the assertion (falling edge) of eighth SCLK. After Busy signal falls, the content of less significant 7 Bits of the internal shift register along with SDI pin will be transfer to Flash memory at the eighth rising edge of SCLK. At this rising edge, the checksum register will be updated, and the TP register will be incremented. The status of R_Wn, D_Cn and SDI must be held steady in the mean time.

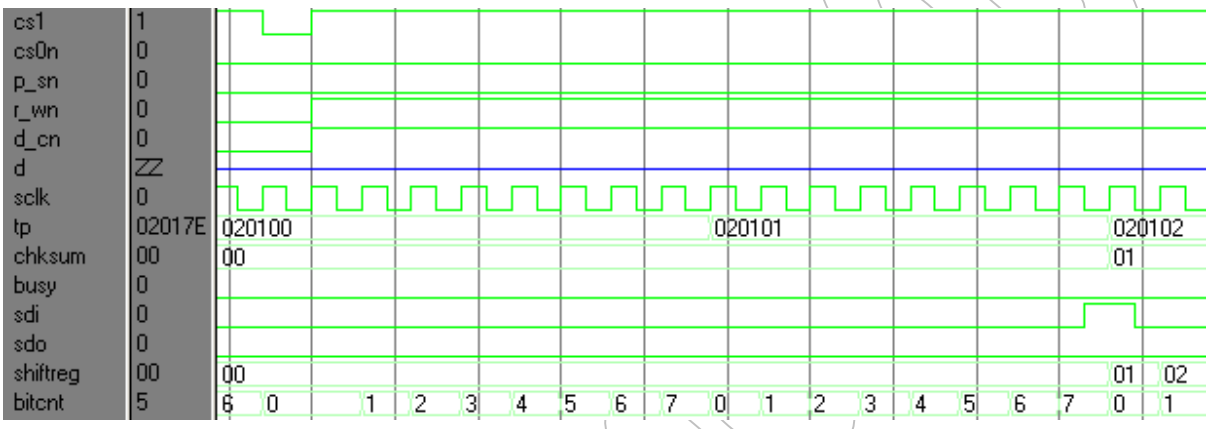


8.4. Serial Read Data Mode

In Flash mode 1 and 4, if both R_Wn, and D_Cn are at high level at the eighth rising edge of SCLK then the contents of Flash memory been addressed will be latched into the internal shift register. Then the contents of shift register can be shifted out with the next eight rising edges of SCLK.

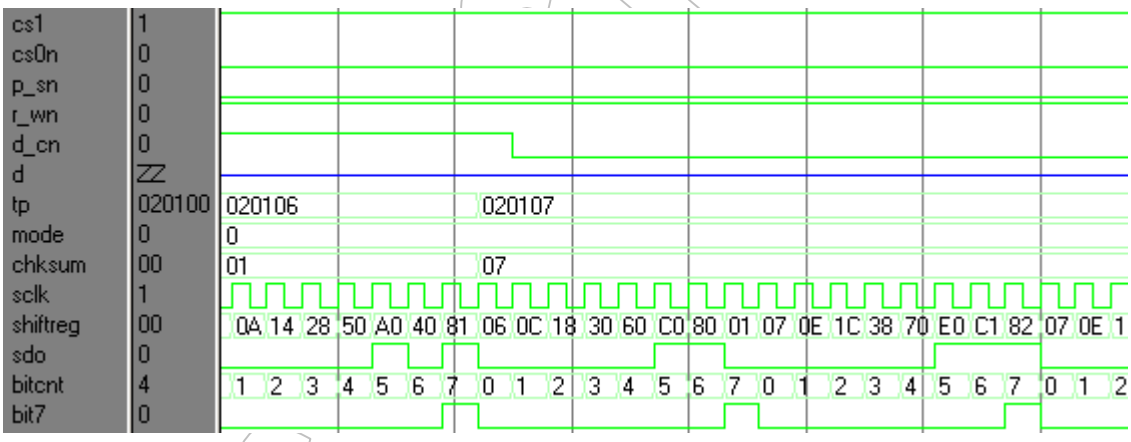
So one thing important should be noted here when using the Serial Data Interface to read FLASH data is that one dummy read should be performed before the real data can be shifted out from SDO

pin.



8.5. Serial Read Checksum Mode

Reading checksum in serial mode is similar to Read data mode except that the D_Cn is at low level instead of high.



9. Power consideration

In order to conserve power consumed by the device, the static power consumption by Flash memory Sense Amplifier need to be minimized. Since the Sense Amplifier is on whenever the device is selected and Strobe/SCLK is asserted low in Data Read Mode. Therefore the way to save power is to minimize the duty of the overall Strobe/SCLK signal to an extent that it is just long enough to satisfy the access time so that the static power consumption can be lowered.

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10. Absolute Maximum Rating

Items	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.3 to 3.6 V	
Input Voltage	V_{IN}	-0.3 to Vdd+0.3 V	
Operating Temperature	T_{OPR}	-0 to 70 °C	
Storage Temperature	T_{STR}	-55 to 125 °C	

11. AC Electrical Characteristics

READ CYCLE

Item	**Symbol**	**VCC=3.3V ± 0.3V**		**Unit**
		Min	**Max**	
Access Time	tacc		TBD	ns

12. Electrical Characteristics

(VSS = 0V, VDD = 3.3 V, TOPR = 25°C unless otherwise noted)

Parameter	Sym.	Min.	Typ.	Max	Unit	Condition
Supply Voltage	VDD	2.7	-	3.6	V	
Operating Current	IDD	-	TBD	-	mA	No load
Standby Current	IDD	-	10	-	μA	No load
Input voltage	VIH VIL	0.7 0	- -	1 0.3	VDD	VDD = 2.7V ~ 3.6V
Input current leakage	IIL	-	-	+/- 10	μA	

13. Application Circuit

The application circuit diagram shows one of the JESS's MCU uses two HF88F04 as non-volatile Read/Write memory extension. Please note that the SDO pin of the first device drive SDI pin of the second device and only one device select pin DEV1 is used to select between one of the two device. The P_Sn pins are tied to ground operate at serial mode.

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