

SELF-OSCILLATING HALF-BRIDGE DRIVER IC

Features

- Integrated 600V Half-Bridge Gate Driver
- CT, RT programmable oscillator
- 15.4V Zener Clamp on VCC
- Micropower Startup
- Non-latched shutdown on CT pin (1/6th VCC)
- Internal bootstrap FET
- Excellent Latch Immunity on All Inputs & Outputs
- +/- 50V/ns dV/dt immunity
- ESD Protection on All Pins
- 8-lead SOIC or PDIP package
- 1.1 usec (typ.) internal deadtime

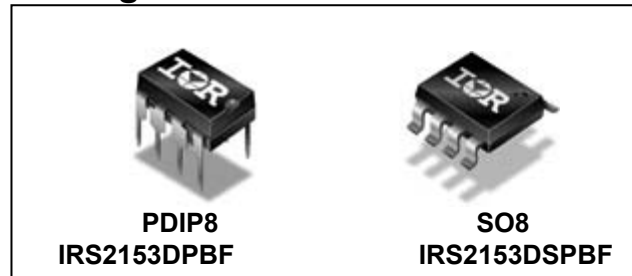
Product Summary

VOFFSET	600V Max
Duty Cycle	50%
Driver source/sink current	180/260mA typ.
Vclamp	15.4V typ.
Deadtime	1.1us typ.

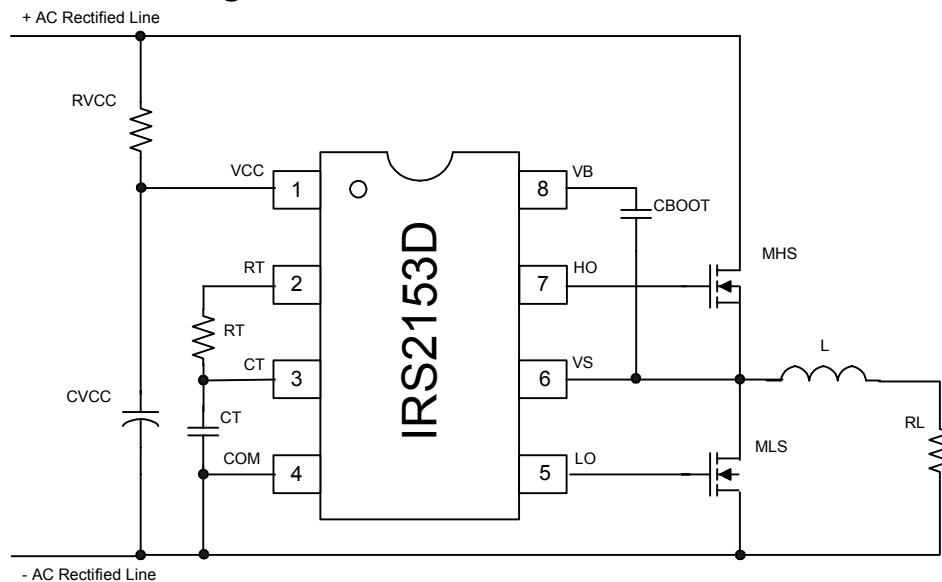
Description

The IRS2153D is based on the popular IR2153 self-oscillating half-bridge gate driver IC using a more advanced silicon platform, and incorporates a high voltage half-bridge gate driver with a front end oscillator similar to the industry standard CMOS 555 timer. HVIC and latch immune CMOS technologies enable rugged monolithic construction. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. Noise immunity is achieved with low di/dt peak of the gate drivers.

Package



Typical Connection Diagram



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter		Min.	Max.	Units
Symbol	Definition			
V _B	High Side Floating Supply Voltage	-0.3	625	V
V _S	High Side Floating Supply Offset Voltage	V _B - 25	V _B + 0.3	V
V _{HO}	High-Side Floating Output Voltage	V _S - 0.3	V _B + 0.3	V
V _{LO}	Low-Side Output Voltage	-0.3	V _{CC} + 0.3	V
I _{RT}	R _T Pin Current	-5	5	mA
V _{RT}	R _T Pin Voltage	-0.3	V _{CC} + 0.3	V
V _{CT}	C _T Pin Voltage	-0.3	V _{CC} + 0.3	V
I _{CC}	Supply Current (Note 1)	---	20	mA
IOMAX	Maximum allowable current at LO and HO due to external power transistor Miller effect.	-500	500	
dV _S /dt	Allowable Offset Voltage Slew Rate	-50	50	V/ns
P _D	Maximum Power Dissipation @ T _A ≤ +25°C, 8-Pin DIP	---	1.0	W
P _D	Maximum Power Dissipation @ T _A ≤ +25°C, 8-Pin SOIC	---	0.625	W
R _{θJA}	Thermal Resistance, Junction to Ambient, 8-Pin DIP	---	85	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, 8-Pin SOIC	---	128	°C/W
T _J	Junction Temperature	-55	150	°C
T _S	Storage Temperature	-55	150	
T _L	Lead Temperature (Soldering, 10 seconds)	---	300	

Note 1: This IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.4V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the V_{CLAMP} specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

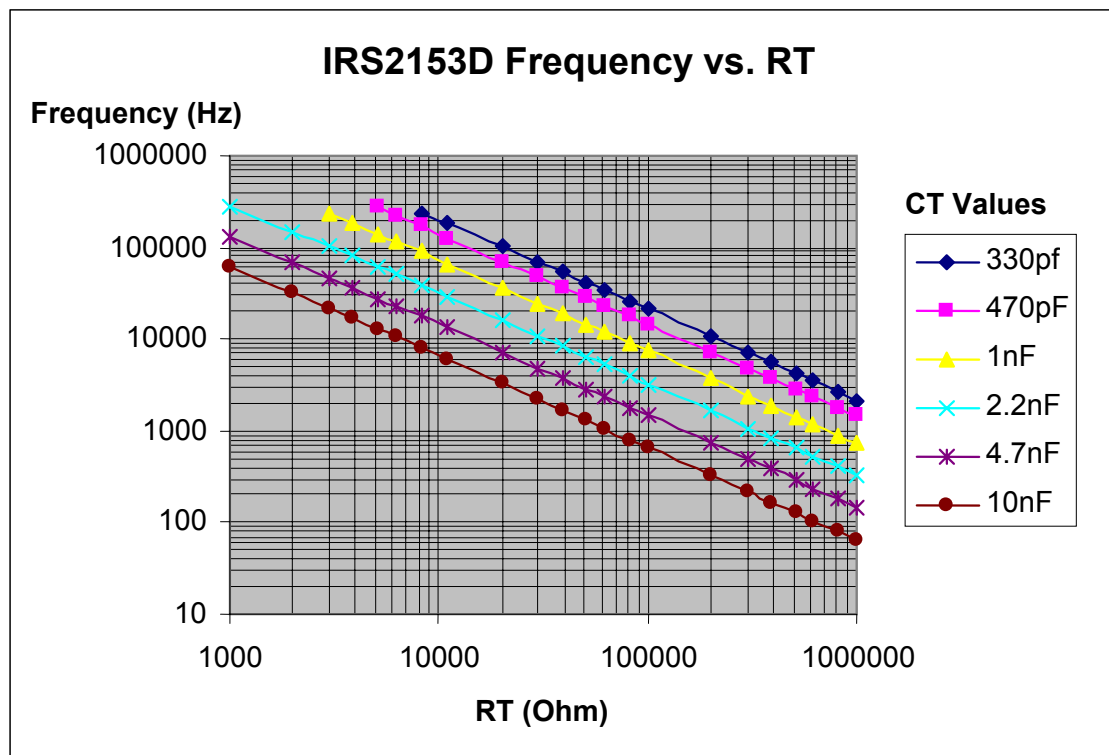
Parameter		Min.	Max.	Units
Symbol	Definition			
V_{BS}	High Side Floating Supply Voltage	$V_{CC} - 0.7$	V_{CLAMP}	V
V_S	Steady State High Side Floating Supply Offset Voltage	-3.0 (Note 2)	600	V
V_{CC}	Supply Voltage	$V_{CCUV+} + 0.1V$	$V_{CC CLAMP}$	V
I_{CC}	Supply Current	(Note 3)	5	mA
T_J	Junction Temperature	-40	125	°C

Note 2: Care should be taken to avoid output switching conditions where the V_S node flies inductively below ground by more than 5V.

Note 3: Enough current should be supplied to the V_{CC} pin of the IC to keep the internal 15.6V zener diode clamping the voltage at this pin.

Recommended Component Values

Parameter		Min.	Max.	Units
Symbol	Component			
R_T	Timing Resistor Value	1	---	k Ω
C_T	C_T Pin Capacitor Value	330	---	pF



Electrical Characteristics

VBIAS (V_{CC}, V_{BS}) = 14V, C_T = 1 nF, V_S=0V and T_A = 25°C unless otherwise specified. The output voltage and current (V_O and I_O) parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

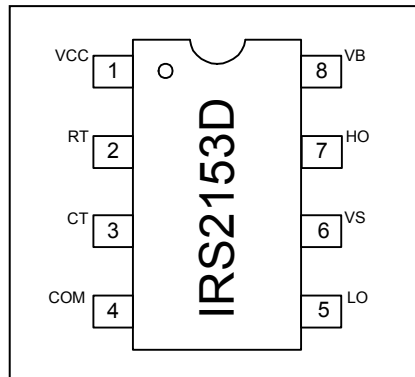
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Low Voltage Supply Characteristics						
V _{CCUV+}	Rising V _{CC} Undervoltage Lockout Threshold	10.2	10.8	11.5	V	
V _{CCUV-}	Falling V _{CC} Undervoltage Lockout Threshold	8.3	8.8	9.4		
V _{CCUVHYS}	V _{CC} Undervoltage Lockout Hysteresis	1.6	2.0	2.4		
I _{CCUV}	Micropower Startup V _{CC} Supply Current	---	130	170	μA	V _{CC} ≤ V _{CCUV-}
I _{CC}	Quiescent V _{CC} Supply Current	---	800	1000	μA	
I _{CC}	V _{CC} Supply Current	---	1.8	---	mA	R _T = 36.9kΩ
V _{CCCLAMP}	V _{CC} Zener Clamp Voltage	14.4	15.4	16.8	V	I _{CC} = 5mA
Floating Supply Characteristics						
I _{QBS}	Quiescent V _{BS} Supply Current	---	60	80	μA	
V _{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold	8.0	9.0	9.5	V	
V _{BSUV-}	V _{BS} Supply Undervoltage negative Going Threshold	7.0	8.0	9.0		
I _{LK}	Offset Supply Leakage Current	---	---	50	μA	V _B = V _S = 600V
Oscillator I/O Characteristics						
f _{OSC}	Oscillator Frequency	18.4	19.0	19.6	kHz	R _T = 36.5kΩ
		88	93	100		R _T = 7.15kΩ
d	R _T Pin Duty Cycle	---	50	---	%	f _o < 100kHz
I _{CT}	C _T Pin Current	---	0.02	1.0	μA	
I _{CTUV}	UV-Mode C _T Pin Pulldown Current	0.20	0.30	0.6	mA	V _{CC} = 7V
V _{CT+}	Upper C _T Ramp Voltage Threshold	---	9.32	---	V	
V _{CT-}	Lower C _T Ramp Voltage Threshold	---	4.66	---		
V _{CTSD}	C _T Voltage Shutdown Threshold	2.2	2.3	2.4		
V _{RT+}	High-Level R _T Output Voltage, V _{CC} - V _{RT}	---	10	50	mV	I _{RT} = -100μA
		---	100	300	mV	I _{RT} = -1mA
V _{RT-}	Low-Level R _T Output Voltage	---	10	50	mV	I _{RT} = 100μA
		---	100	300	mV	I _{RT} = 1mA
V _{RTUV}	UV-Mode R _T Output Voltage	---	0	100	mV	V _{CC} ≤ V _{CCUV-}
V _{RTSD}	SD-Mode R _T Output Voltage, V _{CC} - V _{RT}	---	10	50	mV	I _{RT} = -100μA, V _{CT} = 0V
		---	100	300	mV	I _{RT} = -1mA, V _{CT} = 0V

Electrical Characteristics

VBIAS (VCC, VBS) = 14V, CT = 1 nF, VS=0V and TA = 25°C unless otherwise specified. The output voltage and current (VO and IO) parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

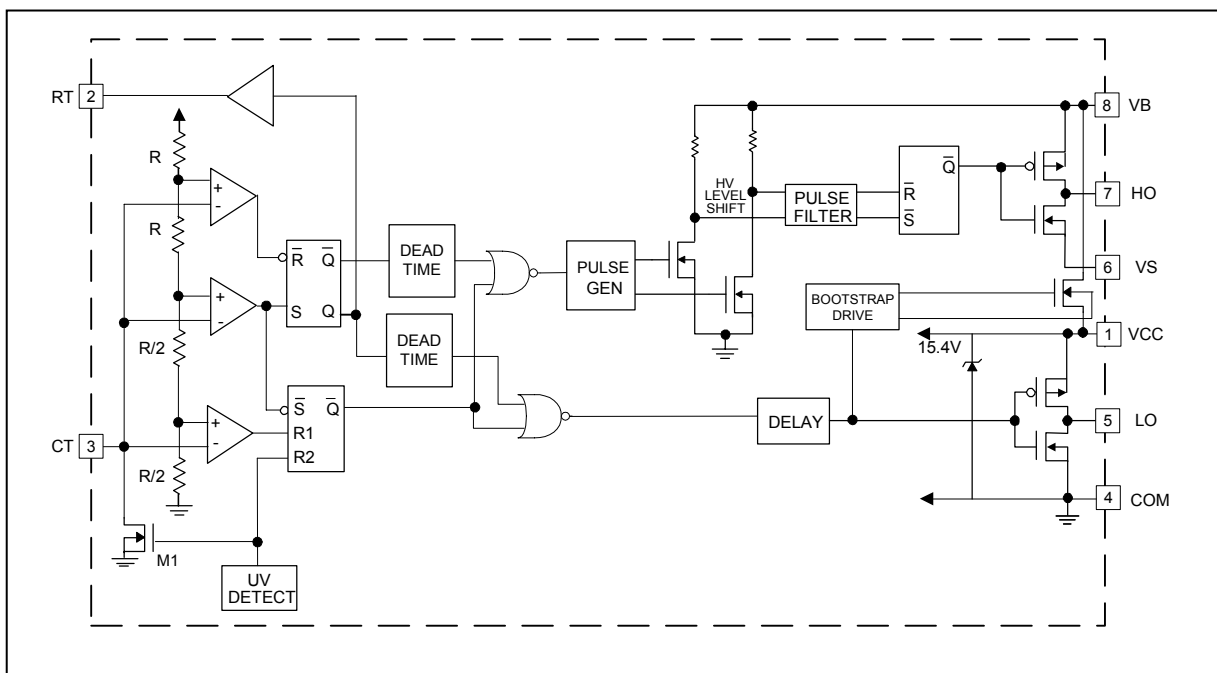
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Gate Driver Output Characteristics						
V _{OH}	High-Level Output Voltage	---	VCC	---		I _O = 0A
V _{OL}	Low-Level Output Voltage	---	COM	---		I _O = 0A
V _{OL_UV}	UV-Mode Output Voltage	---	COM	---		I _O = 0A, V _{CC} ≤ V _{CCUV}
t _r	Output Rise Time	---	120	220	nsec	
t _f	Output Fall Time	---	50	80		
t _{sd}	Shutdown Propagation Delay	---	350	---		
t _d	Output Deadtime (HO or LO)	0.65	1.1	1.75	μsec	
IO+	Output source current	---	180	---	mA	
IO-	Output sink current	---	260	---		
Bootstrap FET Characteristics						
VB_ON	VB when the bootstrap FET is on	---	13.7	---	V	
IB_CAP	VB source current when FET is on	40	55	---	mA	CBS=0.1uF
IB_10V	VB source current when FET is on	10	12	---		VB=10V

Lead Definitions



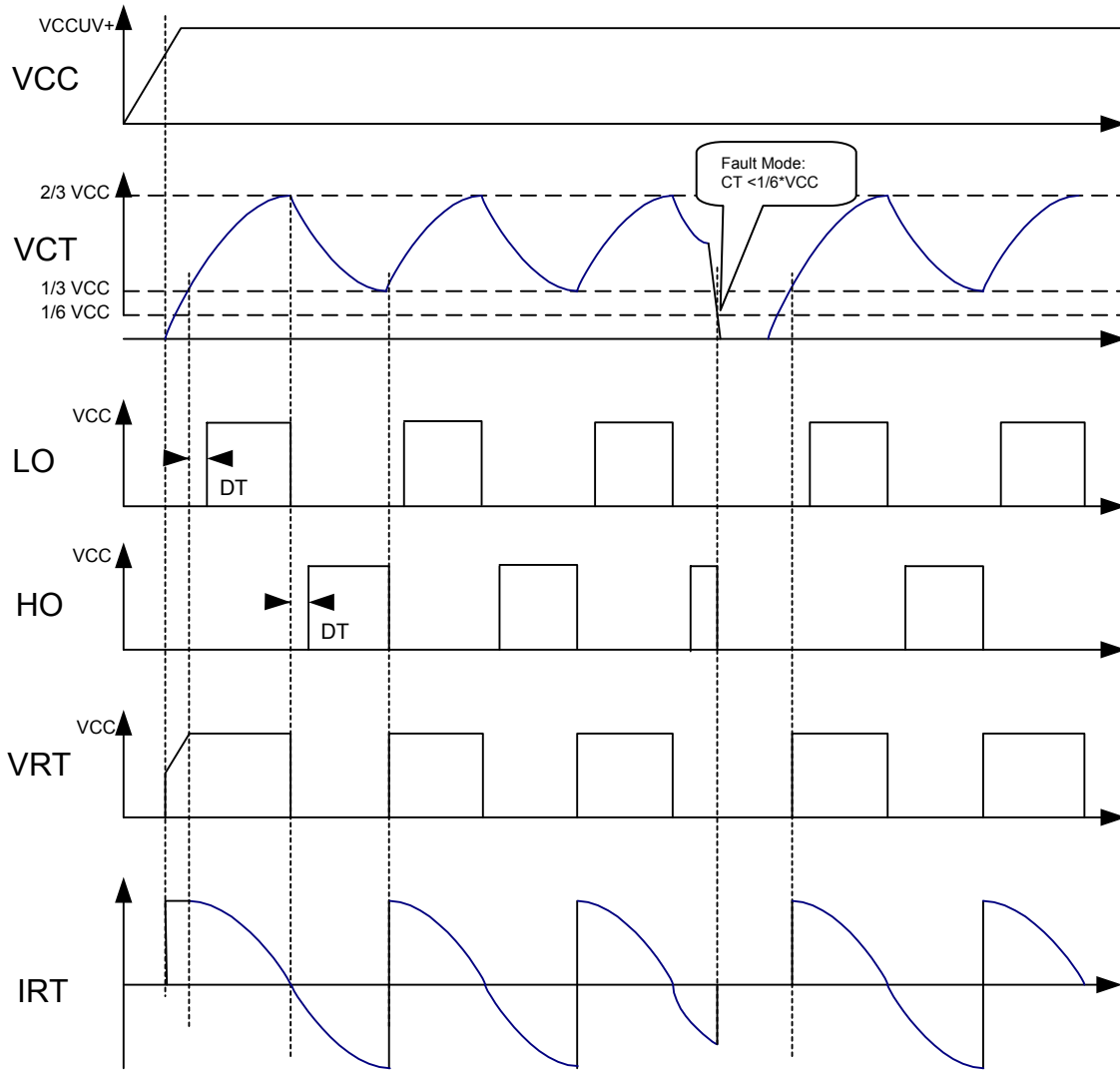
Lead	
Symbol	Description
V _{CC}	Logic and internal gate drive supply voltage
R _T	Oscillator timing resistor input
C _T	Oscillator timing capacitor input
COM	IC power and signal ground
LO	Low-side gate driver output
V _S	High voltage floating supply return
HO	High-side gate driver output
V _B	High side gate driver floating supply

Functional Block Diagram

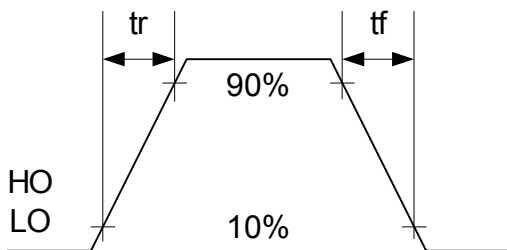


Timing Diagram

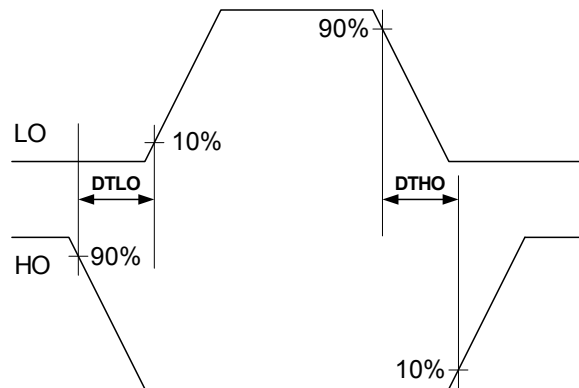
Operating Mode



Switching Time Waveform



Deadtime Waverform



Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lockout mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. The IRS2153D under voltage lock-out is designed to maintain an ultra low supply current of less than 155uA, and to guarantee the IC is fully functional before the high and low side output drivers are activated. During under voltage lock-out mode, the high and low-side driver outputs HO and LO are both low.

Supply voltage

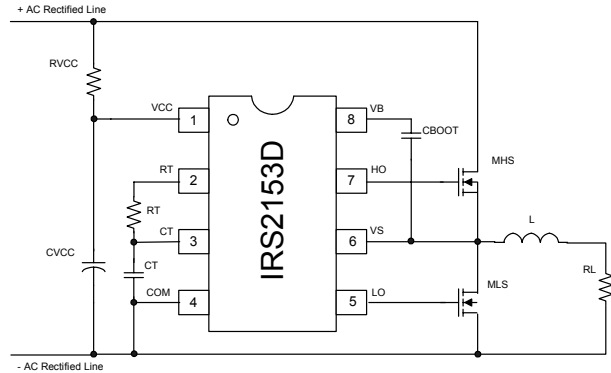


Fig. 1 Typical Connection Diagram

Fig. 1 shows an example of supply voltage. The start-up capacitor (C_{VCC}) is charged by current through supply resistor (R_{VCC}) minus the start-up current drawn by the IC. This resistor is chosen to provide sufficient current to supply the IRS2153D from the DC bus. C_{VCC} should be large enough to hold the voltage at Vcc above the UVLO threshold for one half cycle of the line voltage as it will only be charged at the peak, typically 0.1uF. It will be necessary for R_{VCC} to dissipate around 1W.

The use of a two diode charge pump made of DC1, DC2 and CVS (Fig. 2) from the half bridge (VS) is also possible however the above approach is simplest and the dissipation in R_{VCC} should not be unacceptably high.

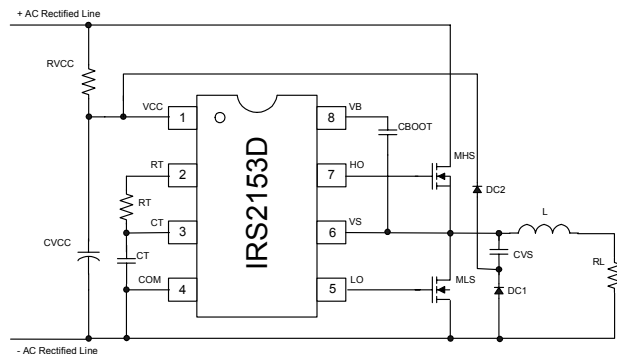


Fig. 2 Charge pump circuit

The supply resistor (R_{VCC}) must be selected such that enough supply current is available over all operating conditions.

Once the capacitor voltage on VCC reaches the start-up threshold V_{CCUV+} , the IC turns on and HO and LO begin to oscillate.

Bootstrap MOSFET

The internal bootstrap FET and supply capacitor (C_{BOOT}) comprise the supply voltage for the high side driver circuitry. The internal bootstrap FET only turns on when LO is high. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin.

Normal operating mode

Once the V_{CCUV+} threshold is passed, the MOSFET M1 opens, RT increases to approximately VCC ($V_{CC}-V_{RT+}$) and the external CT capacitor starts charging. Once the CT voltage reaches V_{CT-} (about 1/3 of VCC), established by an internal resistor ladder, LO turns on with a delay equivalent to the deadtime t_d . Once the CT voltage reaches V_{CT+} (approximately 2/3 of VCC), LO goes low, RT goes down to approximately ground (V_{RT-}), the CT capacitor discharges and the deadtime circuit is activated. At the end of the deadtime, HO goes high. Once the CT voltage reaches V_{CT-} , HO goes low, RT goes high again, the deadtime is activated. At the end of the deadtime, LO goes high and the cycle starts over again.

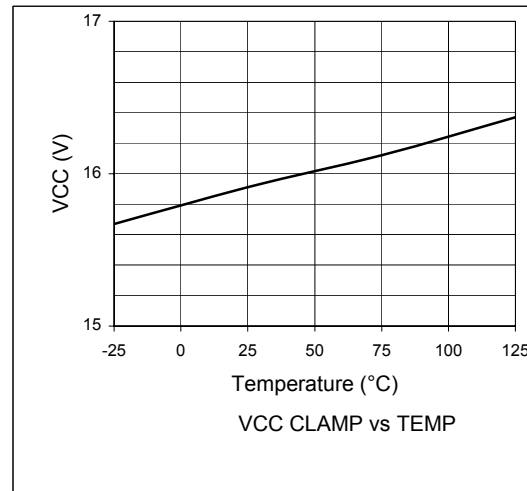
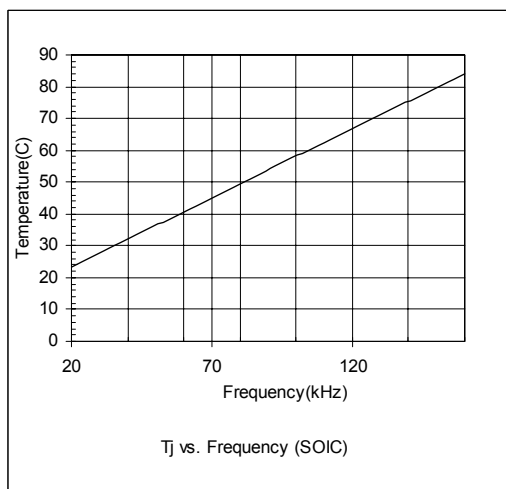
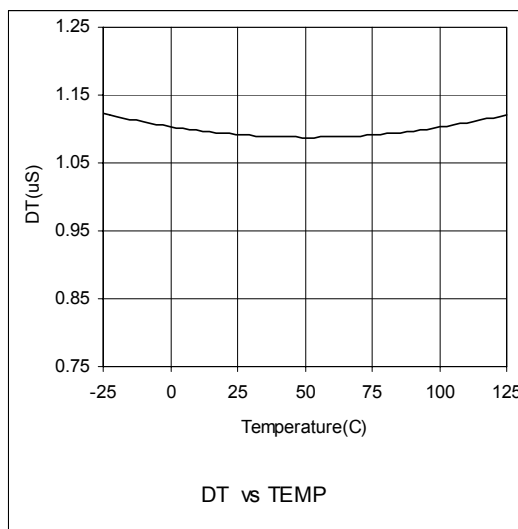
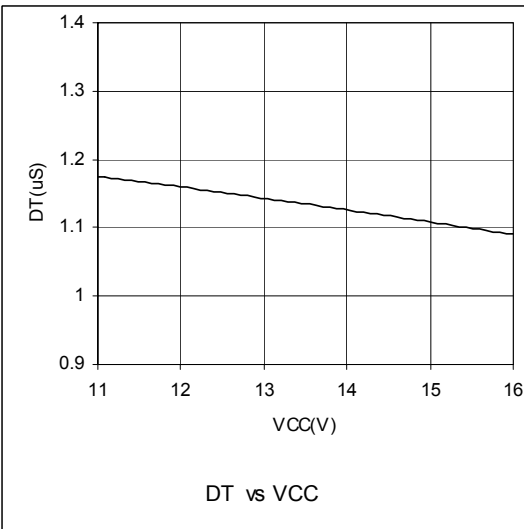
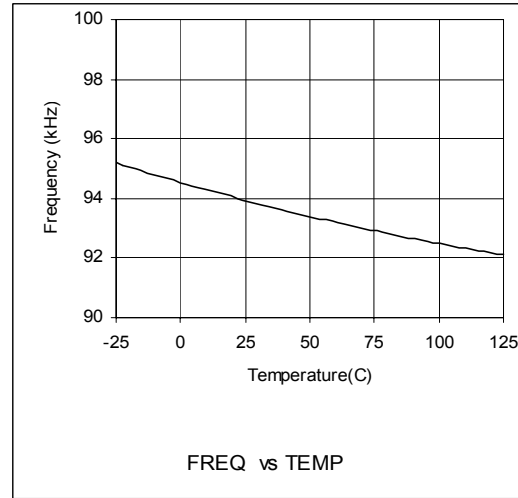
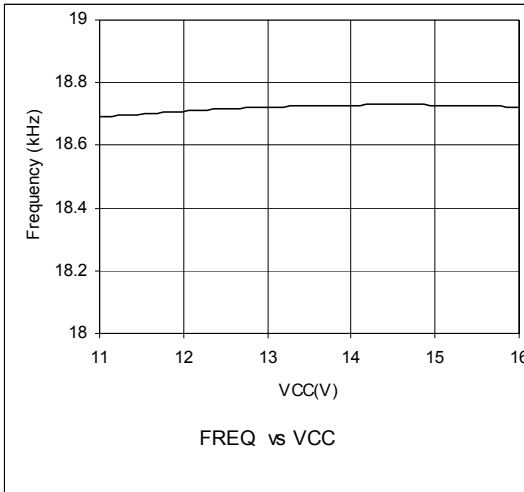
The following equation provides the oscillator frequency:

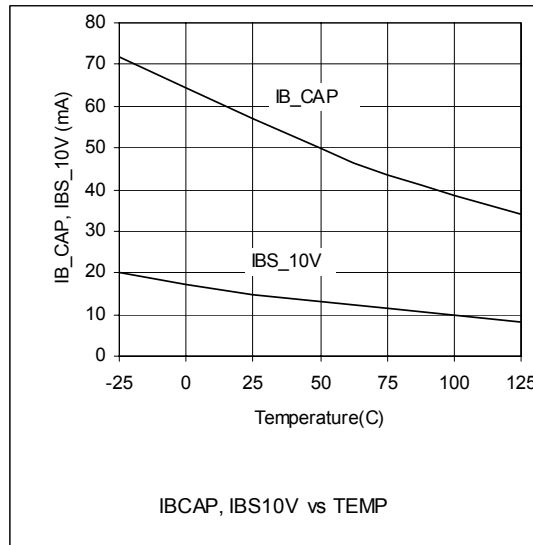
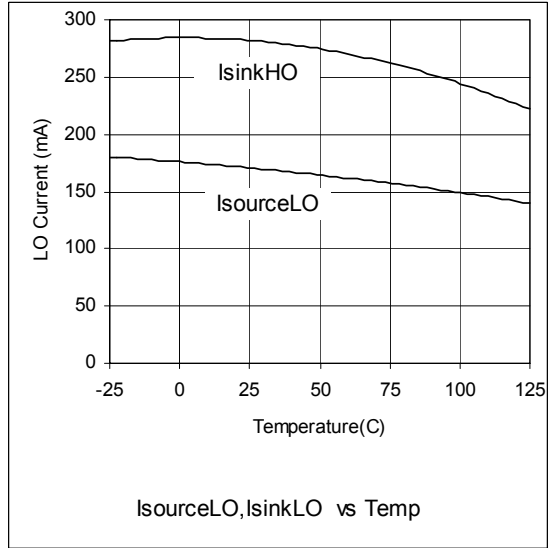
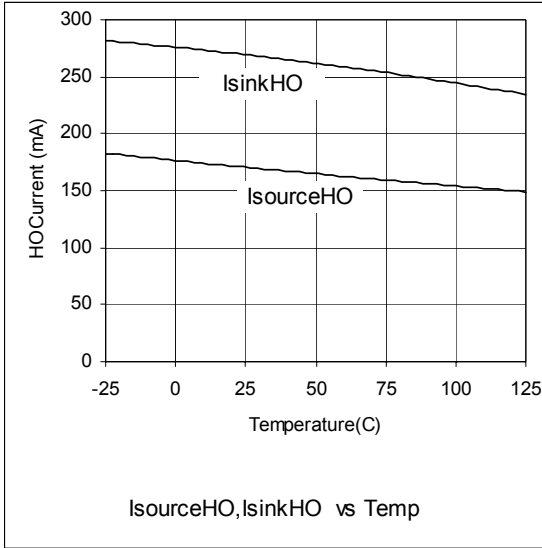
$$f \sim \frac{1}{1.453 \times RT \times CT}$$

This equation can vary slightly from actual measurements due to internal comparator over- and under-shoot delays. For a more accurate determination of the output frequency, the frequency characteristic curves should be used (RT vs. Frequency, Page 3).

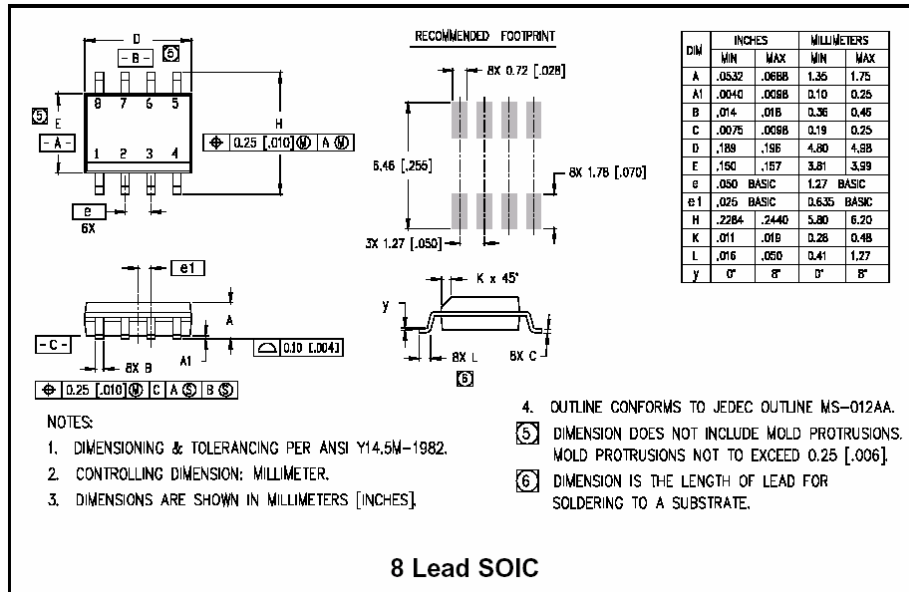
Shut-down

If CT is pulled down below V_{CTSD} (approximately 1/6 of VCC) by an external circuit, CT doesn't charge up and oscillation stops. LO is held low and the bootstrap FET is off. Oscillation will resume once CT is able to charge up again to V_{CT-} .

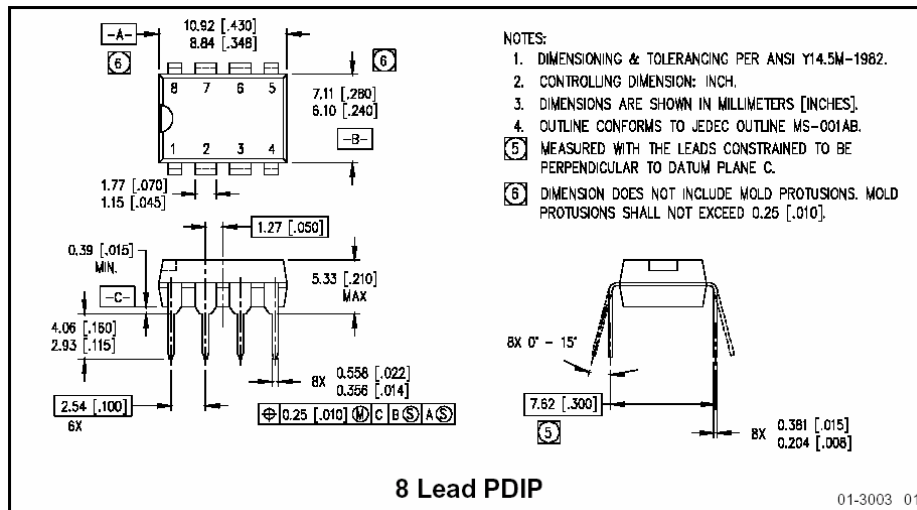




IRS2153DSPbF

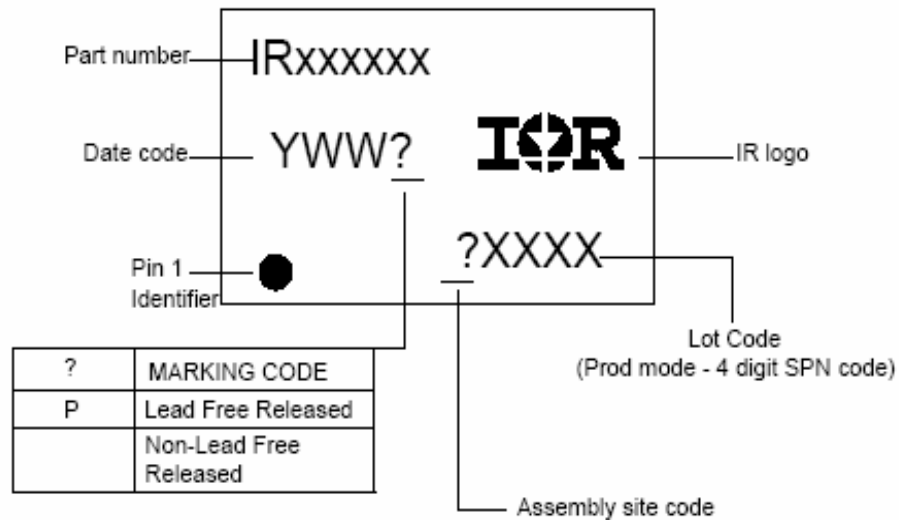


IRS2153DPbF



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LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Leadfree Part

8-Lead PDIP IRS2153D order IRS2153DPbF

8-Lead SOIC IRS2153DS order IRS2153DSPbF

WORLD HEADQUARTERS:
 233 Kansas St., El Segundo, California 90245, Tel: (310) 726 8000

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