HARRIS SEMICONDUCTOR

RFD7N10LE, RFD7N10LESM RFP7N10LE

7A, 100V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs (MegaFETs)

February 1994

Features

- **7A, 100V**
- **$r_{DS(ON)}$ = 0.300Ω**
- **2KV ESD Protected**
- ***Temperature Compensating* PSPICE Model**
- **Can be Driven Directly from CMOS, NMOS, TTL Circuits**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**
- **+175°C Operating Temperature**

Description

The RFD7N10LE, RFD7N10LESM and RFP7N10LE N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

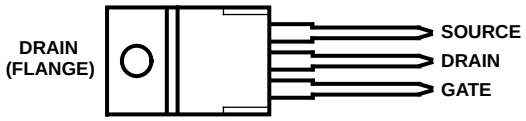
The RFD7N10LE is supplied in the JEDEC TO-251AA plastic package, the RFD7N10LESM is supplied in the JEDEC TO-252AA plastic package and the RFP7N10LE is supplied in the JEDEC TO-220AB plastic package. Due to space limitations the RFD7N10LE and RFD7N10LESM are branded 7N10LE; the RFP7N10LE is branded FP7N10LE.

When ordering use the entire part number; e.g. RFD7N10LESM.

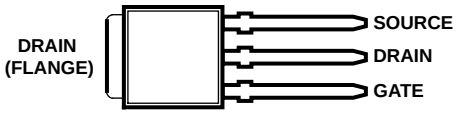
Formerly developmental type TA49046.

Packaging

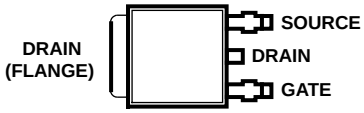
JEDEC TO-220AB
TOP VIEW



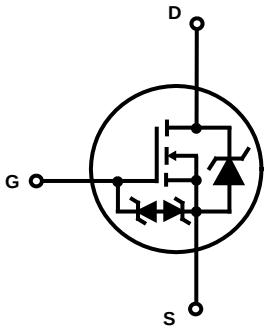
JEDEC TO-251AA
TOP VIEW



JEDEC TO-252AA
TOP VIEW



Symbol



Absolute Maximum Ratings (T_C = +25°C)

		RFD7N10LE, RFD7N10LESM, RFP7N10LE	UNITS
Drain Source Voltage	V_{DSS}	100	V
Drain Gate Voltage	V_{DGR}	100	V
Gate Source Voltage	V_{GS}	+10, -8	V
Drain Current			
RMS Continuous	I_D	7	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
(T_C = +25°C)	P_D	47	W
Derate above +25°C	P_T	0.318	W/°C
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	KV
Operating and Storage Temperature	T_{STG},T_J	-55 to +175	°C

File Number **3598**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 0.25mA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = +10, -8V		-	-	10	µµA
On Resistance	$r_{DS(ON)}$	I_D = 7A, V_{GS} = 5V		-	-	0.300	W
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 7A R_L = 7.1Ω, V_{GS} = 5V R_{GS} = 2.5Ω		-	-	110	ns
Turn-On Delay Time	$t_{D(ON)}$			-	10	-	ns
Rise Time	t_R			-	65	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	23	-	ns
Fall Time	t_F			-	18	-	ns
Turn-Off Time	t_{OFF}			-	-	60	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 10V	V_{DD} = 80V I_D = 7A, R_L = 11.4Ω	-	125	150	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0 to 5V		-	67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 1V		-	3.7	4.5	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D = 7A, V_{DS} = 15V		-	-	4.0	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz		-	360	-	pF
Output Capacitance	C_{OSS}			-	70	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	20	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.15	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251 and TO-252 Package		-	-	100	°C/W
		TO-220 Package				80	

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 7A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 7A, dI_{SD}/dt = 100A/µs	-	-	130	ns

Typical Performance Curves

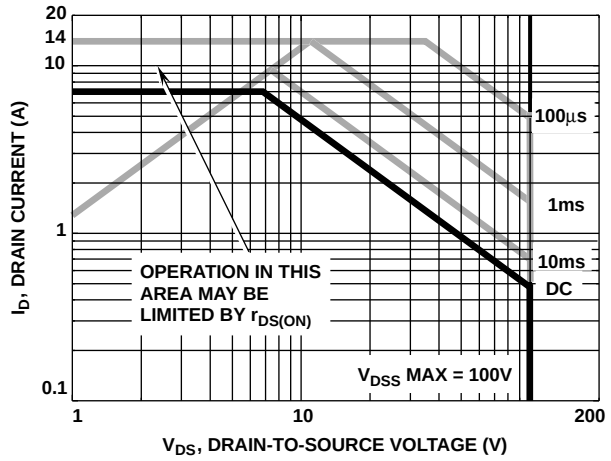


FIGURE 1. SAFE OPERATING AREA CURVE

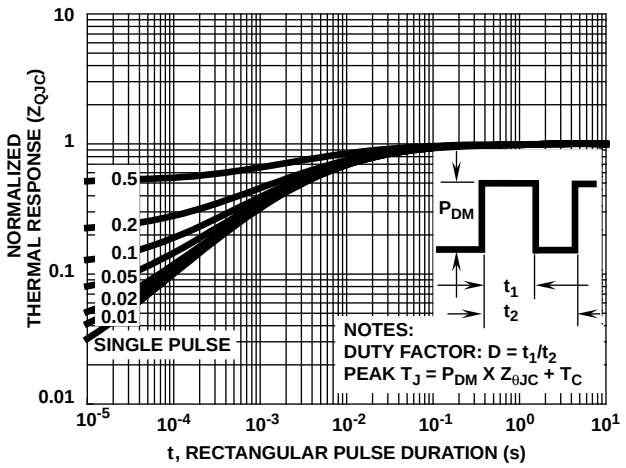


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

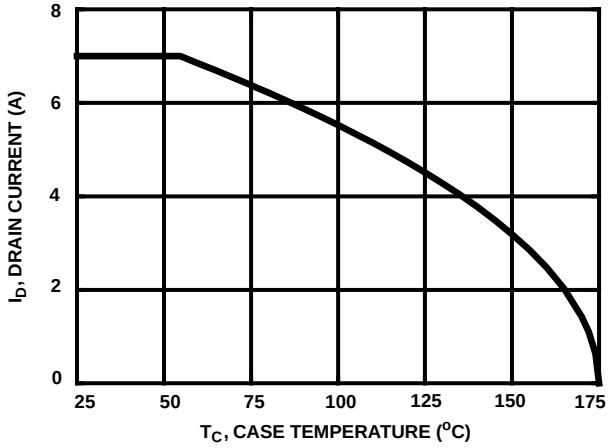


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

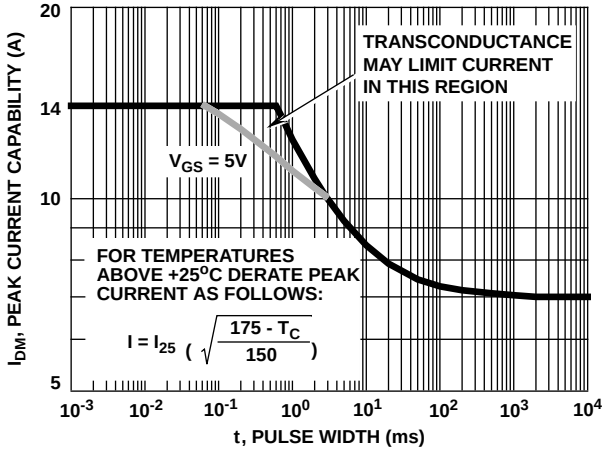


FIGURE 4. PEAK CURRENT CAPABILITY

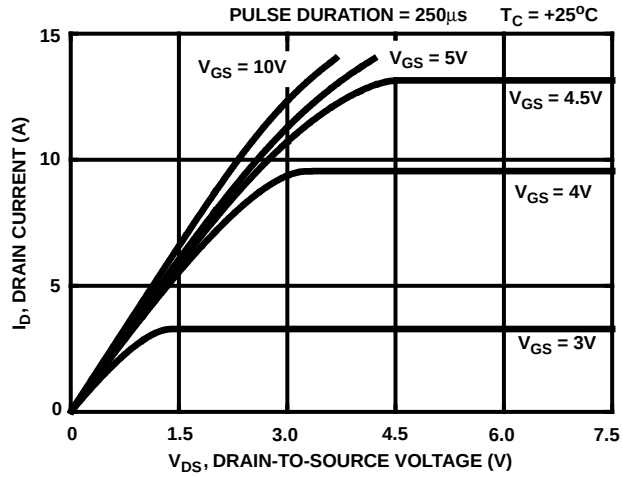


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

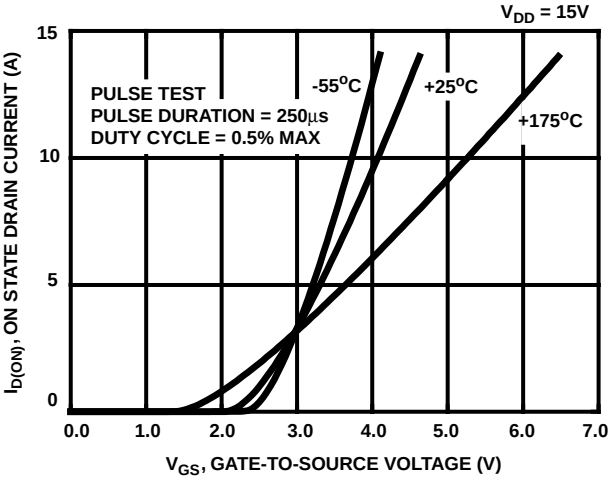


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

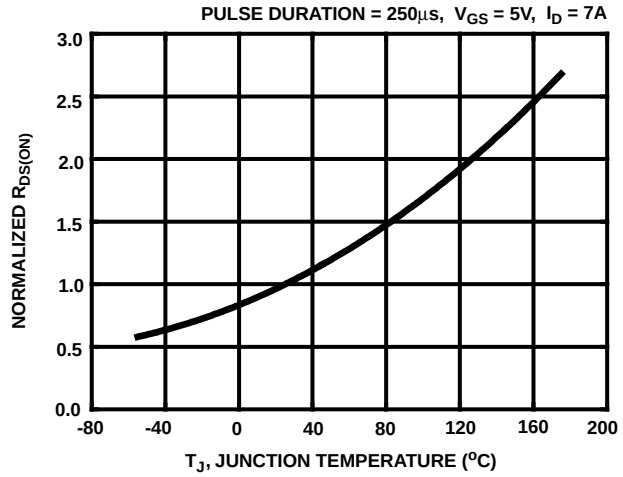


FIGURE 7. NORMALIZED $R_{DS(ON)}$ vs JUNCTION TEMPERATURE

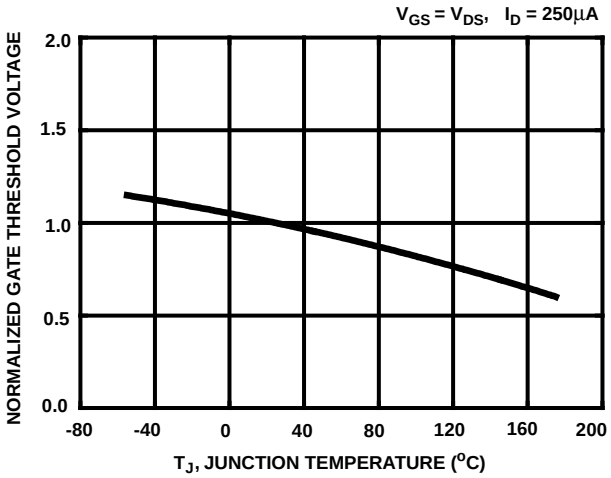


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

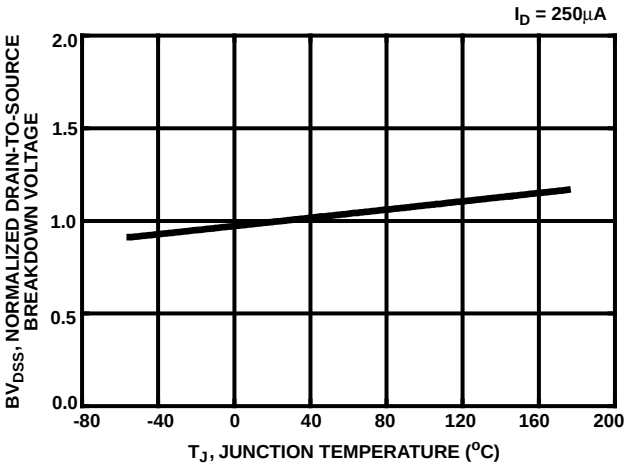


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

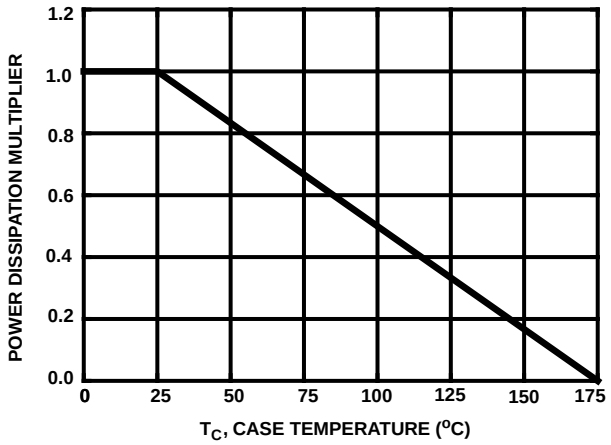


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

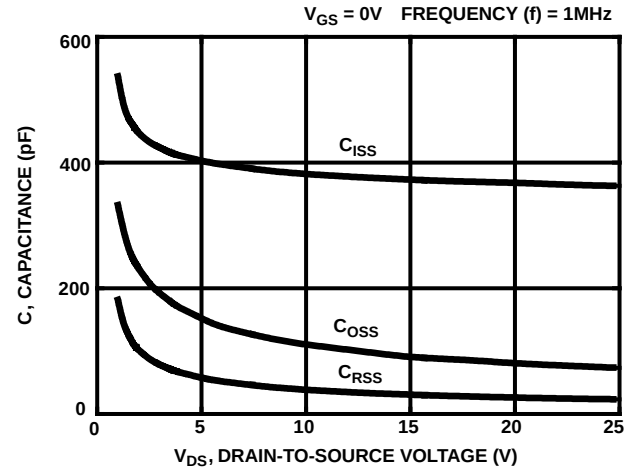


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN -TO-SOURCE VOLTAGE

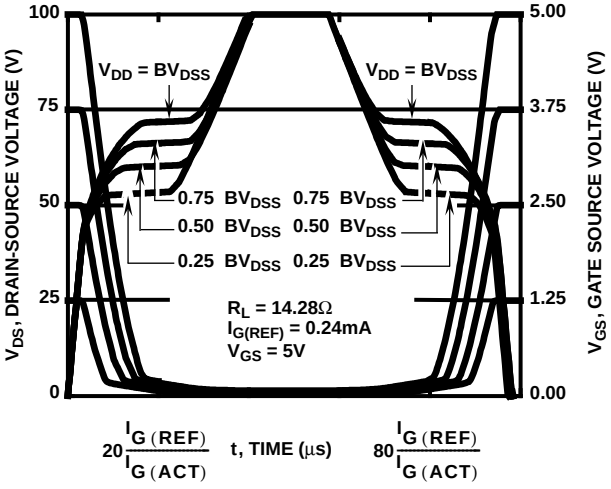


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

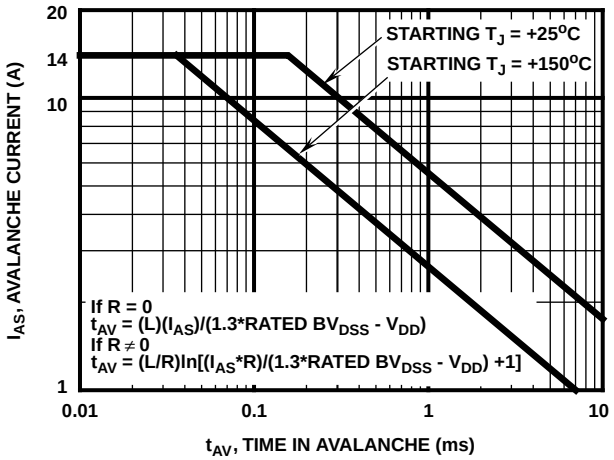


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits

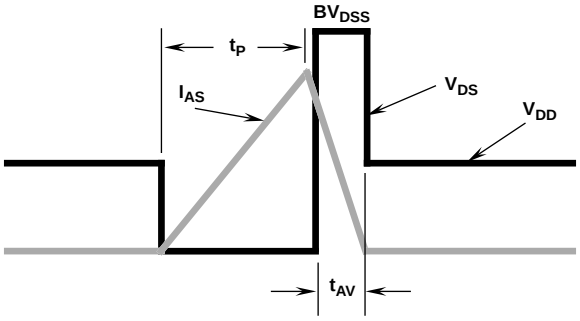


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

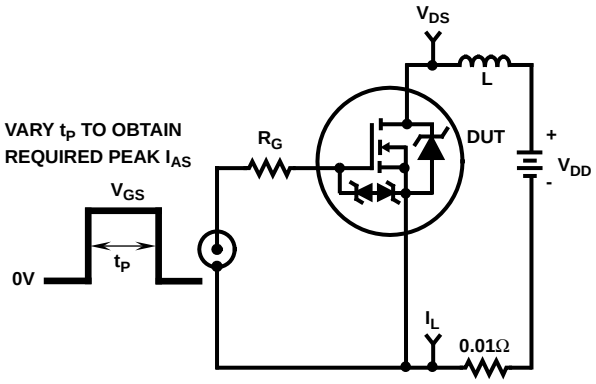


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

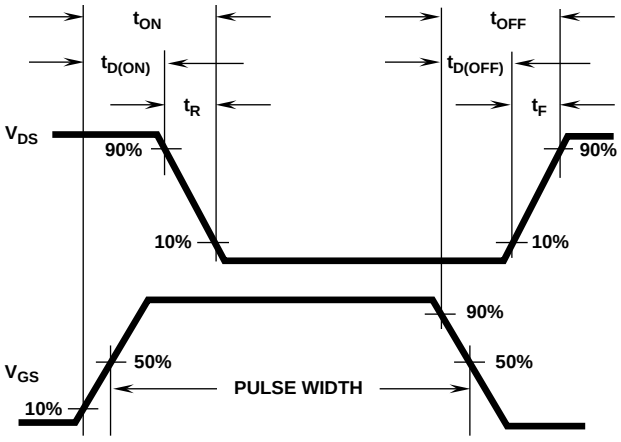


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

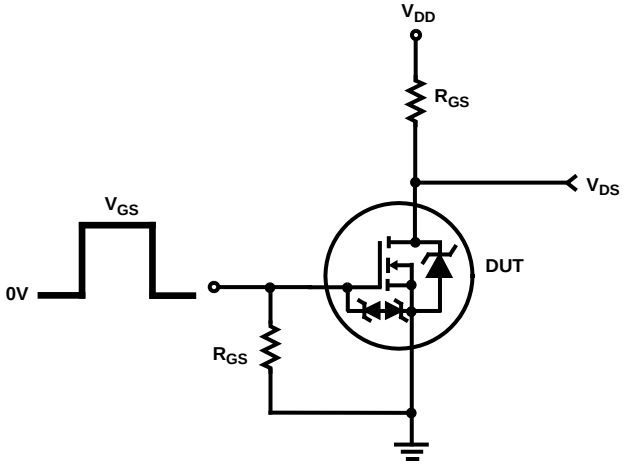


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

PSpice Model Listing

Temperature Compensated PSPICE for the RFD7N10LE, RFD7N10LESM, RFP7N10LE

```
SUBCKT RFD7N10LE 2 1 3;       rev 6/2/93

CA 12 8 1.102e-9
CB 15 14 1.157e-9
CIN 6 8 0.370e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 115.8
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.58e-9
LSOURCE 3 7 3.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 136.9e-3
RGATE 9 20 7.61
RIN 6 8 1e9
RSCL1 5 51 RSLVCMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 84.4e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.444

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/(15.5),7.25))}

.MODEL DBDMOD D (IS=5.07e-14  RS=1.37e-2  TRS1=1.72e-3  TRS2=-1.59e-6  CJO=2.57e-10  TT=3.84e-8)
.MODEL DBKMOD D (RS=2.32e-1  TRS1=6.50e-4  TRS2=1.72e-6)
.MODEL DESD1MOD D (BV=13.0 TBV1=2.2e-4 TBV2=0 RS=49 TRS1=0 TRS2=0)
.MODEL DESD2MOD D (BV=11.7 TBV1=-5.5e-4 TBV2=-8.5e-7 RS=0 TRS1=0 TRS2=0)
.MODEL DPLCAPMOD D (CJO=0.184e-9  IS=1e-30  N=10)
.MODEL MOSMOD NMOS (VTO=2.045  KP=14.07  IS=1e-30  N=10  TOX=1  L=1u  W=1u)
.MODEL RBKMOD RES (TC1=1.13e-3  TC2=4.74e-8)
.MODEL RDSMOD RES (TC1=7.45e-3  TC2=2.68e-5)
.MODEL RSLVCMOD RES (TC1=1.75e-3 TC2=0)
.MODEL RVTOMOD RES (TC1=-2.73e-3  TC2=-5.46e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-4.35  VOFF=-1.75)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.75  VOFF=-4.35)
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-1.75  VOFF=3.50)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=3.50  VOFF=-1.75)

.ENDS
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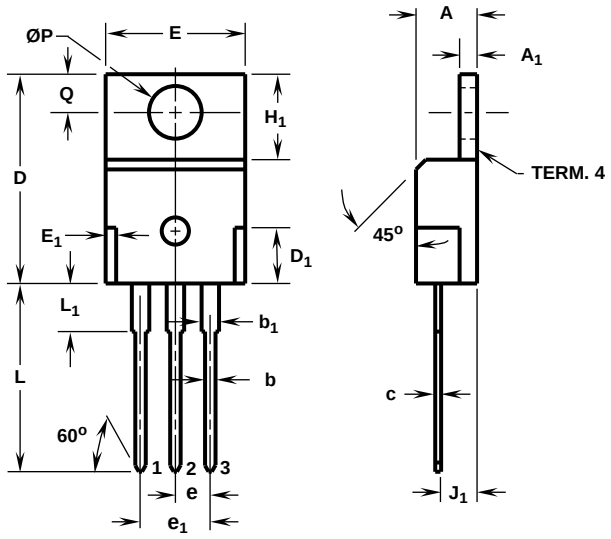
NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records 1991.

Packaging



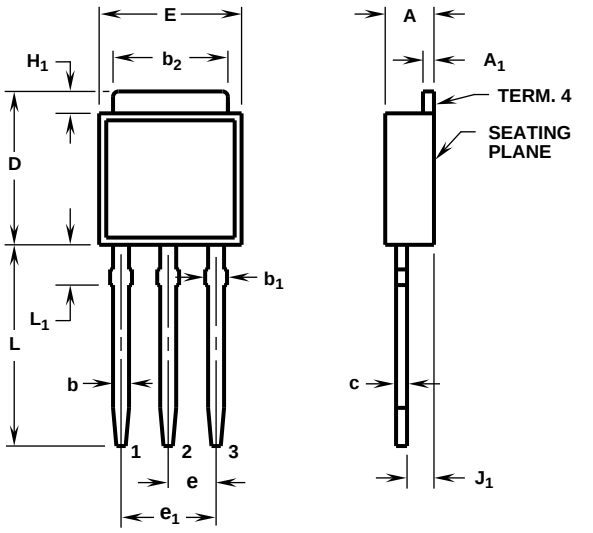
TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.



TO-251AA

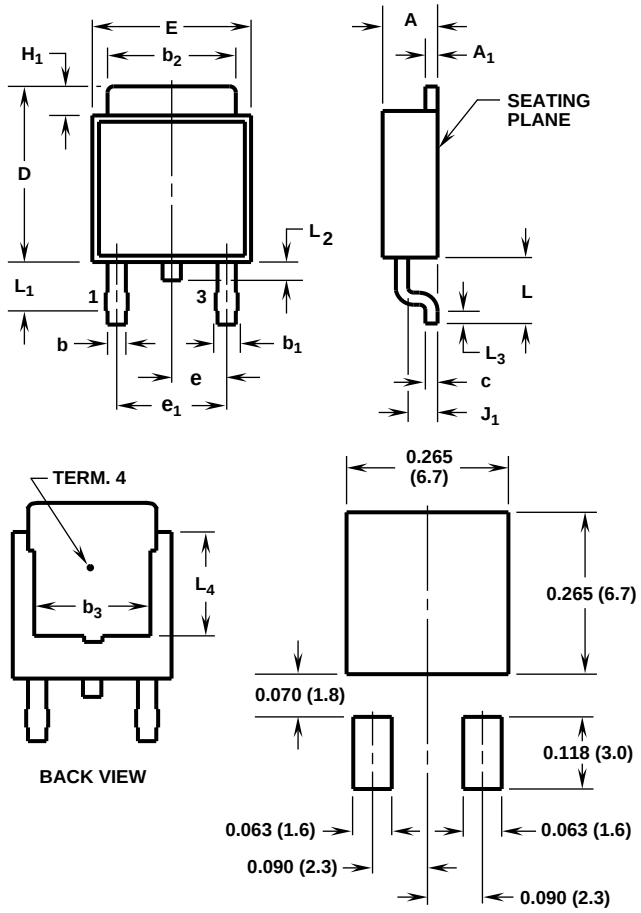
3 LEAD JEDEC TO-251AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled.
3. Dimension (without solder).
4. Add typically 0.0006 inches (0.015mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Packaging (Continued)



TO-252AA

2 LEAD JEDEC TO-252AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.075	0.090	1.91	2.28	3
L_2	0.025	0.040	0.64	1.01	-
L_3	0.020	-	0.51	-	4, 6
L_4	0.170	-	4.32	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_4 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled.
4. Dimension (without solder).
5. Add typically 0.0006 inches (0.015mm) for solder coating.
6. L_3 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 2 dated 1-93.

Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

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