HARRIS Semiconductor

PART WITHDRAWN
PROCESS OBSOLETE - NO NEW DESIGNS

MCTV75P60E1, MCTA75P60E1

75A, 600V
P-Type MOS Controlled Thyristor (MCT)

April 1999

Features

- **75A, -600V**
- **V_{TM} = -1.3V(Maximum) at I = 75A and +150^{o}C**
- **2000A Surge Current Capability**
- **2000A/μs di/dt Capability**
- **MOS Insulated Gate Control**
- **120A Gate Turn-Off Capability at +150^{o}C**

Description

The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to +150^{o}C with active switching.

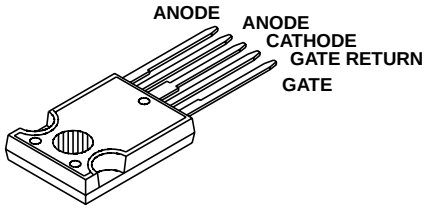
PART NUMBER INFORMATION

PART NUMBER	PACKAGE	BRAND
MCTV75P60E1	TO-247	MV75P60E1
MCTA75P60E1	MO-093AA	MA75P60E1

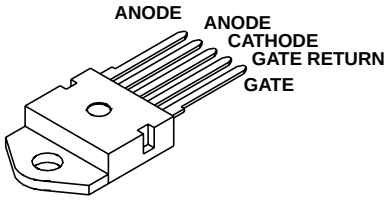
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247 5-LEAD



JEDEC MO-093AA (5-LEAD TO-218)



Symbol

Absolute Maximum Ratings T_C = +25^{o}C, Unless Otherwise Specified

		MCTV75P60E1 MCTA75P60E1	UNITS
Peak Off-State Voltage (See Figure 11)	V_{DRM}	-600	V
Peak Reverse Voltage	V_{RRM}	+5	V
Continuous Cathode Current (See Figure 2)			
T_C = +25^{o}C (Package Limited)	I_{K25}	85	A
T_C = +90^{o}C	I_{K90}	75	A
Non-Repetitive Peak Cathode Current (Note 1)	I_{KSM}	2000	A
Peak Controllable Current (See Figure 10)	I_{KC}	120	A
Gate-Anode Voltage (Continuous)	V_{GA}	±20	V
Gate-Anode Voltage (Peak)	V_{GAM}	±25	V
Rate of Change of Voltage	dv/dt	See Figure 11	
Rate of Change of Current	di/dt	2000	A/μs
Maximum Power Dissipation	P_T	208	W
Linear Derating Factor		1.67	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	^{o}C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	260	^{o}C

NOTE:

1. Maximum Pulse Width of 250μs (Half Sine) Assume T_J (Initial) = +90^{o}C and T_J (Final) = T_J (Max) = +150^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3374.6**

Electrical Specifications T_C = +25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	V_{KA} = -600V,	T_C = +150°C	-	-	3	mA
		V_{GA} = +18V	T_C = +25°C	-	-	100	µA
Peak Reverse Blocking Current	I_{RRM}	V_{KA} = +5V	T_C = +150°C	-	-	4	mA
		V_{GA} = +18V	T_C = +25°C	-	-	100	µA
On-State Voltage	V_{TM}	$I_K = I_{K90}$,	T_C = +150°C	-	-	1.3	V
		V_{GA} = -10V	T_C = +25°C	-	-	1.4	V
Gate-Anode Leakage Current	I_{GAS}	$V_{GA} = \pm 20V$		-	-	200	nA
Input Capacitance	C_{ISS}	V_{KA} = -20V, T_J = +25°C V_{GA} = +18V		-	10	-	nF
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 200µH, $I_K = I_{K90}$ R_G = 1Ω, V_{GA} = +18V, -7V T_J = +125°C V_{KA} = -300V		-	300	-	ns
Current Rise Time	t_{RI}			-	200	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	700	-	ns
Current Fall Time	t_{FI}			-	1.15	1.4	µs
Turn-Off Energy	E_{OFF}			-	10	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	.5	.6	°C/W

Typical Performance Curves

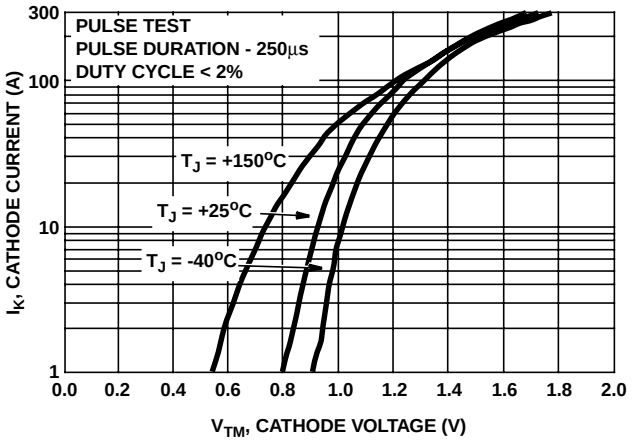


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE (TYPICAL)

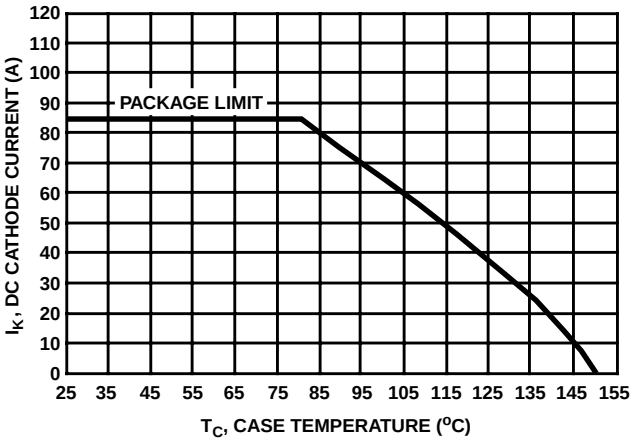


FIGURE 2. MAXIMUM CONTINUOUS CATHODE CURRENT

Typical Performance Curves (Continued)

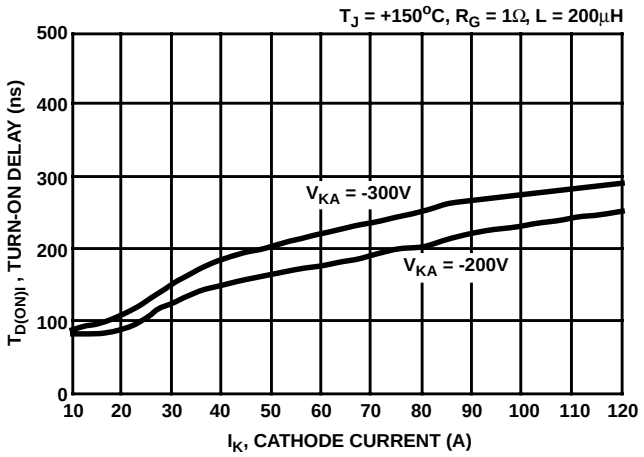


FIGURE 3. TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

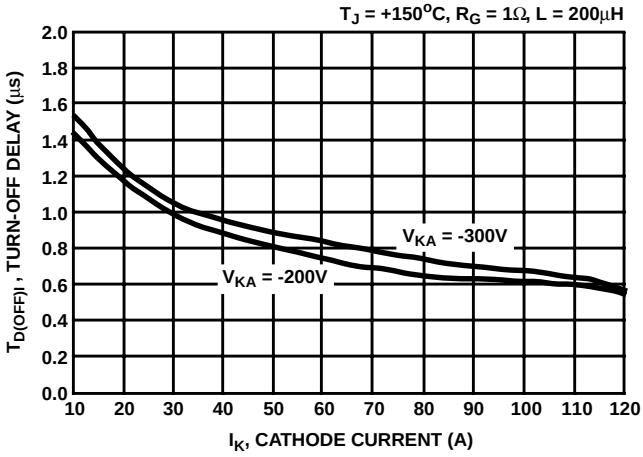


FIGURE 4. TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

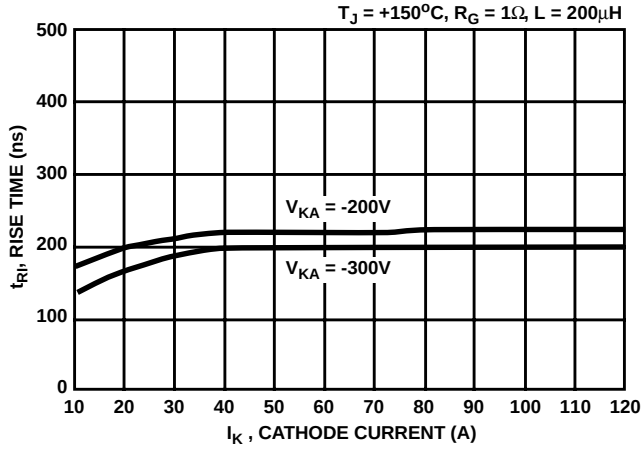


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

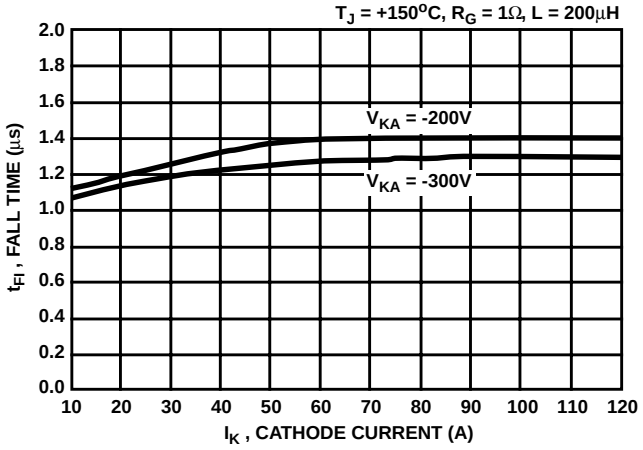


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

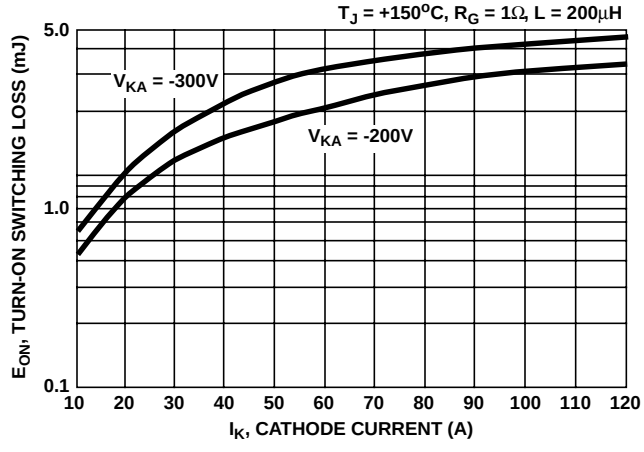


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

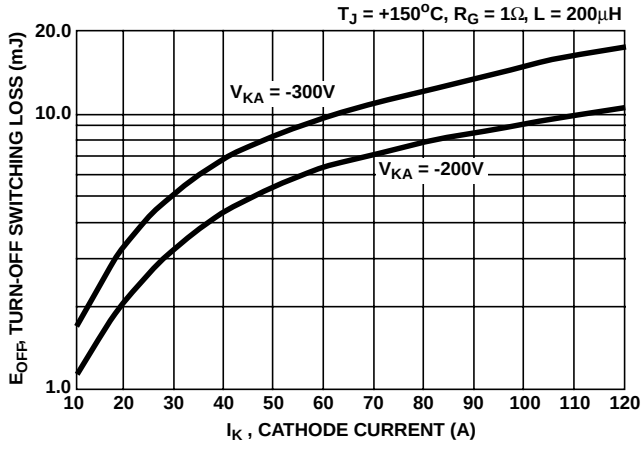


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

Typical Performance Curves (Continued)

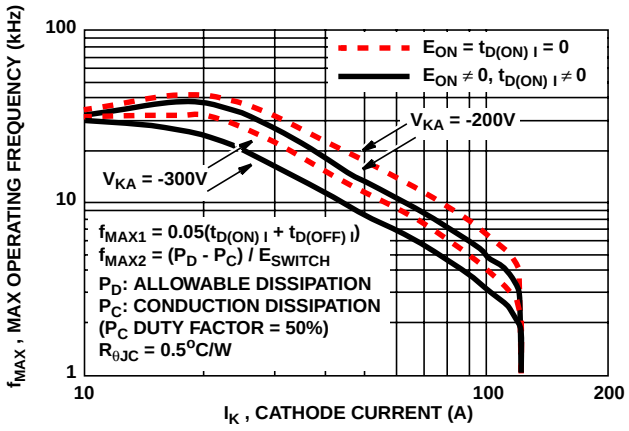


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT (TYPICAL)

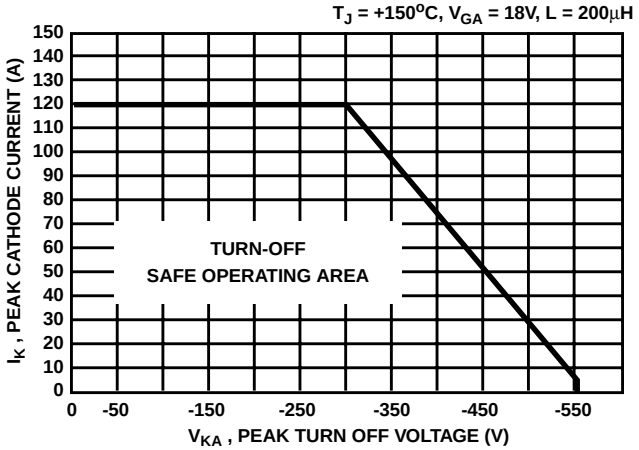


FIGURE 10. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

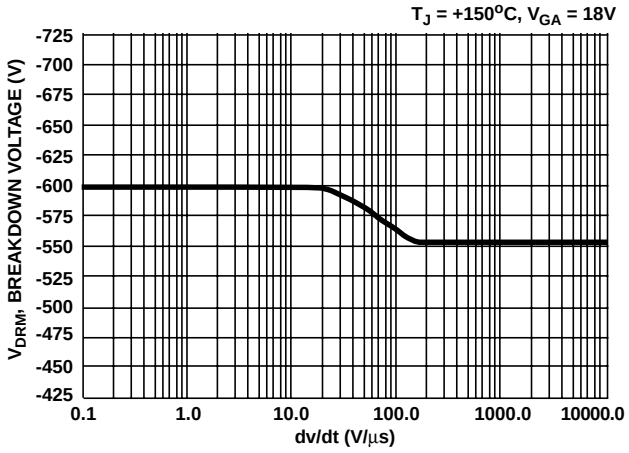


FIGURE 11. BLOCKING VOLTAGE vs dv/dt

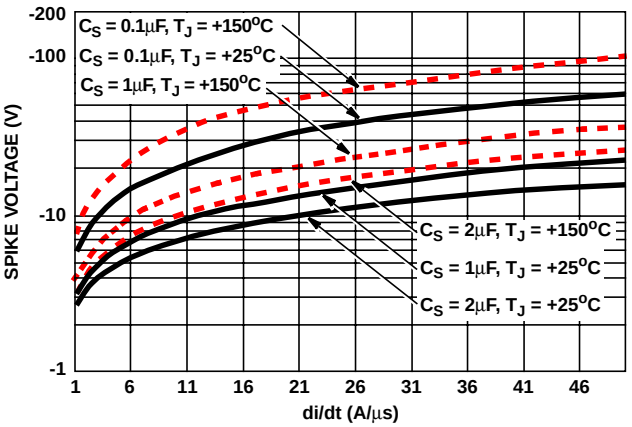


FIGURE 12. SPIKE VOLTAGE vs di/dt (TYPICAL)

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figures 3 to 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(ON)I} + t_{D(OFF)I})$. $t_{D(ON)I} + t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(ON)I}$ is defined as the 10% point of the leading edge of the input pulse and the point where the cathode current rises to 10% of its maximum value. $t_{D(OFF)I}$ is defined as the 90% point of the trailing edge of the input pulse and the point where the cathode current falls to 90% of its maximum value. Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{ON} + E_{OFF})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\Theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{AK} \bullet I_{AK})$ / (duty factor/100). E_{ON} is defined as the sum of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals saturation voltage ($V_{AK} = V_{TM}$). E_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet (E_{ON} + E_{OFF})$. Because Turn-on switching losses can be greatly influenced by external circuit conditions and components, f_{MAX} curves are plotted both including and neglecting turn-on losses.

Test Circuits

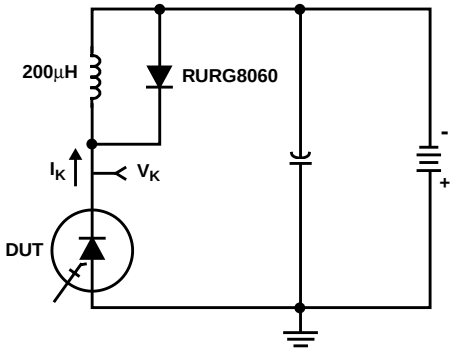


FIGURE 13. SWITCHING TEST CIRCUIT

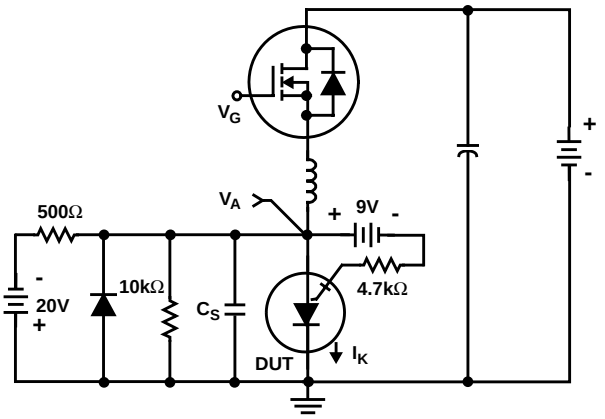


FIGURE 14. V_{SPIKE} TEST CIRCUIT

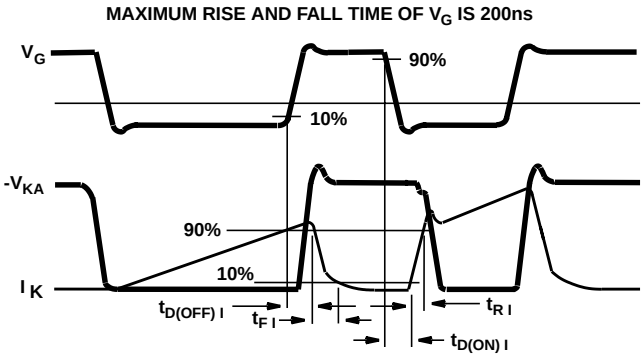


FIGURE 15. SWITCHING TEST WAVEFORMS

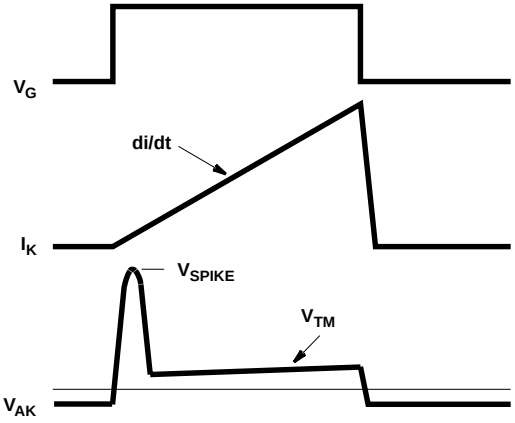


FIGURE 16. V_{SPIKE} TEST WAVEFORMS

Handling Precautions for MCT's

MOS Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORB LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating - Never exceed the gate-voltage rating of V_{GA}. Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. Gate Protection - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.