intersil

HMP8156

August 1997

NTSC/PAL Encoder

Features

- (M) NTSC and (B, D, G, H, I, M, N, CN) PAL Operation
- ITU-R BT.601 and Square Pixel Operation
- Digital Input Formats
  - 4:2:2 YCbCr
    - 8-Bit or 16-Bit
  - 4:4:4 RGB
    - 16-Bit (5, 6, 5) or 24-Bit (8, 8, 8)
    - Linear or Gamma-Corrected
  - 8-Bit Parallel ITU-R BT.656
  - Seven Overlay Colors
- Analog Output Formats
  - Y/C + Two Composite
  - RGB + Composite (SCART)
- Flexible Video Timing Control
  - Timing Master or Slave
  - Selectable Polarity on Each Control Signal
  - Programmable Blank Output Timing
  - Field Output
- Closed Caption Encoding for NTSC and PAL
- 2x Upscaling of SIF Video
- Four 2x Oversampling, 10-Bit DACs
- I^2C Interface
- Verilog Models Available. . . . .

Applications

- Multimedia PCs
- Video Conferencing
- Video Editing
- Related Products
  - NTSC/PAL Encoders: HMP8154
  - NTSC/PAL Decoders: HMP8112A, HMP8115

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HMP8156CN	0 to 70	64 PQFP	Q64.14x14
HMP8156EVAL1	Daughter Card Evaluation Platform (Note)		
HMP8156EVAL2	Frame Grabber Evaluation Platform (Note)		

NOTE: Described in the Applications Section

Description

The HMP8156 NTSC and PAL encoder is designed for use in systems requiring the generation of high-quality NTSC and PAL video from digital image data.

YCbCr or RGB digital video data drive the P0-P23 inputs. Overlay inputs are processed and the data is 2x upsampled. The Y data is optionally lowpass filtered to 5MHz and drives the Y analog output. Cb and Cr are each lowpass filtered to 1.3MHz, quadrature modulated, and summed. The result drives the C analog output. The digital Y and C data are also added together and drive the two composite analog outputs.

The YCbCr data may also be converted to RGB data to drive the DACs, allowing support for the European SCART connector.

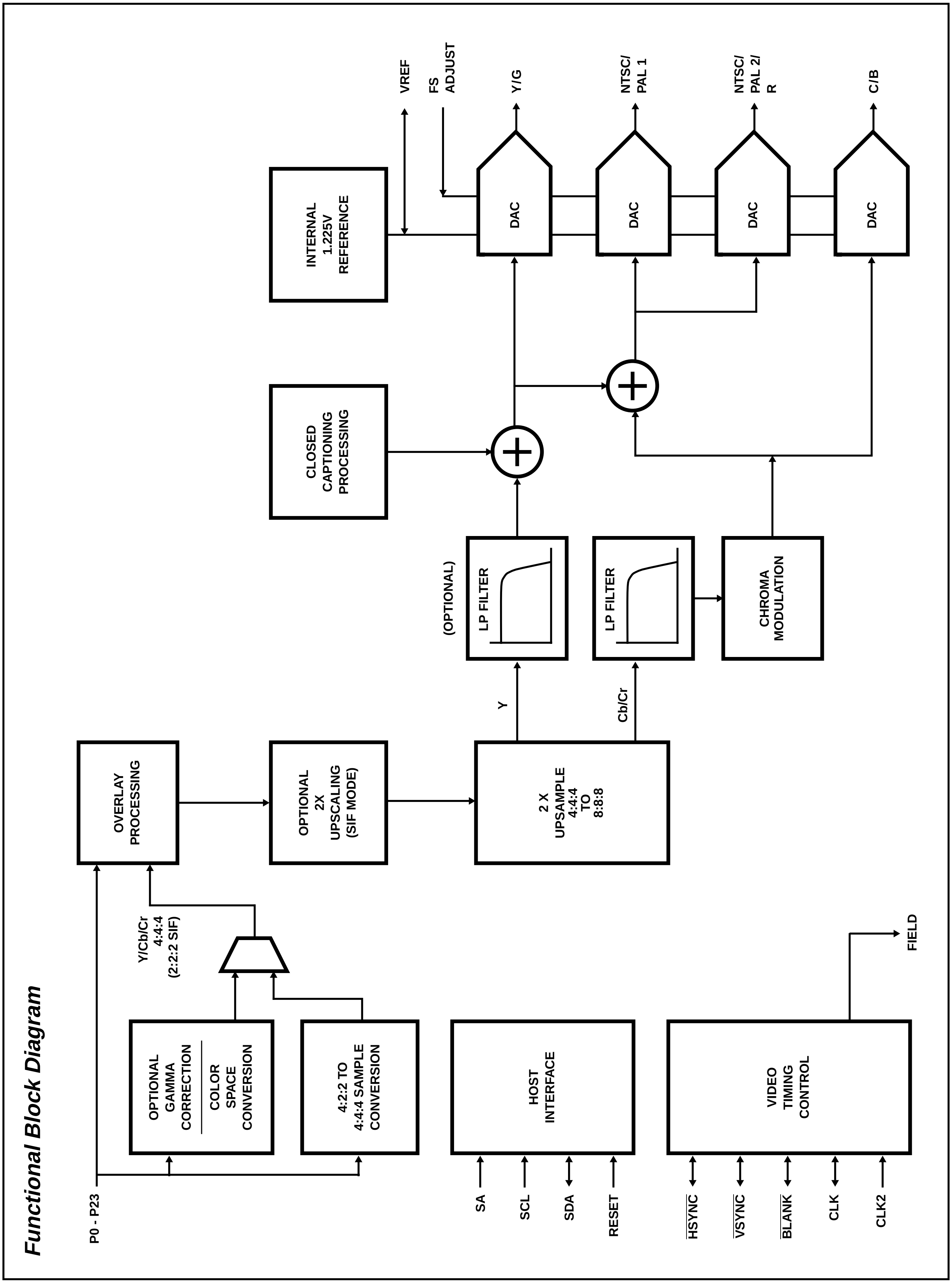
The DACs can drive doubly-terminated (37.5Ω) lines, and run at a 2x oversampling rate to simplify the analog output filter requirements.

Table of Contents

Page

Functional Block Diagram. 2
Functional Operation 3
Pixel Data Input Formats 3
Input Processing. 4
Pixel Input and Control Signal Timing. 5
Video Timing Control 10
Video Processing 12
Analog Outputs. 14
Host Interfaces 15
Pinout 22
Pin Descriptions 22
Applications Information 30
Evaluation Kits 32

Functional Block Diagram



Functional Operation

The HMP8156 is a fully integrated digital encoder. It accepts digital video input data and generates four analog video output signals. The input data format is selectable and includes YCbCr, RGB, and overlay data. The outputs are configurable to be either two composite video signals and Y/C (S-Video) or one composite and component RGB video.

The HMP8156 accepts pixel data in one of several formats and transforms it into 4:4:4 sampled luminance and chrominance (YCbCr) data. If enabled, the encoder also mixes overlay data with the input data. The encoder then interpolates the YCbCr data to twice the pixel rate and low pass filters it to match the bandwidth of the video output format. If enabled, the encoder also adds Closed Captioning information to the Y data. At the same time, the encoder modulates the chrominance data with a digitally synthesized subcarrier. Finally, the encoder outputs the luminance, chrominance, and their sum as analog signals using 10-bit D/A converters.

The HMP8156 provides operating modes to support all versions of the NTSC and PAL standards and accepts full and SIF size input data with rectangular (ITU-R BT.601) and square pixel ratios. It operates from a single clock at twice the pixel clock rate determined by the operating mode.

The HMP8156's video timing control is flexible. It may operate as the master generating the system's video timing control signals or it may accept external timing controls. The polarity of the timing controls and the number of active pixels and lines are programmable.

Pixel Data Input Formats

The HMP8156 accepts pixel data via the P0-P23 input pins. The definition of each pixel input pin is determined by the input format selected in the input format register. The definition for each mode is shown in Table 1.

YCbCr Pixel Data

The HMP8156 accepts 4:2:2 sampled YCbCr input data. The luminance and color difference signals are each 8 bits, scaled 0 to 255. Values outside their nominal ranges (16-235 for Y and 16-240 for Cb and Cr) are processed normally. The color difference signals are time multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr busses may be input in parallel (16-bit mode) or may be time multiplexed and input as a single bus (8-bit mode). The single bus may also contain SAV and EAV video timing reference codes (ITU-R BT.656 mode).

RGB Data

The HMP8156 accepts 4:4:4 sampled RGB component video input data. The color signals may be (8,8,8) for 24-bit mode or (5,6,5) for 16-bit mode. In 24-bit mode, they are scaled 0 to 255, black to white. In 16-bit mode, the encoder left shifts the input so that it has the same scale as 24-bit input. The RGB data may be linear or gamma corrected; if enabled, the encoder will gamma correct the input data.

Overlay Data

The HMP8156 accepts 5 bits of pixel overlay input data and combines it with the input pixel data. The data specifies an overlay color and the fractions of the new and original colors to be summed.

Blue Screen Generation

In blue screen mode, the HMP8156 ignores the pixel input data and generates a solid, blue screen. The overlay inputs may be used to place information over the blue screen.

TABLE 1. PIXEL DATA INPUT FORMATS

PIN NAME	16-BIT 4:2:2 YCBCR	8-BIT 4:2:2 YCBCR	BT.656	BLUE SCREEN	16-BIT RGB (5, 6, 5)	24-BIT RGB
P0	Cb0, Cr0	Ignored			B0	B0
P1	Cb1, Cr1				B1	B1
P2	Cb2, Cr2				B2	B2
P3	Cb3, Cr3				B3	B3
P4	Cb4, Cr4				B4	B4
P5	Cb5, Cr5				G0	B5
P6	Cb6, Cr6				G1	B6
P7	Cb7, Cr7				G2	B7
P8	Y0	Y0, Cb0, Cr0	YCbCr Data, SAV and EAV Sequences	Ignored	G3	G0
P9	Y1	Y1, Cb1, Cr1			G4	G1
P10	Y2	Y2, Cb2, Cr2			G5	G2
P11	Y3	Y3, Cb3, Cr3			R0	G3
P12	Y4	Y4, Cb4, Cr4			R1	G4
P13	Y5	Y5, Cb5, Cr5			R2	G5
P14	Y6	Y6, Cb6, Cr6			R3	G6
P15	Y7	Y7, Cb7, Cr7			R4	G7
P16	OL0					R0
P17	OL1					R1
P18	OL2					R2
P19	M0					R3
P20	M1					R4
P21	-					R5
P22	-					R6
P23	-					R7

Input Processing

COLOR SPACE CONVERSION

For linear RGB input formats, the encoder applies gamma-correction using a selectable gamma value of 1/2.2 or 1/2.8. The gamma-corrected RGB data from either the correction function in linear mode or the input port otherwise is converted to 4:4:4 sampled YCbCr data.

For the YCbCr input formats, the encoder converts the 4:2:2 sampled data to 4:4:4 sampled data. The conversion is done by 2x upsampling the Cb and Cr data. The upsampling function uses linear interpolation.

OVERLAY PROCESSING

The HMP8156 accepts overlay data via the OL0-OL2, M0, and M1 pins. Overlay mixing is done using the 4:4:4 YCbCr pixel data from the color space converter. The YCbCr data following overlay processing is used as input data by the video processing functions.

The OL0-OL2 inputs select the color to be mixed with the pixel data. Overlay colors 1-7 are standard color bar colors. Overlay color 0 is special and disables mixing on a pixel by pixel basis. The overlay color palette is shown in Table 2.

TABLE 2. OVERLAY COLOR PALETTE

OL2-OL0	COLOR
000	Pixel Data
001	75% Blue
010	75% Red
011	75% Magenta
100	75% Green
101	75% Cyan
110	75% Yellow
111	100% White

Note that overlay capability is not available when the 24-bit RGB input format is used.

The encoder provides 4 methods for mixing the overlay data with the pixel data: disabled, external mixing, internal mixing and no mixing. The method used is selected in the input format control register.

Overlay Mixing: Disabled

When overlay mixing is disabled, the OL0-OL2, M0, and M1 inputs are ignored and the pixel data is not changed.

Overlay Mixing: External

When external overlay mixing is selected, mixing of overlay data and pixel data is controlled by the M1 and M0 inputs. M1 and M0 indicate the mixing level between the pixel inputs and the overlay inputs, on a pixel-by-pixel basis. M1 and M0 are ignored if OL2-OL0 = 000. Otherwise, they select the percentage of each color to sum as shown in Table 3.

TABLE 3. OVERLAY MIXING FACTORS

M1, M0	% OVERLAY COLOR	% PIXEL COLOR
00	0	100
01	12.5	87.5
10	87.5	12.5
11	100	0

In external mixing mode, there is no minimum number of pixels an overlay color or pixel color must be selected. The mixing level may also vary at any rate.

Overlay Mixing: Internal

Mixing of overlay and pixel data may also be controlled internally, and the M1 and M0 input pins are ignored. A transition from pixel data to overlays, from overlays to pixel data, or between different overlay colors triggers the mixing function. An overlay color must be selected for a minimum of three pixels for proper overlay operation in this mode. Internal overlay mixing should not be used with the BT.656 input format.

When going from pixel to overlay data, mixing starts one pixel before the selection of the overlay color (OL2-OL1!= 000). The first pixel output before the overlay uses 12.5% overlay color plus 87.5% pixel color. The next output is aligned with the selection of the overlay color and uses 87.5% overlay color plus 12.5% pixel color. Additional outputs use 100% overlay color.

When going from overlay to pixel data, mixing starts one pixel before the selection of the pixel color (OL2-OL0 = 000). The last pixel output of the overlay uses 87.5% overlay color plus 12.5% pixel color. The next output uses 12.5% overlay color plus 87.5% pixel color. Additional outputs use 100% pixel color.

When going from one overlay color to another, mixing starts one pixel before the selection of the new overlay color, and uses 12.5% new overlay color plus 87.5% old overlay color. The next output is aligned with the selection of the new overlay color and uses 87.5% new overlay color plus 12.5% old overlay color. Additional outputs use 100% new overlay color.

Overlay Mixing: No Mixing

With no overlay mixing selected, whenever the OL0-OL2 inputs are non-zero, the overlay color is displayed. The M0 and M1 inputs are ignored, and no internal mixing is done. Essentially, this is a hard switch between overlay and pixel data. In this mode, there is no minimum number of pixels an overlay color or pixel color must be selected.

2X Upscaling

Following overlay processing, 2X upscaling may optionally be applied to the pixel data. In this mode, the HMP8156 accepts SIF resolution video at 50 or 59.94 **frames** per second and generates standard interlaced video at 262.5 lines per field (240 active) at 59.94 **fields** per second for (M, NSM) NTSC and (M) PAL, and 312.5 lines per field (288 active) at 50 fields per second for (B, D, G, H, I, N, CN) PAL. This mode of operation allows SIF video to be upscaled to full resolution and recorded on a VCR or displayed on a TV.

The input pixel data rate is reduced by half when 2X upscaling is enabled. The color space conversion generates, and the overlay mixer uses, 2:2:2 YCbCr data instead of 4:4:4 data. For rectangular pixel NTSC and PAL video, the input rate is 6.75MHz during the active portion of each line instead of 13.5MHz. Example SIF input resolutions and resulting output resolutions are shown in Table 4.

TABLE 4. TYPICAL RESOLUTIONS FOR 2X UPSCALING

INPUT ACTIVE RESOLUTION	OUTPUT ACTIVE RESOLUTION
352 x 240	704 x 480
352 x 288	704 x 576
320 x 240	640 x 480
384 x 288	768 x 576

The HMP8156 performs horizontal 2X upscaling by linear interpolation. The vertical scaling is done by line duplication. For typical line duplication, the same frame of SIF pixel input data is used for both the odd and even fields. Note that a frame of SIF size input has about the same number of lines as a field of full size input. After 2X upscaling, the input is 4:4:4 YCbCr data ready for video processing.

Pixel Input and Control Signal Timing

The pixel input timing and the video control signal input/output timing of the HMP8156 depend on the part's operating mode. The periods when the encoder samples its inputs and generates its outputs are summarized in Table 5.

Figures 1-9 show the timing of CLK, CLK2, $\overline{\text{BLANK}}$, and the pixel and overlay input data with respect to each other. $\overline{\text{BLANK}}$ may be an input or an output; the figures show both. When it is an input, $\overline{\text{BLANK}}$ must arrive coincident with the pixel and overlay input data; all are sampled at the same time.

When $\overline{\text{BLANK}}$ is an output, its timing with respect to the pixel and overlay inputs depends on the blank timing select bit in the timing_I/O_1 register. If the bit is cleared, the HMP8156 deasserts $\overline{\text{BLANK}}$ one CLK cycle before it samples the pixel and overlay inputs. As shown in the timing figures, the encoder samples the inputs 1-7 CLK2 periods after negating $\overline{\text{BLANK}}$, depending on the operating mode.

If the bit is set, the encoder deasserts $\overline{\text{BLANK}}$ during the same CLK cycle in which it samples the input data. In effect, the input data must arrive one CLK cycle earlier than when the bit is cleared. This mode is not shown in the figures.

TABLE 5. PIXEL INPUT AND CONTROL SIGNAL I/O TIMING

<table>
<tr><th rowspan="2">INPUT FORMAT</th><th rowspan="2">2X UPSCALING</th><th colspan="2">INPUT PORT SAMPLING</th><th colspan="2">VIDEO TIMING CONTROL (NOTE)</th><th colspan="2">CLK FREQUENCY</th></tr>
<tr><th>PIXEL DATA</th><th>OVERLAY DATA</th><th>INPUT SAMPLE</th><th>OUTPUT ON</th><th>INPUT</th><th>OUTPUT</th></tr>
<tr><td rowspan="2">8-Bit YCbCr</td><td>Off</td><td>Every rising edge of CLK2</td><td>Same edge that latches Y</td><td>Every rising edge of CLK2</td><td>Any rising edge of CLK2</td><td>Ignored</td><td>One-half CLK2</td></tr>
<tr><td>On</td><td>Rising edge of CLK2 when CLK is low.</td><td>Same edge that latches Y data</td><td>Rising edge of CLK2 when CLK is low.</td><td>Rising edge of CLK2 when CLK is high.</td><td colspan="2">One-half CLK2</td></tr>
<tr><td rowspan="2">16-Bit YCbCr,
16-Bit RGB,
or
24-Bit RGB</td><td>Off</td><td colspan="3">Rising edge of CLK2 when CLK is low</td><td>Rising edge of CLK2 when CLK is high.</td><td colspan="2">One-half CLK2</td></tr>
<tr><td>On</td><td colspan="3">2nd rising edge of CLK2 when CLK is low</td><td>Either rising CLK2 edge when CLK is high</td><td colspan="2">One-fourth CLK2</td></tr>
<tr><td rowspan="2">BT.656</td><td>Off</td><td>Every rising edge of CLK2</td><td>Same edge that latches Y</td><td>Not Allowed</td><td>Any rising edge of CLK2</td><td>Ignored</td><td>One-half CLK2</td></tr>
<tr><td>On</td><td colspan="6">Not Available</td></tr>
</table>

NOTE: Video timing control signals include HSYNC, VSYNC, BLANK and FIELD. The sync and blanking I/O directions are independent; FIELD is always an output.

8-Bit YCbCr Format without 2X Upscaling

When 8-bit YCbCr format is selected and 2X upscaling is not enabled, the data is latched on each rising edge of CLK2. The pixel data must be [Cb Y Cr Y' Cb Y Cr Y'. . .], with the first active data each scan line being Cb data. Overlay data is latched when the Y input data is latched. The pixel and overlay input timing is shown in Figure 1.

As inputs, BLANK, HSYNC, and VSYNC are latched on each rising edge of CLK2. As outputs, BLANK, HSYNC, and VSYNC are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency

8-Bit YCbCr Format with 2X Upscaling

When 8-bit YCbCr format is selected, the data is latched on the rising edge of CLK2 while CLK is low. The pixel data must be [Cb Y Cr Y' Cb Y Cr Y'. . .], with the first active data each scan line being Cb data. Overlay data is latched on the rising edge of CLK2 that latches Y pixel input data. The pixel and overlay input timing is shown in Figure 2.

As inputs, BLANK, HSYNC, and VSYNC are latched on the rising edge of CLK2 while CLK is low. As outputs, HSYNC, VSYNC, and BLANK are output following the rising edge of CLK2 while CLK is high. In this mode of operation, CLK is one-half the CLK2 frequency.

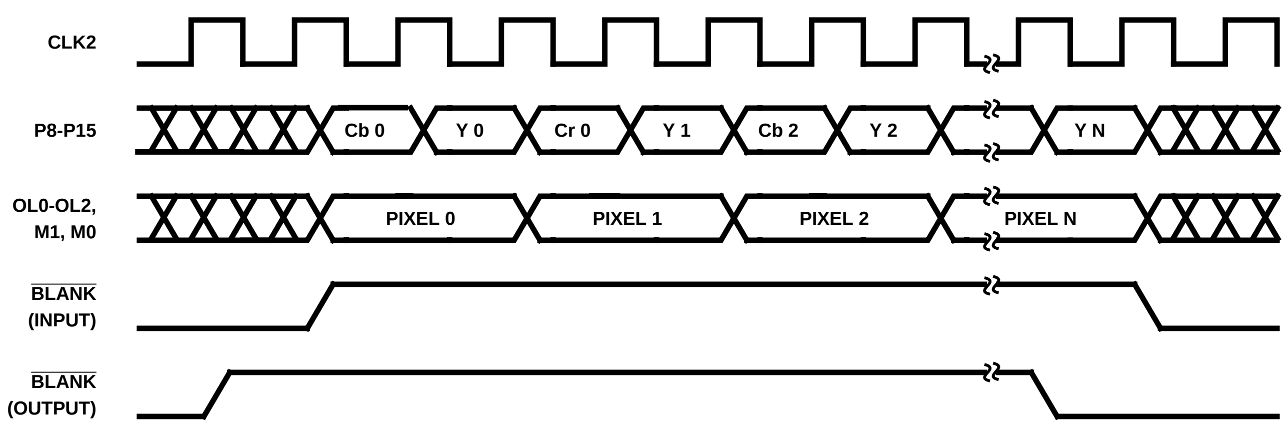


FIGURE 1. PIXEL AND OVERLAY INPUT TIMING - 8-BIT YCBCR WITHOUT 2X UPSCALING

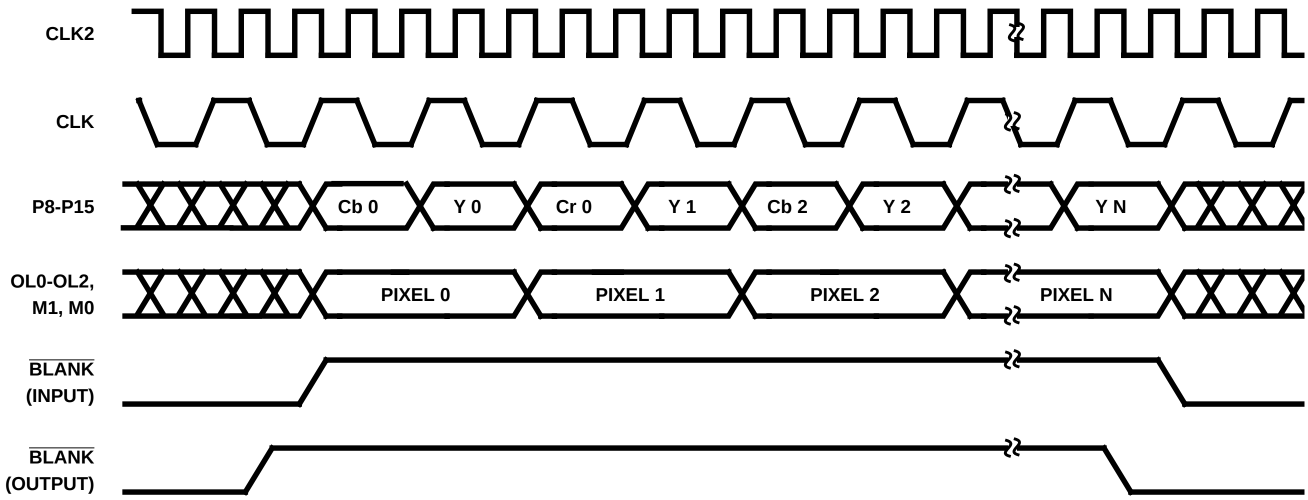


FIGURE 2. PIXEL AND OVERLAY INPUT TIMING - 8-BIT YCBCR WITH 2X UPSCALING

16-Bit YCbCr, 16-Bit RGB, 24-Bit RGB Formats without 2X Upscaling

When 16-bit YCbCr, 16-bit RGB data, or 24-bit RGB format is selected without 2X upscaling, the pixel data is latched on the rising edge of CLK2 while CLK is low. Overlay data is also latched on the rising edge of CLK2 while CLK is low. The pixel and overlay input timing is shown in Figures 3 - 5.

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on the rising edge of CLK2 while CLK is low. As outputs, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are output following the rising edge of CLK2 while CLK is high. In these modes of operation, CLK is one-half the CLK2 frequency.

16-Bit YCbCr, 16-Bit RGB, 24-Bit RGB Formats with 2X Upscaling

When 16-bit YCbCr, 16-bit RGB data, or 24-bit RGB format is selected and 2X upscaling is enabled, data is latched on the rising edge of CLK2 while CLK is low. Overlay data is latched on the rising edge of CLK2 while CLK is low. The pixel and overlay input timing is shown in Figures 6-8

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on the rising edge of CLK2 while CLK is low. As outputs, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are output following the rising edge of CLK2 while CLK is high. CLK is one-fourth the CLK2 frequency.

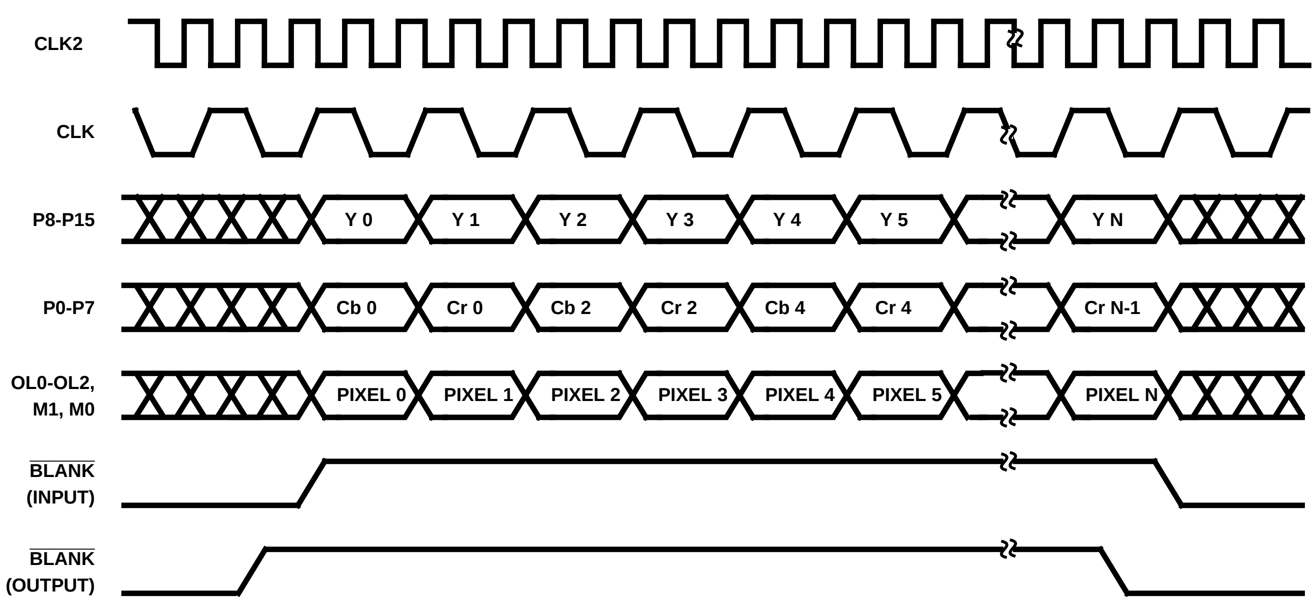


FIGURE 3. PIXEL AND OVERLAY INPUT TIMING 6-BIT YCBCR WITHOUT 2X UPSCALING

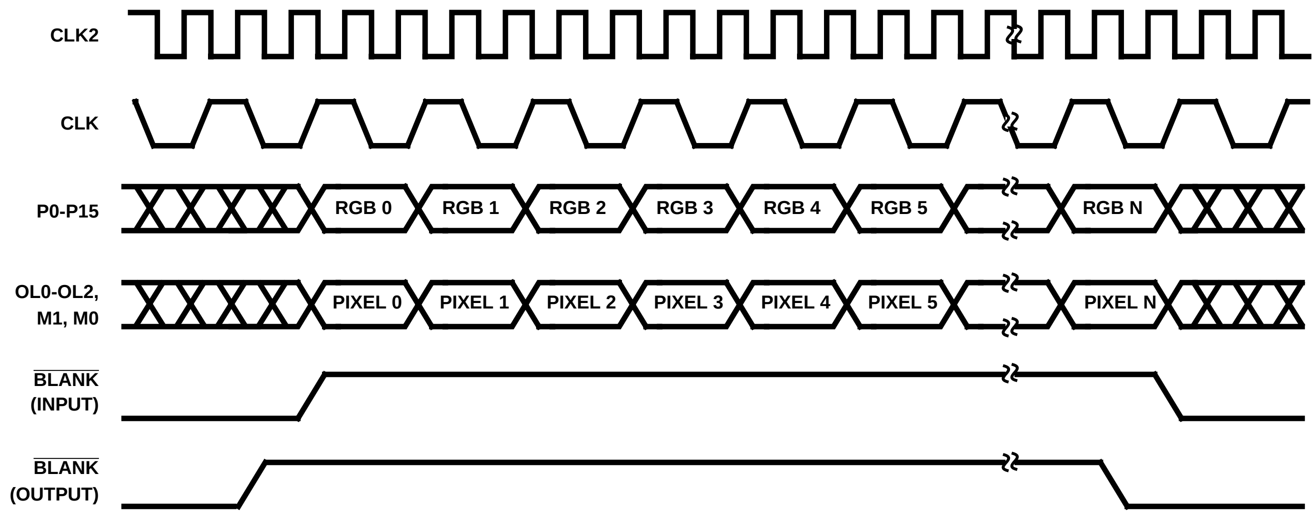


FIGURE 4. PIXEL AND OVERLAY INPUT TIMING - 16-BIT RGB WITHOUT 2X UPSCALING

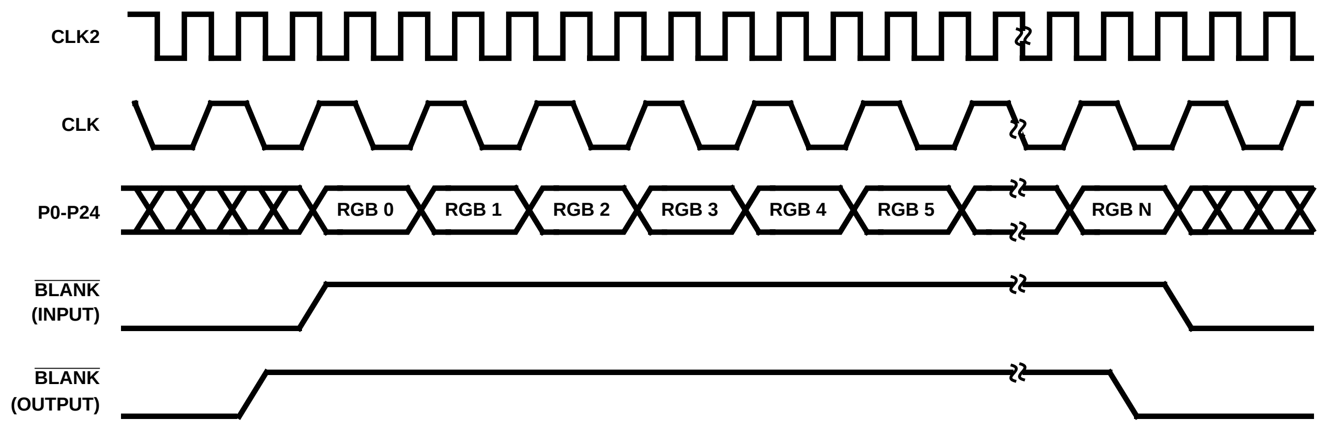


FIGURE 5. PIXEL AND OVERLAY INPUT TIMING - 24-BIT RGB WITHOUT 2X UPSCALING

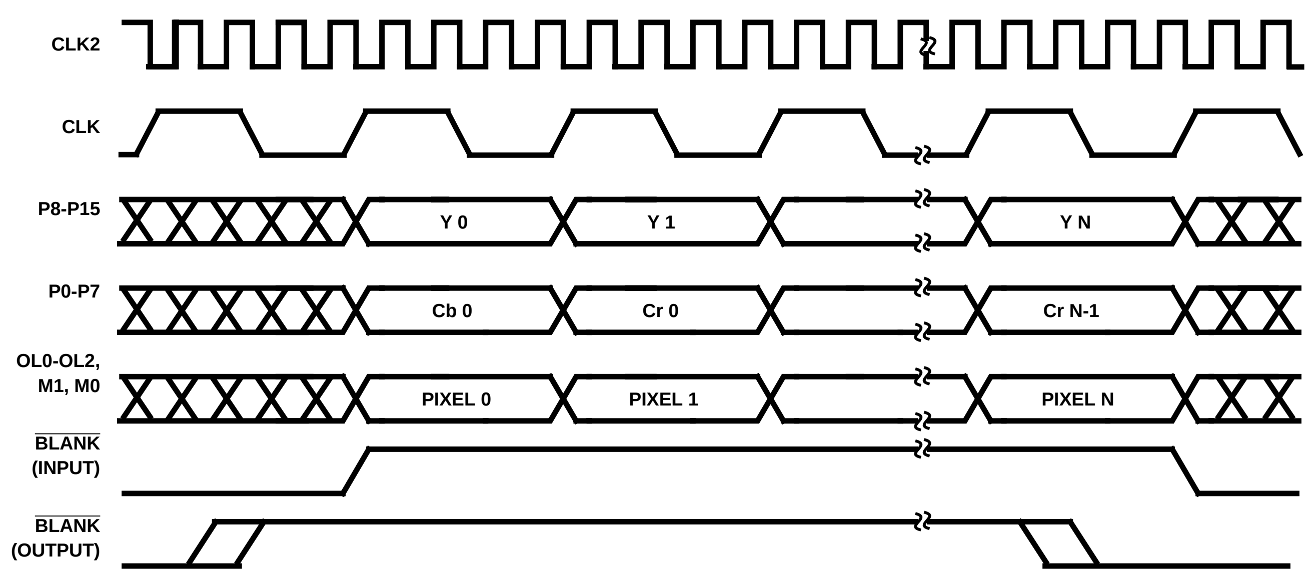


FIGURE 6. PIXEL AND OVERLAY INPUT TIMING - 16-BIT YCBCR WITH 2X UPSAMPLING

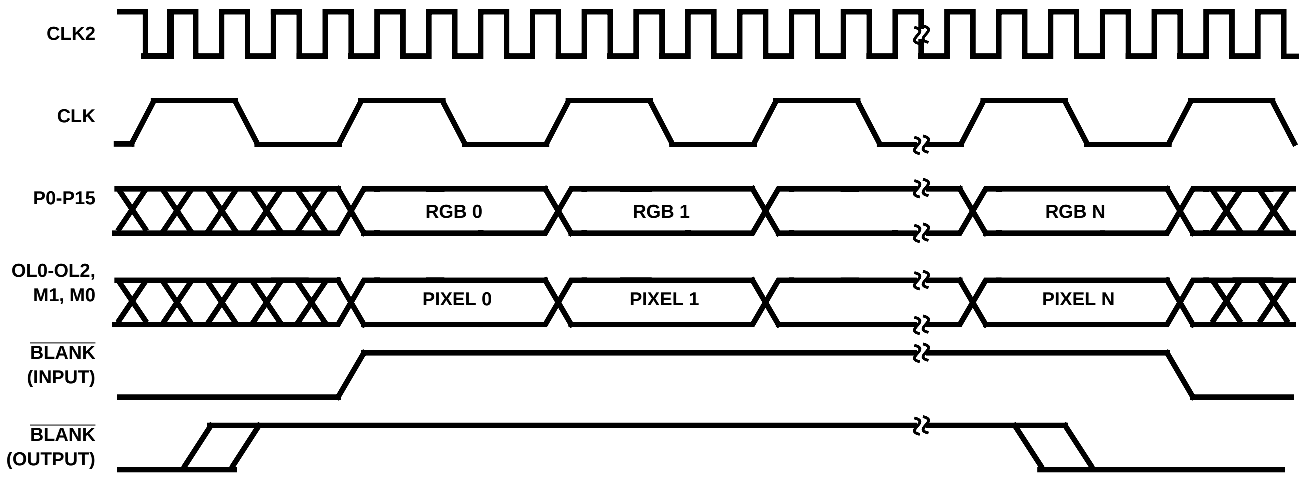


FIGURE 7. PIXEL AND OVERLAY INPUT TIMING - 16-BIT RGB WITH 2X UPSAMPLING

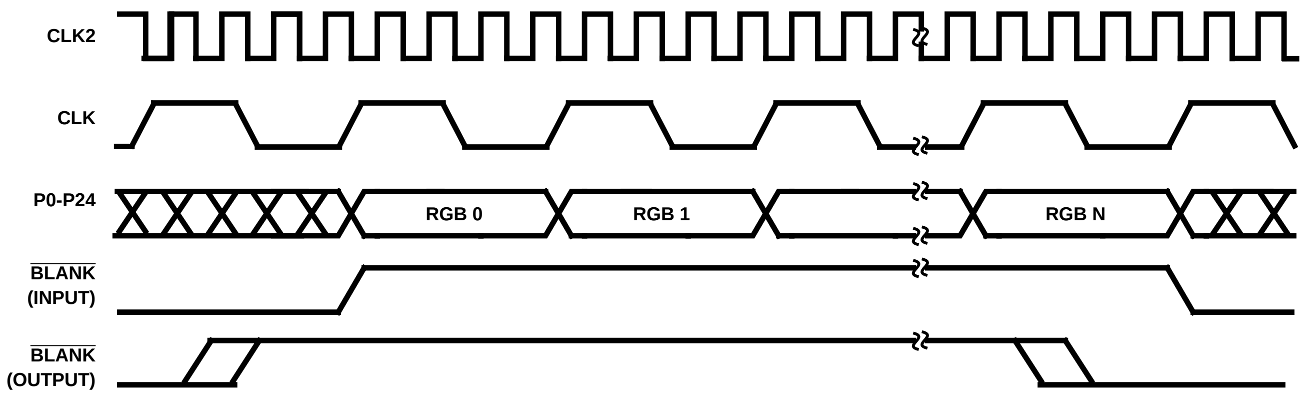


FIGURE 8. PIXEL AND OVERLAY INPUT TIMING - 24-BIT RGB WITH 2X UPSAMPLING

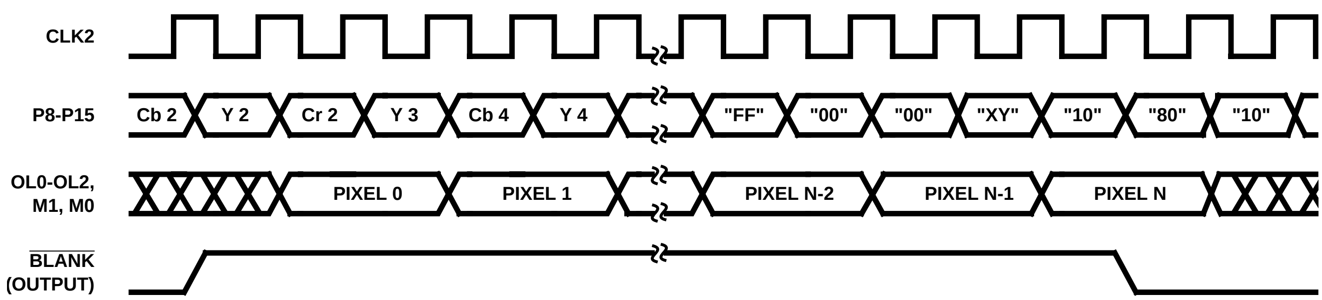


FIGURE 9. PIXEL AND OVERLAY INPUT TIMING - BT.656

8-Bit Parallel ITU-R BT.656 Format

When ITU-R BT.656 format is selected, data is latched on each rising edge of CLK2. Overlay data is latched when the Y input data is latched. However, the overlay data must arrive three pixels after its corresponding Y data. The pixel and overlay input timing is shown in Figure 9.

As inputs, the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, and $\overline{\text{VSYNC}}$ pins are ignored since all timing is derived from the EAV and SAV sequences within the data stream. As outputs, $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency.

Square pixel operation, overlay processing with internal mixing, and SIF mode 2X upsampling are not supported for the BT.656 input format. Also, the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ signals must be configured as outputs.

Video Timing Control

The pixel and overlay data must be presented to the HMP8156 at 50 or 59.94 fields per second (interlaced). The video timing is controlled by the $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, FIELD, and CLK2 pins.

$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD Timing

The leading edge of $\overline{\text{HSYNC}}$ indicates the beginning of a horizontal sync interval. If $\overline{\text{HSYNC}}$ is an output, it is asserted for about 4.7 µs. If $\overline{\text{HSYNC}}$ is an input, it must be active for at least two CLK2 periods. The width of the horizontal composite sync tip is determined from the video standard and does not depend on the width of $\overline{\text{HSYNC}}$.

The leading edge of $\overline{\text{VSYNC}}$ indicates the beginning of a vertical sync interval. If $\overline{\text{VSYNC}}$ is an output, it is asserted for 3 scan lines in (M, NSM) NTSC and (M, N) PAL modes or 2.5 scan lines in (B, D, G, H, I, CN) PAL modes. If $\overline{\text{VSYNC}}$ is an input, it must be asserted for at least two CLK2 periods.

When $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are configured as outputs, their leading edges will occur simultaneously at the start of an odd field. At the start of an even field, the leading edge of $\overline{\text{VSYNC}}$ occurs in the middle of the line.

When $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are configured as inputs, if the leading edge of $\overline{\text{HSYNC}}$ occurs within ±127 CLK2 cycles of the leading edge of $\overline{\text{VSYNC}}$, the encoder assumes it is at the start of an odd field. Otherwise, it assumes it is processing an even field.

The FIELD signal is always an output and changes state near each leading edge of $\overline{\text{VSYNC}}$. The delay between the syncs and FIELD depends on the encoder's operating mode as summarized in Table 6. In modes in which the encoder uses CLK to gate its inputs and outputs, the FIELD signal may be delayed 0-12 additional CLK2 periods.

Figure 10 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and FIELD general timing for (M, NSM) NTSC and (M, N) PAL. Figure 11 illustrates the general timing for (B, D, G, H, I, CN) PAL. In the figures, all the signals are shown active low (their reset state), and FIELD is low during odd fields.

TABLE 6. FIELD OUTPUT TIMING

OPERATING MODE		CLK2 DELAY	COMMENTS
SYNC I/O DIRECTION	BLANK I/O DIRECTION		
Input	Input	148	FIELD lags $\overline{\text{VSYNC}}$ switching from odd to even. FIELD lags the earlier of $\overline{\text{VSYNC}}$ and $\overline{\text{HSYNC}}$ when syncs are aligned when switching from even to odd.
Input	Output	138	FIELD lags $\overline{\text{VSYNC}}$.
Output	Don't Care	32	FIELD leads $\overline{\text{VSYNC}}$.

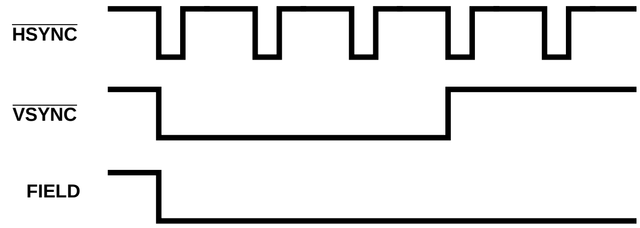


FIGURE 10A. BEGINNING AN ODD FIELD

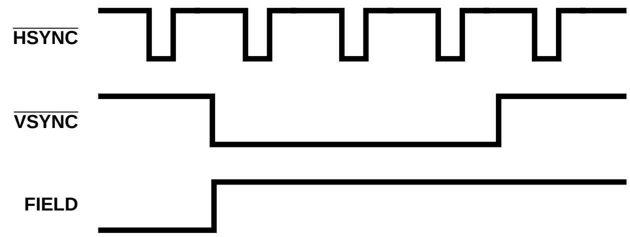


FIGURE 10B. BEGINNING AN EVEN FIELD

FIGURE 10. $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, AND FIELD TIMING FOR (M, NSM) NTSC AND (M, N) PAL

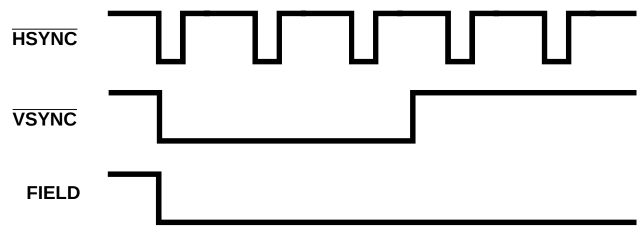


FIGURE 11A. BEGINNING AN ODD FIELD

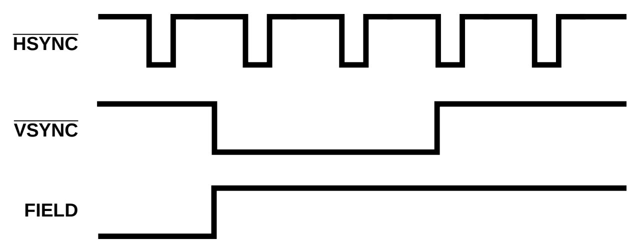


FIGURE 11B. BEGINNING AN EVEN FIELD

FIGURE 11. $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, AND FIELD TIMING FOR (B, D, G, H, I, CN) PAL

BLANK Timing

The encoder uses the HSYNC, VSYNC, FIELD signals to generate a standard composite video waveform with no active video. The signal includes only sync tips, color burst, and optionally, a 7.5 IRE blanking setup. Based on the BLANK signal, the encoder adds the pixel and overlay input data to the video waveform.

The encoder ignores the pixel and overlay input data when BLANK is asserted. Instead of the input data, the encoder generates the blanking level. The encoder also ignores the pixel and overlay inputs when generating closed captioning data on a specific line, even if BLANK is negated.

There must be an even number of active and total pixels per line. In the 8-bit YCbCr modes, the number of active and total pixels per line must be a multiple of four. Note that if BLANK is an output, half-line blanking on the output video cannot be done.

The HMP8156 never adds a 7.5 IRE blanking setup during the active line time on scan lines 1-21 and 263-284 for (M, NSM) NTSC, scan lines 523-18 and 260-281 for (M) PAL, and scan lines 623-22 and 311-335 for (N) PAL, allowing the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately.

The relative timing of BLANK, HSYNC, and the output video depends on the blanking and sync I/O directions. The typical timing relation is shown in Figure 12. The delays which vary with operating mode are indicated. The width of the composite sync tip and the location and duration of the color burst are fixed based on the video format.

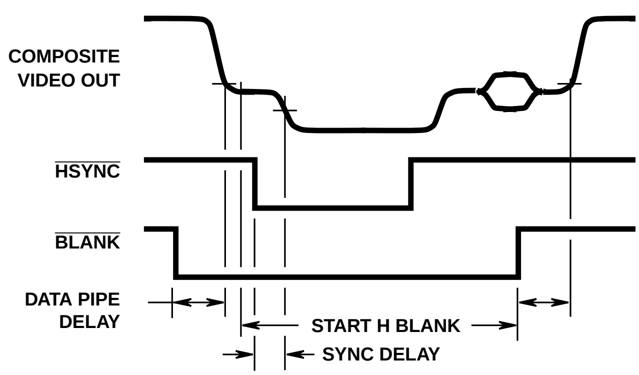


FIGURE 12. HSYNC, BLANK, AND OUTPUT VIDEO TIMING

When BLANK is an output, the encoder asserts it during the inactive portions of active scan lines and for all of each inactive scan line. The inactive scan lines blanked each field are determined by the start_v_blank and end_v_blank registers. The inactive portion of active scan lines is determined by the start_h_blank and end_h_blank registers.

The zero count for horizontal blanking is 32 CLK2 cycles before the 50% point of the composite sync. From this zero point, the HMP8156 counts every other CLK2 cycle. When the count reaches the value in the start_h_blank register, the encoder negates BLANK. When the count reaches the value in the end_h_blank register, BLANK is asserted. There may be an additional 0-7 CLK2 delays in modes which use CLK.

The data pipeline delay through the HMP8156 is 26 CLK2 cycles. In operating modes which use CLK to gate the inputs into the encoder, the delay may be an additional 0-7 CLK2 cycles. The delay from BLANK to the start or end of active video is an additional one-half CLK cycle when the blank timing select bit is cleared. The active video may also appear to end early or start late since the HMP8156 controls the blanking edge rates.

The delay from the active edge of HSYNC to the 50% point of the composite sync is 4-39 CLK2 cycles depending on the HMP8156 operating mode. The delay is shortest when the encoder is the timing master; it is longest when in slave mode.

CLK2 Input

The CLK2 input clocks all of the HMP8156, including its video timing counters. For proper operation, all of the HMP8156 inputs must be synchronous with CLK2. The frequency of CLK2 depends on the device's operating mode and the total number of pixels per line. The standard clock frequencies are shown in Table 7.

Note that the color subcarrier is derived from the CLK2 input. Any jitter on CLK2 will be transferred to the color subcarrier, resulting in color changes. Just 400ps of jitter on CLK2 causes up to a 1º color subcarrier phase shift. Thus, CLK2 should be derived from a stable clock source, such as a crystal. The use of a PLL to generate CLK2 is not recommended.

TABLE 7. TYPICAL VIDEO TIMING PARAMETERS

VIDEO STANDARD	PIXELS PER LINE		HBLANK REGISTER VALUES		VBLANK REGISTER VALUES		CLK2 (MHZ)
	TOTAL	ACTIVE	START	END	START	END	
FULL INPUT RESOLUTION, RECTANGULAR PIXELS							
(M, NSM) NTSC	858	720	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(B, D, G, H, I) PAL	864	720	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
(M) PAL	858	720	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(N) PAL	864	720	853 (0x355)	133 (0x85)	309 (0x135)	21 (0x15)	27.0
(CN) PAL	864	720	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
FULL INPUT RESOLUTION, SQUARE PIXELS							
(M, NSM) NTSC	780	640	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(B, D, G, H, I) PAL	944	768	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
(M) PAL	780	640	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(N) PAL	944	784	923 (0x39b)	155 (0x9b)	309 (0x135)	21 (0x15)	29.5
(CN) PAL	944	768	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
SIF INPUT RESOLUTION, RECTANGULAR PIXELS							
(M, NSM) NTSC	429	352	834 (0x342)	130 (0x82)	259 (0x103)	19 (0x13)	27.0
(B, D, G, H, I) PAL	432	352	845 (0x34d)	141 (0x8d)	310 (0x136)	22 (0x16)	27.0
(M) PAL	429	352	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(N) PAL	432	352	853 (0x355)	133 (0x85)	309 (0x135)	21 (0x15)	27.0
(CN) PAL	432	352	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
SIF INPUT RESOLUTION, SQUARE PIXELS							
(M, NSM) NTSC	390	320	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(B, D, G, H, I) PAL	472	384	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
(M) PAL	390	320	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(N) PAL	472	392	923 (0x39b)	155 (0x9b)	309 (0x135)	21 (0x15)	29.5
(CN) PAL	472	384	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5

Video Processing

Upsampling

Video processing begins with the 4:4:4 sampled YCbCr data from the input processor. After overlay mixing and optional 2X upscaling, the HMP8156 upsamples the 4:4:4 data to generate 8:8:8 data. The encoder uses linear interpolation for the upsampling.

Filtering

If enabled, the HMP8156 lowpass filters the Y data to 5.0MHz. Lowpass filtering Y removes any aliasing artifacts due to the upsampling process, and simplifies the analog output filters. The Y 5.0MHz lowpass filter response is shown in Figure 13. At this point, the HMP8156 also scales the Y data to generate the proper output levels for the various video standards

The HMP8156 lowpass filters the Cb and Cr data to 1.3MHz prior to modulation. The lowpass filtering removes any aliasing artifacts due to the upsampling process (simplifying the analog output filters) and also properly bandwidth-limits Cb and Cr prior to modulation. The chrominance filtering is not optional like luminance filtering. The Cb and Cr 1.3MHz lowpass filter response is shown in Figure 14.

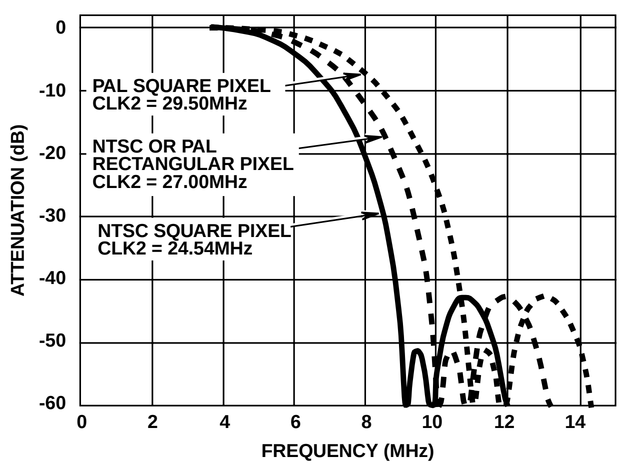


FIGURE 13A. FULL SPECTRUM

FIGURE 13. Y LOWPASS FILTER RESPONSE

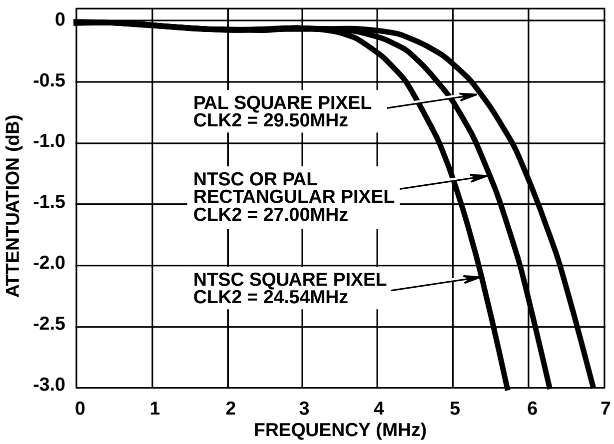


FIGURE 13B. PASS BAND

FIGURE 13. Y LOWPASS FILTER RESPONSE

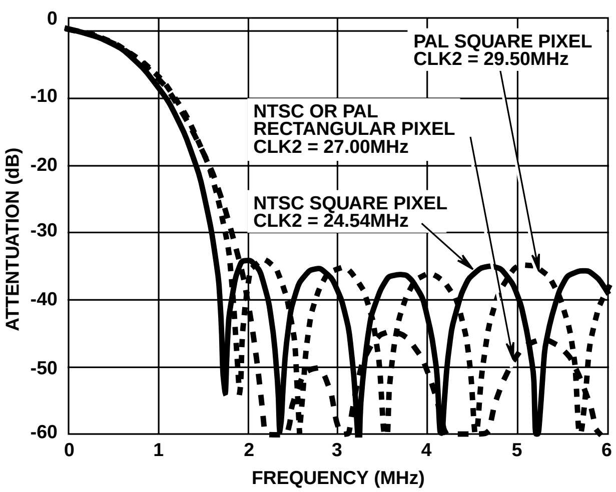


FIGURE 14A. FULL SPECTRUM

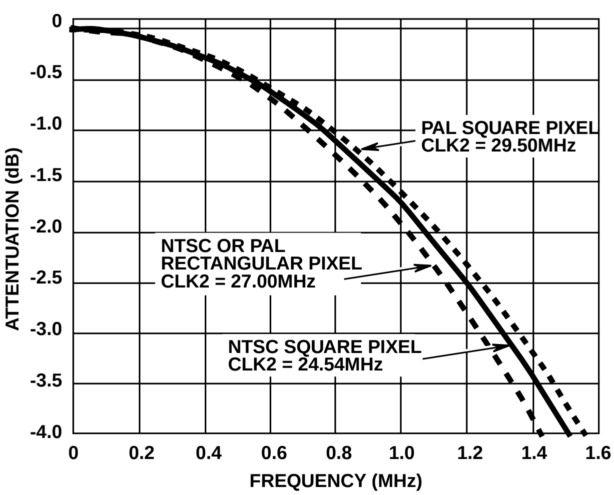


FIGURE 14B. PASS BAND

FIGURE 14. Cb AND Cr LOWPASS FILTER RESPONSE

Chrominance Modulation

The HMP8156 uses a numerically controlled oscillator (NCO) clocked by CLK2 and a sine look up ROM to generate the color subcarrier. The subcarrier from the ROM is pre-scaled to generate the proper levels for the various video standards. Prescaling outside the CbCr data path minimizes color processing artifacts. The HMP8156 modulates the filtered 8:8:8 chrominance data with the synthesized subcarrier.

Subcarrier Phase

The SCH phase is 0º after reset but then changes monotonically over time due to residue in the NCO. In an ideal system, zero SCH phase would be maintained forever. In reality, this is impossible to achieve due to pixel clock frequency tolerances.

If enabled, the HMP8156 resets the NCO periodically to avoid an accumulation of SCH phase error. The reset occurs at the beginning of each field to burst phase sequence. The sequence repeats every 4 fields for NTSC or 8 fields for PAL.

Resetting the SCH phase every four fields (NTSC) or eight fields (PAL) avoids the accumulation of SCH phase error at the expense of requiring any NTSC/PAL decoder after the encoder be able to handle very minor “jumps” (up to 2º) in the SCH phase at the beginning of each four-field or eight-field sequence. Most NTSC/PAL decoders are able to handle this due to video editing requirements.

Composite Video Limiting

The HMP8156 adds the luminance and modulated chrominance together with the sync, color burst, and optional blanking pedestal to form the composite video data. If enabled in the video processing register, the encoder limits the active video so that it is always greater than one-eighth of full scale. This corresponds to approximately one-half the sync height. This allows the generation of “safe” video in the event non-standard YCbCr values are input to the device.

Closed Captioning

If enabled in the auxiliary data control register, the HMP8156 generates closed captioning data on specified scan lines. The captioning data stream includes clock run-in and start bits followed by the captioning data. During closed captioning encoding, the pixel and overlay inputs are ignored on the scan lines containing captioning information.

The HMP8156 has two 16-bit registers containing the captioning information. Each 16-bit register is organized as two cascaded 8-bit registers. One 16-bit register (caption 21) is read out serially during line 18, 21 or 22; the other 16-bit register (caption 284) is read out serially during line 281, 284 or 335. The data registers are shifted out LSB first.

The bytes may be written in any order but both must be written within one frame time for proper operation. If the registers are not updated, the encoder resends the previously loaded values.

The HMP8156 provides a write status bit for each captioning line. The encoder clears the write status bit to '0' when captioning is enabled and both bytes of the captioning data register have been written. The encoder sets the write status bit to '1' after it outputs the data, indicating the registers are ready to receive new data.

Captioning information may be enabled for either line, both lines, or no lines. The captioning modes are summarized in Table 8.

Controlled Edges

The NTSC and PAL video standards specify edge rates and rise and fall times for portions of the video waveform. The HMP8156 automatically implements controlled edge rates and rise and fall times on these edges:

1. Analog horizontal sync (rising and falling edges)
2. Analog vertical sync interval (rising and falling edges)
3. Color burst envelope
4. Blanking of analog active video
5. Overlay with internal mixing
6. Closed captioning information

TABLE 8. CLOSED CAPTIONING MODES

CLOSED CAPTIONING ENABLE BITS	OUTPUT LINE(S)	CAPTIONING REGISTER		WRITE STATUS BIT	
		284A 284B	21A 21B	284	21
00	None	Ignored	Ignored	Always 1	Always 1
01	21 (NTSC) 18 (M PAL) 22 (Other PAL)	Ignored	Caption Data	Always 1	0 = Loaded 1 = Output
10	284 (NTSC) 281 (M PAL) 335 (Other PAL)	Caption Data	Ignored	0 = Loaded 1 = Output	Always 1
11	21, 284 (NTSC) 18, 281 (M PAL) 22, 335 (Other PAL)	Caption Data	Caption Data	0 = Loaded 1 = Output	0 = Loaded 1 = Output

Analog Outputs

The HMP8156 converts the video data into analog signals using four 10-bit DACs running at the CLK2 rate. The DACs output a current proportional to the digital data. The full scale output current is determined by the reference voltage VREF and an external resistor RSET. The full scale output current is given by

$$I_{FULLSCALE}\text{ (mA)} = 3.6 * \text{VREF (V)} / \text{RSET (k}\Omega\text{)} \qquad \text{(EQ 1.)}$$

VREF must be chosen such that it is within the part's operating range; RSET must be chosen such that the maximum output current is not exceeded.

If the VREF pin is not connected, the HMP8156 provides an internal reference voltage. Otherwise, the applied voltage overdrives the internal reference. If an external reference is used, it must decoupled from any power supply noise. An example external reference circuit is shown in the Applications section.

The HMP8156 generates $1V_{PP}$ nominal video signals across 37.5Ω loads corresponding to doubly terminated 75Ω lines. The encoder may also drive larger loads. The full scale output current and load must be chosen such that the maximum output voltage is not exceeded.

Output DAC Filtering

Since the DACs run at 2x the pixel sample rate, the sin(x)/x rolloff of the outputs is greatly reduced, and there are fewer high frequency artifacts in the output spectrum. This allows using simple analog output filters. The analog output filter should be flat to $F_S/4$ and have good rejection at $3F_S/4$. Example filters are shown in the Applications section.

Composite + Y/C Output Mode

The HMP8156 provides three output modes: S-video, RGB, and power down. When S-video outputs are selected, the encoder outputs the luminance, modulated chrominance, and two copies of the composite video signals. All four outputs are time aligned.

To reduce power dissipation, the second composite output DAC may be turned off. The output may be disabled in the host control register.

Composite + RGB Output Mode

When analog RGB video is selected, the HMP8156 transforms the filtered 8:8:8 YCbCr data into 8:8:8 RGB data. The transform matrix uses fixed coefficients to generate PAL video levels for interfacing to a European SCART connector. The encoder will not generate proper video levels if RGB output is selected with NTSC format.

The analog RGB outputs have a range of 0.3-1.0V with no blanking pedestal. Composite sync information (0.0-0.3V) may be optionally added to the green output. Closed captioning data is not included on the RGB outputs.

The HMP8156 also generates composite video when in RGB output mode. The analog composite video is output onto the NTSC/PAL 1 pin. Red information is output onto the NTSC/PAL 2 pin, blue information is output onto the C pin, and green information is output onto the Y pin. All four outputs are time aligned.

Power Down Mode

When the power down mode is enabled, all of the DACs are powered down (forcing their outputs to zero) and most of the internal clocks are stopped. The host processor may still read from and write to the internal control registers.

Host Interfaces

Reset

The HMP8156 resets to its default operating mode on power up, when the reset pin is asserted for at least four CLK cycles, or when the software reset bit of the host control register is set. During the reset cycle, the encoder returns its internal registers to their reset state and deactivates the I^2C interface.

I^2C Interface

The HMP8156 provides a standard I^2C interface and supports fast-mode (up to 400 KBPS) transfers. The device acts as a slave for receiving and transmitting data only. It will not respond to general calls or initiate a transfer. The encoder's slave address is either 0100 $000x_B$ when the SA input pin is low or 0100 $001x_B$ when it is high. (The 'x' bit in the address is the I^2C read flag.)

The I^2C interface consists of the SDA and SCL pins. When the interface is not active, SCL and SDA must be pulled high using external 4-6kΩ pull-up resistors. The I^2C clock and data timing is shown in Figures 15 and 16.

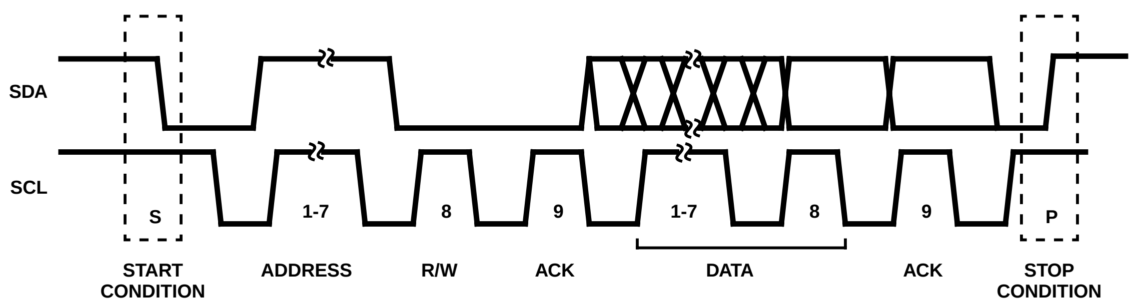


FIGURE 15. I^2C SERIAL TIMING FLOW

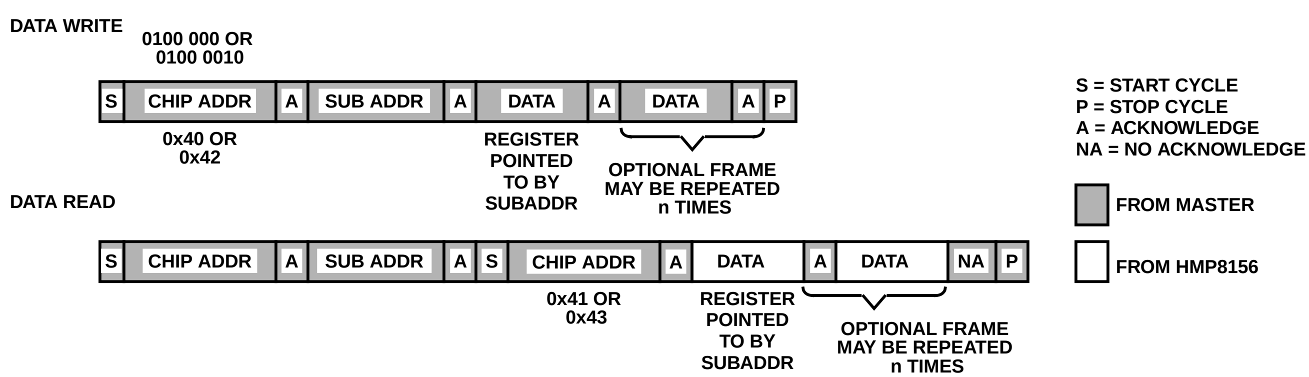


FIGURE 16. REGISTER WRITE PROGRAMMING FLOW

During I^2C write cycles, the first data byte after the slave address specifies the sub address, and is written into the address register. Only the seven LSBs of the subaddress are used; the MSB is ignored. Any remaining data bytes in the I^2C write cycle are written to the control registers, beginning with the register specified by the address register. The 7-bit address register is incremented after each data byte in the I^2C write cycle. Data written to reserved bits within registers or reserved registers is ignored.

During I^2C read cycles, data from the control register specified by the address register is output. The address register is incremented after each data byte in the I^2C read cycle. Reserved bits within registers return a value of “0”. Reserved registers return a value of $00_{H.}$

The HMP8156’s operating modes are determined by the contents of its internal registers which are accessed via the I^2C interface. All internal registers may be written or read by the host processor at any time. However, some of the bits and words are read only or reserved and data written to these bits is ignored.

Table 9 lists the HMP8156’s internal registers. Their bit descriptions are listed in Tables 10-27.

TABLE 9. CONTROL REGISTER NAMES

SUB ADDRESS (HEX)	CONTROL REGISTER	RESET CONDITION
00	Product ID	56_H
01	Output Format	00_H
02	Input Format	06_H
03	Video Processing	$A0_H$
04	Timing I/O 1	00_H
05	Timing I/O 2	00_H
06	Aux Data Enable	00_H
07-0E	Reserved	-
0F	Host Control	18_H
10	Closed Caption_21A	80_H
11	Closed Caption_21B	80_H
12	Closed Caption_284A	80_H
13	Closed Caption_284B	80_H
14-1F	Reserved	-
20	Start H_Blank Low	$4A_H$
21	Start H_Blank High	03_H
22	End H_Blank	$7A_H$
23	Start V_Blank Low	03_H
24	Start V_Blank High	01_H
25	End V_Blank	13_H
26-2F	Reserved	-
30-7F	Test and Unused	-

TABLE 10. PRODUCT ID REGISTER

SUB ADDRESS = 00_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Product ID	This 8-bit register specifies the last two digits of the product number. It is a read-only register. Data written to it is ignored.	56_H

TABLE 11. OUTPUT FORMAT REGISTER

SUB ADDRESS = 01_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Video Timing Standard	000 = (M) NTSC 001 = (M) NTSC with a 0 IRE setup; also called (NSM) NTSC 010 = (B, D, G, H, I) PAL 011 = (M) PAL 100 = (N) PAL 101 = combination (N) PAL; also called (CN) PAL 110 = reserved 111 = reserved	000_B
4-3	Output Format	These bits must be set to “00” during (M, NSM) NTSC and (M, N, CN) PAL modes. 00 = Composite + Y/C 01 = reserved 10 = Composite + RGB (no sync on green) 11 = Composite + RGB (with sync on green)	00_B
2-0	Reserved		000_B

TABLE 12. INPUT FORMAT REGISTER

SUB ADDRESS = 02_H			
BIT NUMBER	FUNCTION	DESCRIPTION	RESET STATE
7-5	Input Format	000 = 16-bit 4:2:2 YCbCr 001 = 8-bit 4:2:2 YCbCr 010 = 8-bit parallel ITU-R BT.656 011 = 16-bit linear RGB 100 = 16-bit gamma-corrected RGB 101 = 24-bit linear RGB 110 = 24-bit gamma-corrected RGB 111 = Blue screen	000_B
4	Gamma Select	These bits are ignored except during linear RGB input modes. 0 = 1 / 2.2 1 = 1 / 2.8	0_B
3	Reserved		0_B
2-1	Overlay Mixing Mode	These bits must be set to “11” in 24-bit RGB input modes. Internal mixing should not be selected in BT.656 input mode. 00 = No mixing 01 = Internal mixing 10 = External mixing 11 = Disable overlays	11_B
0	Input Resolution	This bit must be set to “0” during BT.656 input mode. 0 = Full resolution (2x upscaling disabled) 1 = SIF resolution (2x upscaling enabled)	0_B

TABLE 13. VIDEO PROCESSING REGISTER

SUB ADDRESS = 03_H			
BIT NUMBER	FUNCTION	DESCRIPTION	RESET STATE
7	Luminance Processing	0 = None 1 = Y Lowpass filtering enabled	1_B
6	Composite Video Limiting	0 = None 1 = Lower limit of composite active video is about half the sync height	0_B
5	SCH Phase Mode	0 = Never reset SCH phase 1 = Reset SCH phase every 4 (NTSC) or 8 (PAL) fields	1_B
4-0	Reserved		00000_B

TABLE 14. TIMING I/O REGISTER #1

SUB ADDRESS = 04_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	$\overline{\text{BLANK}}$ Timing Select	This bit is ignored unless $\overline{\text{BLANK}}$ is configured to be an output. 0 = Data for the first active pixel of the scan line must arrive the CLK cycle after the encoder negates $\overline{\text{BLANK}}$. 1 = Data for the first active pixel of the scan line must arrive immediately after the encoder negates $\overline{\text{BLANK}}$.	0_B
6	Reserved		0_B
5	$\overline{\text{BLANK}}$ Output Control	0 = $\overline{\text{BLANK}}$ is an input 1 = $\overline{\text{BLANK}}$ is an output	0_B
4	$\overline{\text{BLANK}}$ Polarity	0 = Active low (low during blanking) 1 = Active high (high during blanking)	0_B
3	$\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ Output Control	0 = $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are inputs 1 = $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ are outputs	0_B
2	$\overline{\text{HSYNC}}$ Polarity	0 = Active low (low during horizontal sync) 1 = Active high (high during horizontal sync)	0_B
1	$\overline{\text{VSYNC}}$ Polarity	0 = Active low (low during vertical sync) 1 = Active high (high during vertical sync)	0_B
0	FIELD Polarity	0 = Active low (low during odd fields) 1 = Active high (high during odd fields)	0_B

TABLE 15. TIMING I/O REGISTER #2

SUB ADDRESS = 05_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Reserved		000_B
4	CLK Output Control	0 = CLK is an input 1 = CLK is an output	0_B
3	Aspect Ratio Mode	This bit must be set to “0” during BT.656 input mode. 0 = Rectangular (BT.601) pixels 1 = Square pixels	0_B
2-0	Reserved		00_B

TABLE 16. AUXILIARY DATA ENABLE REGISTER

SUB ADDRESS = 06_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Closed Captioning Enable	00 = Closed caption disabled 01 = Closed caption enabled for odd fields: line 21 for NTSC, line 18 for (M) PAL, or line 22 for (B, D, G, H, I, N, CN) PAL 10 = Closed caption enabled for even fields: line 284 for NTSC, line 281 for (M) PAL, or line 335 for (B, D, G, H, I, N, CN) PAL 11 = Closed caption enabled for both odd and even fields	00_B
5-0	Reserved		000000_B

TABLE 17. HOST CONTROL REGISTER

SUB ADDRESS = $0F_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Software Reset	Setting this bit to “1” initiates a software reset. It is automatically reset to a “0” after the reset sequence is complete.	0_B
6	Power Down Enable	0 = Normal operation 1 = Power down mode	0_B
5	NTSC/PAL 2 Output Mode	0 = Enabled 1 = Disabled	0_B
4	Closed Caption Line 21 Write Status	0 = Caption_21A and Caption_21B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1_B
3	Closed Caption Line 284 Write Status	0 = Caption_284A and Caption_284B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1_B
2-0	Reserved		000_B

TABLE 18. CLOSED CAPTION_21A DATA REGISTER

SUB ADDRESS = 10_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 21 Caption Data (First Byte)	This register is cascaded with the closed caption_21B data register and they are read out serially as 16 bits during line 18, 21, or 22 if line 21 captioning is enabled. Bit D0 of the 21A data register is shifted out first.	80_H

TABLE 19. CLOSED CAPTION_21B DATA REGISTER

SUB ADDRESS = 11_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 21 Caption Data (Second Byte)	This register is cascaded with the closed caption_21A data register and they are read out serially as 16 bits during line 18, 21, or 22 if line 21 captioning is enabled. Bit D0 of the 21A data register is shifted out first.	80_H

TABLE 20. CLOSED CAPTION_284A DATA REGISTER

SUB ADDRESS = 12_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 284 Caption Data (First Byte)	This register is cascaded with the closed caption_284B data register and they are read out serially as 16 bits during line 281, 284, or 335 if line 284 captioning is enabled. Bit D0 of the 284A data register is shifted out first.	80_H

TABLE 21. CLOSED CAPTION_284B DATA REGISTER

SUB ADDRESS = 13_H			
BIT NUMBER	FUNCTION	DESCRIPTION	RESET STATE
7-0	Line 284 Caption Data (Second Byte)	This register is cascaded with the closed caption_284A data register and they are read out serially as 16 bits during line 281, 284, or 335 if line 284 captioning is enabled. Bit D0 of the 284A data register is shifted out first.	80_H

TABLE 22. START H_BLANK LOW REGISTER

SUB ADDRESS = 20_H			
BIT NUMBER	FUNCTION	DESCRIPTION	RESET STATE
7-0	Assert $\overline{\text{BLANK}}$ Output Signal (Horizontal)	This 8-bit register is cascaded with Start H_Blank High Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1x clock cycles) at which to start ignoring pixel data each scan line. The leading edge of $\overline{\text{HSYNC}}$ is count 020_H. This register is ignored unless $\overline{\text{BLANK}}$ is configured as an output.	$4A_H$

TABLE 23. START H_BLANK HIGH REGISTER

SUB ADDRESS = 21_H			
BIT NUMBER	FUNCTION	DESCRIPTION	RESET STATE
7-2	Reserved		000000_B
1-0	Assert $\overline{\text{BLANK}}$ Output Signal (Horizontal)	This 2-bit register is cascaded with Start H_Blank Low Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1x clock cycles) at which to start ignoring pixel data each scan line. The leading edge of $\overline{\text{HSYNC}}$ is count 020_H. This register is ignored unless $\overline{\text{BLANK}}$ is configured as an output.	11_B

TABLE 24. END H_BLANK REGISTER

SUB ADDRESS = 22_H			
BIT NUMBER	FUNCTION	DESCRIPTION	RESET STATE
7-0	Negate $\overline{\text{BLANK}}$ Output Signal (Horizontal)	This 8-bit register specifies the horizontal count (in 1x clock cycles) at which to start inputting pixel data each scan line. The leading edge of $\overline{\text{HSYNC}}$ is count 000_H. This register is ignored unless $\overline{\text{BLANK}}$ is configured as an output.	$7A_H$

TABLE 25. START V_BLANK LOW REGISTER

SUB ADDRESS = 23_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{\text{BLANK}}$ Output Signal (Vertical)	This 8-bit register is cascaded with Start V_Blank High Register to form a 9-bit start_vertical_blank register. During normal operation, it specifies the line number (n) to start ignoring pixel input data (and what line number to start blanking the output video) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). During SIF input mode, the register value (n) specifies the line number to start ignoring pixel input data each noninterlaced input frame. The output video will be blanked starting on line number (n) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). The leading edge of $\overline{\text{VSYNC}}$ at the start of an odd field is count 000_H (note that this does not follow standard NTSC or PAL line numbering). This register is ignored unless $\overline{\text{BLANK}}$ is configured as an output.	03_H

TABLE 26. START V_BLANK HIGH REGISTER

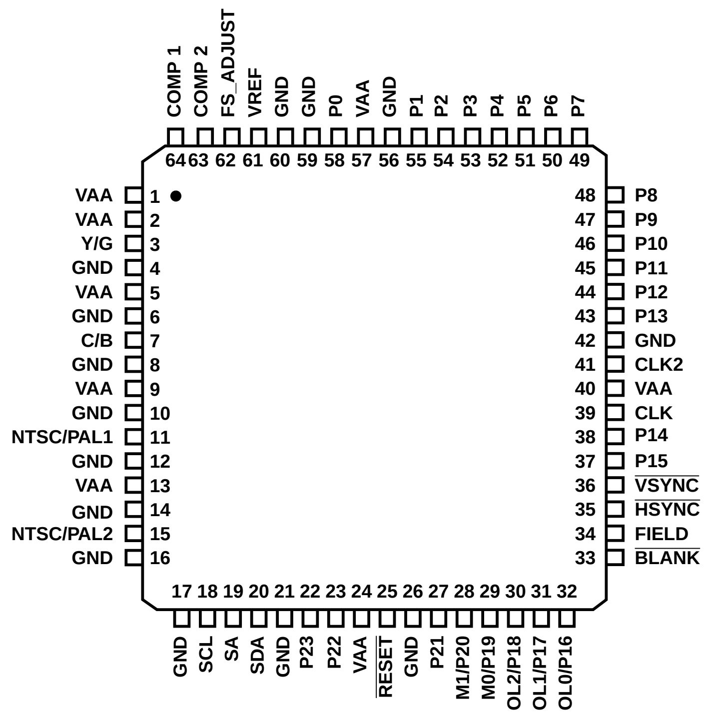
SUB ADDRESS = 24_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-1	Reserved		0000000_B
0	Assert $\overline{\text{BLANK}}$ Output Signal (Vertical)	This 1-bit register is cascaded with Start V_Blank Low Register to form a 9-bit start_vertical_blank register. This register is ignored unless $\overline{\text{BLANK}}$ is configured as an output.	1_B

TABLE 27. END V_BLANK REGISTER

SUB ADDRESS = 25_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{\text{BLANK}}$ Output Signal (Vertical)	During normal operation, this 8-bit register specifies the line number (n) to start inputting pixel input data (and what line number to start generating active output video) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). During SIF input mode, the register value (n) specifies the line number to start inputting pixel input data each noninterlaced input frame. The output video will be active starting on line number (n) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). The leading edge of $\overline{\text{VSYNC}}$ at the start of an odd field is count 000_H (note that this does not follow standard NTSC or PAL line numbering). This register is ignored unless $\overline{\text{BLANK}}$ is configured as an output.	13_H

Pinout

HMP8156
(PQFP)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
P0-P15	58, 55-43, 38, 37	I	Pixel input pins. See Table 1.
P16-P23	32-27, 23, 22	I	Overlay or pixel inputs. See Table 1.
FIELD	34	O	FIELD output. The field output indicates that the encoder is outputting the odd or even video field. The polarity of FIELD is programmable.
HSYNC	35	I/O	Horizontal sync input/output. As an input, this pin must be asserted during the horizontal sync intervals. If it occurs early, the line time will be shortened. If it occurs late, the line time will be lengthen by holding the outputs at the front porch level. As an output, it is asserted during the horizontal sync intervals. The polarity of HSYNC is programmable.
VSYNC	36	I/O	Vertical sync input/output. As an input, this pin must be asserted during the vertical sync intervals. If it occurs early, the field time will be shortened. If it occurs late, the field time will be lengthened by holding the outputs at the blanking level. As an output, it is asserted during the vertical sync intervals. The polarity of VSYNC is programmable.
BLANK	33	I/O	Composite blanking input/output. As an input, this pin must be asserted during the horizontal and vertical blanking intervals. As an output, it is asserted during the horizontal and vertical blanking intervals. The polarity of BLANK is programmable.
CLK	39	I/O	1x pixel clock input/output. As an input, this clock must be free-running and synchronous to the clock signal on the CLK2 pin. As an output, this pin may drive a maximum of one LS TTL load. CLK is generated by dividing CLK2 by two or four, depending on the mode.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
CLK2	41	I	2x pixel clock input. This clock must be a continuous, free-running clock.
SCL	18	I	I^2C interface clock input.
SA	19	I	I^2C interface address select input.
SDA	20	I/O	I^2C interface data input/output. The circuit for this pin should include a 4-6kΩ pull up resistor connected to VAA.
$\overline{\text{RESET}}$	25	I	Reset control input. A logical zero for a minimum of four CLK cycles resets the device. $\overline{\text{RESET}}$ must be a logical one for normal operation.
Y (G)	3	O	Luminance analog current output. This output contains luminance video, sync, blanking, and closed captioning information. In analog RGB output mode, green analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
C (B)	7	O	Chrominance analog current output. This output contains chrominance video, and blanking information. In analog RGB output mode, blue analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
NTSC/PAL 1	11	O	Composite video analog current output. This output contains composite video, sync, blanking, and closed captioning information. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
NTSC/PAL 2 (R)	15	O	Composite video analog current output. This output contains composite video, sync, blanking, and closed captioning information. In analog RGB output mode, red analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
VREF	61	I	Voltage reference input. An optional external 1.235V reference may be used to drive this pin. If left floating, the internal voltage reference is used.
FS_ADJUST	62		Full scale adjust control. A resistor (RSET) connected between this pin and GND sets the full-scale output current of each of the DACs.
COMP 1	64		Compensation pin. A 0.1µF ceramic chip capacitor should be connected between this pin and VAA, as close to the device as possible.
COMP 2	63		Compensation pin. A 0.1µF ceramic chip capacitor should be connected between this pin and VAA, as close to the device as possible.
VAA			+5V power. A 0.1µF ceramic capacitor, in parallel with a 0.01µF chip capacitor, should be used between each group of VAA pins and GND. These should be as close to the device as possible.
GND			Ground

Absolute Maximum Ratings

V_{AA} . . . . . +6V
All Signal Pins . . . . . -0.5V to +6V
Analog Output Short Circuit Duration . . . . . Indefinite
Input Current, All Pins 1mA
Vapor Phase Soldering, 1 Minute . . . . . 220^{o}C

Operating Conditions

Temperature Range . . . . . 0^{o}C to 70^{o}C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ^{o}C/W
PQFP Package 47
Maximum Junction Temperature . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(PQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{AA} = +5V ±5%, RSET = 124Ω, VREF_IN = 1.225V, Unless otherwise specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DC PARAMETERS, DIGITAL INPUTS EXCEPT CLK2, SDA, SCL					
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0.4V	-	-	-1	μ A
Input Logic High Current, I_{IH}	V_{IN} = 2.4V	-	-	1	μ A
Input Capacitance, C_{IN}		-	5	-	pF
DC PARAMETERS, CLK2 INPUT					
Input Logic Low Voltage, V_{IL}		-	-	0.3 x V_{AA}	V
Input Logic High Voltage, V_{IH}		0.7 x V_{AA}	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0.5V	-	-	-10	m A
Input Logic High Current, I_{IH}	V_{IN} = V_{AA} -0.5V	-	-	10	m A
Input Capacitance, C_{IN}		-	5	-	pF
DC PARAMETERS, SDA AND SCL INPUTS					
Input Logic Low Voltage, V_{IL}		-	-	0.3 x V_{AA}	V
Input Logic High Voltage, V_{IH}		0.7 x V_{AA}	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0.5V	-	-	-1	m A
Input Logic High Current, I_{IH}	V_{IN} = V_{AA} -0.5V	-	-	1	m A
Input Capacitance, C_{IN}		-	5	-	pF
DC PARAMETERS, DIGITAL OUTPUTS					
Output Logic Low Voltage, V_{IL}	I_{OL} = 2mA	-	-	0.4	V
Output Logic High Voltage, V_{IH}	I_{OH} = -2mA	2.4	-	-	V
Output Capacitance, C_{OUT}		-	5	-	pF
DC PARAMETERS, ANALOG OUTPUTS					
DAC Resolution		10	10	10	Bits
Integral Nonlinearity, INL		-	2	-	LSB
Differential Nonlinearity, DNL		-	0.5	-	LSB

Electrical Specifications V_{AA} = +5V ±5%, RSET = 124Ω, VREF_IN = 1.225V, Unless otherwise specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Current		-	-	34.8	mA
Output Impedance		-	100K	-	Ohms
Output Capacitance	I_{OUT} = 0mA, CLK = 13.5MHz	-	25	-	pF
Output Compliance Range		0	-	1.4	V
Video Level Error Internal Voltage Reference External Voltage Reference	Note 2	-	-	± 10 ±5	% %
DAC to DAC Matching		-	-	5	%
VREF Output Voltage	Pin not driven, using internal reference	1.13	1.225	1.32	V
VREF Output Current	Pin not driven, using internal reference	-50	-	50	µA
VREF Input Voltage	Pin connected to external reference shown in Figure 32	1.112	1.235	1.358	V
VREF Input Current	Pin connected to external reference shown in Figure 32	-500	-	500	µA
AC PARAMETERS, ANALOG OUTPUTS					
Differential Gain Error	Using analog output filter shown in Figure 33A.	-	1	-	%
Differential Phase Error		-	1	-	Degree
SNR (Weighted)		-	70	-	dB
Hue Accuracy		-	2	-	Degree
Color Saturation Accuracy		-	2	-	%
Luminance Nonlinearity		-	1	-	%
Residual Subcarrier		-	-60	-	dB
SCH Phase	SCH Phase Reset enabled	-1.5	0	1.5	Degree
Analog Output Skew, T_{ASK}		-	-	5	ns
Analog Output Delay, T_{AD}		-	-	12	ns
DAC-DAC Crosstalk		-	-60	-	dB
Glitch Energy	Using analog output filter shown in Figure 33A. Includes clock and data feedthrough	-	35	-	pV-s
AC PARAMETERS, PIXEL INTERFACE - INPUTS					
Pixel Setup Time, T_S		6	-	-	ns
Pixel Hold Time, T_H		0	-	-	ns
Control Setup Time, T_S		6	-	-	ns
Control Hold Time, T_H		0	-	-	ns
CLK Frequency		-	-	14.75	MHz
CLK High Time, CLK_H		27.1	-	40.7	ns
CLK Low Time, CLK_L		27.1	-	40.7	ns
CLK2 Frequency		-	-	29.5	MHz

Electrical Specifications V_{AA} = +5V ±5%, RSET = 124Ω, VREF_IN = 1.225V, Unless otherwise specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
CLK2 High Time, $CLK2_H$		13.6	-	20.3	ns
CLK2 Low Time, $CLK2_L$		13.6	-	20.3	ns
CLK to CLK2 Setup Time, CLK_{SU}		6	-	-	ns
CLK to CLK2 Hold Time, CLK_H		0	-	-	ns
AC PARAMETERS, PIXEL INTERFACE - OUTPUTS					
Control Output Delay, T_D		3	-	12	ns
CLK2 to CLK Output Delay, CLK_D		0	-	12	ns
AC PARAMETERS, I^2C INTERFACE					
All AC and DC parameters meet the fast-mode I^2C Bus Interface specification.					
RESET* Pulse Width Low, T_{RES}		4	-	-	CLK Cycles
POWER SUPPLY CHARACTERISTICS					
DAC PSRR at DC	Note 4	-	50	-	dB
Power Supply Range, V_{AA}		4.75	5.0	5.25	V
Normal Supply Current, I_{AA}		-	-	260	mA
Power-Down Supply Current, I_{AA}	Note 3	-	-	750	µA
Power Dissipation		-	1100	1300	mW

NOTES:

2. Output level is dependent on the voltage on VREF, the value of RSET, and the load.
3. If using an external voltage reference, it is not powered down. The internal voltage reference is always powered down.
4. The supply voltage rejection is the relative variation of the full-scale output driving a 37.5Ω load for a ±0.5% supply variation: PSRR = 20 x log ($\Delta V_{AA}/\Delta V_{OUT}$).

Typical Performance Curves

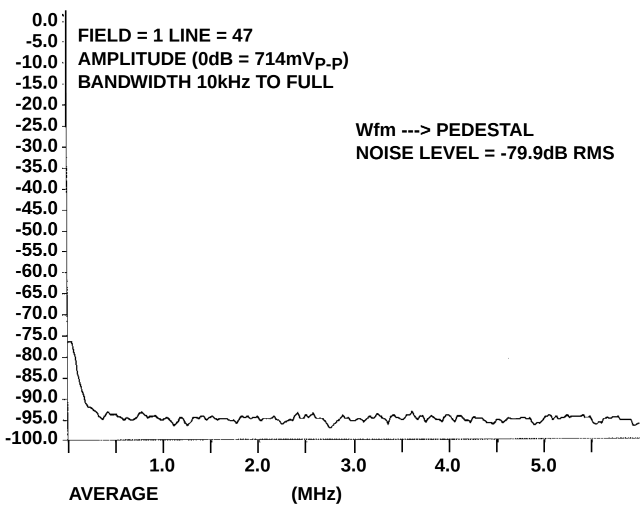


FIGURE 17. NOISE SPECTRUM (NTSC)

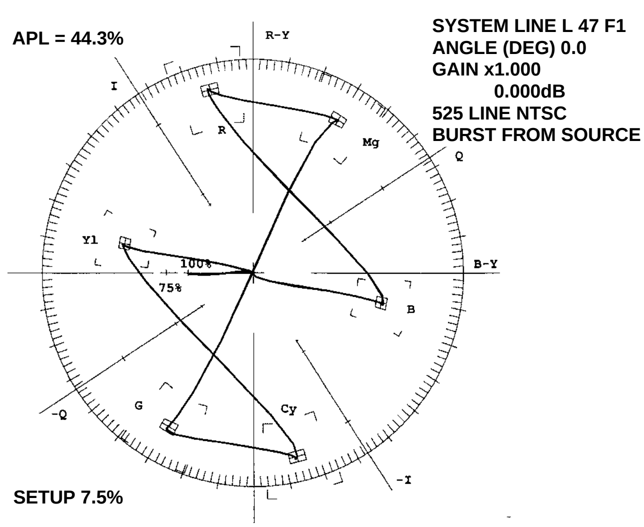


FIGURE 18. NTSC COLOR BAR VECTOR SCOPE PLOT

Typical Performance Curves (Continued)

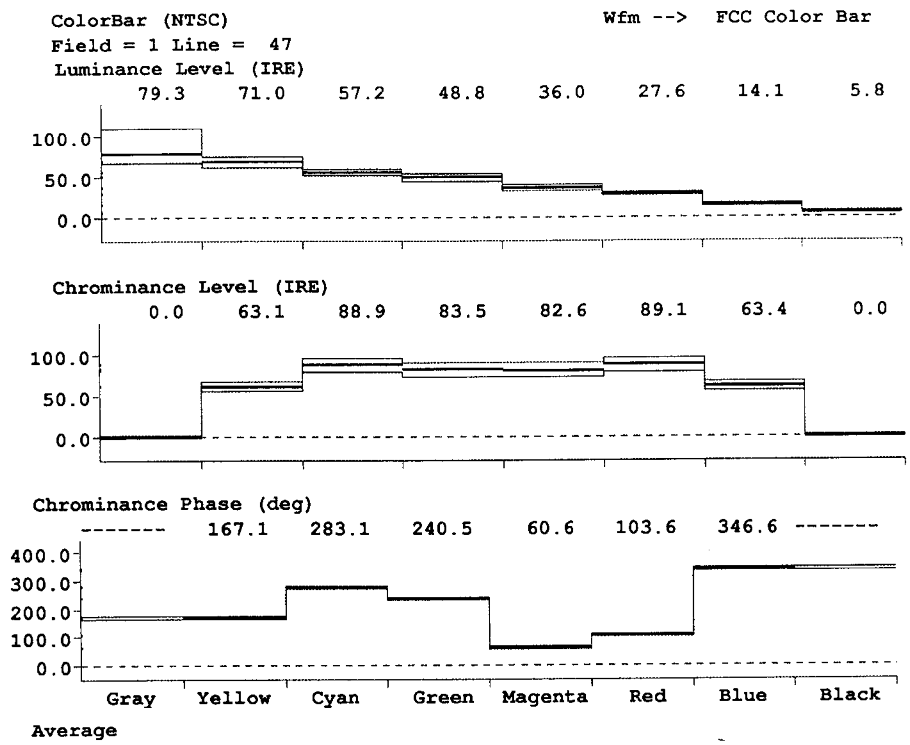


FIGURE 19. NTSC FCC COLOR BAR

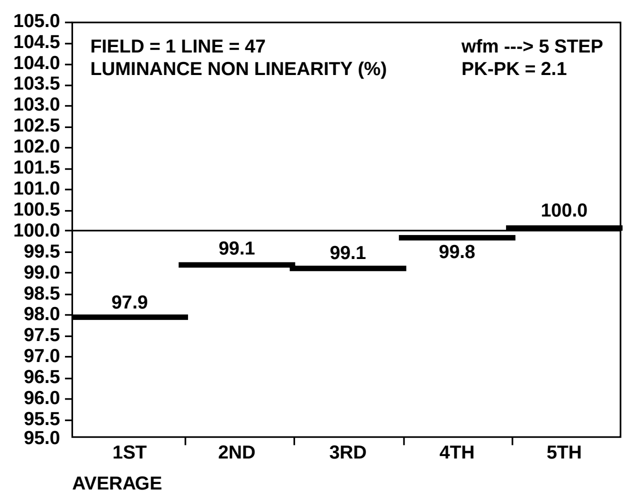


FIGURE 20. LUMINANCE NON LINEARITY (NTSC)

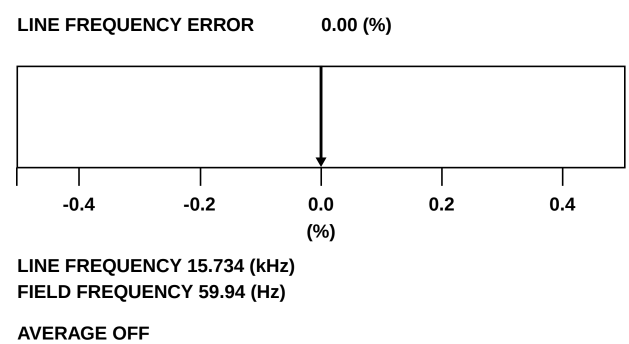


FIGURE 21. LINE FREQUENCY (NTSC)

Typical Performance Curves (Continued)

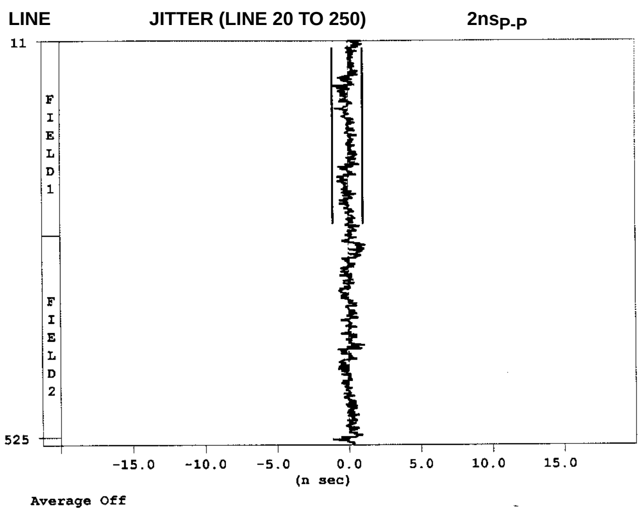


FIGURE 22. H SYNC JITTER IN A FRAME (NTSC)

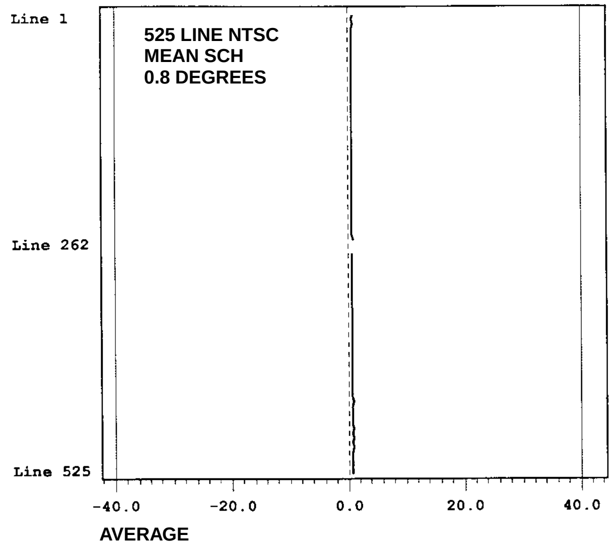


FIGURE 23. SCH PHASE MEASUREMENT

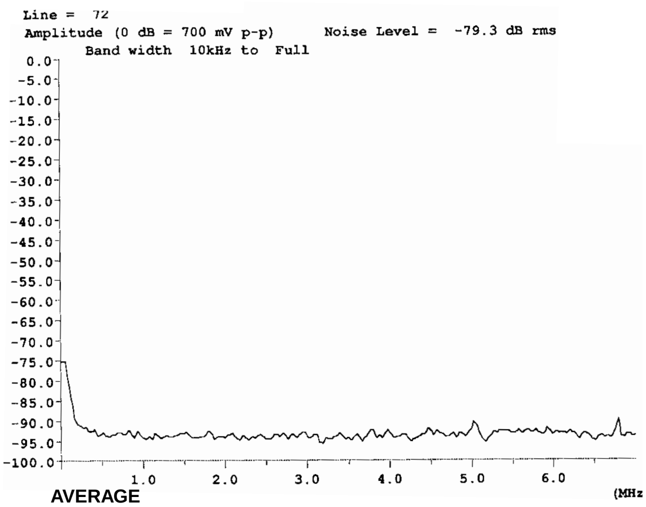


FIGURE 24. NOISE SPECTRUM (PAL)

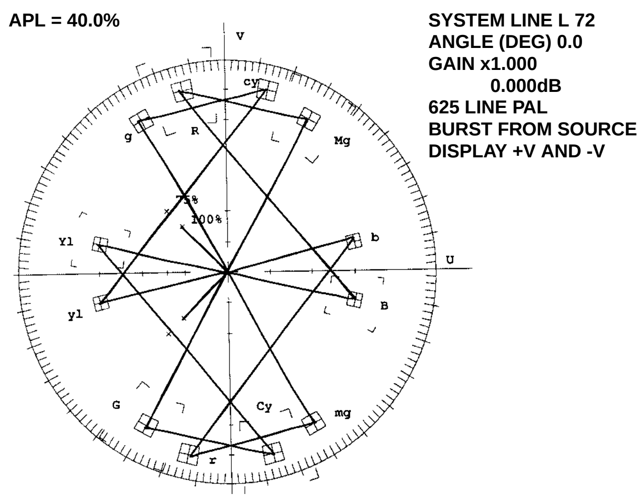


FIGURE 25. PAL COLOR BAR VECTOR SCAPE PLOT

Typical Performance Curves (Continued)

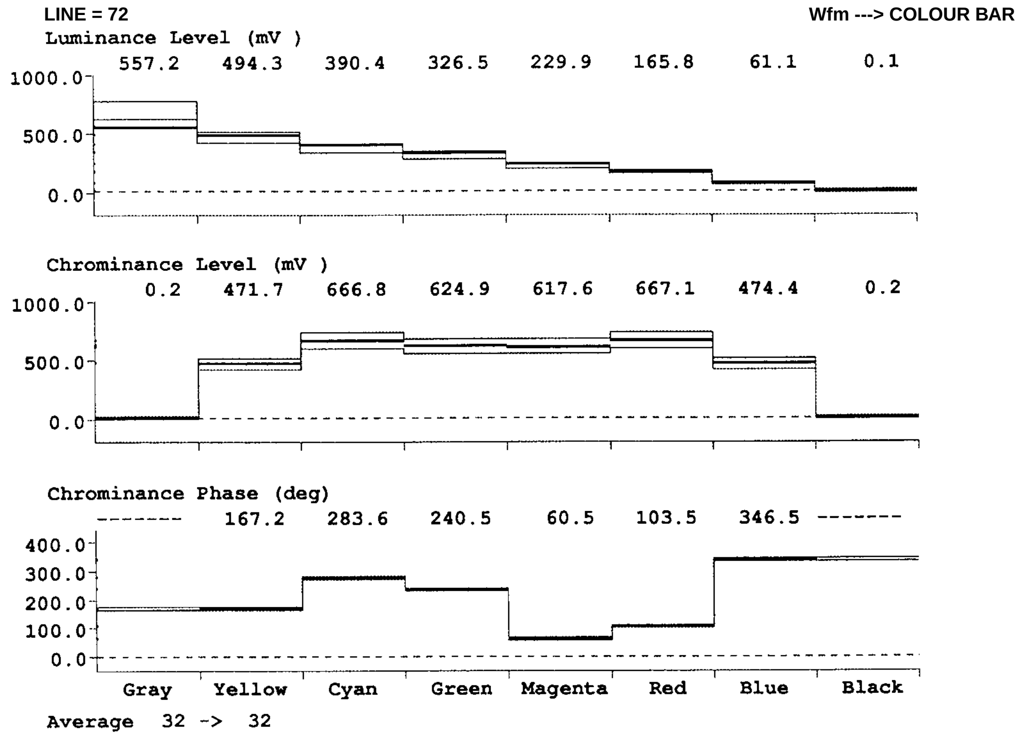


FIGURE 26. COLOURBAR (PAL)

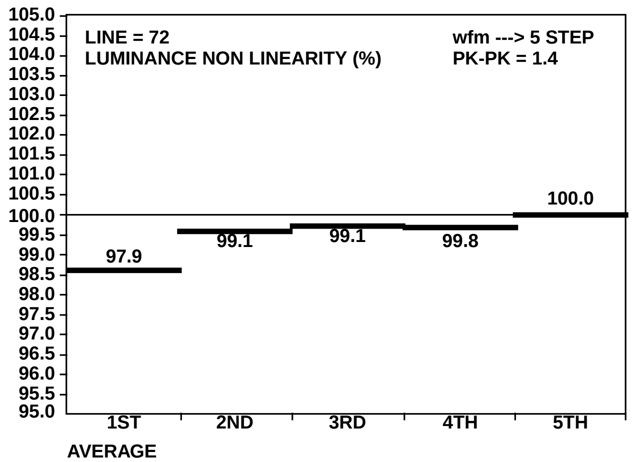


FIGURE 27. LUMINANCE NON LINEARITY (PAL)

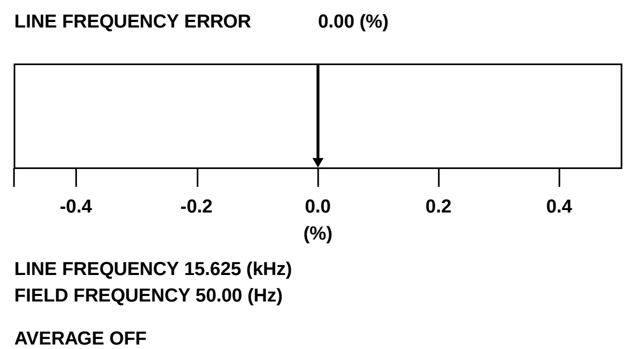


FIGURE 28. LINE FREQUENCY (PAL)

Typical Performance Curves (Continued)

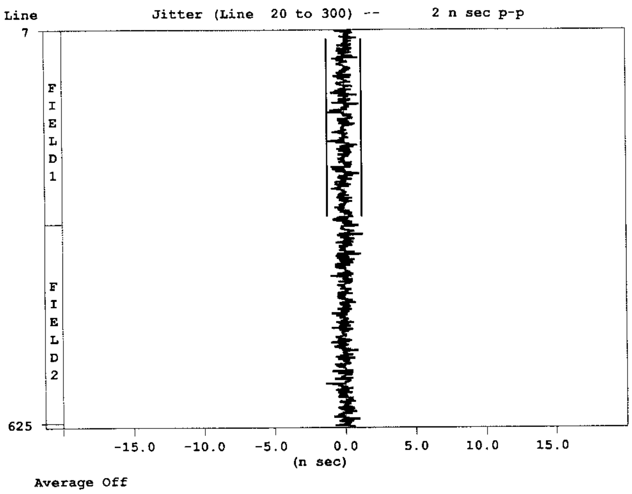


FIGURE 29. H SYNC JITTER IN A FRAME (PAL)

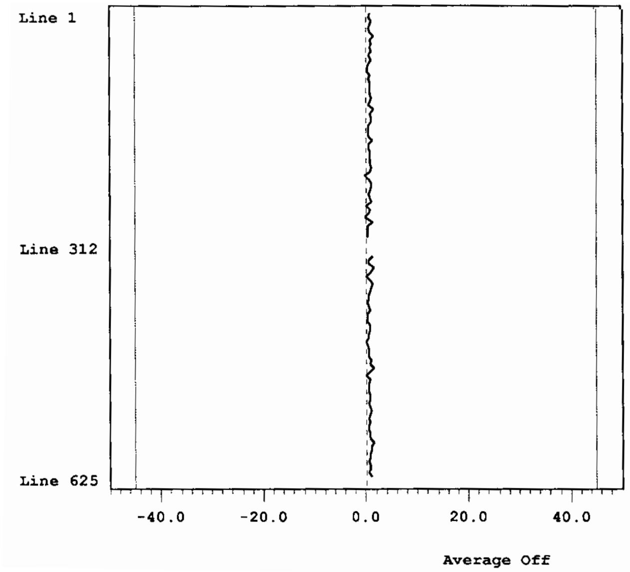


FIGURE 30. SCH PHASE MEASUREMENT

Applications Information

PAL Teletext

Teletext encoding may be implemented on any line by driving the pixel inputs with appropriate data. For YCbCr input modes, Cb and Cr should equal 128 to disable the color information. For RGB input modes, R, G, and B should always have the same value to disable the color information.

Vertical blanking must be negated on the first scan line containing teletext information. If there are unused scan lines between teletext data and active video, $\overline{\text{BLANK}}$ must remain off and the pixel inputs should be set to the black level.

Video Test Signals

Video test signals may be generated by driving the pixel inputs with appropriate data. Most of the video test signals require using YCbCr pixel data.

Vertical blanking must be negated on the first scan line containing video test signals. If there are unused scan lines between test signal data and active video, $\overline{\text{BLANK}}$ must remain off and the pixel inputs should be set to the black level.

PCB Considerations

A PCB board with a minimum of 4 layers is recommended, with layers 1 and 4 (top and bottom) for signals and layers 2 and 3 for power and ground. The PCB layout should implement the lowest possible noise on the power and ground planes by providing excellent decoupling. PCB trace lengths between groups of V_{AA} and GND pins should be as short as possible.

Component Placement

The optimum layout places the HMP8156 at the edge of the PCB and as close as possible to the video output connector. External components should be positioned as close as possible to the appropriate pin, ideally such that traces can be connected point to point. Chip capacitors are recommended where possible, with radial lead ceramic capacitors the second-best choice.

Traces containing digital signals should not be routed over, under, or adjacent to the analog output traces to minimize crosstalk. If this is not possible, coupling can be minimized by routing the digital signals at a 90 degree angle to the analog signals. The analog output traces should also not overlay the HMP8156 and V_{CC} power planes to maximize high-frequency power supply rejection.

Power and Ground Planes

A common ground plane for all devices, including the HMP8156, is recommended. However, placing the encoder on an electrically connected GND peninsula reduces noise levels. All GND pins on the HMP8156 must be connected to the ground plane. Typical power and ground planes are shown in Figure 31.

The HMP8156 should have its own power plane that is isolated from the common power plane of the board, with a gap between the two power planes of at least 1/8 inch. All V_{AA} pins of the HMP8156 must be connected to this HMP8156 power plane.

The HMP8156 power plane should be connected to the board's normal V_{CC} power plane at a single point though a low-resistance ferrite bead, such as a Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001. The ferrite bead provides resistance to switching currents, improving the performance of HMP8156. A single, large capacitor should also be used between the HMP8156 power plane and the ground plane to control low-frequency power supply ripple.

For proper operation, power supply decoupling is required. It should be done using a 0.1μF ceramic capacitor in parallel with a 0.01μF chip capacitor for each group of V_{AA} pins to ground. These capacitors should be located as close to the V_{AA} and GND pins as possible, using short, wide traces.

If a separate linear regulator is used to provide power to the HMP8156 power plane, the power-up sequence should be designed to ensure latchup will not occur. A separate linear regulator is recommended if the power supply noise on the V_{AA} pins exceeds 200mV. About 10% of the noise (that is less than 1MHz) on the V_{AA} pins will couple onto the analog outputs.

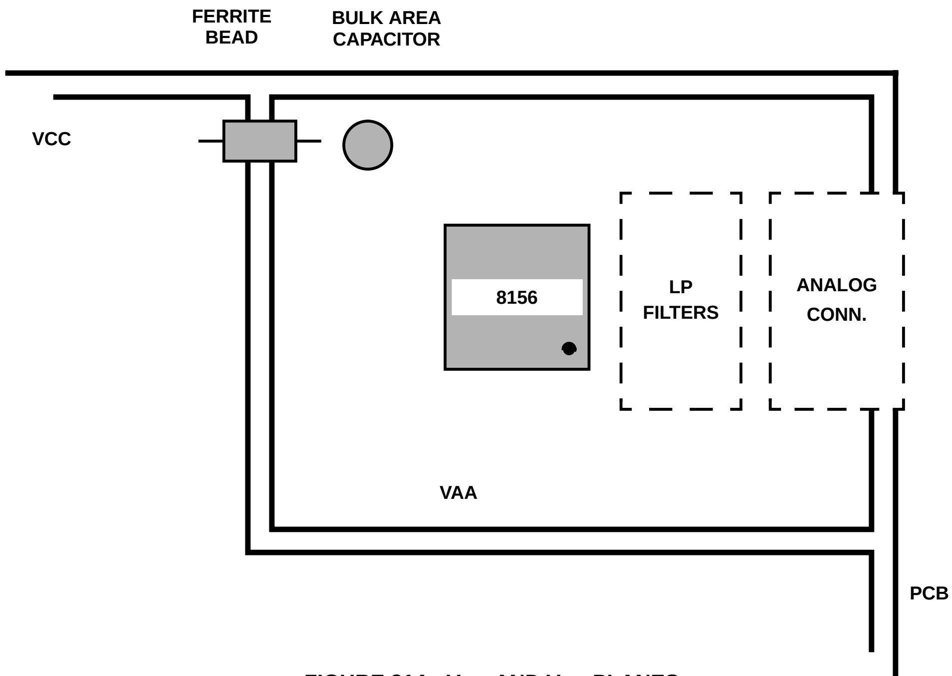


FIGURE 31A. V_{CC} AND V_{AA} PLANES

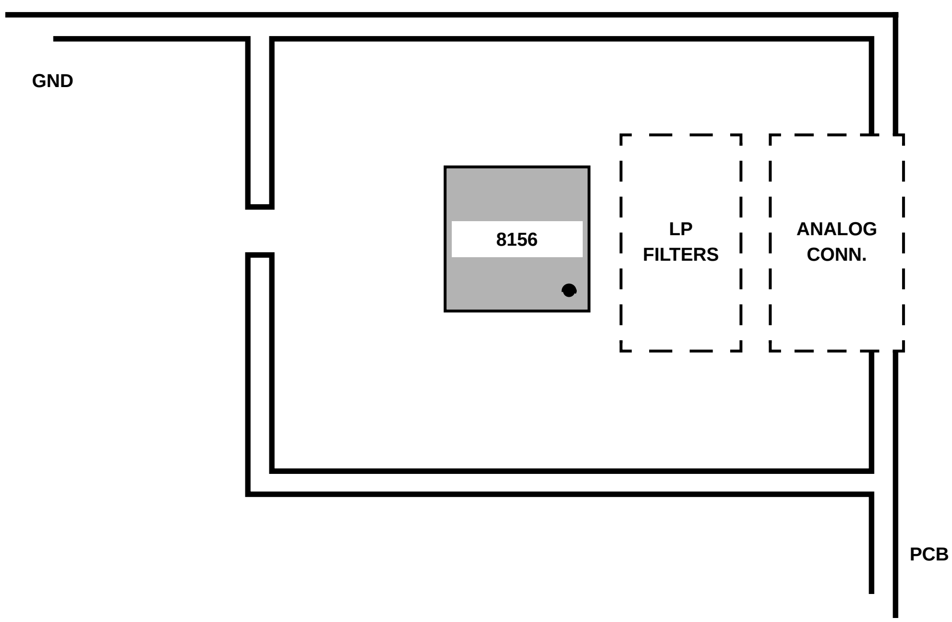


FIGURE 31B. COMMON GROUND PLANE

FIGURE 31. EXAMPLE POWER AND GROUND PLANES

External Reference Voltage

If an external reference voltage is used, its circuitry should receive power from the same plane as the HMP8156. The external VREF must also be stable and well decoupled from the power plane. An example VREF circuit using a band gap reference diode is shown in Figure 32.

Analog Output Filters

The various video standards specify the freqency response of the video signal. The HMP8156 uses 2X oversampling DACs to simplify the reconstruction filter required. Example post filters are shown in Figure 33. The analog output filters should be as close as possible to the HMP8156.

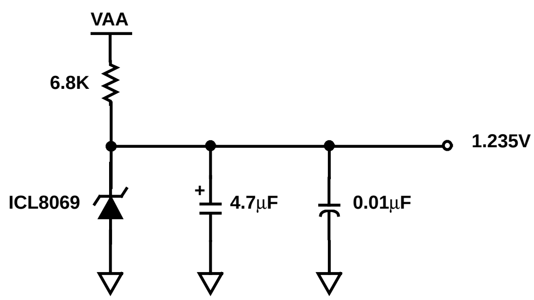


FIGURE 32. EXTERNAL REFERENCE VOLTAGE CIRCUIT

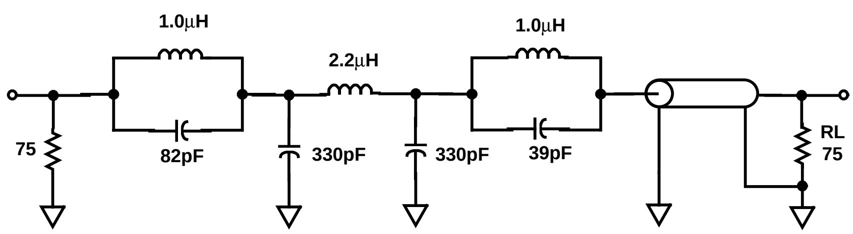


FIGURE 33A. HIGH QUALITY FILTER

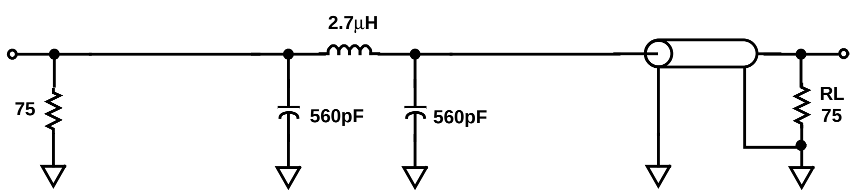


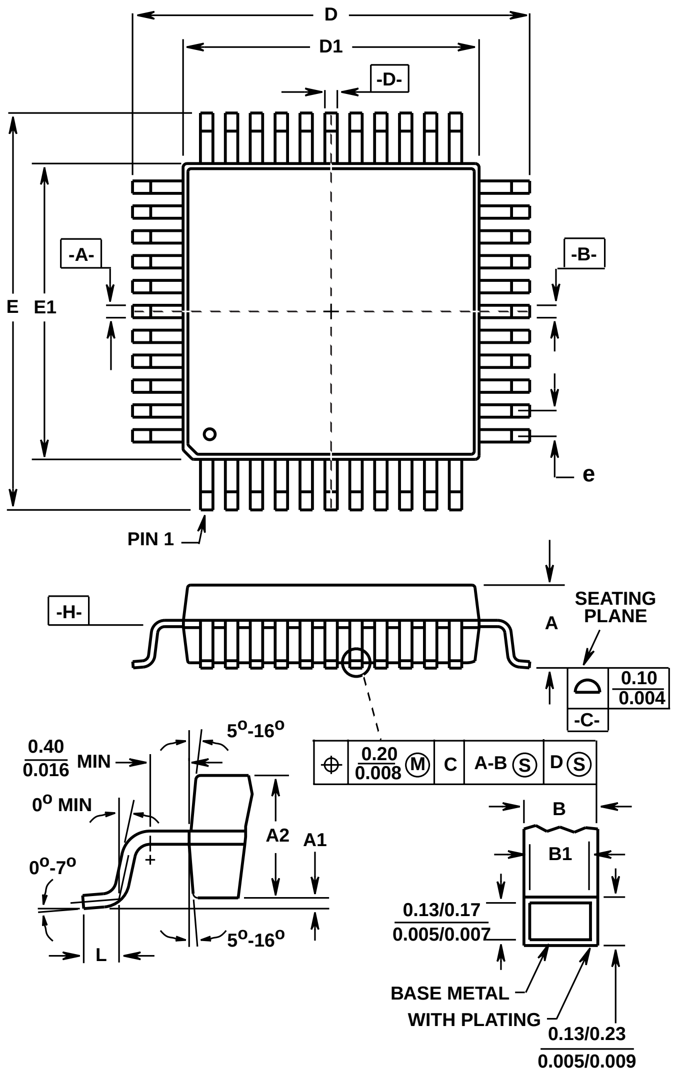
FIGURE 33B. LOW COST FILTER
FIGURE 33. EXAMPLE POST-FILTER CIRCUITS

Evaluation Kits

There are two evaluation platforms available. The HMP8156EVAL1 is a small daughter card containing the encoder, voltage references and bypassing, analog output filters and connectors, a BT.656 interface and connector, and a 50 pin two row header. The header allows connecting the pixel and control pins of the encoder into an existing system. The analog outputs allow the encoder's performance to be observed and measured.

The HMP8156EVAL2 is a standard size PC add in card with an ISA bus interface and application software. The HMP8156EVAL2 kit is a complete system which allows demonstrating all of the encoder's operating modes. It has analog video inputs for composite, S-video, and component RGB signals. The analog signals are converted/decoded to the digital domain and input to the encoder. The board also provides a 3 megabyte video RAM for image capture and display and a BT.656 connector and interface.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q64.14x14 **(JEDEC MO-108BD-2 ISSUE A)**
64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.130	-	3.30	-
A1	0.004	0.010	0.10	0.25	-
A2	0.100	0.120	2.55	3.05	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.667	0.687	16.95	17.45	3
D1	0.547	0.555	13.90	14.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	64		64		7
e	0.032 BSC		0.80 BSC		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C- .
4. Dimensions D1 and E1 to be determined at datum plane -H- .
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.