Data Sheet June 1999 File Number 3150.2

Single 16 and 8, Differential 8-Channel and 4-Channel CMOS Analog MUXs with Active Overvoltage Protection

The HI-546, HI-547, HI-548 and HI-549 are analog multiplexers with active overvoltage protection and guaranteed r_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-546, HI-547, HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. All devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-546 is a single 16-Channel, the HI-547 is an 8-Channel differential, the HI-548 is a single 8-Channel and the HI-549 is a 4-Channel differential device. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

For MIL-STD-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 and HI-549/883 datasheets.

Features

- Analog Overvoltage Protection . . . . . $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Guaranteed r_{ON} Matching
- Maximum Power Supply 44V
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

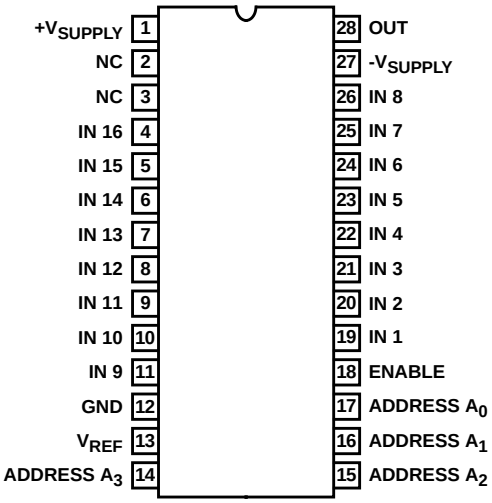
- Data Acquisition
- Industrial Controls
- Telemetry

Ordering Information

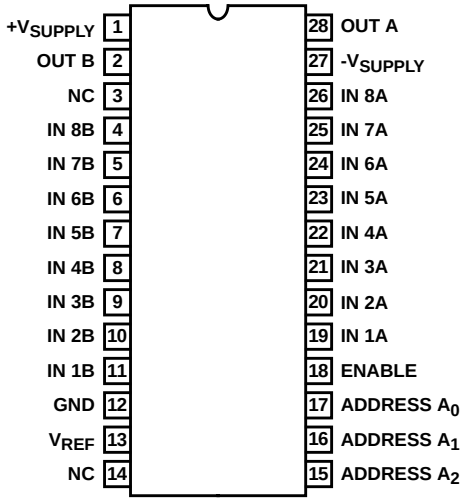
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1-0546-5	0 to 75	28 Ld CERDIP	F28.6
HI1-0546-2	-55 to 125	28 Ld CERDIP	F28.6
HI3-0546-5	0 to 75	28 Ld PDIP	E28.6
HI4P0546-5	0 to 75	28 Ld PLCC	N28.45
HI9P0546-9	-40 to 85	28 Ld SOIC	M28.3
HI1-0547-5	0 to 75	28 Ld CERDIP	F28.6
HI3-0547-5	0 to 75	28 Ld PDIP	E28.6
HI4P0547-5	0 to 75	28 Ld PLCC	N28.45
HI9P0547-9	-40 to 85	28 Ld SOIC	M28.3
HI1-0548-2	-55 to 125	16 Ld CERDIP	F16.3
HI1-0548-5	0 to 75	16 Ld CERDIP	F16.3
HI3-0548-5	0 to 75	16 Ld PDIP	E16.3
HI4P0548-5	0 to 75	20 Ld PLCC	N20.35
HI9P0548-5	0 to 75	16 Ld SOIC	M16.15
HI9P0548-9	-40 to 85	16 Ld SOIC	M16.15
HI1-0549-2	-55 to 125	16 Ld CERDIP	F16.3
HI3-0549-5	0 to 75	16 Ld PDIP	E16.3
HI4P0549-5	0 to 75	20 Ld PLCC	N20.35
HI9P0549-5	0 to 75	16 Ld SOIC	M16.15
HI9P0549-9	-40 to 85	16 Ld SOIC	M16.15

Pinouts

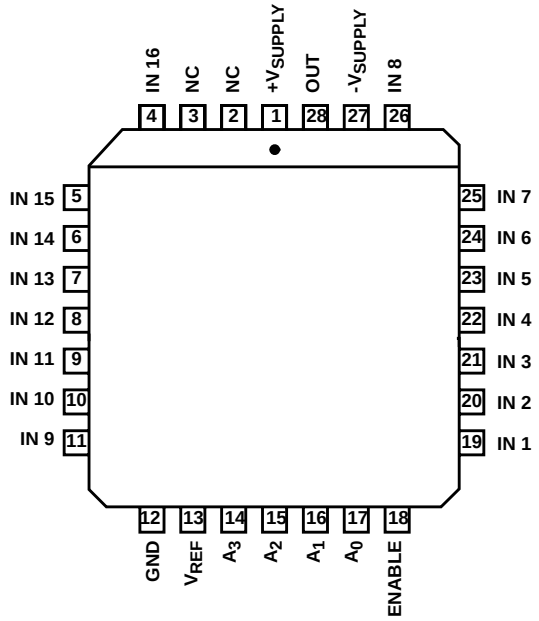
HI-546 (CERDIP, PDIP, SOIC)
TOP VIEW



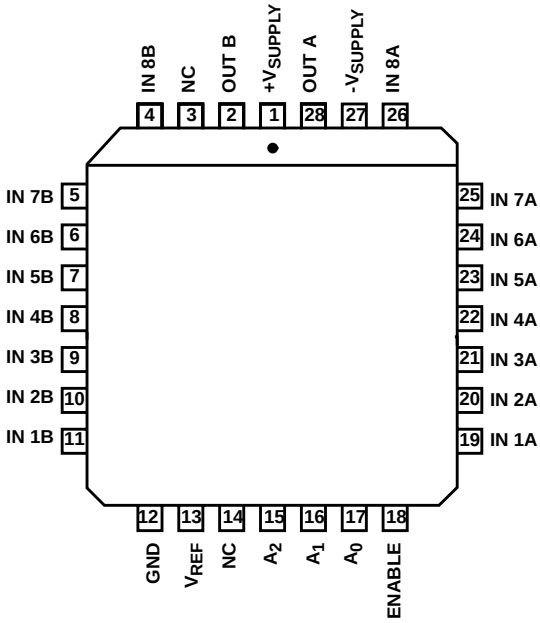
HI-547 (CERDIP, PDIP, SOIC)
TOP VIEW



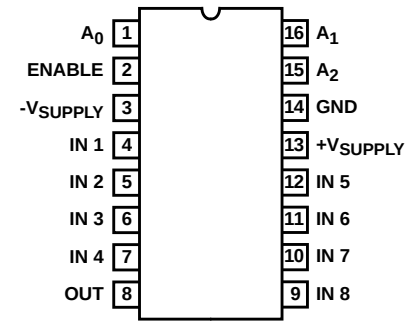
HI-546 (PLCC)
TOP VIEW



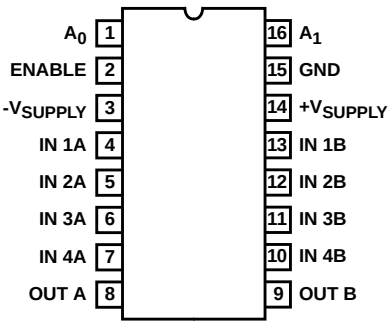
HI-547 (PLCC)
TOP VIEW



HI-548 (CERDIP, PDIP, SOIC)
TOP VIEW

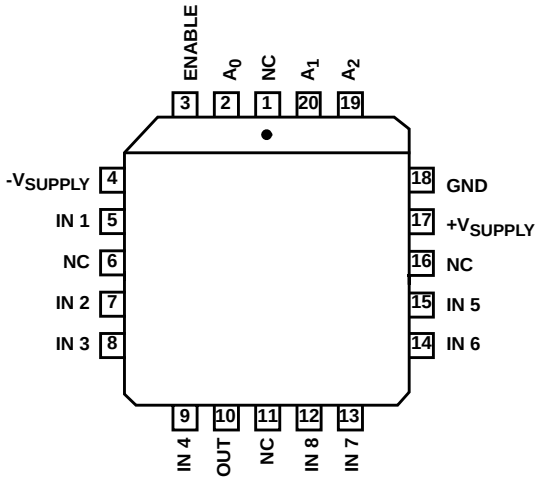


HI-549 (CERDIP, PDIP, SOIC)
TOP VIEW

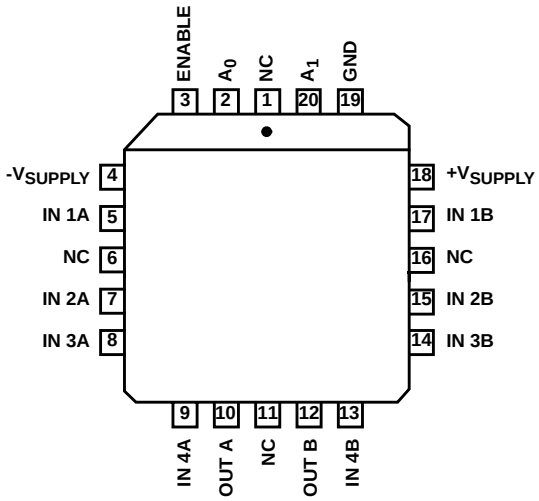


Pinouts (Continued)

HI-548 (PLCC)
TOP VIEW



HI-549 (PLCC)
TOP VIEW



TRUTH TABLE HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

TRUTH TABLE HI-547

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5

TRUTH TABLE HI-547 (Continued)

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE HI-548

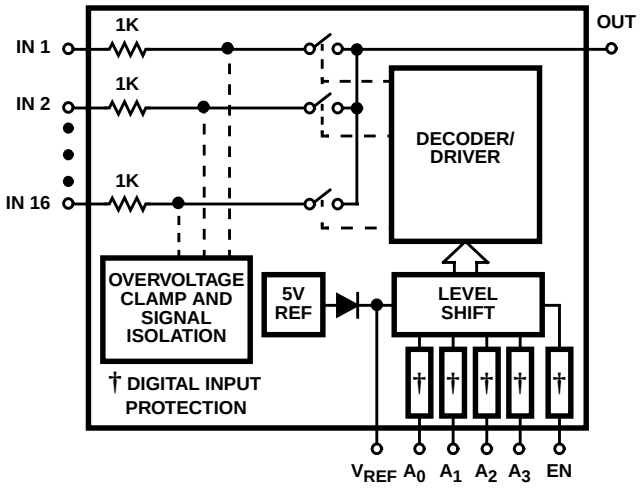
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

TRUTH TABLE HI-549

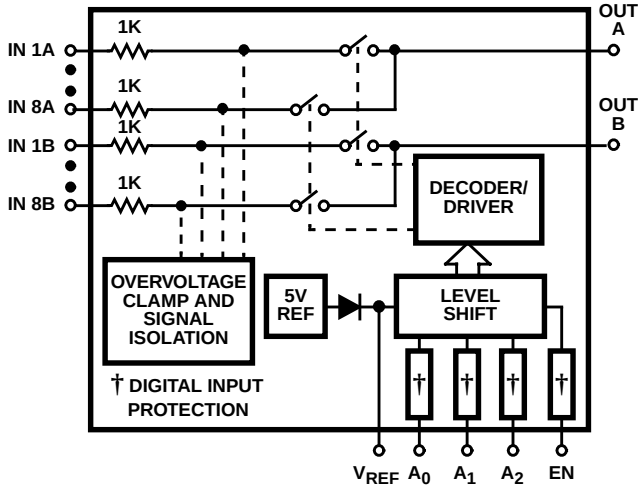
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Functional Diagrams

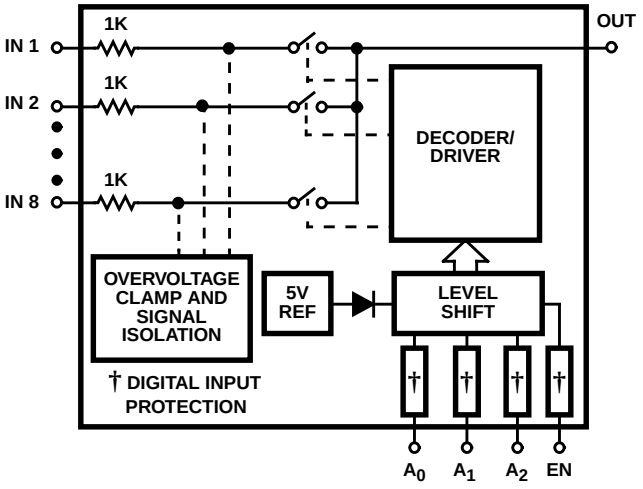
HI-546



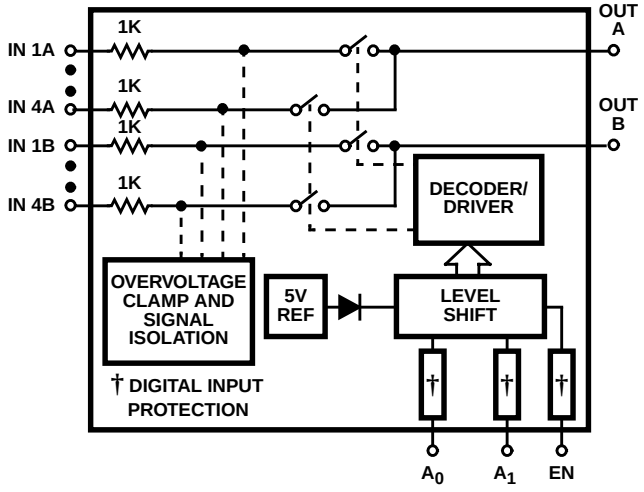
HI-547



HI-548

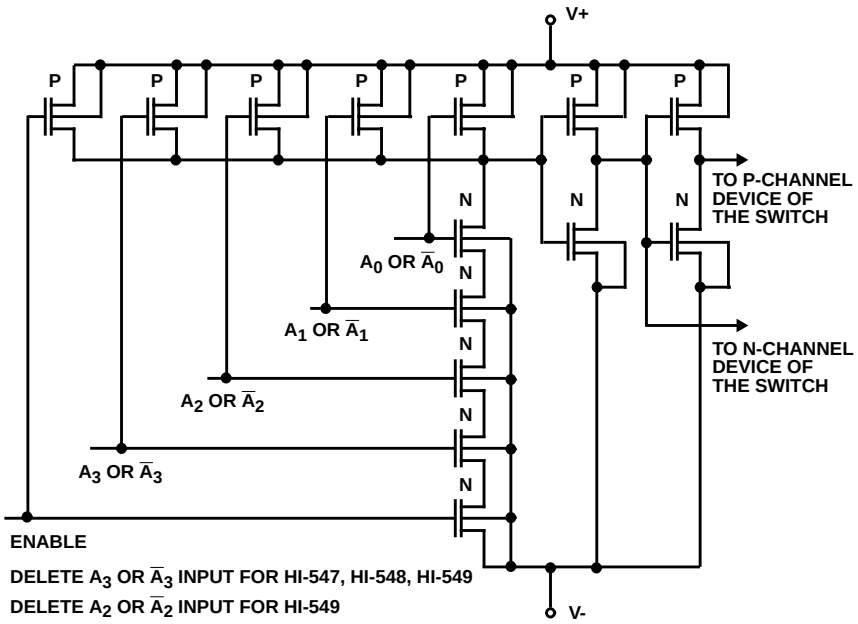


HI-549

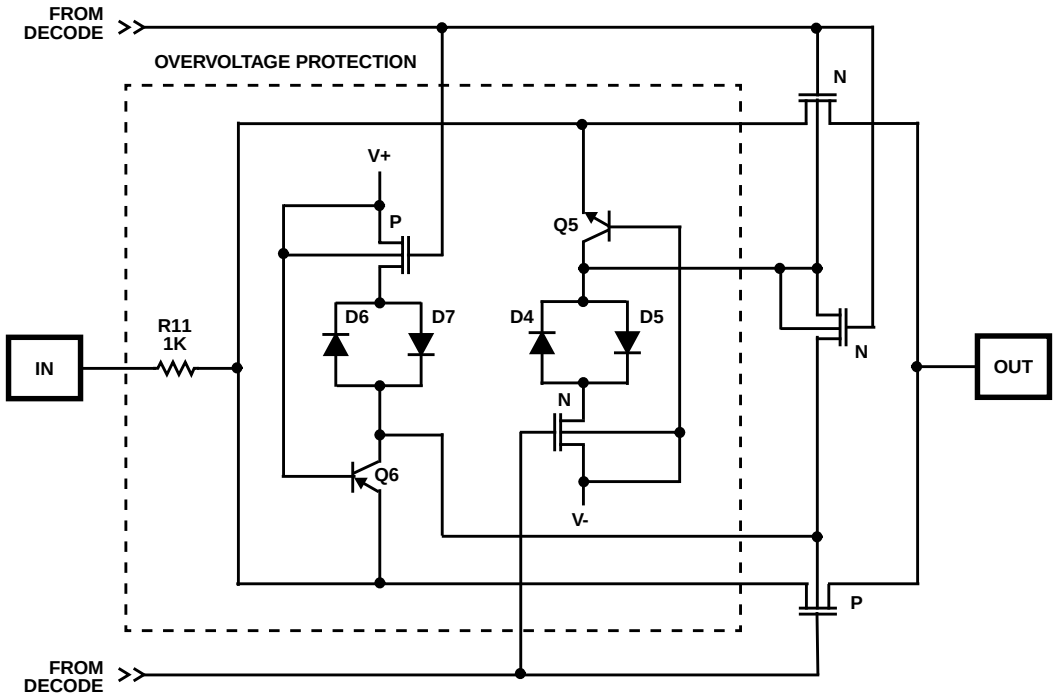


Schematic Diagrams

ADDRESS DECODER

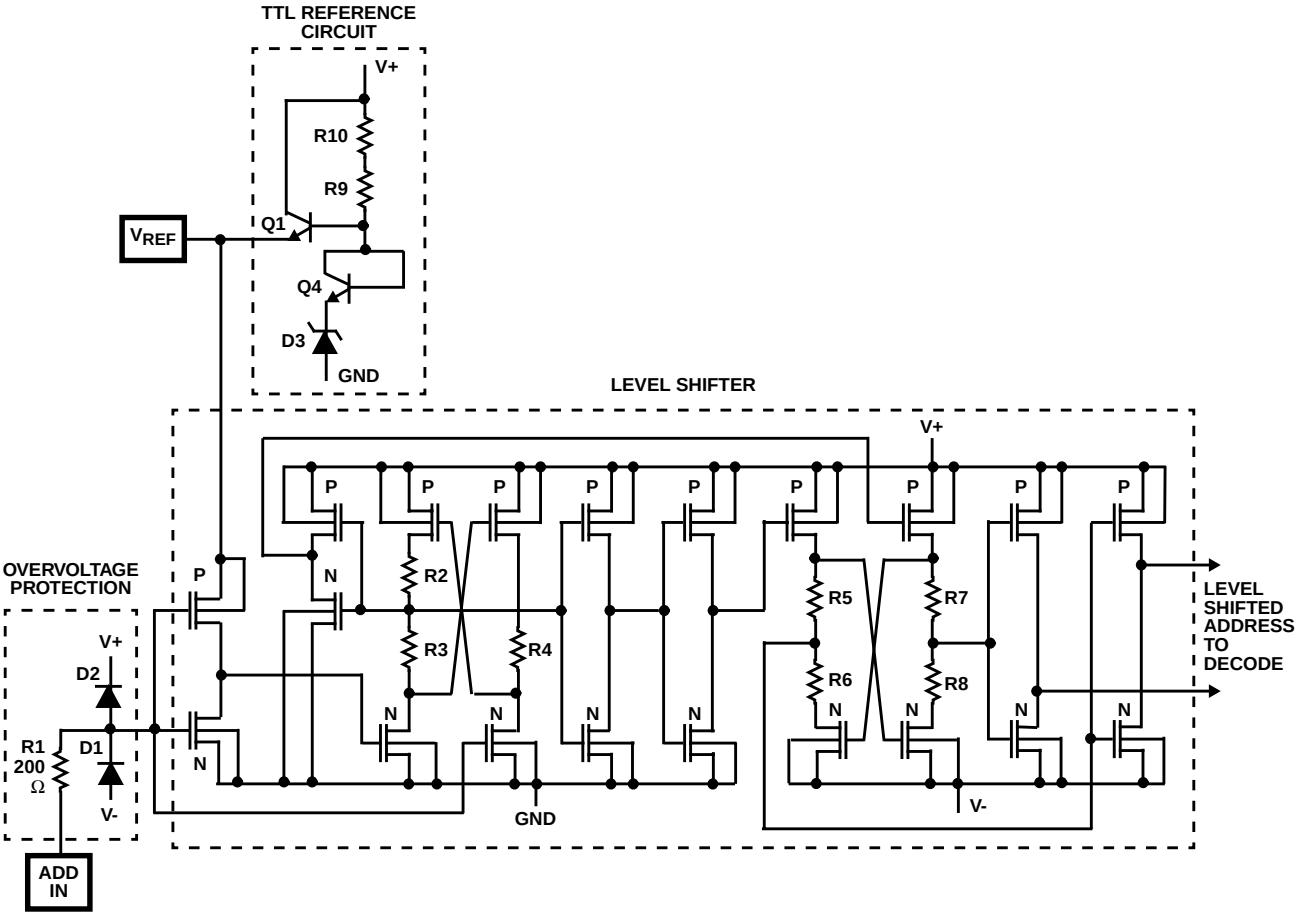


MULTIPLEX SWITCH



Schematic Diagrams (Continued)

ADDRESS INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

V+ to V- . . . . . +44V
V+ to GND . . . . . +22V
V- to GND. . . . . -25V
Digital Input Voltage (V_{EN}, V_A) . . . . . (V-) -4V to (V+) +4V
Analog Signal (V_{IN}, V_{OUT}). . . . . (V-) -20V to (V+) +20V
or 20mA, Whichever Occurs First
Continuous Current, IN or OUT 20mA
Peak Current, IN or OUT (Pulsed 1ms, 10% Duty Cycle Max) . . 40mA

Operating Conditions

Temperature Ranges
HI-546/548/549-2 . . . . . -55^oC to 125^oC
HI-546/547/548/549-5 . . . . . 0^oC to 75^oC
HI-546/547/548/549-9 . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
16 Ld CERDIP Package	85	32
28 Ld CERDIP Package	55	18
28 Ld PDIP Package	60	N/A
16 Ld PDIP Package	90	N/A
28 Ld PLCC Package	70	N/A
20 Ld PLCC Package	80	N/A
28 Ld SOIC Package	75	N/A
16 Ld SOIC Package	105	N/A

Maximum Junction Temperature
Ceramic Packages . . . . . 175^oC
Plastic Packages . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(PLCC, SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V; Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section

PARAMETER	TEST CONDITIONS	TEMP (^oC)	-2			-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A		25	-	0.5	-	-	0.5	-	µs
		Full	-	-	1.0	-	-	1.0	µs
Break-Before Make Delay, t_{OPEN}		25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time	To 0.1%	25	-	1.2	-	-	1.2	-	µs
	To 0.01%	25	-	3.5	-	-	3.5	-	µs
Off Isolation	Note 6	25	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	10	-	-	10	-	pF
Channel Output Capacitance $C_{D(OFF)}$									
HI-546		25	-	52	-	-	52	-	pF
HI-547		25	-	30	-	-	30	-	pF
HI-548		25	-	25	-	-	25	-	pF
HI-549		25	-	12	-	-	12	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, TTL Drive, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (Note 8)		Full	4.0	-	-	4.0	-	-	V
MOS Drive, V_{AL} (HI-546/547 Only)	V_{REF} = 10V	25	-	-	0.8	-	-	0.8	V
MOS Drive, V_{AH} (HI-546/547 Only)	V_{REF} = 10V	25	6.0	-	-	6.0	-	-	V
Input Leakage Current (High or Low), I_A	Note 5	Full	-	-	1.0	-	-	1.0	µA

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V; Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (^{O}C)	-2			-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}		Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	Note 2	25	-	1.2	1.5	-	1.5	1.8	kΩ
		Full	-	1.5	1.8	-	1.8	2.0	kΩ
Δr_{ON}, (Any Two Channels)		25	-	-	7.0	-	-	7.0	%
Off Input Leakage Current, $I_{S(OFF)}$	Note 3	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Note 3	25	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
$I_{D(OFF)}$ With Input Overvoltage Applied	Note 4	25	-	4.0	-	-	4.0	-	nA
		Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$	Note 3	25	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current I_{DIFF} (HI-547, HI-549 Only)		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	7.5	-	-	7.5	-	mW
Current, I+	Note 7	Full	-	0.5	2.0	-	0.5	2.0	mA
Current, I-	Note 7	Full	-	0.02	1.0	-	0.02	1.0	mA

NOTES:

2. V_{OUT} = ±10V, I_{OUT} = ∓100µA.
3. 10nA is the practical lower limit for high speed measurement in the production test environments.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25^{O}C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz.
7. V_{EN}, V_A = 0V or 4V.
8. To drive from DTL/TTLCircuits, 1kΩ pull-up resistors to +5V supply are recommended.

Test Circuits and Waveforms $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

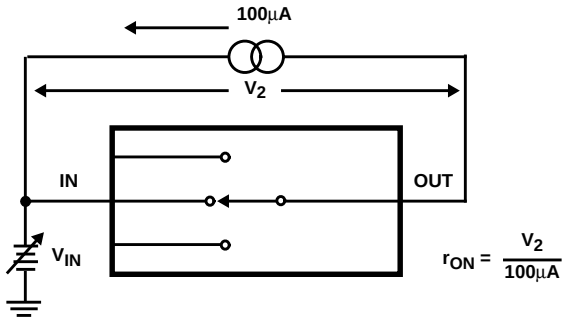


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

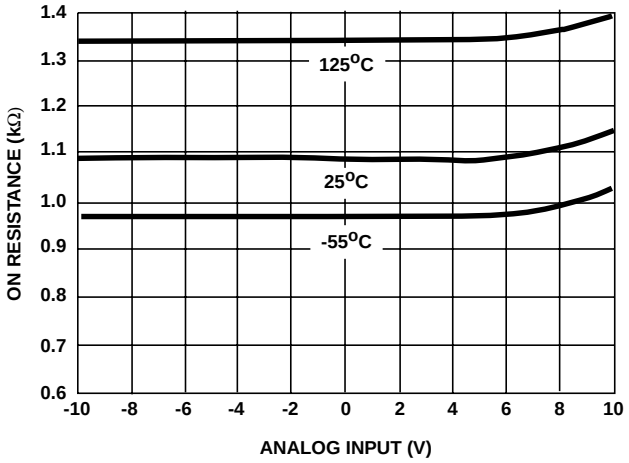


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

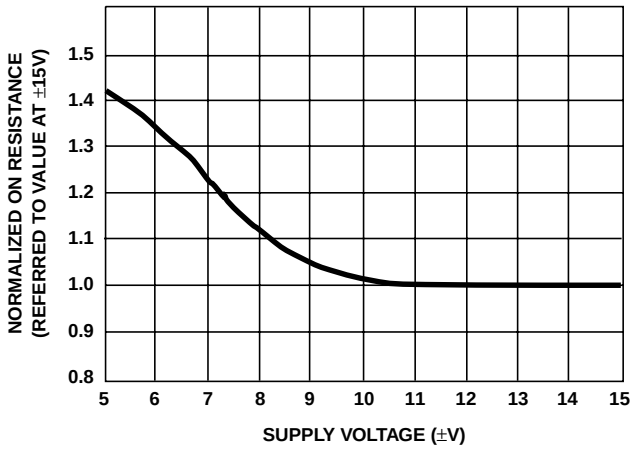


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

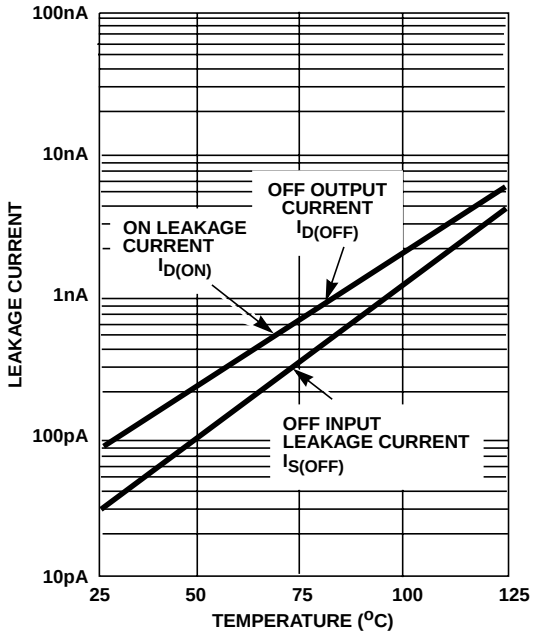


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

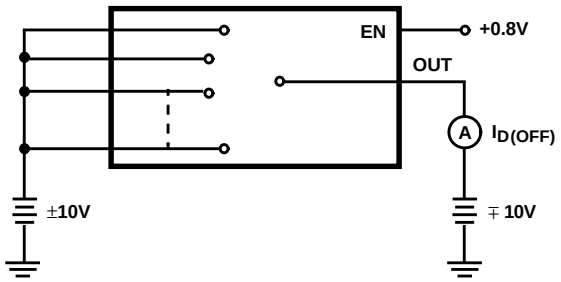


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 9)

Test Circuits and Waveforms $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

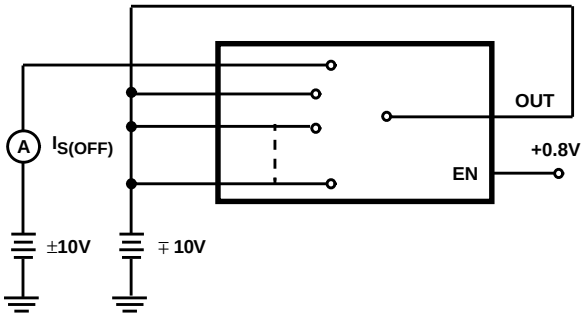


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 9)

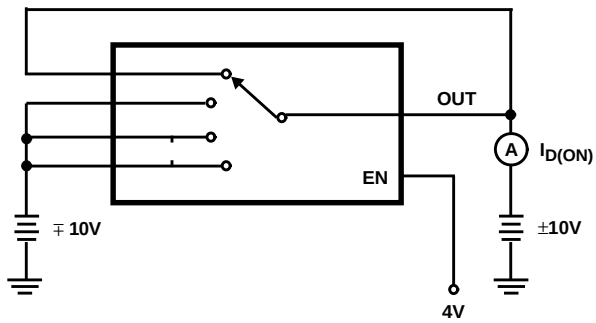


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT (NOTE 9)

NOTE:

9. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$: ±10V and ∓10V.)

FIGURE 2. LEAKAGE CURRENTS

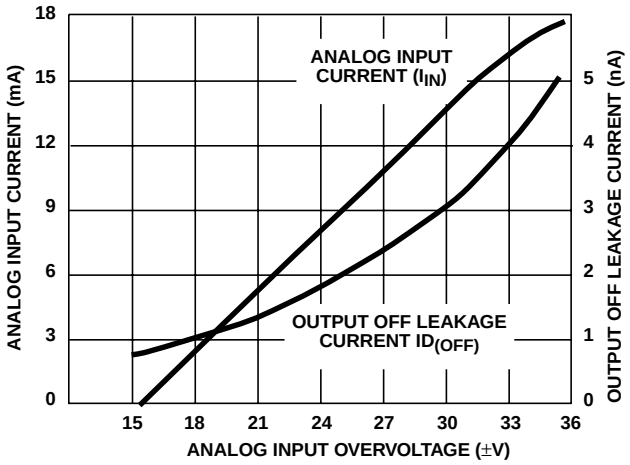


FIGURE 3A. ANALOG INPUT CURRENT AND OUTPUT OFF LEAKAGE CURRENT vs ANALOG INPUT OVER-VOLTAGE

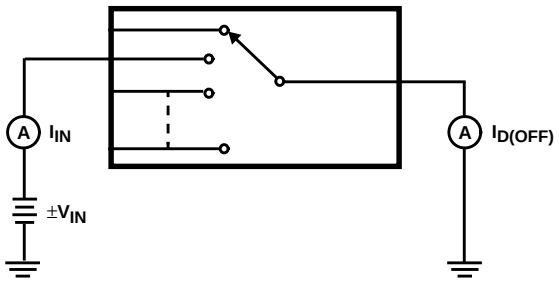


FIGURE 3B. TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

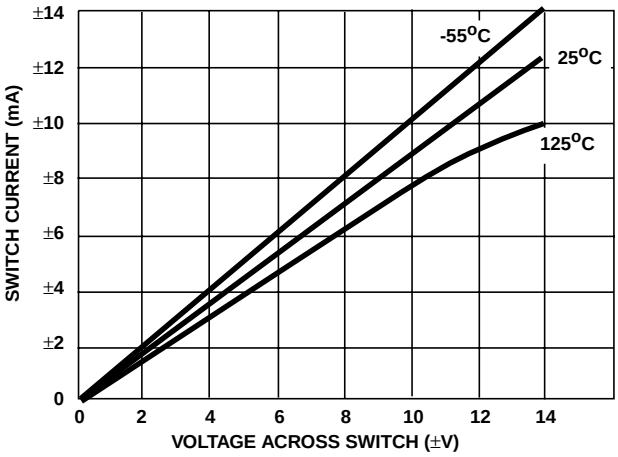


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

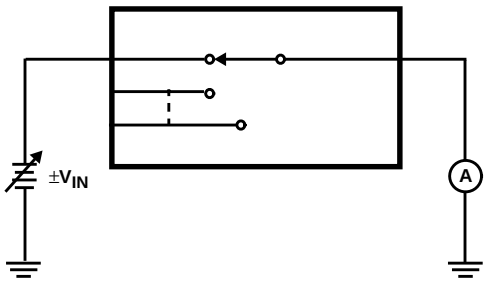


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Test Circuits and Waveforms $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

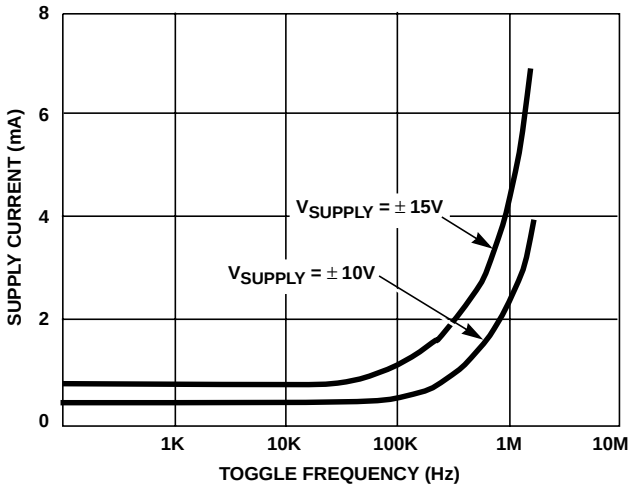
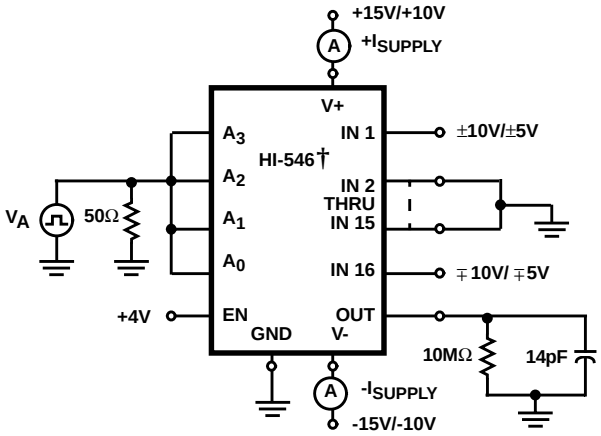


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-547/HI-548/HI-549.

FIGURE 5B. TEST CIRCUIT

FIGURE 5. DYNAMIC SUPPLY CURRENT

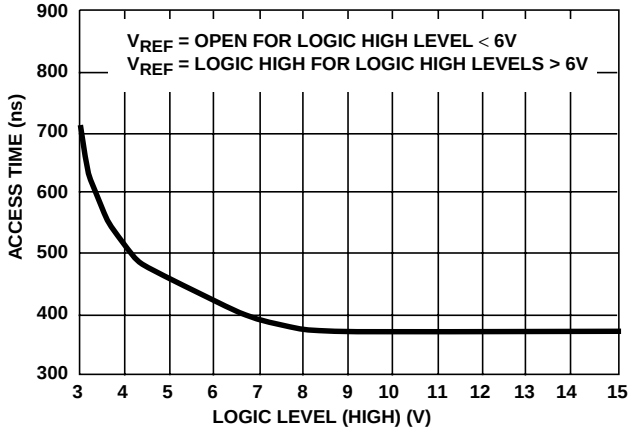
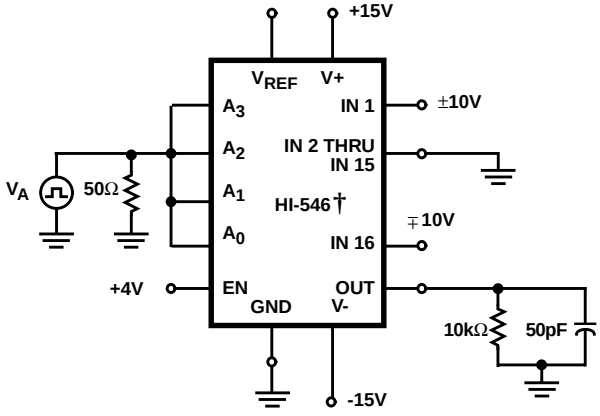


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-547/HI-548/HI-549.

FIGURE 6B. TEST CIRCUIT

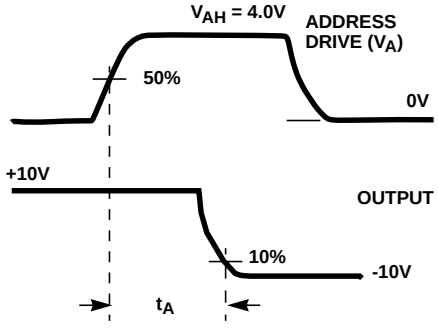


FIGURE 6C. MEASUREMENT POINTS

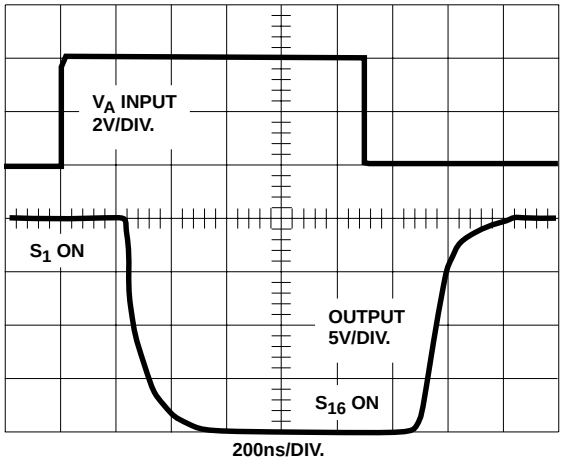
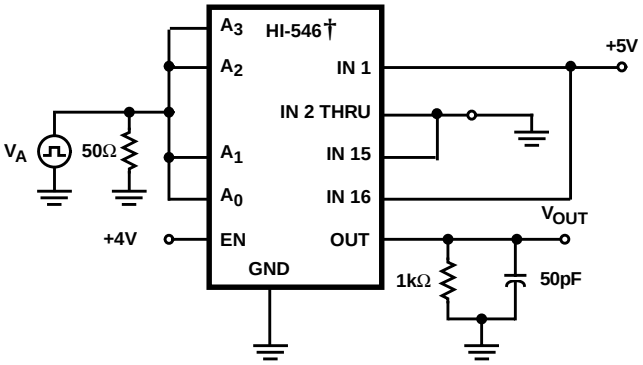


FIGURE 6D. WAVEFORMS

FIGURE 6. ACCESS TIME

Test Circuits and Waveforms $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**



†Similar connection for HI-547/HI-548/HI-549

FIGURE 7A. TEST CIRCUIT

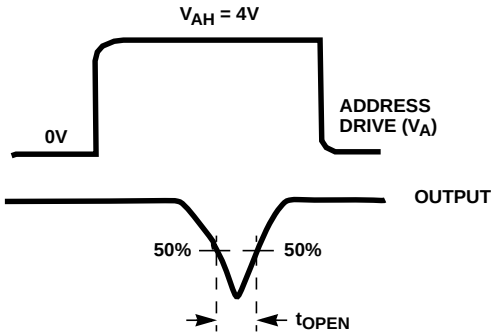


FIGURE 7B. MEASUREMENT POINTS

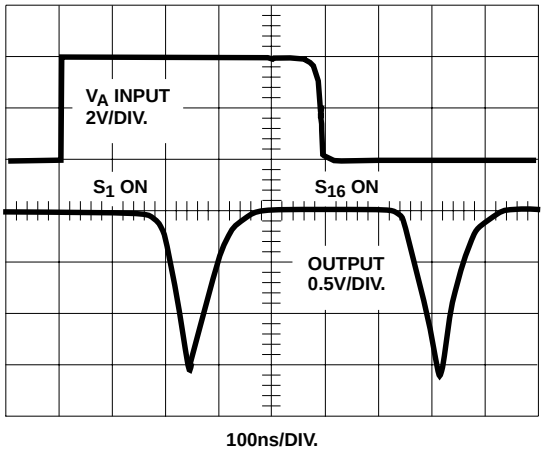
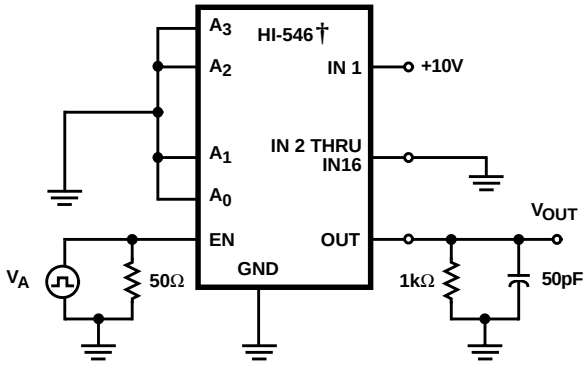


FIGURE 7C. WAVEFORMS

FIGURE 7. BREAK-BEFORE-MAKE DELAY



†Similar connection for HI-547/HI-548/HI-549

FIGURE 8A. TEST CIRCUIT

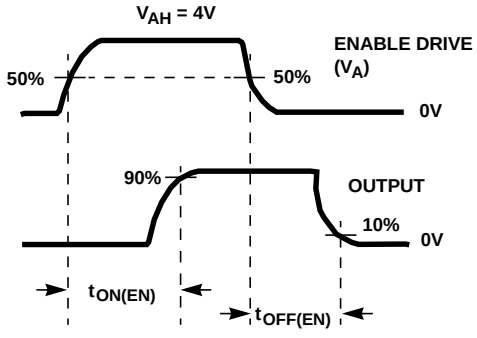


FIGURE 8B. MEASUREMENT POINTS

Test Circuits and Waveforms $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

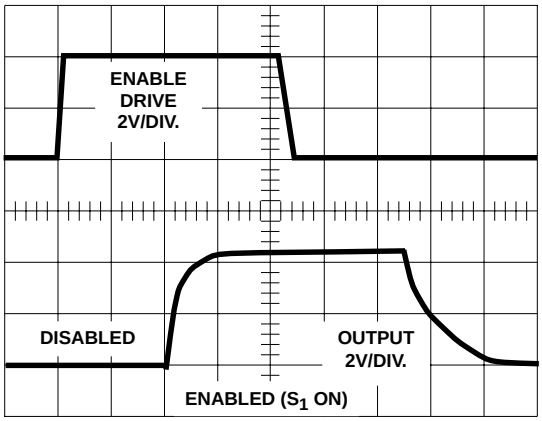


FIGURE 8C. WAVEFORMS

FIGURE 8. ENABLE DELAYS

Die Characteristics

DIE DIMENSIONS:

83.9 mils x 159 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

485

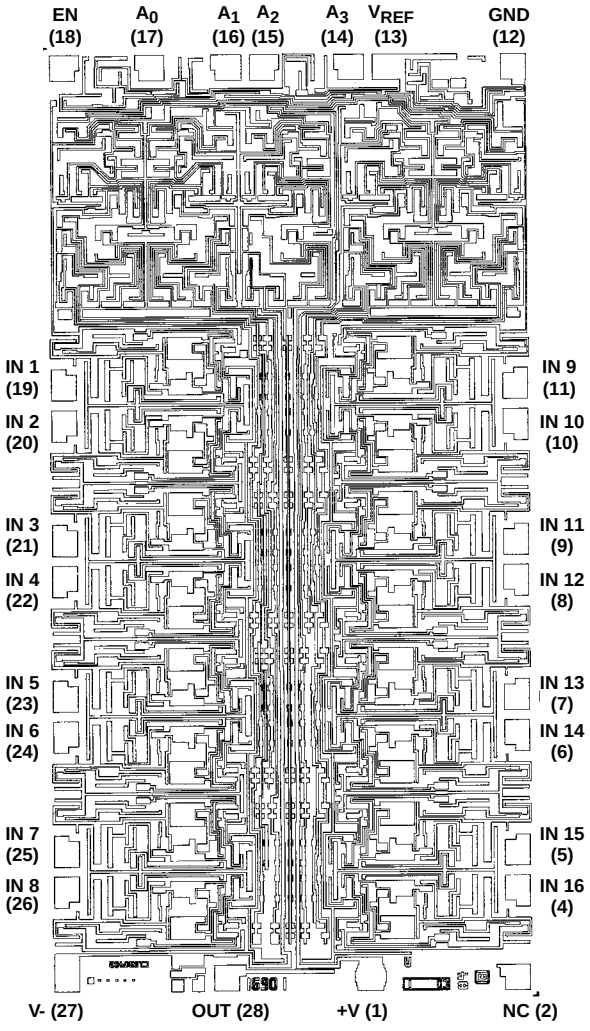
PROCESS:

CMOS-DI

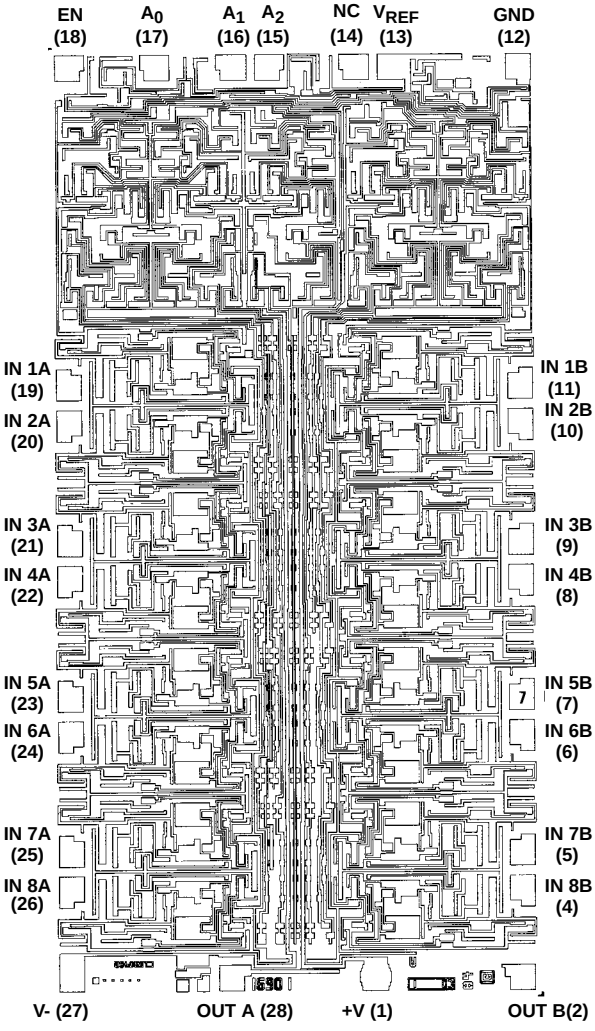
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-546



HI-547



Die Characteristics

DIE DIMENSIONS:

83 mils x 108 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1kÅ
Silox Thickness: 12kÅ ±2kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm

TRANSISTOR COUNT:

253

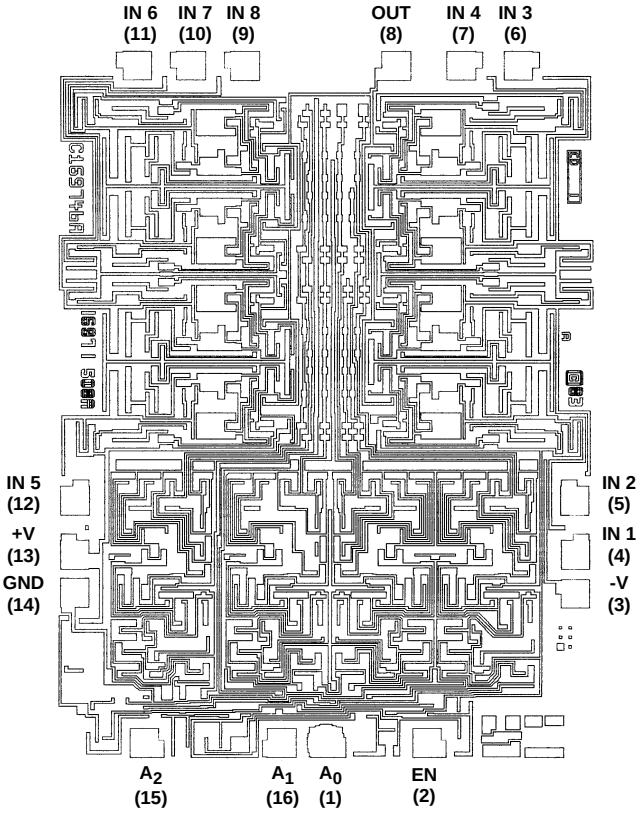
PROCESS:

CMOS-DI

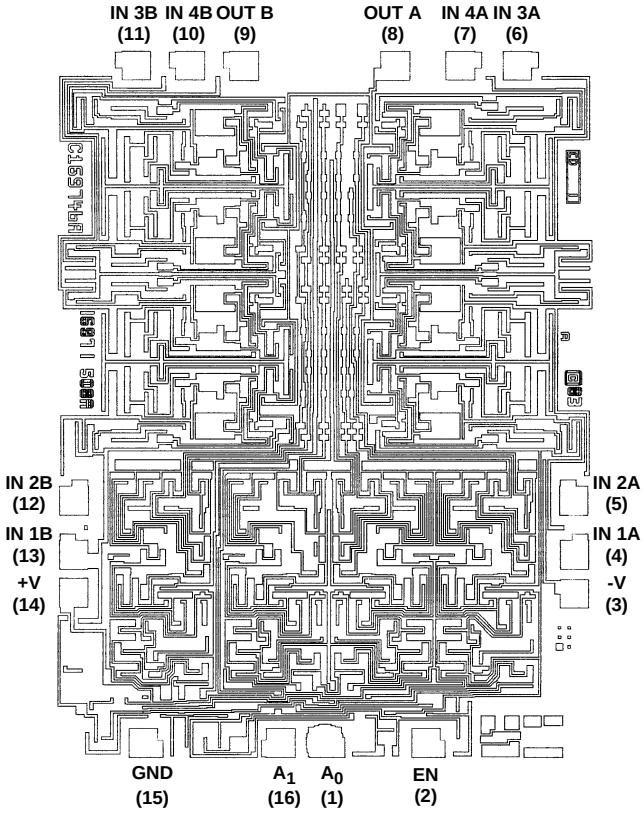
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-548



HI-549



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.