HD-15531/883

March 1997

CMOS Manchester Encoder-Decoder

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Support of MIL-STD-1553**
- **Data Rate (15531B) . . . . . 2.5 Megabit/Sec**
- **Data Rate (15531). . . . . 1.25 Megabit/Sec**
- **Variable Frame Length to 32-Bits**
- **Sync Identification and Lock-In**
- **Separate Manchester II Encode, Decode**
- **Low Operating Power . . . . . 50mW at 5V**

Description

The Intersil HD-15531/883 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions. This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

The HD-15531/883 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus, the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

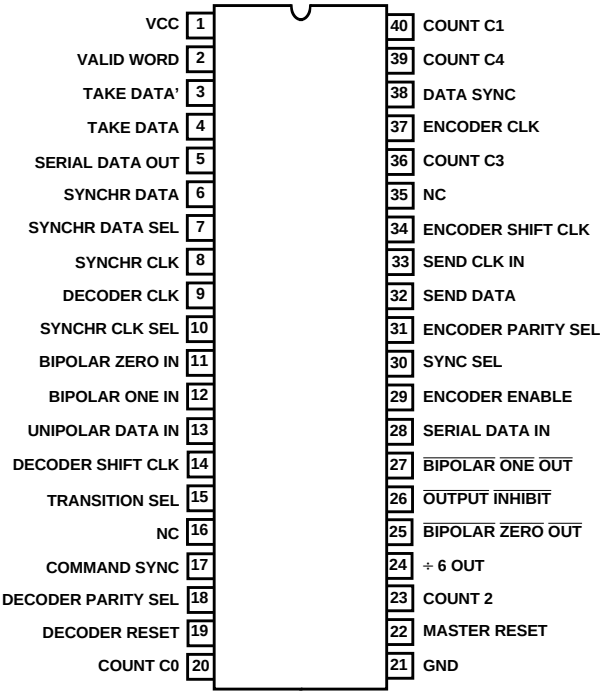
The HD-15531/883 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair or fiber optic cable throughout a building.

Ordering Information

PACKAGE	TEMPERATURE RANGE	1.25MBIT/SEC	2.5MBIT/SEC	PKG. NO.
CERDIP	-55^{o}C to +125^{o}C	HD1-15531/883	HD1-15531B/883	F40.6

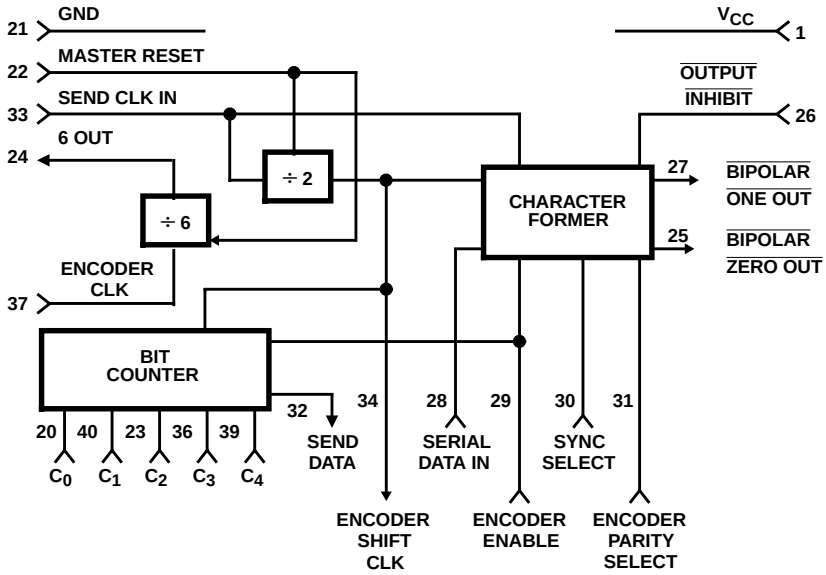
Pinout

HD-15531/883 (CERDIP)
TOP VIEW



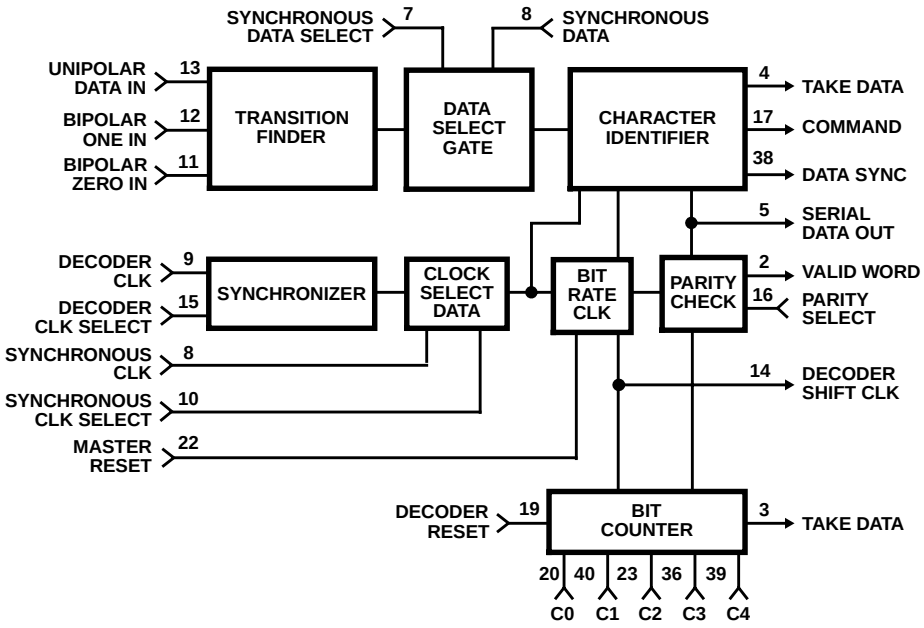
Block Diagrams

ENCODER



Block Diagrams (Continued)

DECODER



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to VCC +0.5V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$35^oC/W$	$9^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . . -55^oC to $+125^oC$
Encoder/Decoder Clock Rise Time (TECR, TDCR) . . . . . 8ns Max
Encoder/Decoder Clock Fall Time (TECF, TDCF) . . . . . 8ns Max
Sync. Transition Span (TD2) . . . . . 18 TDC Typical, (Note 1)
Short Data Transition Span (TD4) . . . . . 6 TDC Typical, (Note 1)
Long Data Transition Span (TD5) . . . . . 12 TDC Typical, (Note 1)

TABLE 1. HD-15531/883, HD-15531B/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input LOW Voltage	VIL	VCC = 4.5V and 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.2 VCC	V
Input HIGH Voltage	VIH	VCC = 4.5V and 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	0.7 VCC	-	V
Input LOW Clock Voltage	VILC	VCC = 4.5V and 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	GND +0.5	V
Input HIGH Clock Voltage	VIHC	VCC = 4.5V and 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	VCC -0.5	-	V
Output LOW Voltage	VOL	IOL = +1.8mA, VCC = 4.5V (Note 2)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Output HIGH Voltage	VOH	IOH = -3.0mA, VCC = 4.5V (Note 2)	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Input Leakage Current	II	VI = VCC or GND, VCC = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Standby Supply Current	ICCSB	VIN = VCC = 5.5V, Outputs Open	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	2	mA
Functional Test	FT	(Note 3)	7, 8	$-55^oC \le T_A \le +125^oC$	-	-	-

NOTES:

1. TDC = Decoder clock period = 1/FDC.
2. Interchanging of force and sense conditions is permitted.
3. Tested as follows: f = 15MHz, VIH = 70% VCC, VIL = 20% VCC, CL = 50pF, VOH ≥ VCC/2 and VOL ≤ VCC/2.

TABLE 2. HD-15531/883, HD-15531B/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	(NOTE 2) CONDI-TIONS	GROUP A SUB-GROUPS	TEMPERATURE	HD-15531/883		HD-15531B/883		UNITS
					MIN	MAX	MIN	MAX	
ENCODER TIMING									
Encoder Clock Frequency	FEC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	15	-	30	MHz
Send Clock Frequency	FESC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	2.5	-	5.0	MHz

TABLE 2. HD-15531/883, HD-15531B/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	(NOTE 2) CONDI-TIONS	GROUP A SUB-GROUPS	TEMPERATURE	HD-15531/883		HD-15531B/883		UNITS
					MIN	MAX	MIN	MAX	
Encoder Data Rate	FED	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	1.25	-	2.5	MHz
Master Reset Pulse Width	TMR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Shift Clock Delay	TE1	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	125	-	80	ns
Serial Data Setup	TE2	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	50	-	ns
Serial Data Hold	TE3	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	50	-	ns
Enable Setup	TE4	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	90	-	90	-	ns
Enable Pulse Width	TE5	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Sync Setup	TE6	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	55	-	55	-	ns
Sync Pulse Width	TE7	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Send Data Delay	TE8	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	50	0	50	ns
Bipolar Output Delay	TE9	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	130	-	130	ns
Enable Hold	TE10	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	ns
Sync Hold	TE11	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	95	-	95	-	ns
DECODER TIMING									
Decoder Clock Frequency	FDC	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	15	-	30	MHz
Decoder Sync Clock	FDS	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	2.5	-	5.0	MHz
Decoder Data Rate	FDD	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	1.25	-	2.5	MHz
Decoder Re-set Pulse Width	TDR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Decoder Re-set Setup Time	TDRS	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	75	-	ns
Decoder Re-set Hold Time	TDRH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	10	-	10	-	ns
Master Reset Pulse	TMR	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	150	-	150	-	ns
Bipolar Data Pulse Width	TD1	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	TDC +10 (Note 1)	-	TDC +10 (Note 1)	-	ns
One Zero Overlap	TD3	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	TDC-10 (Note 1)	-	TDC-10 (Note 1)	ns
Sync Delay (ON)	TD6	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-20	110	-20	110	ns

TABLE 2. HD-15531/883, HD-15531B/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

PARAMETER	SYMBOL	(NOTE 2) CONDI-TIONS	GROUP A SUB-GROUPS	TEMPERATURE	HD-15531/883		HD-15531B/883		UNITS
					MIN	MAX	MIN	MAX	
Take Data Delay (ON)	TD7	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Serial Data Out Delay	TD8	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	80	-	80	ns
Sync Delay (OFF)	TD9	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Take Data Delay (OFF)	TD10	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Valid Word Delay	TD11	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	110	0	110	ns
Sync Clock to Shift Clock Delay	TD12	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	75	-	75	ns
Sync Data Setup	TD13	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	75	-	75	-	ns

NOTES:

1. TDC = Decoder Clock Period = 1/FDC.
2. AC Testing as follows: VIH = 70% VCC, VIL = 20% VCC; Input rise/fall times driven at 1ns/V; Timing reference levels: VCC/2; Output load: CL = 50pF.

TABLE 3. HD-15531/883, HD-15531B/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CI	VCC = OPEN, f = 1MHz, All measurements referenced to device GND	1	$T_A = +25^oC$	-	25	pF
Input/Output Capacitance	CIO	VCC = OPEN, f = 1MHz, All measurements referenced to device GND	1	$T_A = +25^oC$	-	25	pF
Operating Power Supply Current	ICCOP	VCC = 5.5V, f = 1MHz	1, 2	$-55^oC \le T_A \le +125^oC$	-	10	mA

NOTES:

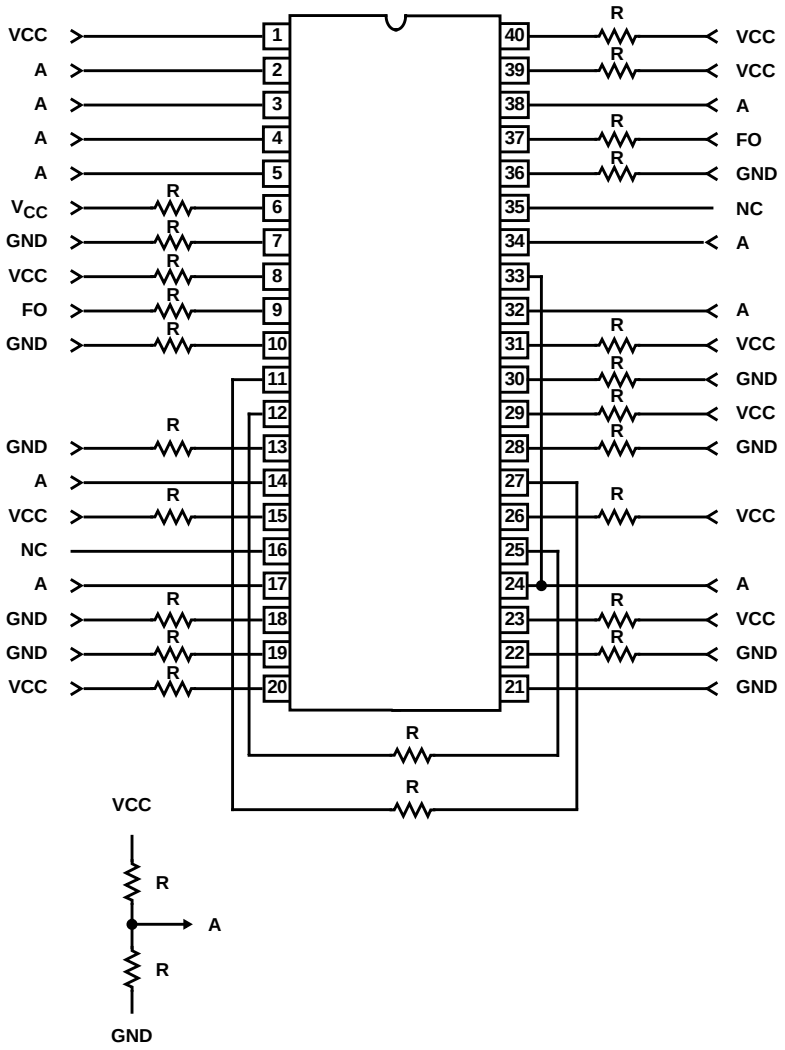
1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.
2. Guaranteed but not 100% tested.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Burn-In Circuit

HD1-15531/883 CERDIP



NOTES:

1. VCC = 5.5V ±0.5V.
2. VIH = 4.5V ±10%.
3. VIL = -0.2V to +0.4V.
4. R = 47kΩ ±5%.
5. F0 = 100kHz ±10%.

Die Characteristics

DIE DIMENSIONS:
155 x 195 x 19 ±1mils

METALLIZATION:
Type: Si-Al

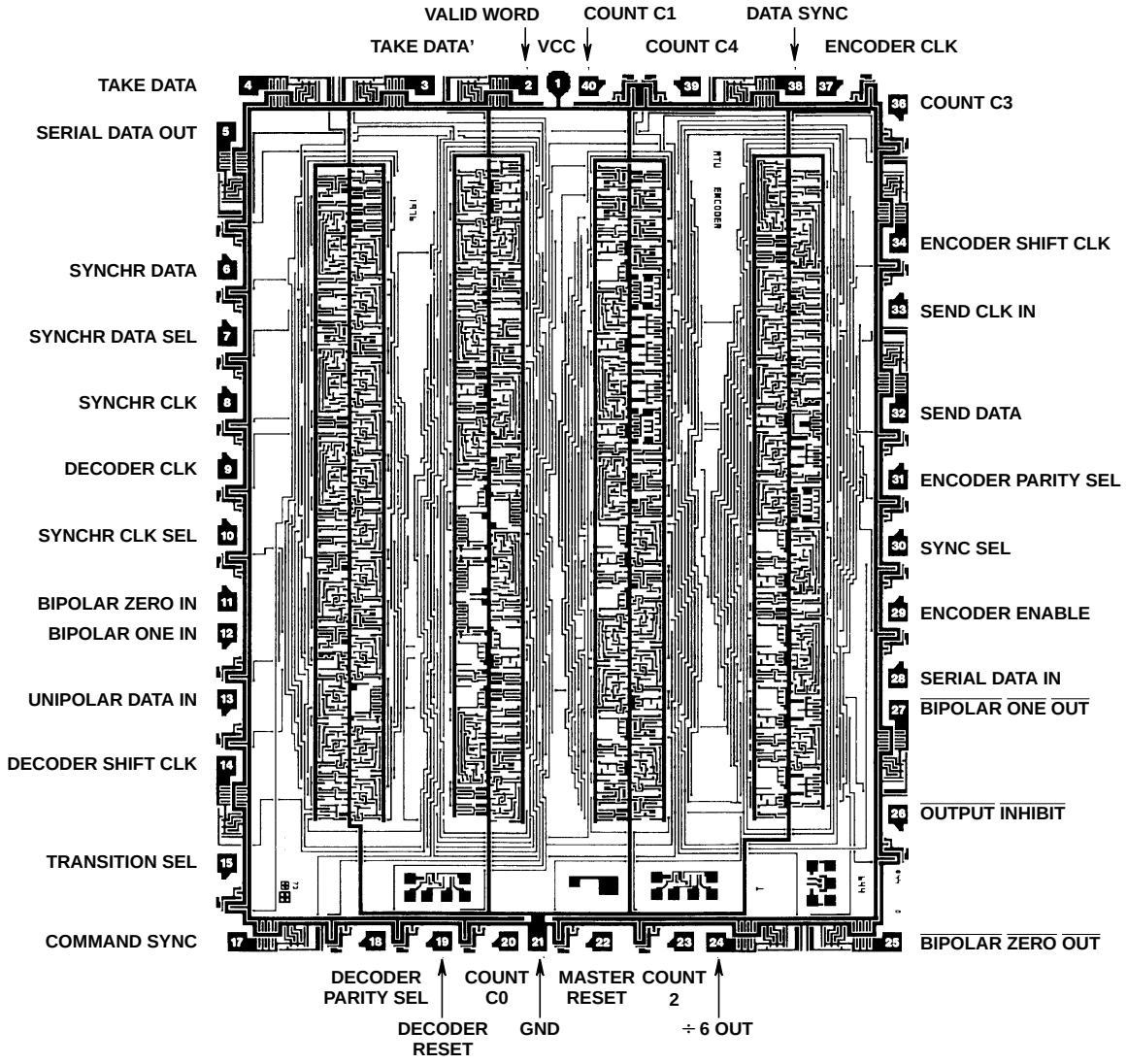
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
2.0 x 10^5 A/cm^2

Metallization Mask Layout

HD-15531/883



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