

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm²/mg
- Single Event Upset (SEU) Immunity < 2 x 10⁻⁹ Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10¹² RAD (Si)/s
- Dose Rate Upset >10¹⁰ RAD (Si)/s 20ns Pulse
- Cosmic Ray Upset Rate 2 x 10⁻⁹ Errors/Bit Day
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
 - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
 - VIL = 0.8V Max
 - VIH = VCC/2
- Input Current Levels I_i ≤ 5μA at VOL, VOH

Description

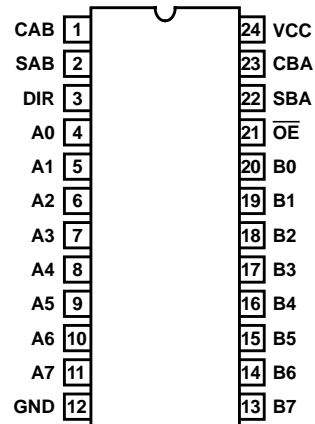
The Intersil HCTS646MS is a Radiation Hardened Three-State Octal Bus Transceiver/Register with Non-Inverting outputs. This device is a bus transceiver with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on a High-to-Low transition of either CAB or CBA clock inputs. Output enable (\overline{OE}) and Direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the \overline{OE} pin is LOW. In the high impedance mode (\overline{OE} high), A data can be stored in one register and B data in the other register. Data at the A or B terminals can be clocked into the storage flip-flops at any time.

The HCTS646MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

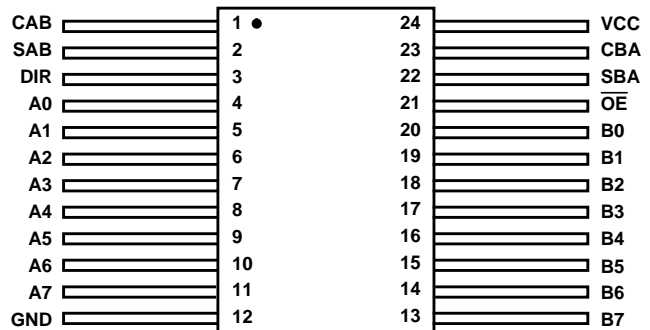
The HCTS646MS is supplied in a 24 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

24 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T24
TOP VIEW



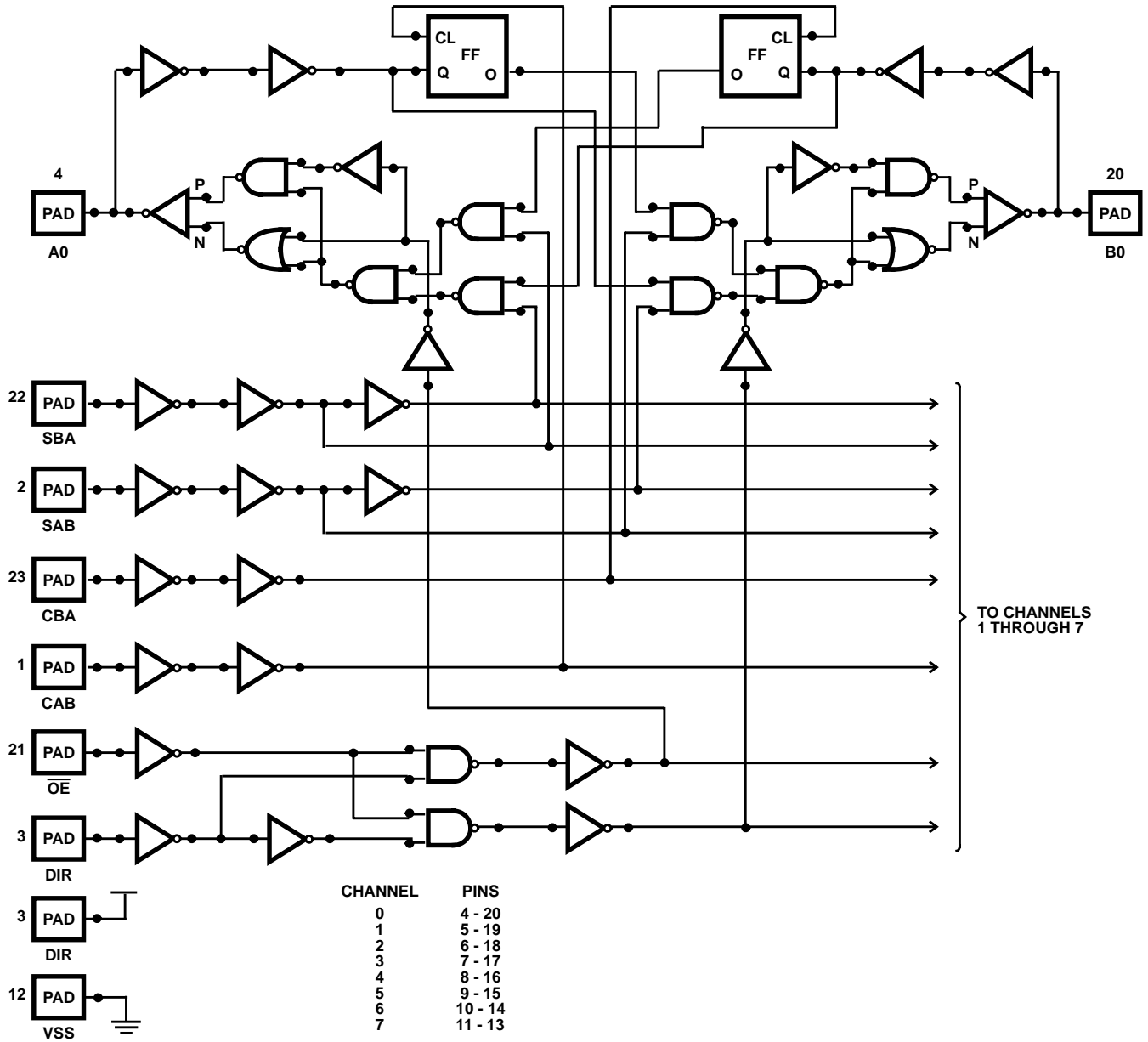
24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFF4-F24
TOP VIEW



Ordering Information

| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|-----------------|-------------------|-----------------------------|--------------------------|
| HCTS646DMSR | -55°C to +125°C | Intersil Class S Equivalent | 24 Lead SBDIP |
| HCTS646KMSR | -55°C to +125°C | Intersil Class S Equivalent | 24 Lead Ceramic Flatpack |
| HCTS646D/Sample | +25°C | Sample | 24 Lead SBDIP |
| HCTS646K/Sample | +25°C | Sample | 24 Lead Ceramic Flatpack |
| HCTS646HMSR | +25°C | Die | Die |

Functional Diagram



TRUTH TABLE

| INPUTS | | | | | | DATA I/O* | | OPERATION OR FUNCTION |
|-----------------|-----|--------|--------|-----|-----|---------------------|---------------------|--|
| \overline{OE} | DIR | CAB | CBA | SAB | SBA | A0 THRU A7 | B0 THRU B7 | |
| X | X | | X | X | X | Input Not Specified | Not Specified Input | Store A, B Unspecified |
| X | X | X | | X | X | Input Not Specified | Input | Store B, A Unspecified |
| H | X | | | X | X | Input | Input | Store A and B Data |
| H | X | H or L | H or L | X | X | Input | Input | Isolation, Hold Storage |
| L | L | X | X | X | L | Output | Input | Real-Time \overline{B} Data to A Bus |
| L | L | X | H or L | X | H | Output | Input | Stored \overline{B} Data to A Bus |
| L | H | X | X | L | X | Input | Output | Real-Time \overline{A} Data to B Bus |
| L | H | H or L | X | H | X | Input | Output | Stored \overline{A} Data to B Bus |

Specifications HCTS646MS

Absolute Maximum Ratings

| | |
|---|--------------------|
| Supply Voltage (VCC) | -0.5V to +7.0V |
| Input Voltage Range, All Inputs | -0.5V to VCC +0.5V |
| DC Input Current, Any One Input | ±10mA |
| DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal) | ±25mA |
| Storage Temperature Range (TSTG) | -65°C to +150°C |
| Lead Temperature (Soldering 10sec) | +265°C |
| Junction Temperature (TJ) | +175°C |
| ESD Classification | Class 1 |

Reliability Information

| | | |
|--|---------------|---------------|
| Thermal Resistance | θ_{JA} | θ_{JC} |
| SBDIP Package | 65°C/W | 25°C/W |
| Ceramic Flatpack Package | 89°C/W | 24°C/W |
| Maximum Package Power Dissipation at +125°C Ambient | | |
| SBDIP Package | 0.77W | |
| Ceramic Flatpack Package | 0.56W | |
| If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate: | | |
| SBDIP Package | 15.4mW/°C | |
| Ceramic Flatpack Package | 11.2mW/°C | |

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

| | | | |
|--|-----------------|--------------------------|--------------|
| Supply Voltage | +4.5V to +5.5V | Input Low Voltage (VIL) | 0.0V to 0.8V |
| Input Rise and Fall Times at 4.5V VCC (TR, TF) | .500ns Max | Input High Voltage (VIH) | VCC/2 to VCC |
| Operating Temperature Range (TA) | -55°C to +125°C | | |

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUB- GROUPS | TEMPERATURE | LIMITS | | UNITS |
|---------------------------------------|--------|---|---------------------------|----------------------|-------------|------|-------|
| | | | | | MIN | MAX | |
| Quiescent Current | ICC | VCC = 5.5V, VIN = VCC or GND | 1 | +25°C | - | 40 | µA |
| | | | 2, 3 | +125°C, -55°C | - | 750 | µA |
| Output Current (Sink) | IOL | VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V | 1 | +25°C | 7.2 | - | mA |
| | | | 2, 3 | +125°C, -55°C | 6.0 | - | mA |
| Output Current (Source) | IOH | VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V | 1 | +25°C | -7.2 | - | mA |
| | | | 2, 3 | +125°C, -55°C | -6.0 | - | mA |
| Output Voltage Low | VOL | VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | - | 0.1 | V |
| | | VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | - | 0.1 | V |
| Output Voltage High | VOH | VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | VCC -0.1 | - | V |
| | | VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | VCC -0.1 | - | V |
| Input Leakage Current | IIN | VCC = 5.5V, VIN = VCC or GND | 1 | +25°C | - | ±0.5 | µA |
| | | | 2, 3 | +125°C, -55°C | - | ±5.0 | µA |
| Three-State Output Leakage Current | IOZ | Applied Voltage = 0V or VCC, VCC = 5.5V | 1 | +25°C | - | ±1 | µA |
| | | | 2, 3 | +125°C, -55°C | - | ±50 | µA |
| Noise Immunity Functional Test | FN | VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2) | 7, 8A, 8B | +25°C, +125°C, -55°C | - | - | - |

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, $VO \geq 4.0V$ is recognized as a logic "1", and $VO \leq 0.5V$ is recognized as a logic "0".

Specifications HCTS646MS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | (NOTES 1, 2) CONDITIONS | GROUP A SUB- GROUPS | TEMPERATURE | LIMITS | | UNITS |
|----------------------------|---------------|----------------------------|---------------------------|---------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| A Data to B Bus (Store) | TPLH, TPHL | VCC = 4.5V | 9 | +25°C | 2 | 31 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 36 | ns |
| B Data to A Bus (Store) | TPLH, TPHL | VCC = 4.5V | 9 | +25°C | 2 | 32 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 37 | ns |
| A Data to B Bus | TPLH, TPHL | VCC = 4.5V | 9 | +25°C | 2 | 24 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 27 | ns |
| B Data to A Bus | TPLH, TPHL | VCC = 4.5V | 9 | +25°C | 2 | 24 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 27 | ns |
| Select to Data | TPLH, TPHL | VCC = 4.5V | 9 | +25°C | 2 | 30 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 34 | ns |
| DIR to Output | TPLZ, TPHZ | VCC = 4.5V | 9 | +25°C | 2 | 28 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 31 | ns |
| Enable to Output | TPLZ, TPHZ | VCC = 4.5V | 9 | +25°C | 2 | 28 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 31 | ns |
| DIR to Output | TPZL, TPZH | VCC = 4.5V | 9 | +25°C | 2 | 28 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 34 | ns |
| Enable to Output | TPZL, TPZH | VCC = 4.5V | 9 | +25°C | 2 | 30 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 36 | ns |

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume $R_L = 500\Omega$, $C_L = 50\text{pF}$, Input $T_R = T_F = 3\text{ns}$, $V_{IL} = \text{GND}$, $V_{IH} = 3\text{V}$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|----------------------------------|---------------|----------------------|-------|---------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Capacitance Power Dissipation | CPD | VCC = 5.0V, f = 1MHz | 1 | +25°C | - | 54 | pF |
| | | | 1 | +125°C, -55°C | - | 123 | pF |
| Input Capacitance | CIN | VCC = 5.0V, f = 1MHz | 1 | +25°C | - | 10 | pF |
| | | | 1 | +125°C | - | 10 | pF |
| Output Transition Time | TTHL, TTLH | VCC = 4.5V | 1 | +25°C | - | 12 | ns |
| | | | 1 | +125°C, -55°C | - | 18 | ns |
| Max Operating Frequency | FMAX | VCC = 4.5V | 1 | +25°C | - | 25 | MHz |
| | | | 1 | +125°C, -55°C | - | 17 | MHz |
| Setup Time Data to Clock | TSU | VCC = 4.5V | 1 | +25°C | 12 | - | ns |
| | | | 1 | +125°C, -55°C | 18 | - | ns |
| Hold Time Data to Clock | TH | VCC = 4.5V | 1 | +25°C | 5 | - | ns |
| | | | 1 | +125°C, -55°C | 5 | - | ns |
| Pulse Width Clocks | TW | VCC = 4.5V | 1 | +25°C | 25 | - | ns |
| | | | 1 | +125°C, -55°C | 38 | - | ns |

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

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TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | (NOTES 1, 2) CONDITIONS | TEMPERATURE | 200K RAD LIMITS | | UNITS |
|------------------------------------|---------------|---|-------------|--------------------|------|-------|
| | | | | MIN | MAX | |
| Quiescent Current | ICC | VCC = 5.5V, VIN = VCC or GND | +25°C | - | 0.75 | mA |
| Output Current (Sink) | IOL | VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V | +25°C | 6.0 | - | mA |
| Output Current (Source) | IOH | VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V | +25°C | -6.0 | - | mA |
| Output Voltage Low | VOL | VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V, IOL = 50µA | +25°C | - | 0.1 | V |
| Output Voltage High | VOH | VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V, IOH = -50µA | +25°C | VCC -0.1 | - | V |
| Input Leakage Current | IIN | VCC = 5.5V, VIN = VCC or GND | +25°C | - | ±5 | µA |
| Three-State Output Leakage Current | IOZ | Applied Voltage = 0V or VCC, VCC = 5.5V | +25°C | - | ±50 | µA |
| Noise Immunity Functional Test | FN | VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 3) | +25°C | - | - | - |
| A Data to B Bus (Store) | TPLH, TPHL | VCC = 4.5V | +25°C | 2 | 36 | ns |
| B Data to A Bus (Store) | TPLH, TPHL | VCC = 4.5V | +25°C | 2 | 37 | ns |
| A Data to B Bus | TPLH, TPHL | VCC = 4.5V | +25°C | 2 | 27 | ns |
| B Data to A Bus | TPLH, TPHL | VCC = 4.5V | +25°C | 2 | 27 | ns |
| Select to Data | TPLH, TPHL | VCC = 4.5V | +25°C | 2 | 34 | ns |
| DIR to Output | TPLZ, TPHZ | VCC = 4.5V | +25°C | 2 | 31 | ns |
| Enable to Output | TPLZ, TPHZ | VCC = 4.5V | +25°C | 2 | 31 | ns |
| DIR to Output | TPZL, TPZH | VCC = 4.5V | +25°C | 2 | 34 | ns |
| Enable to Output | TPZL, TPZH | VCC = 4.5V | +25°C | 2 | 36 | ns |

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

| PARAMETER | GROUP B SUBGROUP | DELTA LIMIT |
|-----------|---------------------|----------------|
| ICC | 5 | 12µA |
| IOL/IOH | 5 | -15% of 0 Hour |
| IOZL/IOZH | 5 | ±200nA |

Specifications HCTS646MS

TABLE 6. APPLICABLE SUBGROUPS

| CONFORMANCE GROUPS | | METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|--------------------------------|--------------|-------------|---------------------------------------|------------------------------|
| Initial Test (Preburn-In) | | 100%/5004 | 1, 7, 9 | ICC, IOL/H, IOZL/H |
| Interim Test I (Postburn-In) | | 100%/5004 | 1, 7, 9 | ICC, IOL/H, IOZL/H |
| Interim Test II (Postburn-In) | | 100%/5004 | 1, 7, 9 | ICC, IOL/H, IOZL/H |
| PDA | | 100%/5004 | 1, 7, 9, Deltas | |
| Interim Test III (Postburn-In) | | 100%/5004 | 1, 7, 9 | |
| PDA | | 100%/5004 | 1, 7, 9, Deltas | |
| Final Test | | 100%/5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A (Note 1) | | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | Sample/5005 | 1, 7, 9 | |
| Group D | | Sample/5005 | 1, 7, 9 | |

NOTE: 1. Alternate Group A inspection in accordance with Method 5005 of Mil-Std-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

| CONFORMANCE GROUPS | METHOD | TEST | | READ AND RECORD | |
|--------------------|--------|---------|----------|-----------------|------------------|
| | | PRE RAD | POST RAD | PRE RAD | POST RAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 (Note 1) |

NOTE: Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

| OPEN | GROUND | 1/2 VCC = 3V ± 0.5V | VCC = 6V ± 0.5V | OSCILLATOR | |
|----------------------------|-------------------|---------------------|-----------------|------------|---------|
| | | | | 50kHz | 25kHz |
| STATIC I BURN-IN (Note 1) | | | | | |
| 4 - 11 | 1 - 3, 12 - 23 | - | 24 | - | - |
| STATIC II BURN-IN (Note 1) | | | | | |
| - | 12 | - | 1 - 11, 13 - 24 | - | - |
| DYNAMIC BURN-IN (Note 2) | | | | | |
| - | 1 - 3, 12, 21, 22 | 4 - 11 | 24 | 23 | 13 - 20 |

NOTES:

1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

| OPEN | GROUND | VCC = 5V ± 0.5V |
|------|--------|-----------------|
| - | 12 | 1 - 11, 13 - 24 |

NOTE: Each pin except VCC and GND will have a resistor of 47kΩ ± 5% for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

HCTS646MS

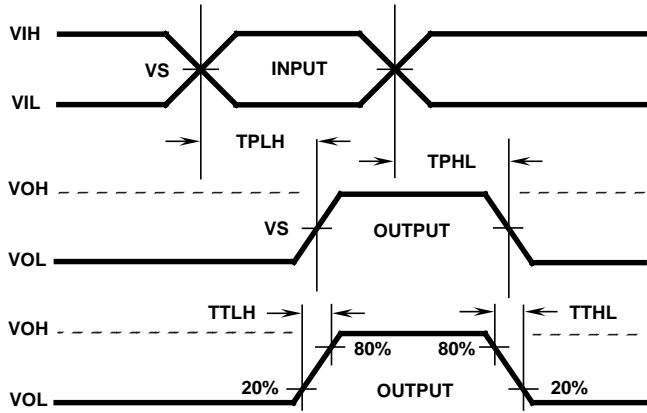
Intersil Space Level Product Flow - 'MS'

| | |
|--|--|
| Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM) | 100% Interim Electrical Test 1 (T1) |
| GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects | 100% Delta Calculation (T0-T1) |
| 100% Nondestructive Bond Pull, Method 2023 | 100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015 |
| Sample - Wire Bond Pull Monitor, Method 2011 | 100% Interim Electrical Test 2 (T2) |
| Sample - Die Shear Monitor, Method 2019 or 2027 | 100% Delta Calculation (T0-T2) |
| 100% Internal Visual Inspection, Method 2010, Condition A | 100% PDA 1, Method 5004 (Notes 1 and 2) |
| 100% Temperature Cycle, Method 1010, Condition C, 10 Cycles | 100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015 |
| 100% Constant Acceleration, Method 2001, Condition per Method 5004 | 100% Interim Electrical Test 3 (T3) |
| 100% PIND, Method 2020, Condition A | 100% Delta Calculation (T0-T3) |
| 100% External Visual | 100% PDA 2, Method 5004 (Note 2) |
| 100% Serialization | 100% Final Electrical Test |
| 100% Initial Electrical Test (T0) | 100% Fine/Gross Leak, Method 1014 |
| 100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015 | 100% Radiographic, Method 2012 (Note 3) |
| | 100% External Visual, Method 2009 |
| | Sample - Group A, Method 5005 (Note 4) |
| | 100% Data Package Generation (Note 5) |

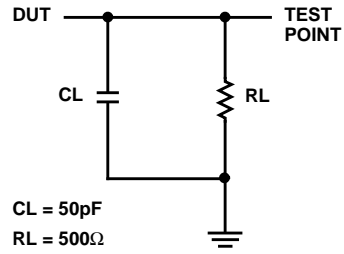
NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
 - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
 - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
 - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
 - X-Ray report and film. Includes penetrometer measurements.
 - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
 - Lot Serial Number Sheet (Good units serial number and lot number).
 - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
 - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Timing Diagrams



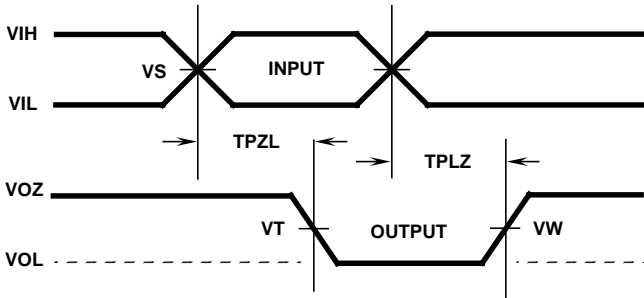
AC Load Circuit



AC VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|-----------|------|-------|
| VCC | 4.50 | V |
| V_{IH} | 3.00 | V |
| V_S | 1.30 | V |
| V_{IL} | 0 | V |
| GND | 0 | V |

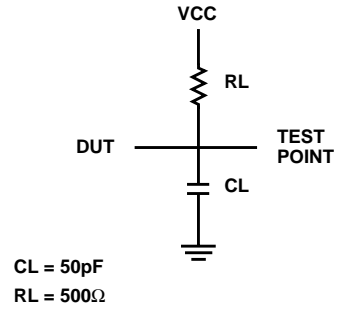
Three-State Low Timing Diagrams



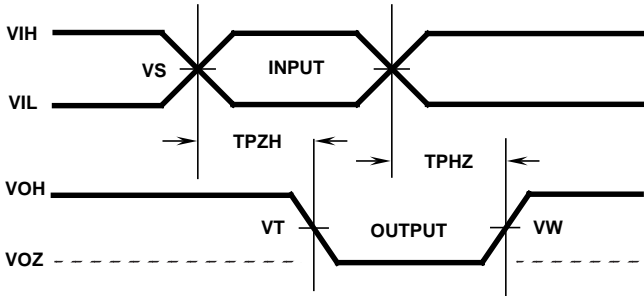
THREE-STATE LOW VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|-----------|------|-------|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VT | 1.30 | V |
| VW | 0.90 | V |
| GND | 0 | V |

Three-State Load Circuit



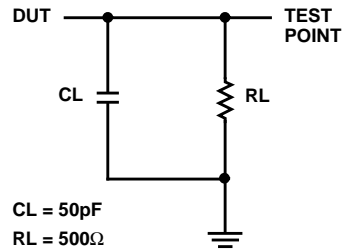
Three-State High Timing Diagrams



THREE-STATE HIGH VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|-----------|------|-------|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VT | 1.30 | V |
| VW | 3.60 | V |
| GND | 0 | V |

Three-State Load Circuit



HCTS646MS

Die Characteristics

DIE DIMENSIONS:

124 x 110 mils

METALLIZATION:

Type: SiAl

Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2

Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5 \text{A/cm}^2$

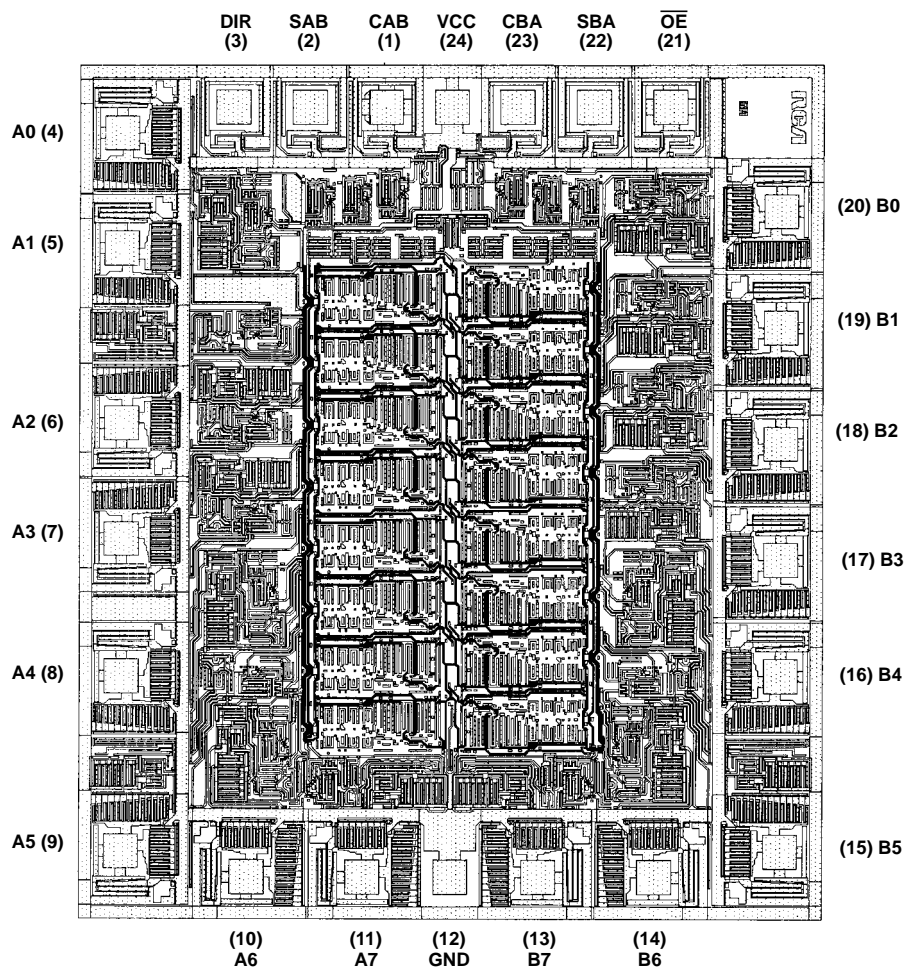
BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$

4 mils x 4 mils

Metallization Mask Layout

HCTS646MS



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS646 is TA14420A.

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