Quad SPST, CMOS Analog Switches

The DG201A and DG202 quad SPST analog switches are designed using Intersil's 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to $30V_{P-P}$ in the OFF state, the DG201A and DG202 offer the advantages of low ON resistance (≤175Ω), wide input signal range (±15V) and provide both TTL and CMOS compatibility.

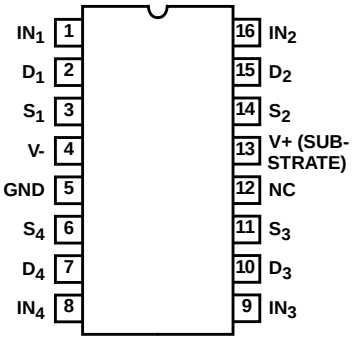
The DG201A and DG202 are specification and pinout compatible with the industry standard devices.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
DG201AAK	-55 to 125	16 Ld CERDIP	F16.3
DG201ABK	-25 to 85	16 Ld CERDIP	F16.3
DG201ACJ	0 to 70	16 Ld PDIP	E16.3
DG201ACY	0 to 70	16 Ld SOIC	M16.3
DG202AK	-55 to 125	16 Ld CERDIP	F16.3
DG202CJ	0 to 70	16 Ld PDIP	E16.3

Pinout

DG201A, DG202
(CERDIP, PDIP, SOIC)
TOP VIEW

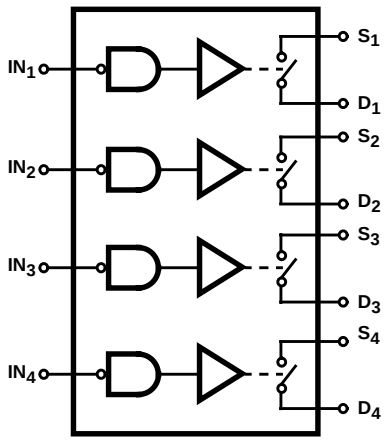


Features

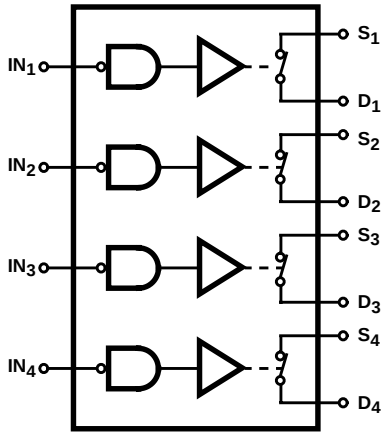
- Input Signal Range . . . . . ±15V
- Low $r_{DS(ON)}$ (Max) 175Ω
- TTL, CMOS Compatible
- Latch-Up Proof
- True Second Source
- Maximum Supply Ratings 44V
- Logic Inputs Accept Negative Voltages

Functional Block Diagrams

DG201A



DG202



SWITCHES SHOWN FOR LOGIC "1" INPUT

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

Absolute Maximum Ratings

V+ to V- 44V
V- to Ground. . . . . -25V
V_{IN} to Ground (Note 1) . . . . . (V-) -2V to (V+) +2V
V_S or V_D to V+ (Note 1). . . . . +2 to (V-) -2V
V_S or V_D to V- (Note 1) . . . . . -2 to (V+) +2V
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) 70mA

Operating Conditions

Temperature Range
"A" Suffix. . . . . -55^oC to 125^oC
"B" Suffix. . . . . -25^oC to 85^oC
"C" Suffix . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20
PDIP Package	100	N/A
SOIC Package	100	N/A

Maximum Junction Temperature
Ceramic Package . . . . . 175^oC
Plastic Package . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on V_S, V_D, or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V+ = 15V, V- = -15V, GND = 0V, $T_A = 25^oC$

PARAMETER	TEST CONDITIONS		"A" SUFFIX MIN	"A" SUFFIX (NOTE 3) TYP	"A" SUFFIX MAX	"B" AND "C" SUFFIX MIN	"B" AND "C" SUFFIX (NOTE 3) TYP	"B" AND "C" SUFFIX MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-ON Time, t_{ON}	See Figure 1		-	480	600	-	480	-	ns
Turn-OFF Time, t_{OFF}	See Figure 1		-	370	450	-	370	-	ns
Charge Injection, Q	C_L = 1nF, R_S = 0, V_S = 0V		-	20	-	-	20	-	pC
OFF Isolation, OIRR	V_{IN} = 5V, R_L = 75Ω, V_S = 2.0V, f = 100kHz		-	70	-	-	70	-	dB
Crosstalk (Channel to Channel), CCRR			-	-90	-	-	-90	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 140kHz, V_{IN} = 5V, V_S = V_D = 0V		-	5.0	-	-	5.0	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$			-	5.0	-	-	5.0	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$			-	16	-	-	16	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Current with Voltage High, I_{IH}	V_{IN} = 2.4V		-1.0	-0.0004	-	-1.0	-0.0004	-	µA
	V_{IN} = 15V		-	0.003	1.0	-	0.003	1.0	µA
Input Current with Voltage Low, I_{IL}	V_{IN} = 0V		-1.0	-0.0004	-	-1.0	-0.0004	-	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_{ANALOG}			-15	-	15	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	115	175	-	115	200	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	0.01	1.0	-	0.01	5.0	nA
		V_S = -14V, V_D = 14V	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.01	1.0	-	0.01	5.0	nA
		V_S = 14V, V_D = -14V	-1.0	-0.02	-	-5.0	-0.02	-	nA

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, $T_A = 25^oC$ (Continued)

PARAMETER	TEST CONDITIONS		"A" SUFFIX MIN	"A" SUFFIX (NOTE 3) TYP	"A" SUFFIX MAX	"B" AND "C" SUFFIX MIN	"B" AND "C" SUFFIX (NOTE 3) TYP	"B" AND "C" SUFFIX MAX	UNITS
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	0.1	1.0	-	0.1	5.0	µA
		$V_D = V_S$ = -14V	-1.0	-0.15	-	-5.0	-0.15	-	µA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	All Channels ON or OFF		-	0.9	2	-	0.9	2	mA
Negative Supply Current, I-			-1	-0.3	-	-1	-0.3	-	mA

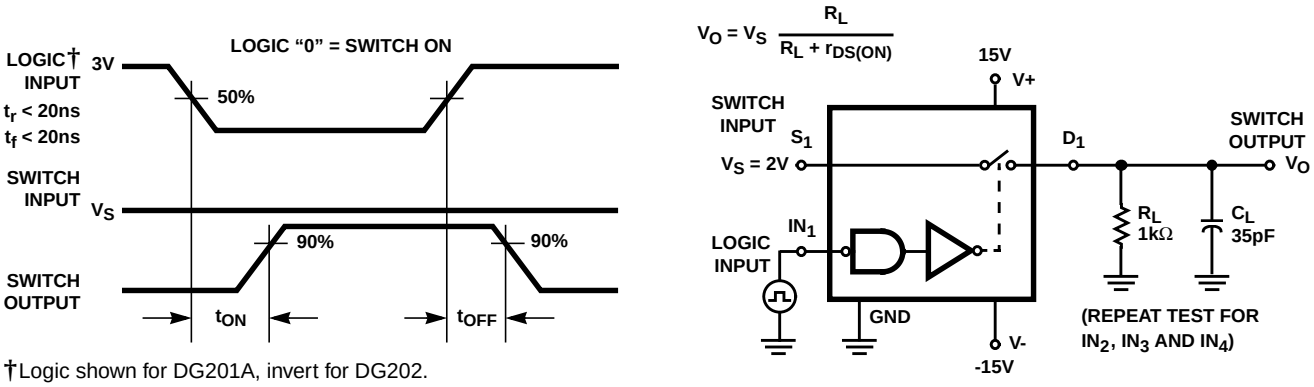
Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, T_A Over Operating Temperature Range

PARAMETER	TEST CONDITIONS		"A" SUFFIX MIN	"A" SUFFIX (NOTE 3) TYP	"A" SUFFIX MAX	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Current with Voltage High, I_{IH}	V_{IN} = 2.4V		-10	-	-	µA
	V_{IN} = 15V		-	-	10	µA
Input Current with Voltage Low, I_{IL}	V_{IN} = 0V		-10	-	-	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}			-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	-	250	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	-	100	nA
		V_S = -14V, V_D = 14V	-100	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	-	100	nA
		V_S = 14V, V_D = -14V	-100	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	-	200	µA
		$V_D = V_S$ = -14V	-200	-	-	µA

NOTES:

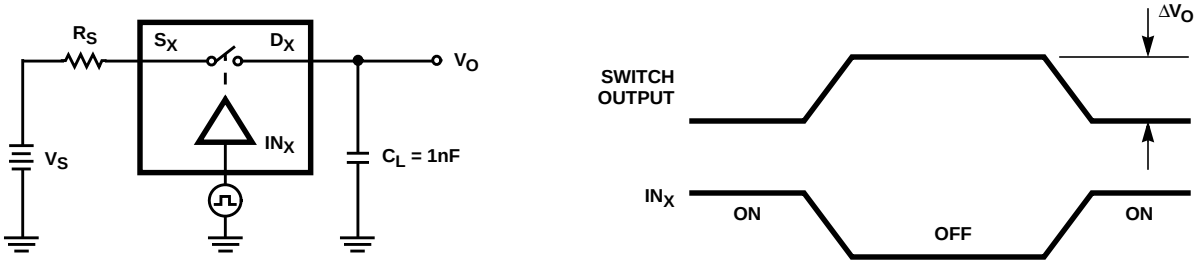
3. Typical values are for design aid only, not guaranteed and not subject to production testing.
4. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
5. $I_{D(ON)}$ is leakage from driver into ON switch.

Test Circuits and Waveforms



†Logic shown for DG201A, invert for DG202.

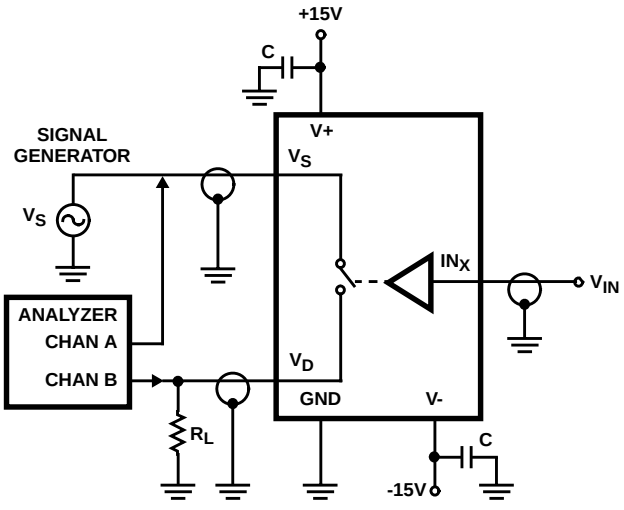
FIGURE 1. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT AND MEASUREMENT POINTS



NOTES:

6. ΔV_O = Measured voltage error due to charge injection.
7. The error in coulombs is Q = C_L x ΔV_O.

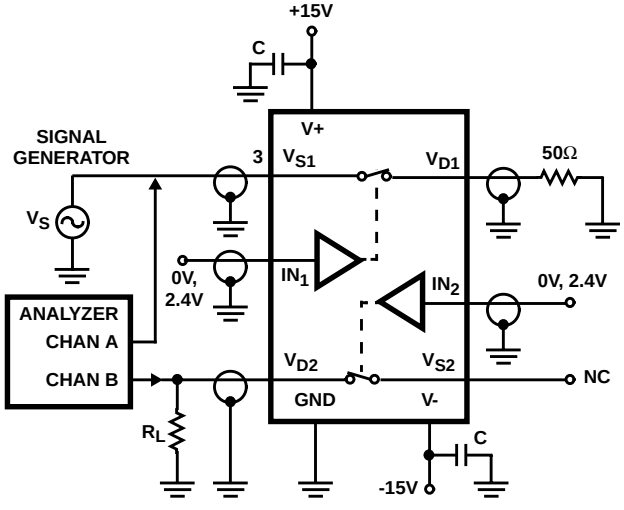
FIGURE 2. CHARGE INJECTION TEST CIRCUIT AND MEASUREMENT POINTS



C = 0.001µF||0.1µF
Chip Capacitors

$$OIRR = 20 \text{ Log} \left| \frac{V_S}{V_D} \right|$$

FIGURE 3. OFF ISOLATION TEST CIRCUIT

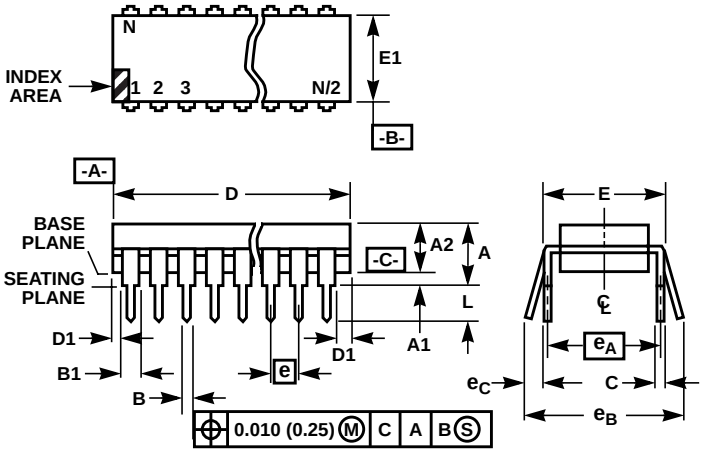


C = 0.001µF||0.1µF
Chip Capacitors

$$CCRR = 20 \text{ Log} \left| \frac{V_{S1}}{V_{D2}} \right|$$

FIGURE 4. CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT

Dual-In-Line Plastic Packages (PDIP)



NOTES:

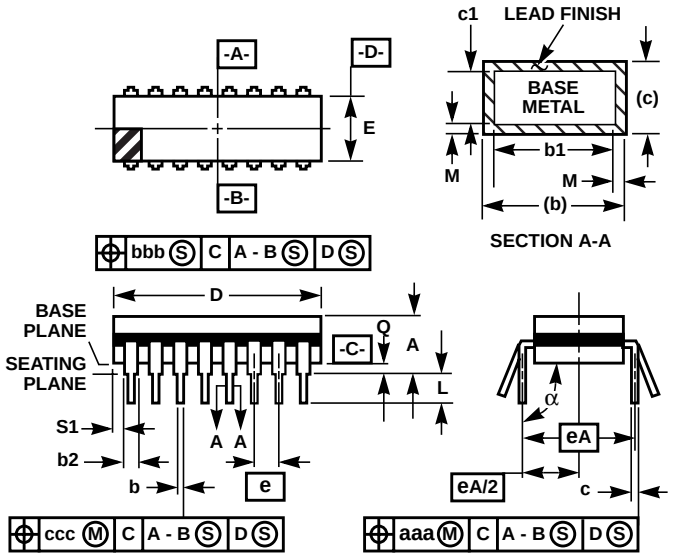
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

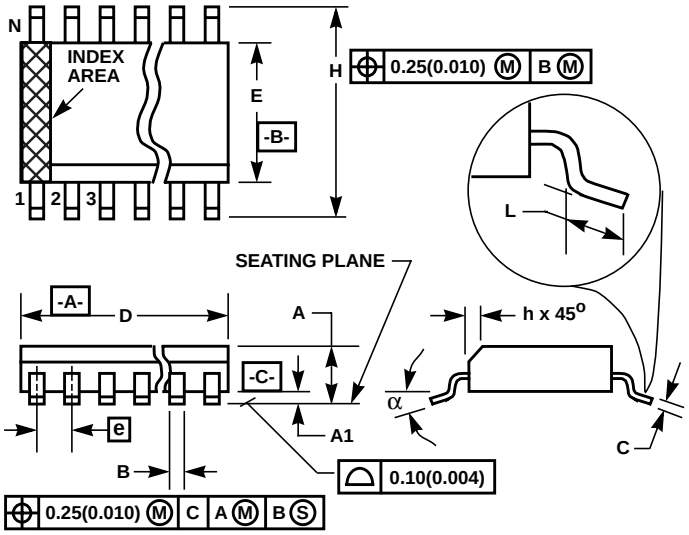
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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