

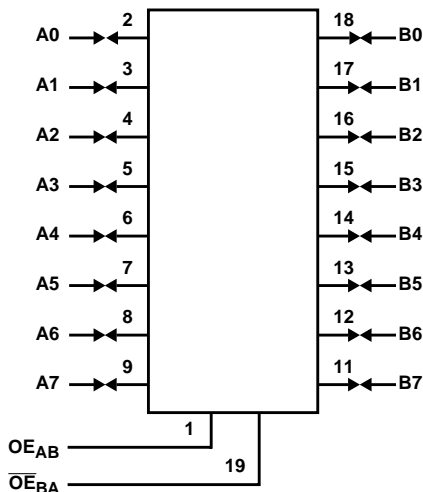
## Octal Bus Transceiver Three-State, Non-Inverting

July 1998

### Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- Meets JEDEC Standard No. 20
- SCR - Latch-Up-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST/A/S with Significantly Reduced Power Consumption
- Functionally and Pin-Compatible with Industry 54 Bipolar Types in the FAST, AS and S Series
- Balanced Propagation Delays
- Military Operating Temperature Range
  - Ceramic (CERDIP) 54 Series: ..... -55 to 125°C
- $\pm 24\text{mA}$  Output Drive Current, Drives  $75\Omega$  Lines without Need for Terminations
- Fan Out (Over Temperature)
  - ACL Loads ..... 2400
  - FAST Loads..... 15
  - AS Loads..... 48
- Operation Voltage ..... 4.5V to 5.5V

### Functional Diagram



### Description

The CD54ACT623F3A is an octal bus transceiver that utilizes Harris Advanced CMOS Logic technology. It is a non-inverting three-state bidirectional transceiver-buffer that allows for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus depending on the logic levels of the Output Enable ( $OE_{AB}$ ,  $\overline{OE}_{BA}$ ) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling  $OE_{AB}$  and  $\overline{OE}_{BA}$ . Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high-impedance, both sets of bus lines will remain in their last states.

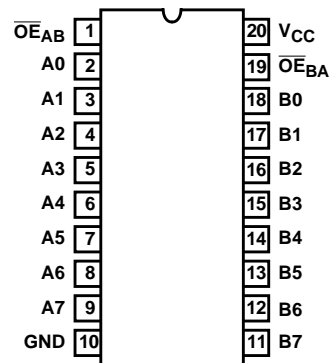
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54ACT623F3A	-55 to 125	20 Ld CERDIP	F20.3

NOTE:

1. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout



## CD54ACT623F3A

### Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to 6V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 50mA$   
 DC Output Source or Sink Current per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 50mA$   
 DC  $V_{CC}$  or Ground Current,  $I_{CC}$  or  $I_{GND}$  (Note 2) .....  $\pm 100mA$

### Thermal Information

Thermal Resistance (Typical, Note 4)       $\theta_{JA}$  ( $^{\circ}C/W$ )     $\theta_{JC}$  ( $^{\circ}C/W$ )  
 CERDIP Package ..... 80      22  
 Maximum Junction Temperature (Hermetic Package or Die) ... 175 $^{\circ}C$   
 Maximum Storage Temperature Range ..... -65 $^{\circ}C$  to 150 $^{\circ}C$   
 Maximum Lead Temperature (Soldering 10s) ..... 300 $^{\circ}C$

### Operating Conditions

Temperature Range,  $T_A$  ..... -55 $^{\circ}C$  to 125 $^{\circ}C$   
 Supply Voltage Range,  $V_{CC}$  (Note 3) ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

#### NOTES:

2. For up to 4 outputs per device, add  $\pm 25mA$  for each additional output.
3. Unless otherwise specified, all voltages are referenced to ground.
4.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	$V_{IH}$	-	-	4.5 to 5.5	2 (Note 5)	-	2 (Note 5)	-	V
Low Level Input Voltage	$V_{IL}$	-	-	4.5 to 5.5	-	0.8 (Note 5)	-	0.8 (Note 5)	V
High Level Output Voltage	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.05	4.5	4.4	-	4.4	-	V
			-24	4.5	3.94 (Note 5)	-	3.7 (Note 5)	-	V
			-50 (Note 6, 7)	5.5	-	-	3.85	-	V
Low Level Output Voltage	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.05	4.5	-	0.1	-	0.1	V
			24	4.5	-	0.36 (Note 5)	-	0.5 (Note 5)	V
			50 (Note 6, 7)	5.5	-	-	-	1.65	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	5.5	-	$\pm 0.1$ (Note 5)	-	$\pm 1$ (Note 5)	$\mu A$
Three-State or Leakage Current	$I_{OZ}$	$V_{IH}$ or $V_{IL}$ $V_O = V_{CC}$ or GND	-	5.5	-	$\pm 0.5$ (Note 5)	-	$\pm 10$ (Note 5)	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	8 (Note 5)	-	160 (Note 5)	$\mu A$
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	$\Delta I_{CC}$	$V_{CC}$ -2.1	-	4.5 to 5.5	-	2.4	-	3	mA

#### NOTES:

5. Tested 100%.
6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum transmission-line-drive capability of 75 $\Omega$  for 54ACT Series.

# CD54ACT623F3A

## ACT Input Load Table

INPUT	UNIT LOAD
An, Bn	0.83
$\overline{OE}_{BA}$	0.64
$OE_{AB}$	0.15

NOTE: Unit load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

## Switching Specifications Input $t_r$ , $t_f = 3ns$ , $C_L = 50pF$ (Worst Case)

PARAMETER	SYMBOL	$V_{CC}$ (V)	-55°C TO 125°C			UNITS
			MIN	TYP	MAX	
Propagation Delay, Data to Output	$t_{PLH}$ , $t_{PHL}$	5 (Note 10)	1.8	-	10.6 (Note 8)	ns
Propagation Delay, Output Disable to Output	$t_{PLZ}$ , $t_{PHZ}$	5	2.5	-	14.4 (Note 8)	ns
Propagation Delay, Output Enable to Output	$t_{PZL}$ , $t_{PZH}$	5	2.5	-	14.4 (Note 8)	ns
Minimum (Valley) $V_{OH}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OHV}$ See Figure 1	5	-	4 at 25°C	-	V
Maximum (Peak) $V_{OL}$ During Switching of Other Outputs (Output Under Test Not Switching)	$V_{OLP}$ See Figure 1	5	-	1 at 25°C	-	V
Three-State Output Capacitance	$C_O$	-	-	-	15	pF
Input Capacitance	$C_I$	-	-	-	10	pF
Power Dissipation Capacitance	$C_{PD}$ (Note 11)	-	-	79	-	pF

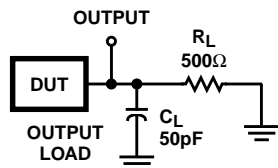
NOTES:

8. Limits tested 100%.
9. 3.3V Min = 3.6V, Max = 3V.
10. 5V Min = 5.5V, Max = 4.5V
11.  $C_{PD}$  is used to determine the dynamic power consumption per gate.  
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Burn-In Test Circuit Connections (Use DC II for F3A Burn-In and AC for Life Test)

DC	DC BURN-IN I			DC BURN-IN II		
	OPEN	GROUND	$V_{CC}$ (6V)	OPEN	GROUND	$V_{CC}$ (6V)
CD54ACT623	2-9	1, 10-19	20	11-18	10	1-9, 19, 20
AC	OPEN	GROUND	$1/2 V_{CC}$ (3V)	$V_{CC}$ (6V)	OSCILLATOR	
					50kHz	25kHz
CD54ACT623	-	10	11-18	19, 20	2-9	1

NOTE: Each pin except  $V_{CC}$  and Gnd will have a resistor of 2k $\Omega$ -47k $\Omega$ .



	CD54ACT
Input Level	3V
Input Switching Voltage, $V_S$	1.5V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$

FIGURE 1. PROPAGATION DELAY TIMES