

Features

- Transmission or Multiplexing of Analog or Digital Signals
- High Voltage Type (20V Rating)
- 20V Digital or $\pm 10V$ Peak-to-Peak Switching
- 280 Ω Typical On-State Resistance for 15V Operation
- Switch On-State Resistance Matched to Within 10 Ω Typ. Over 15V Signal Input Range
- High On/Off Output Voltage Ratio: 65dB Typ. at FIS = 10kHz, RL = 10k Ω
- High Degree of Linearity: <0.5% Distortion Typ. at FIS = 1kHz, VIS = 5Vp-p, VDD-VSS \geq 10V, RL = 10k Ω
- Extremely Low Off State Switch Leakage Resulting in Very Low Offset Current and High Effective Off State Resistance: 100pA Typ. at VDD-VSS = 18V, TA = 25°C
- Extremely High Control Input Impedance (Control circuit Isolated from Signal Circuit: 10¹² Ω Typ.)
- Low Crosstalk Between Switches: -50dB Typ. at FIS = 0.9MHz, RL = 1k Ω
- Matched Control Input to Signal Output Capacitance: Reduces Output Signal Transients
- Frequency Response, Switch On = 40MHz (Typ.)
- 100% Tested for Quiescent Current at 20V
- Maximum Control Input Current of 1 μ A at 18V Over Full Package Temperature Range; 100nA at 18V at +25°C
- 5V, 10V and 15V Parametric Ratings

Applications

- Analog Signal Switching/Multiplexing
- Signal Gating
- Squelch Control
- Chopper
- Modulator
- Demodulator
- Commutating Switch
- Digital Signal Switching/Multiplexing
- CMOS Logic Implementation
- Analog to Digital & Digital to Analog Conversion
- Digital Control of Frequency, Impedance, Phase, and Analog Signal Gain

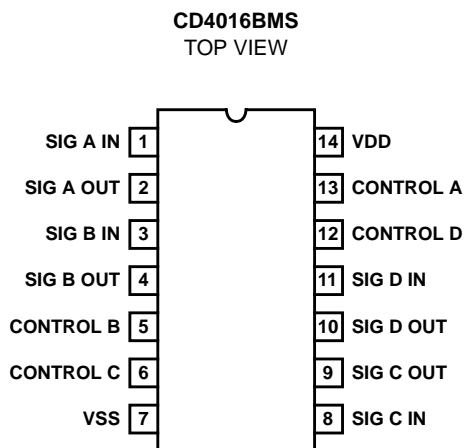
Description

CD4016BMS Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch on or off.

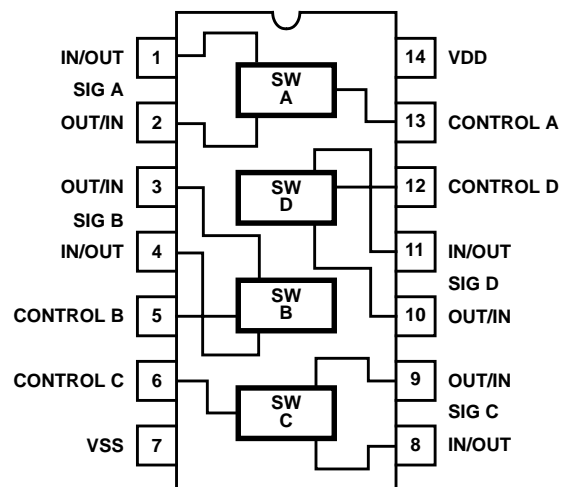
The CD4016BMS is supplied in these 14 lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout



Functional Diagram



Specifications CD4016BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input ±10mA
 Operating Temperature Range -55°C to +125°C
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to +150°C
 Lead Temperature (During Soldering) +265°C
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at +125°C
 For TA = -55°C to +100°C (Package Type D, F, K) 500mW
 For TA = +100°C to +125°C (Package Type D, F, K) Derate
 Linearity at 12mW/°C to 200mW
 Device Dissipation per Output Transistor 100mW
 For TA = Full Package Temperature Range (All Package Types)
 Junction Temperature +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
						MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
				3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VC = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input Leakage Current	IIH	VC = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
Input/Output Leakage Current (Switch Off)	IOZL	VDD = 18V, VC = 0V, VIS = 18V, VOS = 0V		1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
				3	-55°C	-100	-	nA
Input/Output Leakage Current (Switch Off)	IOZH	VDD = 18V, VIS = 18V, VOS = 0V		1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
				3	-55°C	-	100	nA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
On-State Resistance RL = 10K Returned to VDD-VSS/2	RON10	VIS = VDD or VSS, VDD = 10V		1	+25°C	-	660	Ω
				2	+125°C	-	960	Ω
				3	-55°C	-	600	Ω
				1	+25°C	-	2000	Ω
				2	+125°C	-	2600	Ω
				3	-55°C	-	1870	Ω
	RON15	VIS = VDD or VSS, VDD = 15V		1	+25°C	-	400	Ω
				2	+125°C	-	600	Ω
				3	-55°C	-	360	Ω
				1	+25°C	-	850	Ω
				2	+125°C	-	1230	Ω
				3	-55°C	-	775	Ω
Functional (Note 3)	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Switch Threshold RL = 100K to VDD	SWTHR5	VDD = 5V, VC = 1.5V, VIS = GND		1, 2, 3	+25°C, +125°C, -55°C	4.1	-	V
	SWTHR15	VDD = 15V, VC = 2V, VIS = GND		1, 2, 3	+25°C, +125°C, -55°C	14.1	-	V

Specifications CD4016BMS

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Control, Low (Note 2)	VILC	VDD = 5V, VOS = VDD, VIS = VSS, and VDD = 5V, VOS = VSS, VIS = VDD, IIS < 10 μ A	1	+25 $^{\circ}$ C	-	0.7	V
			2	+125 $^{\circ}$ C	-	0.4	V
			3	-55 $^{\circ}$ C	-	0.9	V
Control Input High Voltage (Note 2, Figure 12) VIS = VSS, and VIS = VDD	VIHC	VDD = 5V, IIS = .16mA, 4.6V < VOS < 0.4V	1	+25 $^{\circ}$ C	3.5	-	V
			2	+125 $^{\circ}$ C	3.5	-	V
			3	-55 $^{\circ}$ C	3.5	-	V
	VIHC	VDD = 15V, IIS = 1.2mA, 13.5V < VOS < 1.5V	1	+25 $^{\circ}$ C	11	-	V
			2	+125 $^{\circ}$ C	11	-	V
			3	-55 $^{\circ}$ C	11	-	V

- NOTES: 1. All voltages referenced to device GND, 100% testing being implemented.
 2. Go/No Go test with limits applied to inputs
 3. VDD = 2.8V/3V, RL = 100K to VDD
 VDD = 20V/18V, RL = 10K to VDD

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Signal Input to Signal Output	TPHL TPLH	VDD = 5V, VIN = VDD or GND (Notes 1, 2)	9	+25 $^{\circ}$ C	-	100	ns
			10, 11	+125 $^{\circ}$ C, -55 $^{\circ}$ C	-	135	ns
Propagation Delay Turn On	TPZH TPZL	VDD = 5V, VIN = VDD or GND (Notes 2, 3)	9	+25 $^{\circ}$ C	-	70	ns
			10, 11	+125 $^{\circ}$ C, -55 $^{\circ}$ C	-	95	ns

- NOTES:
 1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
 2. -55 $^{\circ}$ C and +125 $^{\circ}$ C limits guaranteed, 100% testing being implemented.
 3. CL = 50pF, RL = 1K, TR, TF < 20ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55 $^{\circ}$ C, +25 $^{\circ}$ C	-	0.25	μ A
				+125 $^{\circ}$ C	-	7.5	μ A
		VDD = 10V, VIN = VDD or GND	1, 2	-55 $^{\circ}$ C, +25 $^{\circ}$ C	-	0.5	μ A
				+125 $^{\circ}$ C	-	15	μ A
		VDD = 15V, VIN = VDD or GND	1, 2	-55 $^{\circ}$ C, +25 $^{\circ}$ C	-	0.5	μ A
				+125 $^{\circ}$ C	-	30	μ A
Input Voltage Control, Low	VILC	VDD = 10V, VOS = VDD, VIS = VSS and VOS = VSS, VIS = VDD IIS < 10 μ A	1, 2	+25 $^{\circ}$ C-55 $^{\circ}$ C	-	0.7	V
				+125 $^{\circ}$ C	-	0.4	V
				-55 $^{\circ}$ C	-	0.9	V

Specifications CD4016BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Control, High (See Figure 12)	VIHC	VDD = 10V, VIS = VDD or GND	1, 2	+25°C-55°C	7	-	V
			1, 2	+125°C	7	-	V
			1, 2	-55°C	7	-	V
Propagation Delay Signal Input to Signal Output	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	40	ns
		VDD = 15V	1, 2, 3	+25°C	-	30	ns
Propagation Delay Turn On	TPZH TPZL	VDD = 10V	1, 2, 4	+25°C	-	40	ns
		VDD = 15V	1, 2, 4	+25°C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K. Input TR, TF < 20ns.
4. CL = 50pF, RL = 1K

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

- NOTES: 1. All voltages referenced to device GND. 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns. 3. See Table 2 for +25°C limit. 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1μA
ON Resistance	RONDEL10	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

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TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2, 3

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± 0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	2, 3, 9, 10	1, 4-8, 11-13	14			
Static Burn-In 2 Note 1	2, 3, 9, 10	7	1, 4-6, 8, 11-14			
Dynamic Burn-In Note 1	-	7	14	2, 3, 9, 10	5, 6, 12, 13	1, 4, 8, 11
Irradiation Note 2	2, 3, 9, 10	7	1, 4-6, 8, 11-14			

NOTE:

- Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$; $VDD = 18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, $VDD = 10V \pm 0.5V$

Schematic Diagram

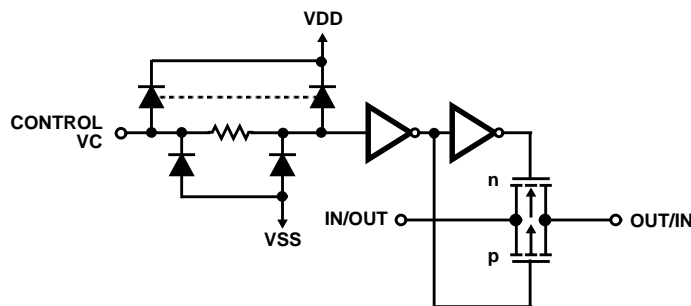


FIGURE 1. 1 OF 4 IDENTICAL SECTIONS

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Typical Performance Characteristics

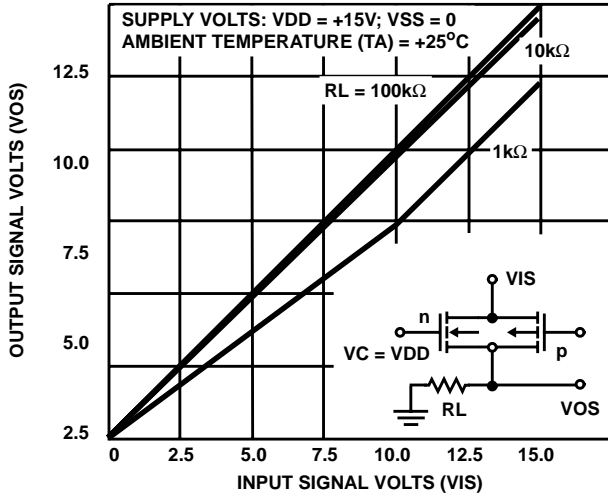


FIGURE 2. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +15V, VSS = 0V

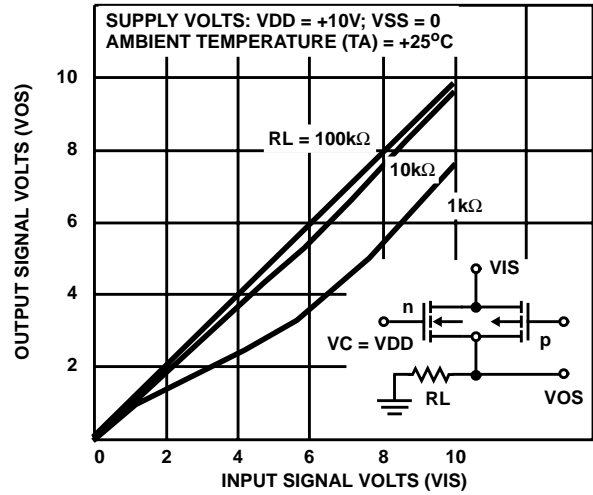


FIGURE 3. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +10V, VSS = 0V

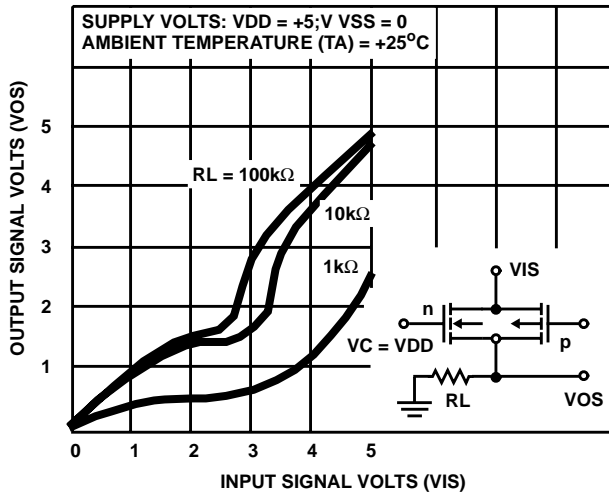


FIGURE 4. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +5V, VSS = 0V

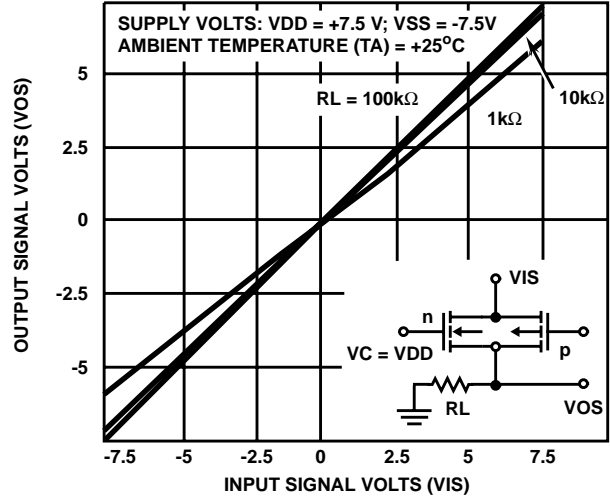


FIGURE 5. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +7.5V, VSS = -7.5V

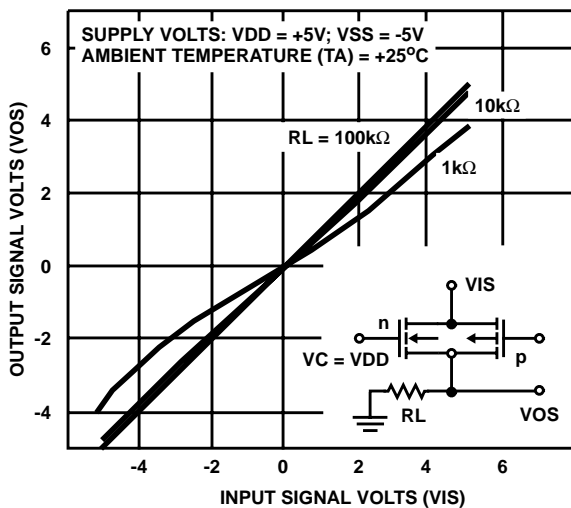


FIGURE 6. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +5V, VSS = -5V

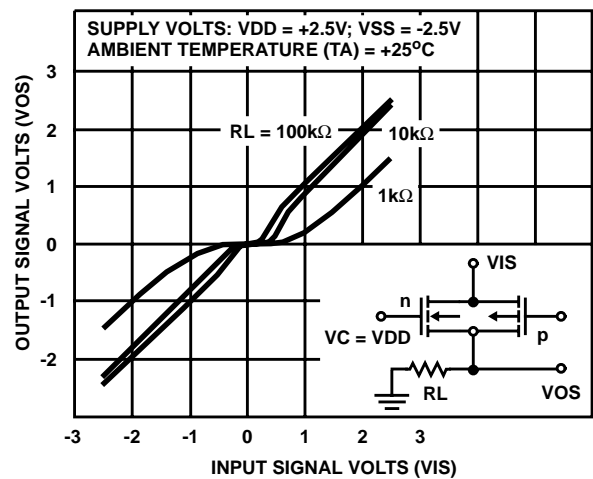


FIGURE 7. TYPICAL ON-STATE CHARACTERISTICS FOR 1 OF 4 SWITCHES WITH VDD = +2.5V, VSS = -2.5V

Typical Performance Characteristics (Continued)

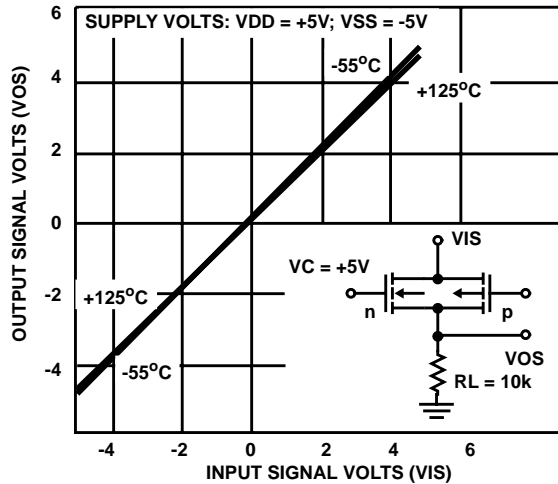


FIGURE 8. TYPICAL ON-STATE CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR 1 OF 4 SWITCHES WITH VDD = +5V, VSS = -5V

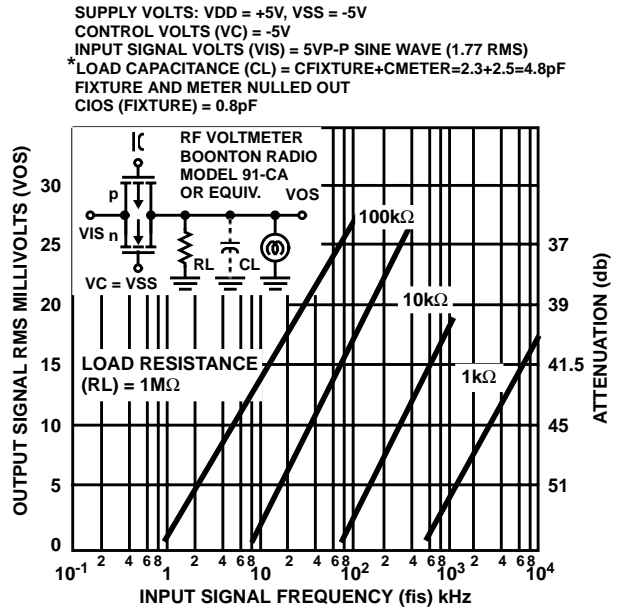


FIGURE 9. TYPICAL FEEDTHRU vs FREQUENCY - SWITCH OFF

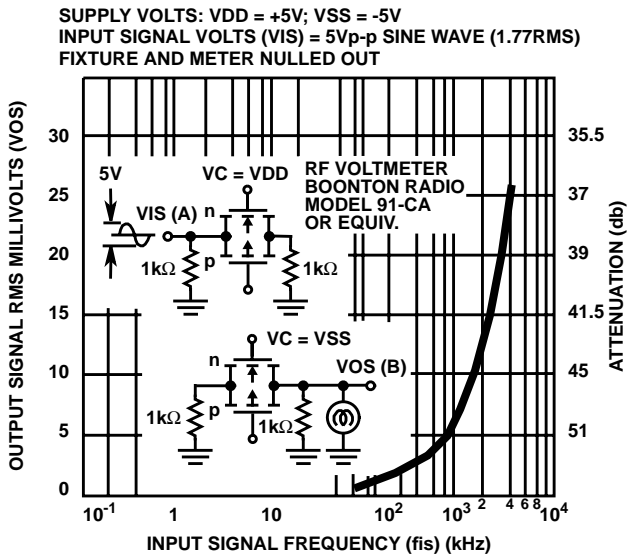


FIGURE 10. TYPICAL CROSTALK BETWEEN SWITCH CIRCUITS IN THE SAME PACKAGE

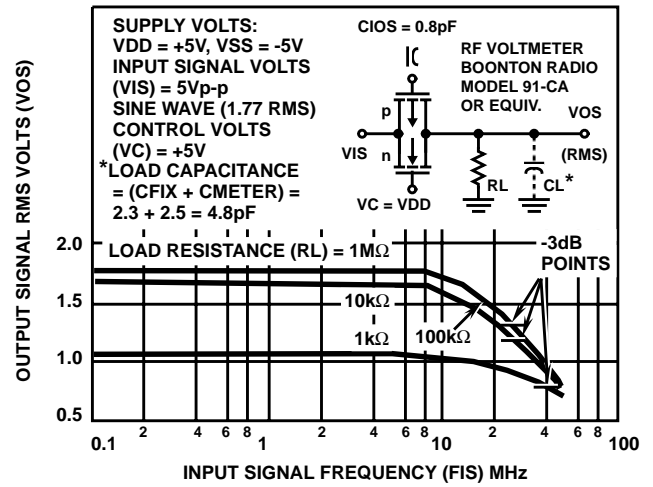


FIGURE 11. TYPICAL FREQUENCY RESPONSE - SWITCH ON

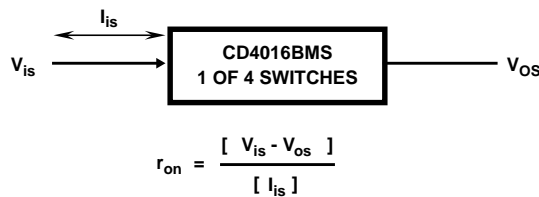


FIGURE 12. DETERMINATION OF RON AS A TEST CONDITION FOR CONTROL INPUT HIGH VOLTAGE (VIHC) SPECIFICATION

CD4016BMS

TYPICAL ON-STATE RESISTANCE CHARACTERISTICS, $T_A = +25^\circ\text{C}$

CHARACTERISTICS*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			RL = 1k Ω		RL = 10k Ω		RL = 100k Ω	
	VDD (V)	VSS (V)	VALUE (Ω)	Vis (V)	VALUE (Ω)	Vis (V)	VALUE (Ω)	Vis (V)
RON	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
RON (max.)	+15	0	300	+11	300	+9.3	320	+9.2
RON	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
RON (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
RON	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
RON (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
RON	+7.5	-7.5	200	+7.5	200	+7.5	180	+7.5
			200	-7.5	200	-7.5	180	-7.5
RON (max.)	+7.5	-7.5	290	± 0.25	280	± 0.25	400	± 0.25
RON	+5	-5	260	+5	250	+5	240	+5
			310	-5	250	-5	240	-5
RON (max.)	+5	-5	600	± 0.25	580	± 0.25	760	± 0.25
RON	+2.5	-2.5	590	+2.5	450	+2.5	490	+2.5
			720	-2.5	520	-2.5	520	-2.5
RON (max.)	+2.5	-2.5	232k	± 0.25	300k	± 0.25	870k	± 0.25

*Variation from perfect switch, ron = 0 Ω

Typical Wave Response

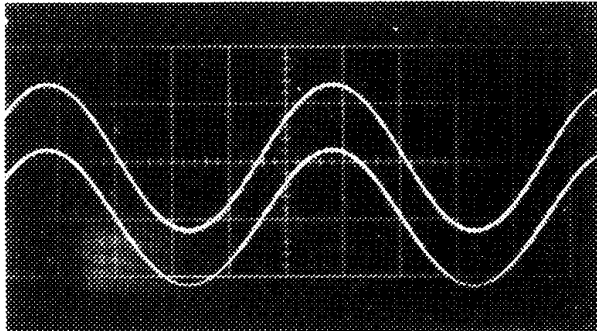


FIGURE 13. TYPICAL SINE WAVE RESPONSE OF VDD = +7.5V, VSS = -7.5V

Scale X = 0.2ms/Div Y = 2.0V/Div
 VDD = VC = +7.5V, RL = 10K Ω
 CL = 15pF
 fis = 1kHz VIS = 5Vp-p
 Distortion = 0.2%

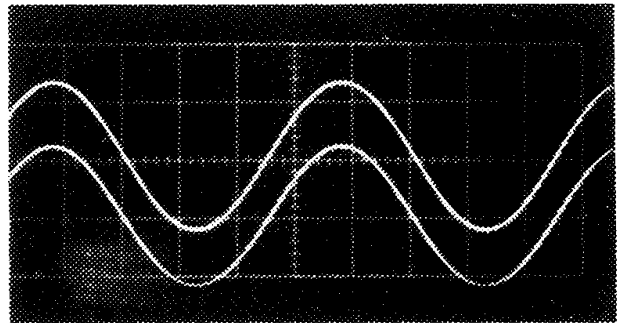


FIGURE 14. TYPICAL SINE WAVE RESPONSE OF VDD = +5V, VSS = -5V

Scale X = 0.2ms/Div Y = 2.0V/Div
 VDD = VC = +5V, RL = 10K Ω
 CL = 15pF
 fis = 1kHz VIS = 5Vp-p
 Distortion = 0.4%

Typical Wave Response (Continued)

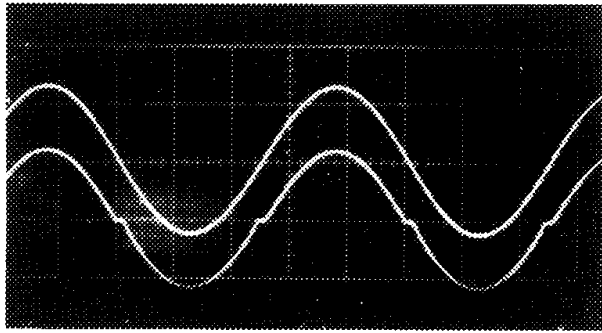


FIGURE 15. TYPICAL SINE WAVE RESPONSE OF VDD = +2.5V, VSS = -2.5V

Scale: X = 0.2ms/Div Y = 2.0V/Div

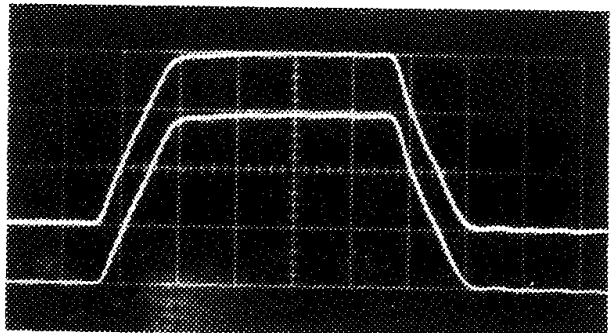


FIGURE 16. TYPICAL SQUARE WAVE RESPONSE AT VDD = VC = +15V, VSS = GND

Scale: X = 100ns/Div Y = 5.0V/Div

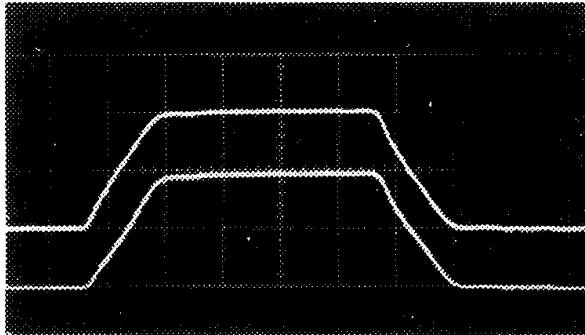


FIGURE 17. TYPICAL SQUARE WAVE RESPONSE AT VDD = VC = +10V, VSS = GND

Scale: X = 100ns/Div Y = 5.0V/Div

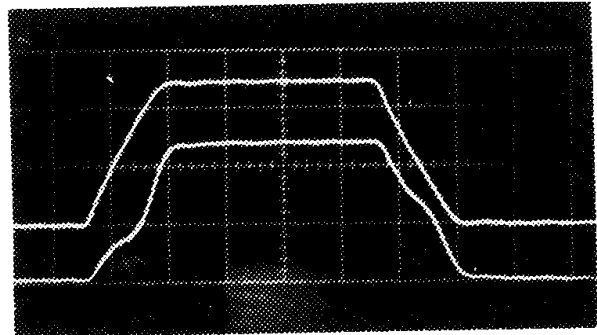
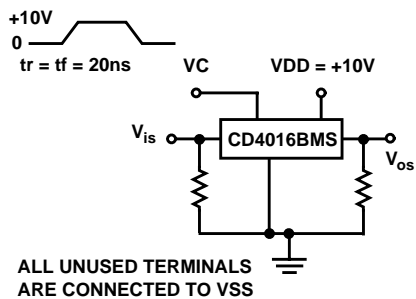


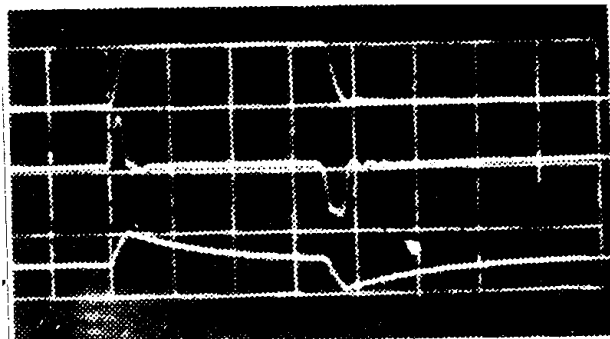
FIGURE 18. TYPICAL SQUARE WAVE RESPONSE AT VDD = VC = +5V, VSS = GND

Scale: X = 100ns/Div Y = 2.0V/Div



(a)

VC →
 VOS WITH TEST UNIT
 (1 SWITCH OF
 CD4016BMS PLUGGED
 IN TEST FIXTURE) →
 VOS FIXTURE ALONE
 (NO UNIT. . . TERM
 5 TO 3 OF SOCKET) →

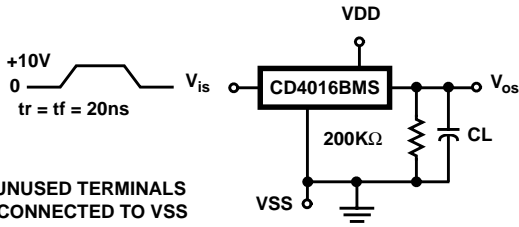


(b)

VC = 10V/Div
 VOS = 0.2V/Div
 t = 100ns/Div

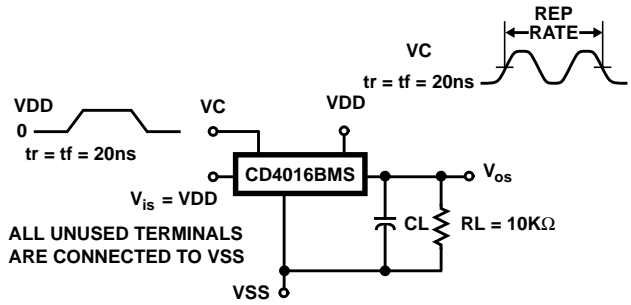
FIGURE 19. CROSSTALK-CONTROL INPUT TO SIGNAL OUTPUT

CD4016BMS



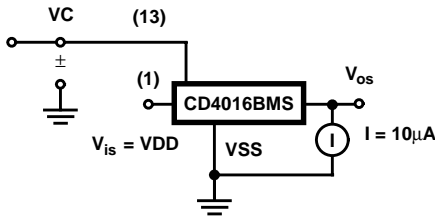
ALL UNUSED TERMINALS ARE CONNECTED TO VSS

FIGURE 20. PROPAGATION DELAY TIME SIGNAL INPUT (V_{IS}) TO SIGNAL OUTPUT (V_{OS})



ALL UNUSED TERMINALS ARE CONNECTED TO VSS

FIGURE 21. MAXIMUM CONTROL-INPUT REPETITION RATE

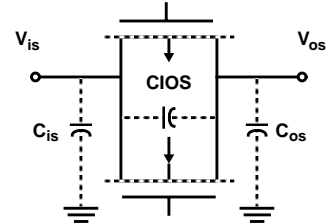


SWITCH THRESHOLD VOLTAGE IS DEFINED AS THE VOLTAGE APPLIED TO A TRANSMISSION GATE CONTROL WHICH CAUSES 10μA OF TRANSMISSION GATE CURRENT

FIGURE 22. SWITCH THRESHOLD VOLTAGE

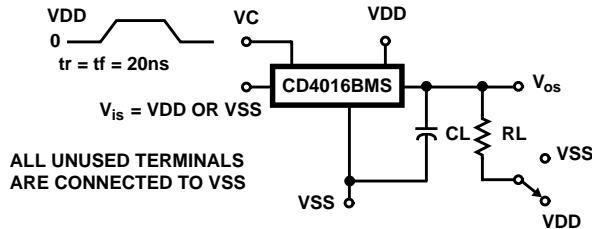
MEASURED ON BOONTON CAPACITANCE BRIDGE MODEL 75A (1MHz)

VC = -5V
VSS = -5V
VDD = +5V



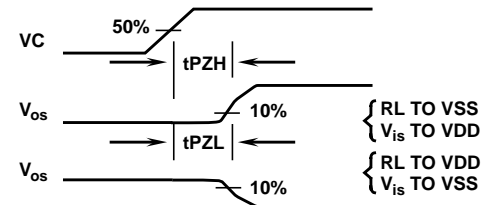
ALL UNUSED TERMINALS ARE CONNECTED TO VSS

FIGURE 23. CAPACITANCE C_{IOS} AND C_{OS}

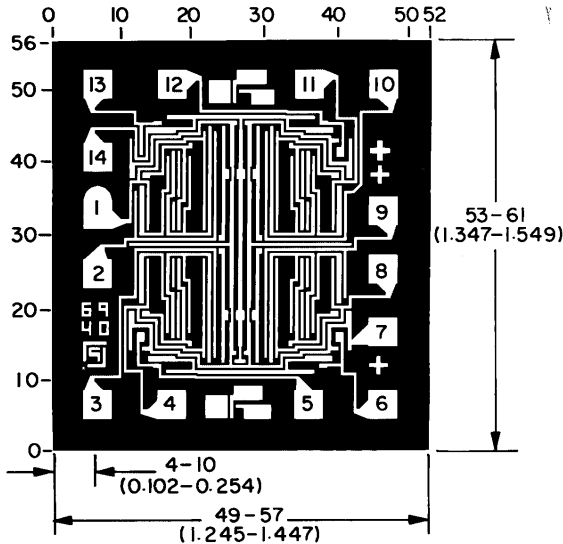


ALL UNUSED TERMINALS ARE CONNECTED TO VSS

FIGURE 24. TURN-ON PROPAGATION DELAY CONTROL INPUT



Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ – 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 i